GSM Baseband and Audio Interface (BAI) PCF5073

FEATURES

- Low power device in 0.5 micron CMOS technology for 3.0 V typical power supply
- Compatible with GSM phase 2 and DCS1800 recommendations
- Complete in-phase and quadrature component interface paths between digital signal processor and IF circuitry (e.g. Philips SA1638)
- Complete linear PCM CODEC for audio signal conversion between earphone/microphone and digital signal processor
- Four auxiliary analog inputs for measurement purposes (e.g. battery monitoring)
- Three auxiliary analog outputs for control purposes (e.g. AFC, AGC and power ramping control)
- Separate baseband, audio and control serial interfaces
- JTAG interface for boundary scan test.

APPLICATIONS

The CMOS integrated circuit PCF5073 is dedicated to wireless telephone handsets following the GSM recommendations phases 1 and 2 and DCS1800.

GENERAL DESCRIPTION

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the digital signal processor. It consists of three parts:

1. The **receive path**, which transforms the quadrature signals from the RF (I/Q) to digital signals.
2. The **transmit path**, which transforms a bitstream to analog quadrature signals for the RF devices.
3. The digital **baseband serial interface**, which exchanges baseband data between the PCF5073 and the digital signal processor. The interface also includes signals to power the transmit path and the receive path up and down.

The voice band CODEC in the PCF5073 is a complete analog front-end circuit. It consists of three parts:

1. The **receive path**, which converts a digital signal to an analog signal for an earpiece, an external loudspeaker or a buzzer.
2. The **transmit path**, which receives the analog external signal from a microphone and converts it into a digital signal.
3. The digital **audio serial interface**, which connects the digital linear PCM signals of the receive and transmit paths to an external digital signal processor. The voice band data is coded in 16-bit linear PCM twos complement words.

The **auxiliary ADC** section consists of four input channels specified for battery management applications.

The **auxiliary DAC** section consists of three digital-to-analog converters for automatic gain control, for automatic frequency control and for power ramping.

The **control serial interface** is used to program a set of control registers, to store the power amplifier ramping characteristics into the dedicated RAM and to transmit auxiliary ADC values to the digital signal processor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5073H	LQFP64	plastic low profile quad flat package; 64 leads; body 7 × 7 × 1.4 mm	SOT414-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (digital)	2.7 (2.5)	3.0	3.6	V
I_{DD}	supply current	–	15	–	mA
$I_{stb(tot)}$	total standby current	–	10	–	µA
f_{clk}	master clock frequency	–	13.0	–	MHz
T_{amb}	operating ambient temperature	–40	+27	+85	°C

BLOCK DIAGRAM

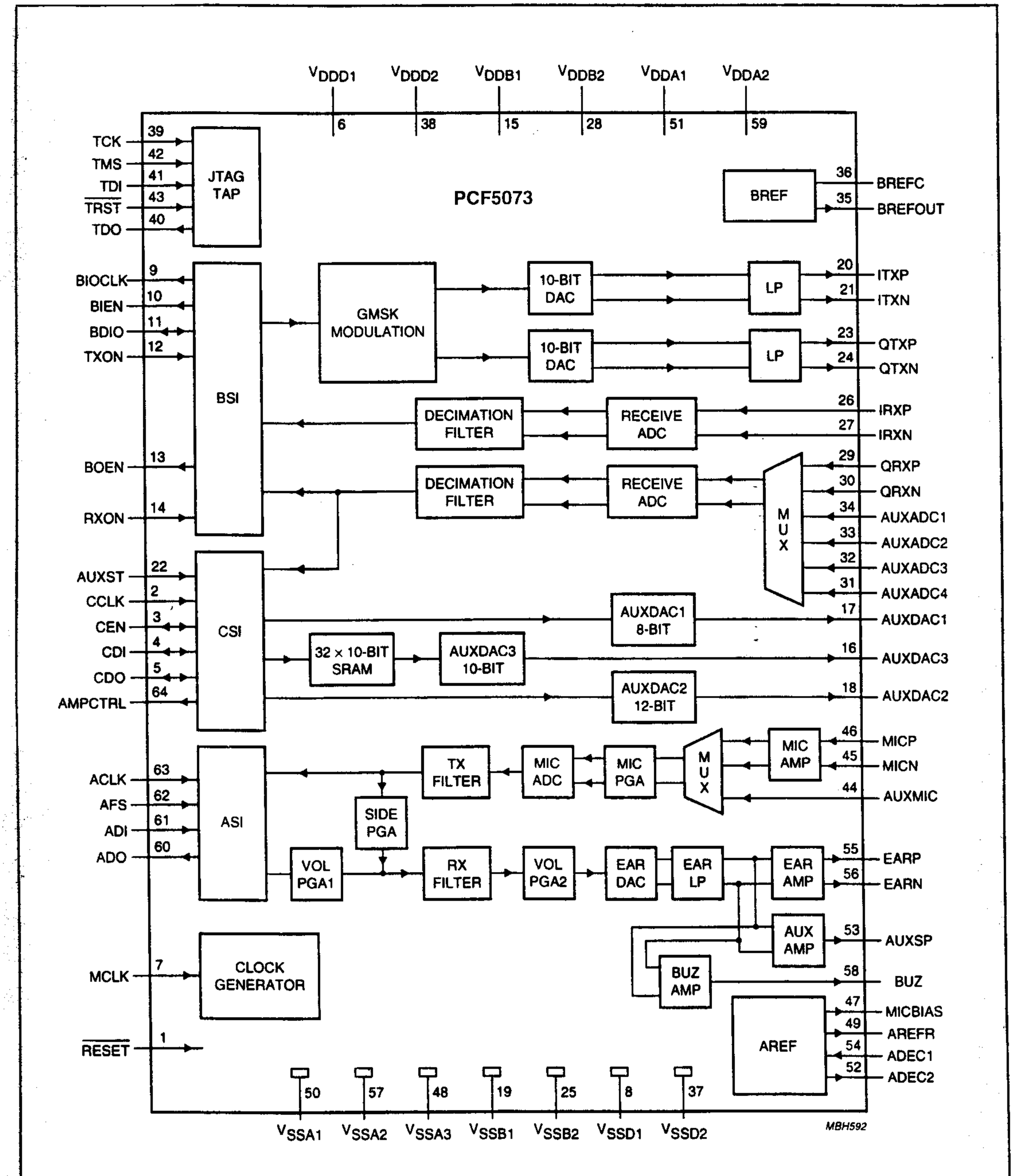

Fig.1 Block diagram.

PINNING

SYMBOL	PIN			DESCRIPTION
	PIN	TYPE	ACTIVE LEVEL/I_{DD}	
$\overline{RESET}$	1	I	LOW	asynchronous reset input
CCLK	2	I	falling	control bus clock input from DSP or UART (f_{max} = 3.25 MHz)
CEN	3	I/O[1]	LOW	control bus data enable from DSP
CDI	4	I/O[1]		control bus data input from DSP (fixed to V_{SS} in UART mode)
CDO	5	I/O	1.5 mA	control bus data output to DSP (data I/O in UART control mode)
V_{DDD1}	6	P		digital power supply 1
MCLK	7	I	rising	low-swing master clock input; f =13 MHz; integrated capacitive coupling
V_{SSD1}	8	G		digital ground 1
BIOCLK	9	O/TS[2]	3 mA	baseband interface data clock (TX: f = 270.833 kHz; RX: f = 13.0 MHz)
BIEN	10	O	LOW/1.5 mA	baseband transmit interface data enable signal
BDIO	11	I/O	1.5 mA	baseband interface data I/O from/to DSP
TXON	12	I	HIGH	baseband transmit path activation signal
BOEN	13	O	LOW/1.5 mA	baseband receive interface data enable signal
RXON	14	I	HIGH	baseband receive path activation signal
V_{DDB1}	15	P		baseband transmit path power supply 1
AUXDAC3	16	O		auxiliary DAC output for power ramping; maximum load 50 pF//2 kΩ
AUXDAC1	17	O		auxiliary DAC output for AGC; maximum load 50 pF//2 kΩ
AUXDAC2	18	O		auxiliary DAC output for AFC; maximum load 50 pF//10 kΩ
V_{SSB1}	19	G		baseband transmit path ground 1
ITXP	20	O		(I) baseband transmit differential positive output to IF circuit
ITXN	21	O		(I) baseband transmit differential negative output to IF circuit
AUXST	22	I	HIGH	status control signal for activation of AUXDAC2 and MCLK input
QTXP	23	O		(Q) baseband transmit differential positive output to IF circuit
QTXN	24	O		(Q) baseband transmit differential negative output to IF circuit
V_{SSB2}	25	G		baseband receive interface ground 2
IRXP	26	I		(I) baseband receive differential positive input from IF circuit
IRXN	27	I		(I) baseband receive differential negative input from IF circuit
V_{DDB2}	28	P		baseband receive interface power supply 2
QRXP	29	I		(Q) baseband receive differential positive input from IF circuit
QRXN	30	I		(Q) baseband receive differential negative input from IF circuit
AUXADC4	31	I		auxiliary ADC input 4
AUXADC3	32	I		auxiliary ADC input 3
AUXADC2	33	I		auxiliary ADC input 2
AUXADC1	34	I		auxiliary ADC input 1 for battery voltage measurement
BREFOUT	35	O	0.2 mA[3]	baseband receive reference voltage noise decoupling pin
BREFC	36	I/O		band gap reference voltage noise decoupling pin
V_{SSD2}	37	G		digital ground 2
V_{DDD2}	38	P		digital power supply 2

SYMBOL	PIN			DESCRIPTION
	PIN	TYPE	ACTIVE LEVEL/I_{DD}	
TCK	39	I		JTAG clock input
TDO	40	O/TS[2]	3 mA	JTAG data output
TDI	41	I		JTAG data input
TMS	42	I		JTAG mode selection input
$\overline{TRST}$	43	I	LOW	JTAG reset input
AUXMIC	44	I		auxiliary microphone single-ended input
MICN	45	I		microphone differential negative input
MICP	46	I		microphone differential positive input
MICBIAS	47	O	0.5 mA	microphone bias voltage
V_{SSA3}	48	G		analog ground 3; shielding substrate contact
AREFR	49	O	12 μA	reference current external resistor to analog ground
V_{SSA1}	50	G		analog ground; audio analog ground 1
V_{DDA1}	51	P		analog power supply; audio analog power supply 1
ADEC2	52	O		audio CODEC buffered DC reference; for noise decoupling
AUXSP	53	O		auxiliary speaker output
ADEC1	54	I		mid-reference non-buffered decoupling connection; $\frac{1}{2}V_{DD}$
EARP	55	O		earphone differential positive output
EARN	56	O		earphone differential negative output
V_{SSA2}	57	G		analog ground, audio analog ground 2
BUZ	58	O		buzzer output
V_{DDA2}	59	P		analog power supply; audio analog power supply 2
ADO	60	O/TS	1.5 mA	audio digital interface PCM data output to DSP
ADI	61	I/O[1]		audio digital interface PCM data input from DSP
AFS	62	I	HIGH	audio digital interface PCM frame synchronisation signal from DSP
ACLK	63	I	rising	audio digital interface PCM clock signal from DSP
AMPCTRL	64	O[4]	1.5 mA	auxiliary speaker external amplifier control signal

Notes

1. Bidirectional for testing only.
2. 3-state (TS) output.
3. Only during start-up time.
4. Active level selectable.

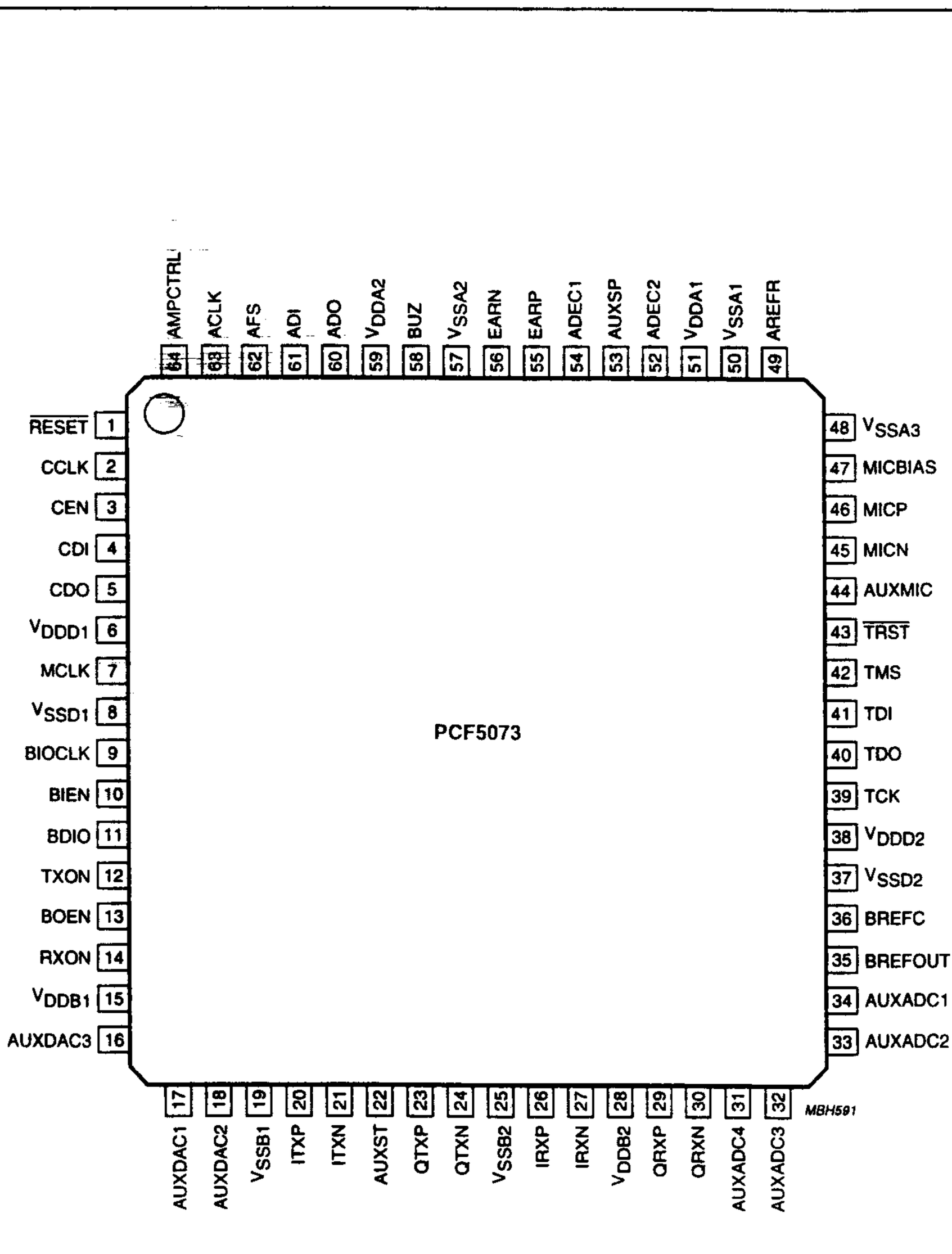

Fig.2 Pin configuration, LQFP64 package.