DL111/D
Rev. 8, July-2001

Bipolar Power Transistor Data

ON Semiconductor™

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DL111/D
Rev. 8, Jun–2001

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CHAPTER 1
Selector Guide

Bipolar Power Transistors

In Brief . . .

ON Semiconductor's broad line of Bipolar Power Transistors includes discrete and Darlington transistors in a variety of packages from the popular surface mount DPAK at 1.75 watts to the 250 watt TO-3. We now have transistors in SO–8 (Dual Transistors) and SOT–223. We have a broad line of Electronic Lamp Ballast Transistors, in the BUL Series and MJD18002D2T4, MJE18002, and MJE18004D24. New products include low $V_{CE(sat)}$ devices in surface mount SOT–223 package, MMJT9435T1/MMJT9410T1 and in the SO–8 package (Dual Transistors), MMDJ3N03BJTR2/ MMDJ3P03BJTR2. We also have a broad line of high performance Audio Output Transistors in TO–3, TO–264 and new products in the Isolated Hole Plastic TO–247 package. The new TO–247 devices are designated MJW21191/2/3/4/5/6 and high f_T, MJW3281A/1302A. These have excellent high voltage FBSOA performance. ON Semiconductor has a commitment to quality and total customer satisfaction.

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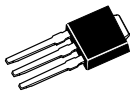
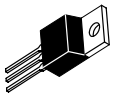
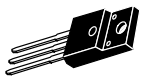
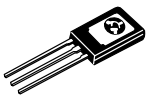
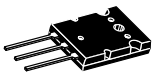
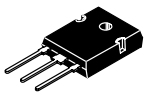
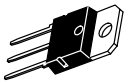
BIPOLAR POWER TRANSISTORS SELECTOR GUIDE

SELECTION BY PACKAGE

Package		I_C Range (Amps)	V_{CE} Range (Volts)	P_D (Watts)
	**TO-204AA (TO-3)**	4.0-30	40-250	115-250
	**TO-204AE (TO–3)**	30–60	60-120	150-300
	**DPAK**	0.5-10	40-450	12.5-20
	**DPAK**	0.5-10	40-450	12.5-20
	**TO-220AB**	0.5-15	60-400	30-125
	**Isolated TO-220 Type**	1.0-12	60-450	20-45
	**TO-225AA (TO-126 Type)**	0.3-5.0	25-400	12.5-40
	**SOT–223**	3.0	30	2.0 (Note 1.)
	**SO–8**	3.0	30	2.0 (Note 2.)
	**TO-264**	15-16	200-250	250
	**D^2PAK**	5.0–8.0	80–450	50–65
	**TO–247**	8.0–16	150–250	200
	**TO–218**	5.0–10	60–350	125–150

1. Tested on 1″ sq. FR4 Board
2. Tested on 1″ sq., 2 oz. copper

Plastic TO–220AB

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 7.)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
1.0	80	TIP29B	TIP30B	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30	725
	100	TIP29C	TIP30C	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30	725
	250	TIP47		30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	747
	300	TIP48	MJE5730	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	747, 581
	350		***MJE5731***	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	581
	400	***TIP50***	***MJE5731A*** (Note 6.)	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40	747, 581
2.0	60	TIP110 (Note 4.)	TIP115 (Note 4.)	500 min	2.0	1.7 typ	1.3 typ	2.0	25 (Note 3.)	50	709
	80	TIP111 (Note 4.)	TIP116 (Note 4.)	500 min	2.0	1.7 typ	1.3 typ	2.0	25 (Note 3.)	50	709
	100	***TIP112*** (Note 4.)	***TIP117*** (Note 4.)	500 min	2.0	1.7 typ	1.3 typ	2.0	25 (Note 3.)	50	709
	400/700	***BUL44***		14/36	0.4	2.75 (Note 5.)	0.175 (Note 5.)	1.0	13 typ	50	279
	450/1000	***BUX85***		30	0.1	3.5	1.4	1.0	4.0	50	313
	450/1000	***MJE18002***		14/34	0.2	3.0 (Note 5.)	0.17 (Note 5.)	1.0	12 typ	40	505
3.0	60	TIP31A	TIP32A	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40	729
	80	***TIP31B***	***TIP32B***	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40	729
	100	BD241C	BD242C	25 min	1.0				3.0	40	157
		TIP31C	***TIP32C***	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40	729
4.0	80	***D44C12***	***D45C12***	40/120	0.2			1.0	40 typ	30	320
	400/700	***MJE13005***		6/30	3.0	3.0	0.7	3.0	4.0	60	468
5.0	60	TIP120 (Note 4.)	TIP125 (Note 4.)	1k min	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 3.)	65	715
	80	TIP121 (Note 4.)	TIP126 (Note 4.)	1k min	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 3.)	65	715
	100	***TIP122*** (Note 4.)	***TIP127*** (Note 4.)	1k min	3.0	1.5 typ	1.5 typ	4.0	4.0 (Note 3.)	75	715
	250	2N6497		10/75	2.5	1.8	0.8	2.5	5.0	80	133
	400/700	***BUL45***		14/34	0.3	1.7 (Note 5.)	0.15 (Note 5.)	1.0	12 typ	75	296
	450/1000	***MJE18004***		14/34	0.3	1.7	0.15	1.0	13	75	522
		MJE18004D2*									512

3. $|h_{FE}|$ @ 1.0 MHz
4. Darlington
5. Switching tests performed with special application simulator circuit. See data sheet for details.
6. V_{CEO} = 375 V
7. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

*D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

Devices listed in **bold**, ***italic*** are ON Semiconductor preferred devices.

Plastic TO–220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 11.)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
6.0	60	TIP41A	TIP42A	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65	742
	80	TIP41B	TIP42B	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65	742
		BD243B	***BD244B***	15 min	3.0	0.4 typ	0.15 typ	3.0	3.0	65	162
	100	***BD243C***	***BD244C***	15 min	3.0	0.4 typ	0.15 typ	3.0	3.0	65	162
		TIP41C	***TIP42C***	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65	742
	400/700	***BUL146***		14/34	0.5	1.75 (Note 10.)	0.15 (Note 10.)	3.0	14 typ	100	263
	450/1000	***MJE18006***		14/34	0.5	3.2 (Note 10.)	0.13 (Note 10.)	3.0	14 typ	100	531
7.0	30	2N6288	2N6111	30/150	3.0	0.4 typ	0.15 typ	3.0	4.0	40	107
	50		2N6109	30/150	2.5	0.4 typ	0.15 typ	3.0	4.0	40	107
	70	2N6292	2N6107	30/150	2.0	0.4 typ	0.15 typ	3.0	4.0	40	107
	150	BU407		30 min	1.5		0.75	5.0	10	60	214
	200	***BU406***		30 min	1.5		0.75	5.0	10	60	214
8.0	60	2N6043 (Note 9.)	2N6040 (Note 9.)	1k/10k	4.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	75	98
		TIP100 (Note 9.)	TIP105 (Note 9.)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	80	704
	80	***BDX53B*** (Note 9.)	***BDX54B*** (Note 9.)	750 min	3.0				4.0 (Note 8.)	60	203
		TIP101 (Note 9.)	***TIP106*** (Note 9.)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	80	704
	100	***2N6045*** (Note 9.)	***2N6042*** (Note 9.)	1k/10k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	75	98
		BDX53C (Note 9.)	***BDX54C*** (Note 9.)	750 min	3.0						203
		TIP102 (Note 9.)	***TIP107*** (Note 9.)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 8.)	80	704
	120	MJE15028	MJE15029	20 min	4.0				30	50	492
	150	***MJE15030***	***MJE15031***	20 min	4.0				30	50	492
	300/600	MJE5740 (Note 9.)		200 min	4.0	8.0 typ	2.0 typ	6.0	4.0	80	585
	300		MJE5850	15 min	2.0	2.0	0.5	4.0		80	590
	350		***MJE5851***	15 min	2.0	2.0	0.5	4.0		80	590
	400	***MJE5742*** (Note 9.)		200 min	4.0	8.0 typ	2.0 typ	6.0		80	585
		MJE13007		5/30	5.0	3.0	0.7	5.0		80	474
			MJE5852	15 min	2.0	2.0	0.5	4.0		80	590

8. $|h_{FE}|$ @ 1.0 MHz
9. Darlington
10. Switching tests performed with special application simulator circuit. See data sheet for details.
11. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Plastic TO–220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 15.)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp			
8.0	400/700	***BUL147***		14/34	1.0	2.5 (Note 14.)	0.18 (Note 14.)	2.0	14 typ	125	272
	450/1000	***MJE18008***		16/34	1.0	2.75 (Note 14.)	0.18 (Note 14.)	2.0	13 typ	125	538
10	60	D44H8	D45H8	40 min	4.0					50	320
		MJE3055T	***MJE2955T***	20/70	4.0					75	560
		2N6387 (Note 13.)	***2N6667*** (Note 13.)	1k/20k	5.0				20 (Note 12.)	65	121, 137
	80	***BDX33B*** (Note 13.)	***BDX34B*** (Note 13.)	750 min	3.0				3.0	70	197
		BD809	***BD810***	15 min	4.0				1.5	90	183
		2N6388 (Note 13.)	***2N6668*** (Note 13.)	1k/20k	5.0				20 (Note 12.)	65	121, 137
		D44H10	D45H10	20 min	4.0	0.5 typ	0.14 typ	5.0	50 typ	50	316
		D44H11	***D45H11***	40 min	4.0	0.5 typ	0.14 typ	5.0	50 typ	50	316
	100	***BDX33C*** (Note 13.)	***BDX34C*** (Note 13.)	750 min	3.0				3.0	70	197
12	400/700	***MJE13009***		6/30	8.0	3.0	0.7	8.0	4.0	100	483
15	60	2N6487	2N6490	20/150	5.0	0.6 typ	0.3 typ	5.0	5.0	75	127
	80	***2N6488***	***2N6491***	20/150	5.0	0.6 typ	0.3 typ	5.0	5.0	75	127
		D44VH10	***D45VH10***	20 min	4.0	0.5	0.09	8.0	50 typ	83	318
	100	***BDW42*** (Note 13.)	***BDW47*** (Note 13.)	1k min	5.0	1.0 typ	1.5 typ	5.0	4.0	85	190

12. $|h_{FE}|$ @ 1.0 MHz
13. Darlington
14. Switching tests performed with special application simulator circuit. See data sheet for details.
15. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Plastic TO–218 Type

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 18.)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
10	60	TIP140 (Note 17.)	TIP145 (Note 17.)	500 min	10	2.5 typ	2.5 typ	5.0	4.0 (Note 16.)	125	720
		TIP141 (Note 17.)	TIP146 (Note 17.)	500 min	10	2.5 typ	2.5 typ	5.0	4.0 (Note 16.)	125	720
	100	***BDV65B*** (Note 17.)	***BDV64B*** (Note 17.)	1k min	5.0					125	187
		TIP33C	TIP34C	20/100	3.0				3.0	80	734
		TIP142 (Note 17.)	***TIP147*** (Note 17.)	500 min	10	2.5 typ	2.5 typ	5.0	4.0 (Note 16.)	125	720
	350	BU323Z (Note 17.)		500/3400	5.0			6.0		150	209
15	60	***TIP3055***	***TIP2955***	5 min	10				2.5	80	727
	150	MJH11018 (Note 17.)	MJH11017 (Note 17.)	400/15k	10				3.0	150	634
	200	MJH11020 (Note 17.)	MJH11019 (Note 17.)	400/15k	10				3.0	150	634
	250	***MJH11022*** (Note 17.)	***MJH11021*** (Note 17.)	400/15k	10				3.0	150	634
16	160	***MJE4343***	***MJE4353***	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125	574
20	100	***MJH6284*** (Note 17.)	***MJH6287*** (Note 17.)	750/18k	10				4.0	125	640
25	60	TIP35A	TIP36A	15/75	15	0.6 typ	0.3 typ	10	3.0	125	737
	100	***TIP35C***	***TIP36C***	15/75	15	0.6 typ	0.3 typ	10	3.0	125	737

16. $|h_{FE}|$ @ 1.0 MHz
17. Darlington
18. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Plastic (Isolated TO-220 Type)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
			NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp			
1.0	250		***MJF47***		30/150	0.3	2.0 typ	0.17 typ	0.3	10	28	622
3.0	100		***MJF31C***	***MJF32C***	10 min	1.0	0.6	0.3	1.0	3.0	28	729
5.0	100		***MJF122*** (Note 20.)	***MJF127*** (Note 20.)	2000 min	3.0	1.5 typ	1.5 typ	3.0	4.0 (Note 19.)	28	601
	450	1000	***MJF18004***		14/34	0.3	1.7 (Note 21.)	0.15 (Note 21.)	1.0	13 typ	35	522
8.0	150		***MJF15030***	***MJF15031***	40 min	3.0	1.0 typ	0.15 typ	3.0	30	35	608
	450	1000	***MJF18008***		16/34	1.0	2.75 (Note 21.)	0.18 (Note 21.)	2.0	13 typ	45	538
10	60		***MJF3055***	***MJF2955***	20/100	4.0				2.0	40	614
	80		***MJF44H11***	***MJF45H11***	40/100	4.0	0.5 typ	0.14 typ	5.0	40	35	618
	100		***MJF6388*** (Note 20.)	***MJF6668*** (Note 20.)	3k/20k	3.0	1.5 typ	1.5 typ		20 (Note 19.)	40	627

Large Plastic TO-264

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp			
15	200	***MJL3281A***	***MJL1302A***	60/175	5.0				30 typ	200	655
16	250	***MJL21194***	***MJL21193***	25/75	8.0				4.0	200	644
		MJL21196	***MJL21195***	25/75	8.0				4.0	200	649

19. $|h_{FE}|$ @ 1.0 MHz
20. Darlington
21. Switching tests performed with special application simulator circuit. See data sheet for details.

Plastic TO–225AA Type (Formerly TO–126 Type)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp			
0.3	350	***MJE3439***		40/160	0.02				15	15	566
0.5	200	***MJE344***		30/300	0.05				15	20.8	568
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20	80
	300	***MJE340***	***MJE350***	30/240	0.05					20.8	563, 570
	350	***2N5657***		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20	80
		BD159		30/240	0.05					20	146
1.0	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30	55, 50
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30	55, 50
	80	***2N4923***	***2N4920***	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30	55, 50
1.5	45	BD135	BD136	40/250	0.15					12.5	142, 144
	60	BD137	BD138	40/250	0.15					12.5	142, 144
	80	***BD139***	***BD140***	40/250	0.15					12.5	142, 144
	400	***MJE13003*** (Note 24.)		5/25	1.0	4.0	0.7	1.0	5.0	40	461
2.0	80	***BD237***	***BD238***	25 min	1.0				3.0	25	154
	100	***MJE270*** (Notes 23. & 24.)	***MJE271*** (Notes 23. & 24.)	1.5k min	0.12				6.0	15	558
3.0	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5	501
	80	***BD179***	***BD180***	40/250	0.15					25	148, 151
		MJE182	***MJE172***	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5	501
	500	***BUH51*** (Note 24.)		8.0 min	1.0					50	254
4.0	40	***MJE521***	***MJE371***	40 min	1.0					40	579, 572
	45	***BD437***	***BD438***	40 min	2.0				3.0	36	166, 169
	60	***BD439***	***BD440***	25 min	2.0				3.0	36	166, 169
		BD677 (Note 23.)	***BD678*** (Note 23.)	750 min	1.5					40	172, 175
		BD677A (Note 23.)	***BD678A*** (Note 23.)	750 min	1.5					40	172, 175
		BD787	***BD788***	20 min	2.0				50	15	178
		2N5191	***2N5194***	25/100	1.5	0.4 typ	0.4 typ	1.5	2.0	40	62, 67
		MJE800 (Note 23.)	***MJE700*** (Note 23.)	750 min	1.5				1.0 (Note 22.)	40	596
		2N6038 (Note 23.)	***2N6035*** (Note 23.)	750/18k	2.0	1.7 typ	1.2 typ	2.0	25	40	92

22. $|h_{FE}|$ @ 1.0 MHz
23. Darlington
24. Case 77, Style 3

Plastic TO–225AA Type (Formerly TO–126 Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
4.0	80	***2N5192***	***2N5195***	25/100	1.5	0.4 typ	0.4 typ	1.5	2.0	40	62, 67
		BD441	***BD442***	15 min	2.0				3.0	36	166, 169
		BD679 (Note 26.)	***BD680*** (Note 26.)	750 min	1.5					40	172, 175
		BD679A (Note 26.)	***BD680A*** (Note 26.)	750 min	2.0					40	172, 175
		MJE802 (Note 26.)	MJE702 (Note 26.)	750 min	1.5				1.0 (Note 25.)	40	596
		MJE803 (Note 26.)	***MJE703*** (Note 26.)	750 min	2.0				1.0 (Note 25.)	40	596
		2N6039 (Note 26.)	***2N6036*** (Note 26.)	750/18k	2.0	1.7 typ	1.2 typ	2.0	25	40	92
	100	***BD681*** (Note 26.)	***BD682*** (Note 26.)	750 min	1.5					40	172, 175
		MJE243	***MJE253***	40/120	0.2	0.15 typ	0.07 typ	2.0	40	15	553
5.0	25	***MJE200***	***MJE210***	45/180	2	0.13 typ	0.035 typ	2.0	65	15	548

25. $|h_{FE}|$ @ 1.0 MHz
26. Darlington

DPAK – Surface Mount Power Packages

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
0.5	300	***MJD340T4***	***MJD350T4***	30/240	0.05					15	438
1.0	250	MJD47T4		30/150	0.3	2.0	0.2	0.3	10	15	452
	400	***MJD50T4***		30/150	0.3	2.0	0.2	0.3	10	15	452
2.0	100	***MJD112T4*** (Note 28.)	***MJD117T4*** (Note 28.)	1000 min	2.0	1.7	1.3	2.0	25 (Note 27.)	20	395
	450	***MJD18002D2T4***		6.0 min	2.0	1.0 typ	0.15 typ	1.0	13 typ	25	407
3.0	40	MJD31T4	MJD32T4	10 min	1.0	0.6	0.3	1.0	3.0	15	433
	100	***MJD31CT4***	***MJD32CT4***	10 min	1.0	0.6	0.3	1.0	3.0	15	433
4.0	80	***MJD6039T4*** (Note 28.)	***MJD6036T4*** (Note 28.)	1k/2k	2.0	1.7	1.2	2.0	25	20	456
	100	***MJD243T4***	***MJD253T4***	40/180	0.2	0.16	0.04	1.0	40	12.5	423
5.0	25	***MJD200T4***	***MJD210T4***	45/180	2.0	0.15	0.04	2.0	65	12.5	418
6.0	100	***MJD41CT4***	***MJD42CT4***	15/75	3.0	0.4	0.15	3.0	3.0	20	442
8.0	80	***MJD44H11T4***	***MJD45H11T4***	40 min	4.0	0.5	0.14	5.0	50 typ	20	448
	100	***MJD122T4*** (Note 28.)	***MJD127T4*** (Note 28.)	1k/2k	4.0	1.5	2.0	4.0	4 (Note 27.)	20	401
10	60	***MJD3055T4***	***MJD2955T4***	20/100	4.0	1.5	1.5	3.0	2.0	20	429
	80	***MJD44ET4*** (Note 28.)		1k min	5.0	2.0	0.5	10		20	446

27. $|h_{FE}|$ @ 1.0 MHz
28. Darlington

Metal TO–204AA (Formerly TO–3)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 31.)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
4.0	250	***MJ15020***	***MJ15021***	30 min	1.0				20	150	344
10	140	2N3442		20/70	4.0					117	35
	250	***MJ15011***	***MJ15012***	20/100	2.0					200	342
12	100		***2N6052*** (Note 30.)	750/18k	6.0	1.6 typ	1.5 typ	6.0	4.0 (Note 29.)	150	102
15	60	***2N3055***	***MJ2955***	20/70	4.0	0.7 typ	0.3 typ	4.0	2.5	115	31
		2N3055A		20/70	4.0				0.8	115	25
	120	***MJ15015***	***MJ15016***	20/70	4.0	0.7 typ	0.3 typ	4.0	1.0	180	25
	140	MJ15001	MJ15002	25/150	4.0				2.0	200	337
	250	***MJ11022*** (Note 30.)	***MJ11021*** (Note 30.)	100 min	15				3.0 (Note 29.)	175	325
16	140	***2N3773***	2N6609	15/60	8.0	1.1 typ	1.5 typ	8.0	4.0	150	46
		2N5631	2N6031	15/60	8.0	1.2 typ	1.2 typ	8.0	1.0	200	76
	200	MJ15022	MJ15023	15/60	8.0				5.0	250	346, 349
	250	***MJ15024***	***MJ15025***	15/60	8.0				5.0	250	346, 349
		MJ21194	***MJ21193***	25/75	8.0				4.0	250	352
		MJ21196	***MJ21195***	25/75	8.0				4.0	250	357
20	60	***2N3772***		15/60	10				2.0	150	38
	80	***2N6283*** (Note 30.)	2N6286 (Note 30.)	750/18k	10	2.5 typ	2.5 typ	10	4.0 (Note 29.)	160	112
	90	2N5038		20/100	12	1.5	0.5	12	60	140	60
	100	***2N6284*** (Note 30.)	***2N6287*** (Note 30.)	750/18k	10	2.5 typ	2.5 typ	10	4.0 (Note 29.)	160	112
	140	***MJ15003***	***MJ15004***	25/150	5.0				2.0	250	340
25	60	2N5885	2N5883	20/100	10	1.0	0.8	10	4.0	200	87
	80	***2N5886***	***2N5884***	20/100	10	1.0	0.8	10	4.0	200	87
	100	2N6338		30/120	10	1.0	0.25	10	40	200	118
	150	***2N6341***		30/120	10	1.0	0.25	10	40	200	118

29. $|h_{FE}|$ @ 1.0 MHz
30. Darlington
31. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Metal TO–204AA (Formerly TO–3) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 34.)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp			
30	40	***2N3771***		15/60	15				2.0	150	42
	60	2N5302		15/60	15	2.0	1.0	10	2.0	200	72
		MJ11012 (Note 33.)		1k min	20				4.0 (Note 32.)	200	322
	100	***MJ802***	***MJ4502***	25/100	7.5				2.0	200	364, 362
	120	***MJ11016*** (Note 33.)	***MJ11015*** (Note 33.)	1k min	20				4.0 (Note 32.)	200	322
	250	***MJ11022*** (Note 33.)	***MJ11021*** (Note 33.)	400/15k	10				3.0 (Note 32.)	200	325
40	200	BUV21 (Note 35.)		10 min	25	1.8	0.4	25	8.0	150	307
	250	***BUV22*** (Note 35.)		10 min	20	1.1	0.35	20	8.0	250	310
50	80	***2N5686*** (Note 35.)	***2N5684*** (Note 35.)	15/60	25	0.5 typ	0.3 typ	25	2.0	300	83
	120	***MJ11032*** (Note 33. & 35.)	***MJ11033*** (Note 33. & 35.)	400 min	50					300	330
	125	***BUV20*** (Note 35.)		10 min	50	1.2	0.25	50	8.0	250	304
		BUV60 (Note 35.)		10 min	80	1.1	0.25	80		250	304
60	80	***MJ14002*** (Note 35.)	***MJ14003*** (Note 35.)	15/100	50					300	333

32. $|h_{FE}|$ @ 1.0 MHz
33. Darlington
34. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
35. Case 197A–03 (TO–204AE)

Isolated Mounting Hole – Plastic TO–247

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
8.0	150	MJW21192	MJW21191	15 min	8.0				4.0	100	660
16	250	MJW21194*	MJW21193*	20/60	8.0				4.0	200	665
16	250	MJW21196*	MJW21195*	20/60	8.0				4.0	200	671
15	230	MJW3281A*	MJW1302A*	60/175	5.0				30	200	677

D^2PAK

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
5.0	450/1000	MJB18004D2T4		6.0	2.0	2.4	0.175	2.5	13 typ	75	367
6.0	100		MJB42CT4	15/75	3.0				3.0	65	381
8.0	80	MJB44H11T4	MJB45H11T4	40/100	4.0	0.5 typ	0.14	5.0	40	50	388

SOT–223

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
3.0	30	MMJT9410T1	MMJT9435T1	50	1.0					0.8	694, 699
0.5	30		MMJT350T1	30/240	0.05					0.8	692

SO–8 (Dual Transistors)

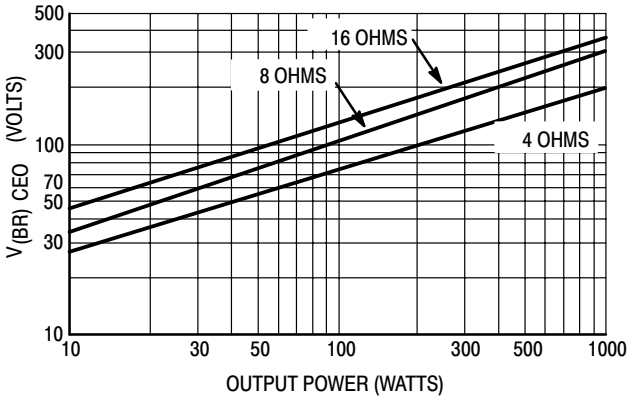
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
3.0	30	MMDJ3N03BJTR2	MMDJ3P03BJTR2	50	1.0				30	2.0	682, 687

*Available in Q2, 2001.

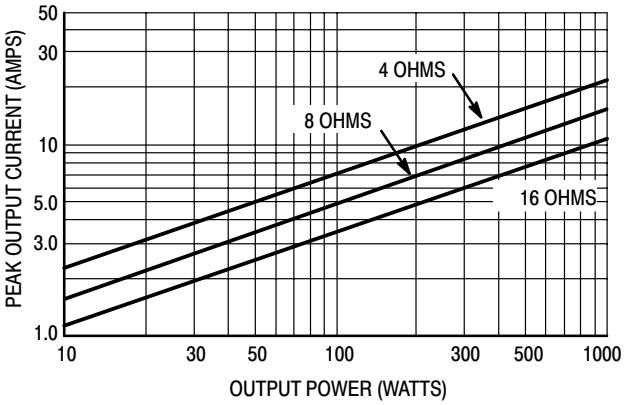
Audio

GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES

$V_{(BR)CEO}$ Required on Output and Driver Transistor versus Output Power for 4, 8 and 18 Ohm Loads



Output Transistor Peak Collector Current versus Output Power for 4, 8 and 16 Ohm Loads



Another important parameter that must be considered before selecting the output transistors is the safe–operating area these devices must withstand. For a complete discussion see Application Note AN485.

Recommended Power Transistors for Audio/Servo Loads

RMS Power Output	NPN	PNP	Case	P_D Watts @ 25°C	V_{CEO}	h_{FE} @ Min/Max	I_C Amps	f_T MHz Typ	ISB Volts/Amps	Page
To 25 W	MJE15030	MJE15031	TO–220	50	150	20 min	4.0	30	14/3.6	492
	MJE15032	MJE15033	TO–220	50	250	50 min	1.0	30	50/1.0	497
25 to 50 W	2N3055A	MJ2955A	TO–204	120	120	20/70	4.0	3.0	60/2.0	25
	MJ15001	MJ15002	TO–204	200	140	25/150	4.0	3.0	40/5.0	337
50 to 100 W	MJ15015	MJ15016	TO–204	180	120	20/70	4.0	3.0	60/3.0	25
	MJ15003	MJ15004	TO–204	250	140	25/150	5.0	3.0	100/1.0	340
	MJ15020	MJ15021	TO–204	150	250	30 min	1.0	30	50/3.0	344
Over 100 W	MJ15024	MJ15025	TO–204	250	250	15/60	8.0	4.0	80/2.2	346, 349
	MJL3281A	MJL1302A	340G–02	150	200	60/175	7.0	30	40/4.0	655
	MJ21194	MJ21193	TO–204	250	250	25/75	8.0	4.0	100/2.0	352
	MJL21194	MJL21193	340G–02	200	200	25/75	8.0	4.0	100/2.0	644
	MJL21196	MJL21195	340G–02	200	200	25/75	8.0	4.0	100/2.0	649
	MJW21192	MJW21191	340K–01	100	150	15 min	4.0	4.0	50/3.0	660
	MJW21194	MJW21193	340K–01	200	250	20/60	8.0	4.0	50/4.0	665
	MJW21196	MJW21195	340K–01	200	250	25/60	8.0	4.0	50/4.0	671
	MJW3281A	MJW1302A	340K–01	200	200	60/175	5.0	30	50/4.0	677

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe–operating area required and the mounting and heat sinking configuration used.

Bipolar Power Transistors for Electronic Lamp Ballasts

Plastic TO–220AB

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C	Page
2.0	400	700	BUL44	0.8	10	2.6 / 3.8	50	279
	450	1000	MJE18002	1.0	6.0	/ 2.75	50	505
4.0	500	800	BUH50	2.0	8.0 typ	/ 2.5	50	246
5.0	400	700	BUL45	2.0	7.0	2.6 / 3.8	75	296
	400	700	BUL45D2*	2.0	10	1.95 / 2.25	75	286
	450	1000	MJE18004	2.0	6.0	/ 2.5	75	522
	450	1000	MJE18004D2*	2.0	6.0	2.1 / 2.4	75	512
6.0	400	700	BUL146	3.0	8.0	2.6 / 3.8	100	263
	450	1000	MJE18006	3.0	6.0	/ 3.2	100	531
8.0	400	700	BUL147	4.5	8.0	2.6 / 3.8	125	272
	450	1000	MJE18008	4.5	6.0	/ 3.2	125	538
10	400	700	BUH100	5.0	10 typ	/ 3.0	100	226
15	400	700	BUH150	10	8.0 typ	/ 2.75	150	236

BUHXXX Series are specified for Halogen applications.
*D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

Bipolar Power Transistors for Electronic Lamp Ballasts

Case 221D-02 is UL RECOGNIZED for its isolation feature. Case 221D-02 has been evaluated to 3500 volts RMS. Actual isolation rating depends on specific mounting position and maintaining required strike and creepage distances.

Plastic (Isolated TO-220 Type)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C	Page
5.0	450	1000	MJF18004	2.0	6.0	/ 2.5	35	522
6.0	400	700	BUL146F	3.0	8.0	2.6 / 3.8	40	263
8.0	450	1000	MJF18008	4.5	6.0	/ 3.2	45	538

Surface Mount Power Packages – DPAK

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C	Page
2.0	400	700	BUD44D2–1*	0.8	20 typ	2.05 / 2.35	25	216

Surface Mount Power Packages – DPAK

I_C Cont Amps Max	$V_{CEO(sus)}$ /V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
2.0	450/1000	MJD18002D2T4		6.0	1.0	1.2	0.150	1.0 A	13 typ	25	407

D^{2}PAK

I_C Cont Amps Max	$V_{CEO(sus)}$ /V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C	Page
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp			
5.0	450/1000	MJB18004D2T4		6.0	2.0	2.4	0.175	2.5 A	13 typ	75	367

Plastic TO–225AA Type (Formerly TO–126 Type)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C	Page
1.5	400	700	MJE13003 (Note 36.)	1.0	6.0 typ	/ 3.0	40	461
3.0	500	800	BUH51 (Note 36.)	1.0	8.0	/ 3.75	50	254

36. Case 77, Style 3

BUHXXX Series are specified for Halogen applications.

*D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

CHAPTER 2
Data Sheets

Complementary Silicon High-Power Transistors

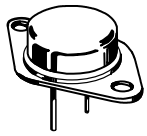
. . . PowerBase™ complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc–to–dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055.

- Current–Gain — Bandwidth–Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) – NPN
  = 2.2 MHz (Min) – PNP
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

NPN
2N3055A
MJ15015*
PNP
MJ15016*

*ON Semiconductor Preferred Device

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60, 120 VOLTS 115, 180 WATTS



CASE 1–07 TO–204AA (TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3055A	MJ15015 MJ15016	Unit
Collector–Emitter Voltage	V_{CEO}	60	120	Vdc
Collector–Base Voltage	V_{CBO}	100	200	Vdc
Collector–Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter–Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	0.98	°C/W

*Indicates JEDEC Registered Data. (2N3055A)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 4
Publication Order Number:
2N3055A/D

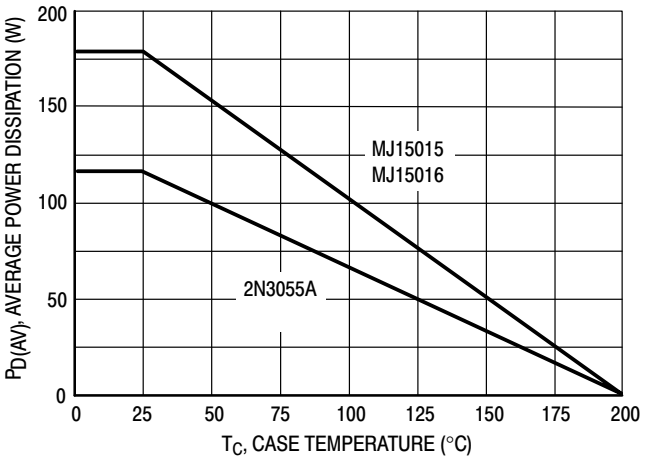


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	— —	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc)	2N3055A		—	0.7	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	MJ15015, MJ15016		—	0.1	
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A MJ15015, MJ15016	I_{CEV}	— —	5.0 1.0	mAdc
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3055A MJ15015, MJ15016		— —	30 6.0	
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A MJ15015, MJ15016	I_{EBO}	— —	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(t = 0.5 s non–repetitive)	2N3055A		1.95	—	
(V_{CE} = 60 Vdc)	MJ15015, MJ15016		3.0	—	
***ON CHARACTERISTICS (1)**					
DC Current Gain		h_{FE}			—
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			10	70	
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			5.0	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 400 mAdc)			—	1.1	
(I_C = 10 Adc, I_B = 3.3 Adc)			—	3.0	
(I_C = 15 Adc, I_B = 7.0 Adc)			—	5.0	
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
***SWITCHING CHARACTERISTICS (2N3055A only)**					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	—	0.5	μs
Rise Time		t_r	—	4.0	μs
Storage Time		t_s	—	3.0	μs
Fall Time		t_f	—	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data. (2N3055A)

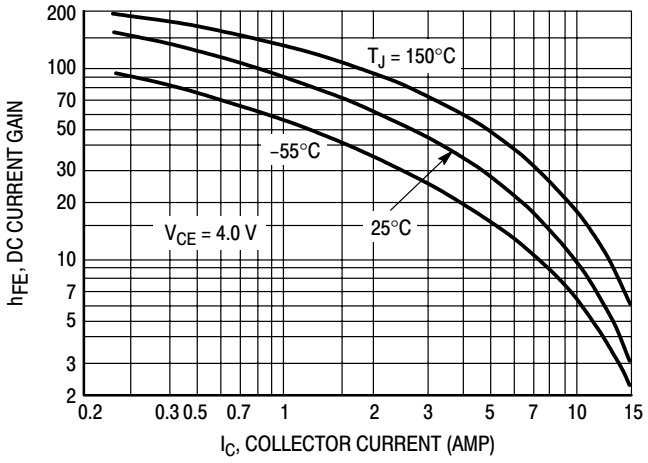


Figure 2. DC Current Gain

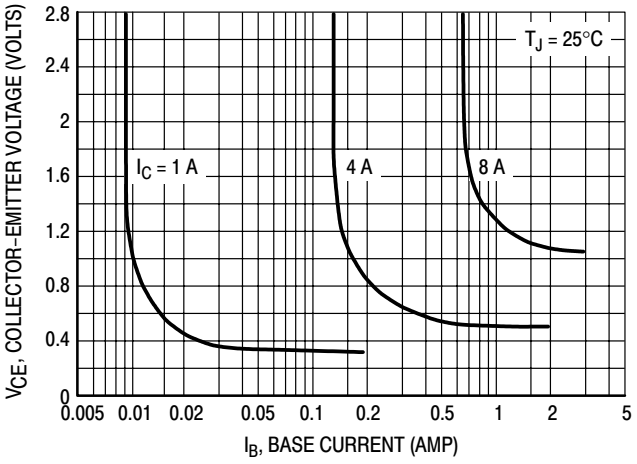


Figure 3. Collector Saturation Region

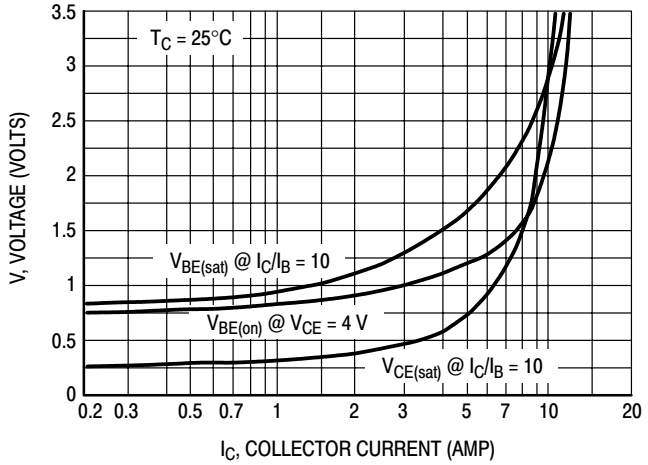


Figure 4. “On” Voltages

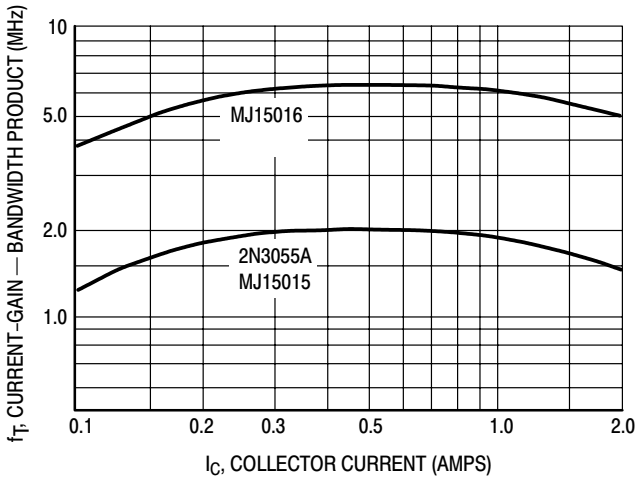


Figure 5. Current−Gain — Bandwidth Product

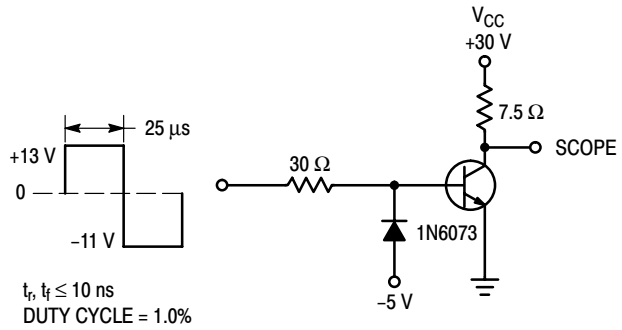


Figure 6. Switching Times Test Circuit (Circuit shown is for NPN)

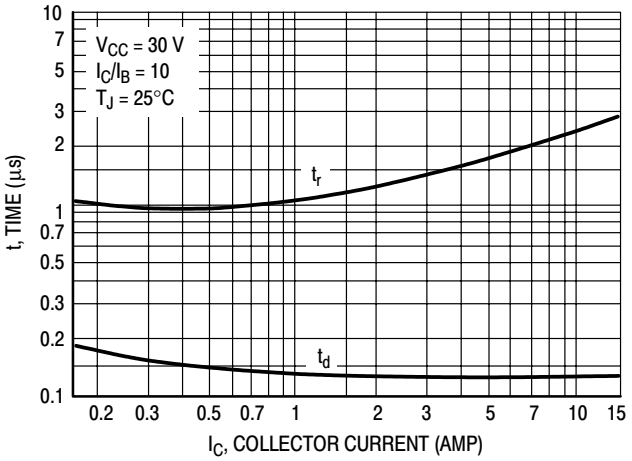


Figure 7. Turn−On Time

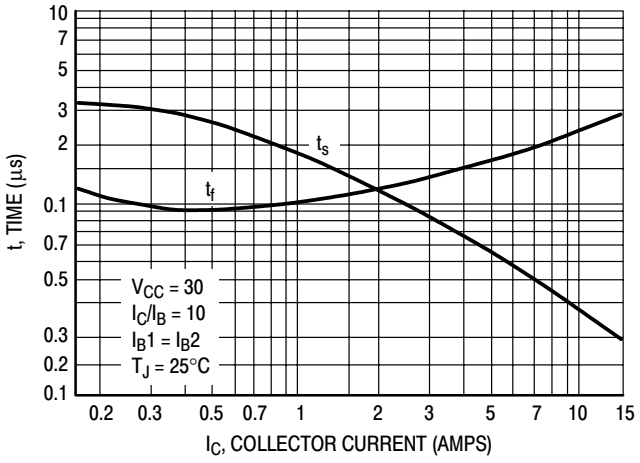


Figure 8. Turn–Off Times

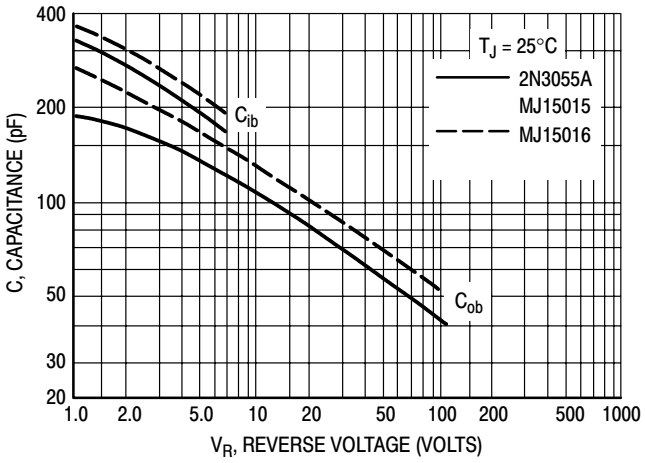


Figure 9. Capacitances

COLLECTOR CUT–OFF REGION

NPN

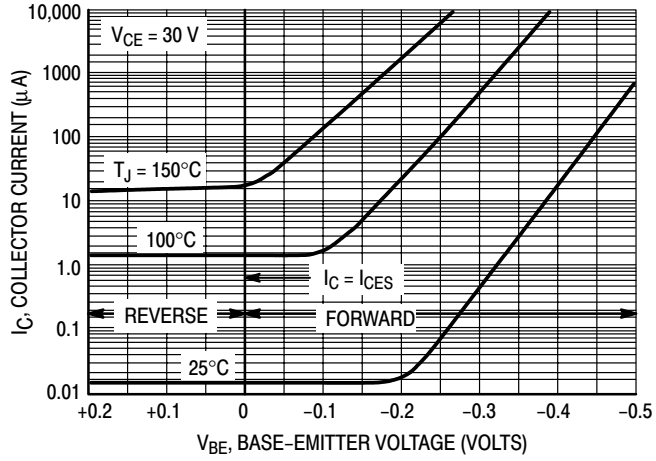


Figure 10. 2N3055A, MJ15015

PNP

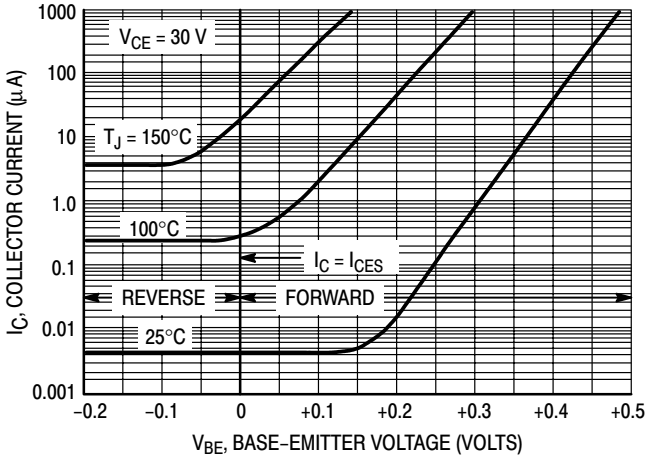


Figure 11. MJ15016

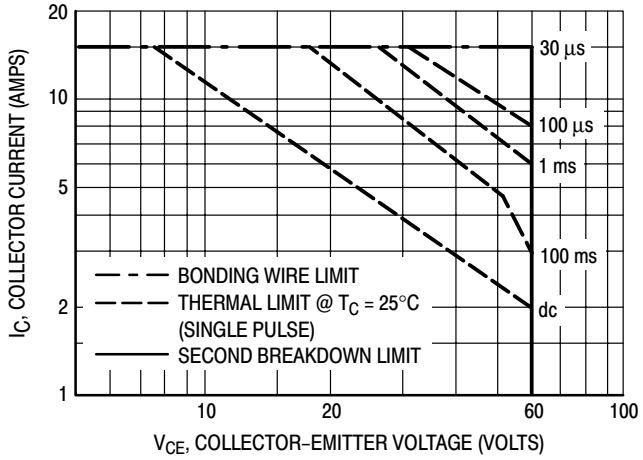


Figure 12. Forward Bias Safe Operating Area 2N3055A

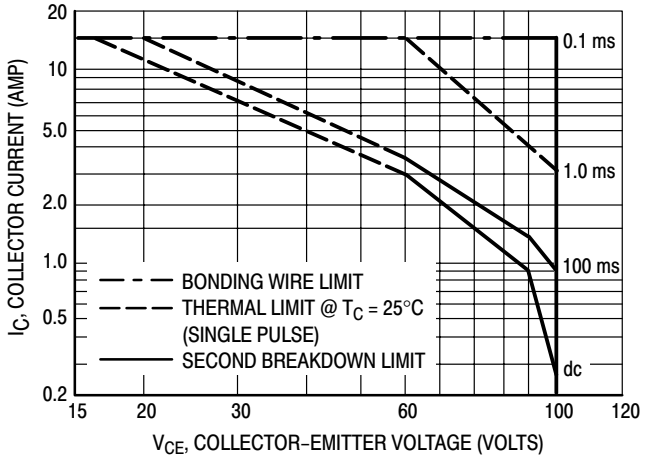


Figure 13. Forward Bias Safe Operating Area MJ15015, MJ15016

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

Complementary Silicon Power Transistors

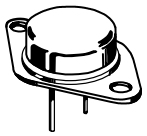
. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4 Adc
- Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

NPN
2N3055 *
PNP
MJ2955 *

***ON Semiconductor Preferred Device**

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
115 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

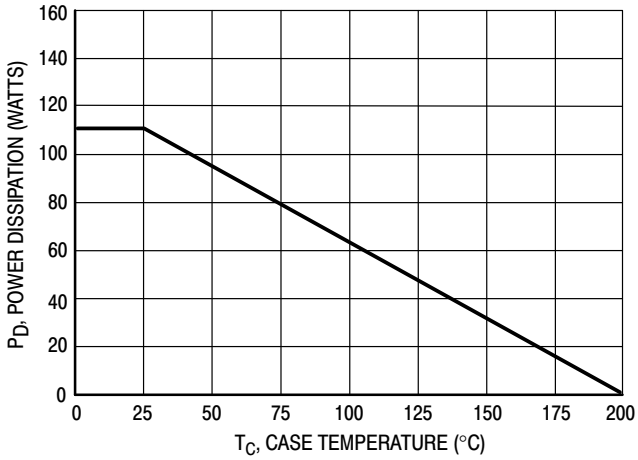


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 —	 1.1 3.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, Nonrepetitive)	$I_{s/b}$	2.87	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
*Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	—
*Small–Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	—	kHz

*Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

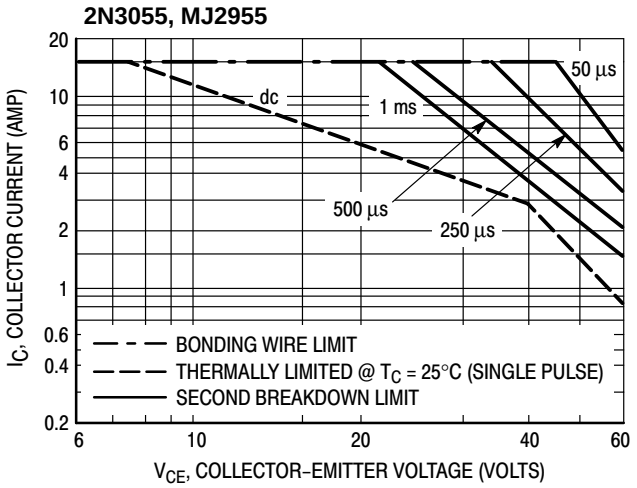


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

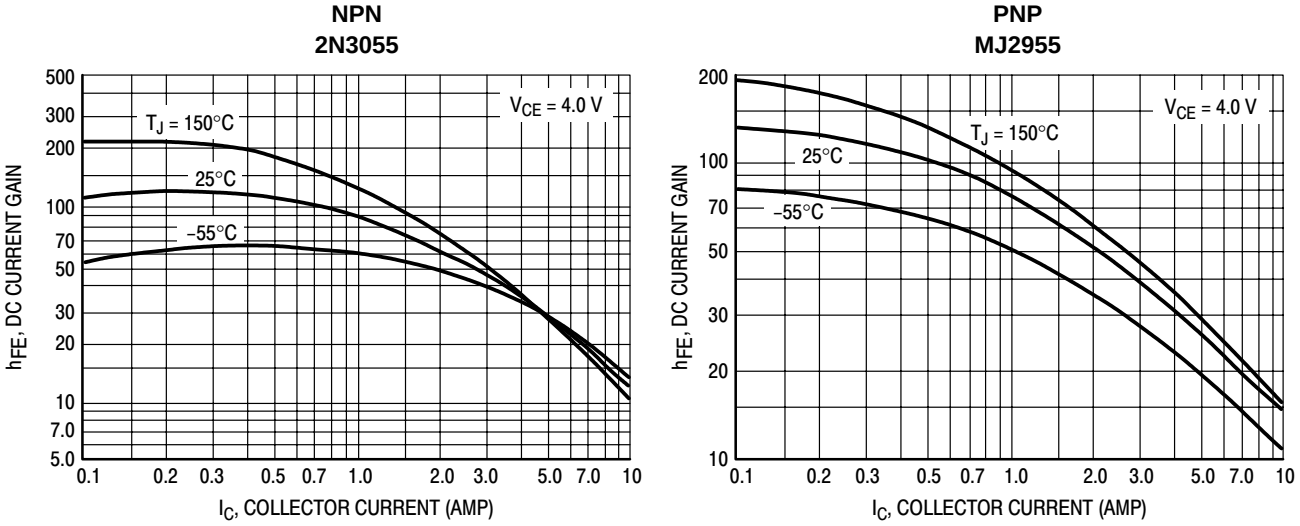


Figure 3. DC Current Gain

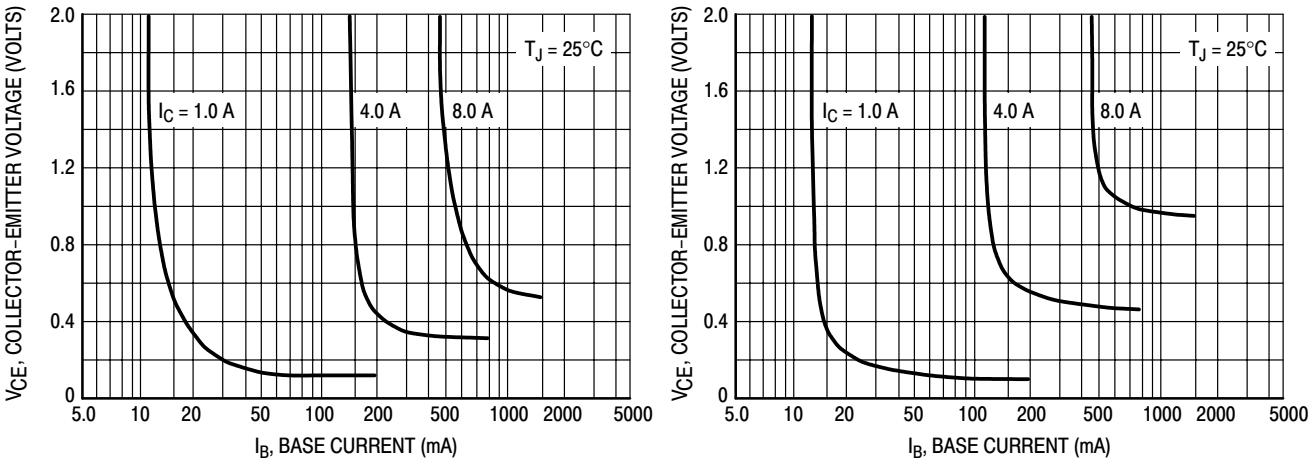


Figure 4. Collector Saturation Region

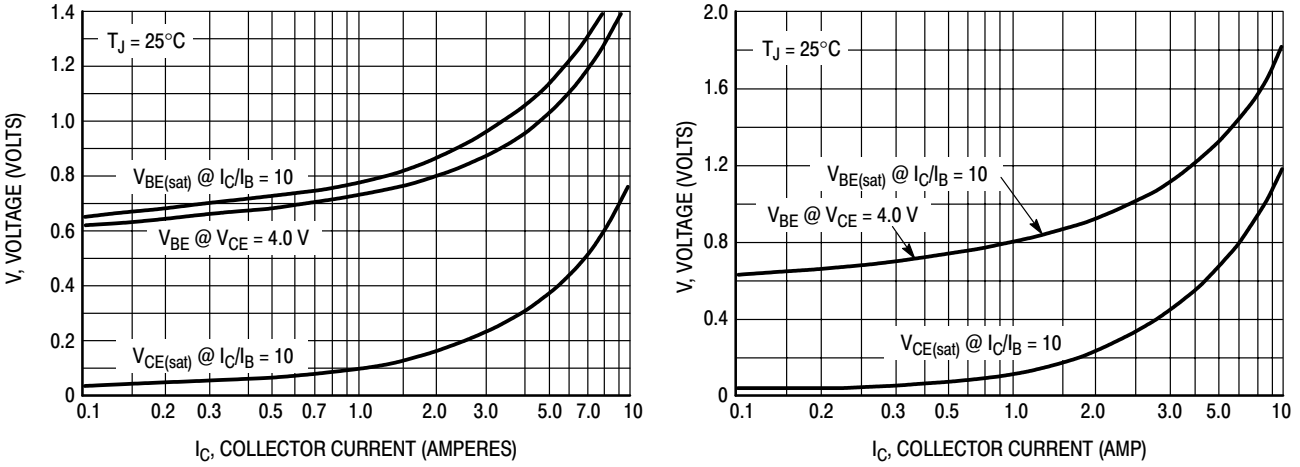


Figure 5. “On” Voltages

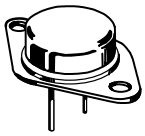
2N3442

High-Power Industrial Transistors

NPN silicon power transistor designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

- Collector –Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 140 Vdc (Min)
- Excellent Second Breakdown Capability

10 AMPERE
POWER TRANSISTOR
NPN SILICON
140 VOLTS
117 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CB}	160	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	10 15**	Adc
Base Current — Continuous Peak	I_B	7.0 —	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

* Indicates JEDEC Registered Data.
** This data guaranteed in addition to JEDEC registered data.

March, 2001 – Rev. 10
Publication Order Number:
2N3442/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	200	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	5.0 30	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 7.5	70 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	—	5.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	5.7	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (2) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	f_T	80	—	kHz
Small–Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	12	72	—

*Indicates JEDEC Registered Data.

NOTES:

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$

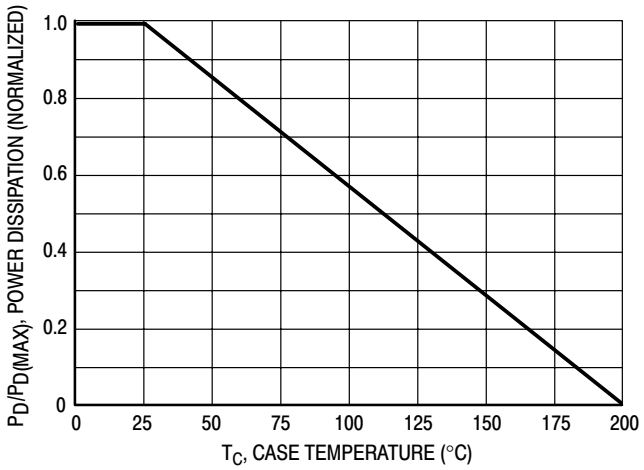


Figure 1. Power Derating

ACTIVE REGION SAFE OPERATING AREA INFORMATION

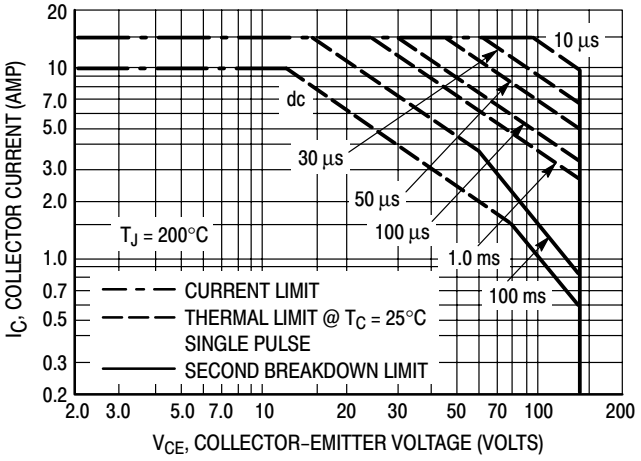


Figure 2. 2N3442

There are two limitations on the power–handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

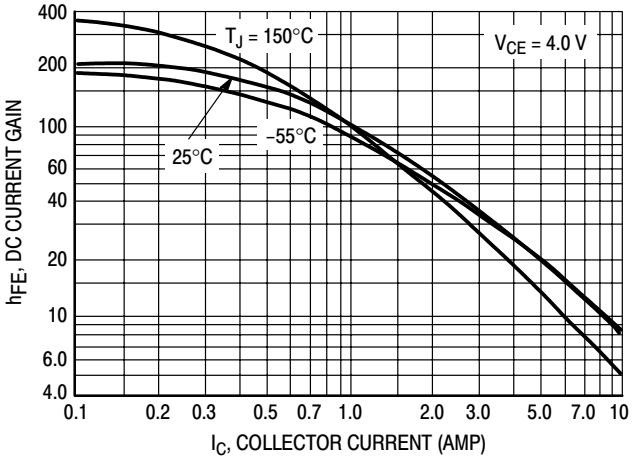


Figure 3. DC Current Gain

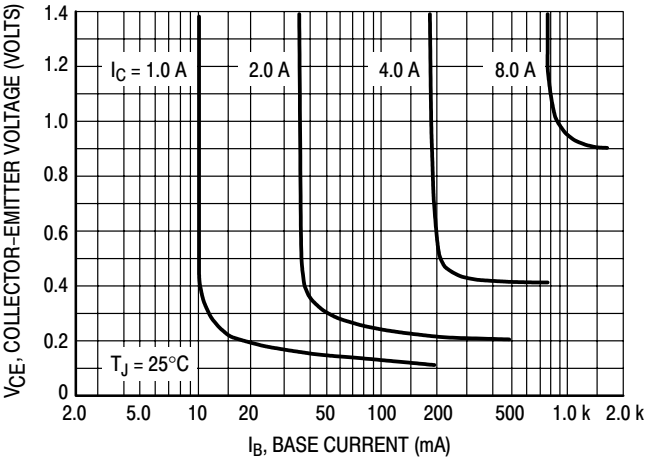


Figure 4. Collector–Saturation Region

High Power NPN Silicon Power Transistors

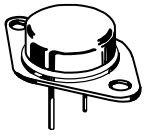
2N3771*
2N3772

*ON Semiconductor Preferred Device

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc — 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc — 2N3772

20 and 30 AMPERE POWER TRANSISTORS NPN SILICON 40 and 60 VOLTS 150 WATTS



CASE 1–07 TO–204AA (TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	Vdc
Collector–Emitter Voltage	V_{CEX}	50	80	Vdc
Collector–Base Voltage	V_{CB}	50	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current — Continuous Peak	I_C	30 30	20 30	Adc
Base Current — Continuous Peak	I_B	7.5 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

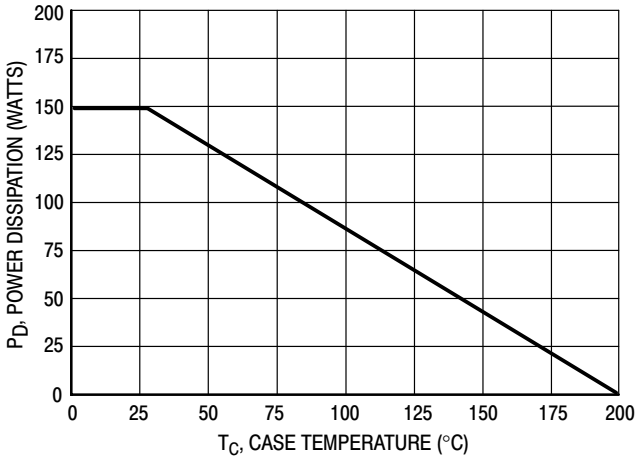


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N3771/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector–Emitter Sustaining Voltage (1) (I_C = 0.2 Adc, I_B = 0)	2N3771 2N3772	$V_{CEO(sus)}$	40 60	— —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CEX(sus)}$	50 80	— —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CER(sus)}$	45 70	— —	Vdc
*Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 25 Vdc, I_B = 0)	 2N3771 2N3772	I_{CEO}	 — —	 10 10	mAdc
*Collector Cutoff Current (V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N3771 2N3772 2N6257 2N3771 2N3772	I_{CEV}	 — — — — —	 2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 2N3771 2N3772	I_{CBO}	 — —	 2.0 5.0	mAdc
*Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0) (V_{BE} = 7.0 Vdc, I_C = 0)	 2N3771 2N3772	I_{EBO}	 — —	 5.0 5.0	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (1) (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc) (I_C = 20 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772 2N3771 2N3772	h_{FE}	 15 15 5.0 5.0	 60 60 — —	—
Collector–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 30 Adc, I_B = 6.0 Adc) (I_C = 20 Adc, I_B = 4.0 Adc)	 2N3771 2N3772 2N3771 2N3772	$V_{CE(sat)}$	 — — — —	 2.0 1.4 4.0 4.0	Vdc
Base–Emitter On Voltage (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772	$V_{BE(on)}$	 — —	 2.7 2.2	Vdc
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	—	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non–repetitive) (V_{CE} = 40 Vdc) (V_{CE} = 60 Vdc)	 2N3771 2N3772	$I_{S/b}$	 3.75 2.5	 — —	Adc

*Indicates JEDEC Registered Data.

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

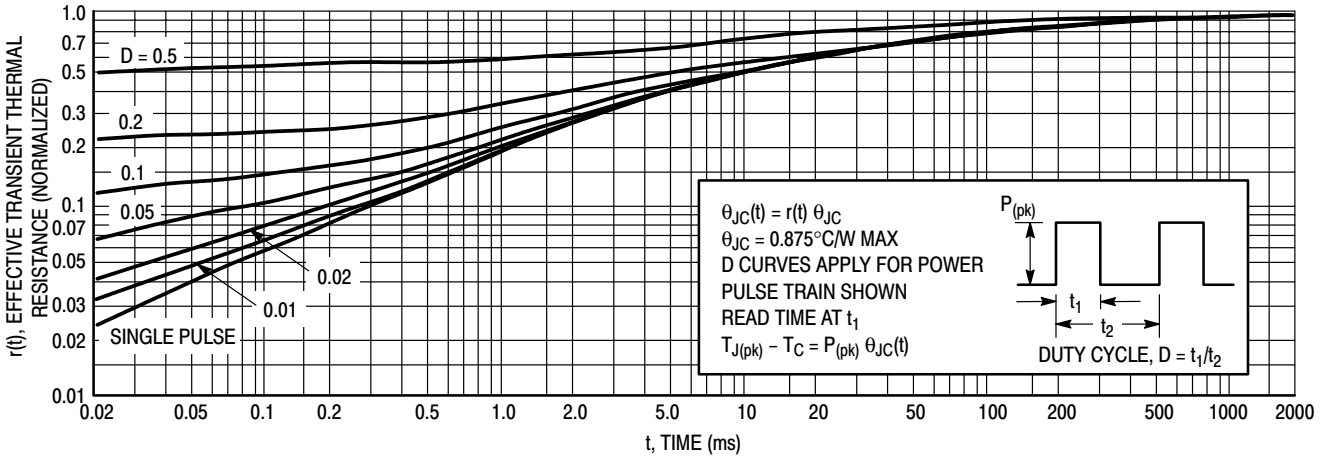


Figure 2. Thermal Response — 2N3771, 2N3772

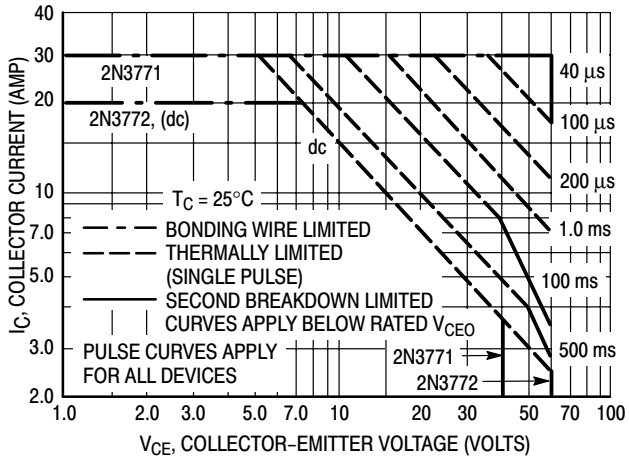


Figure 3. Active−Region Safe Operating Area — 2N3771, 2N3772

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

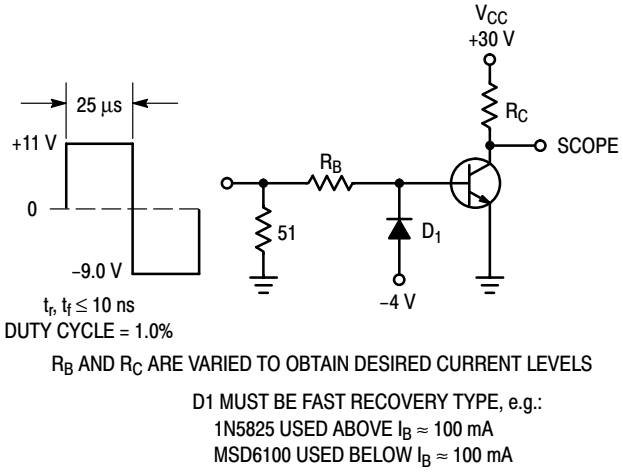


Figure 4. Switching Time Test Circuit

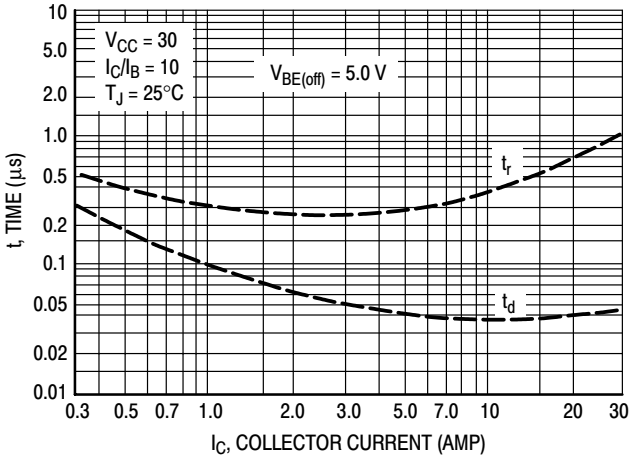


Figure 5. Turn−On Time

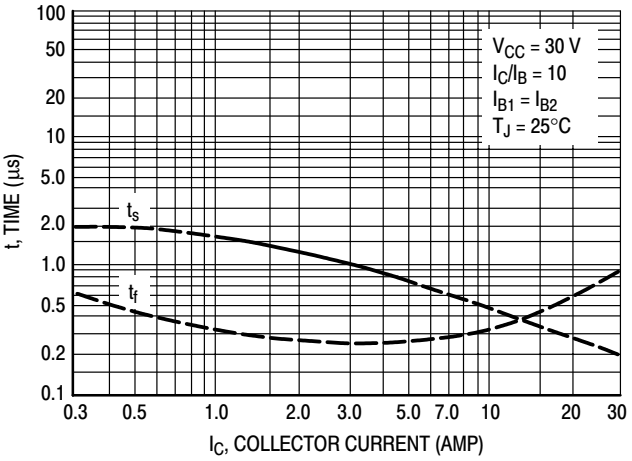


Figure 6. Turn–Off Time

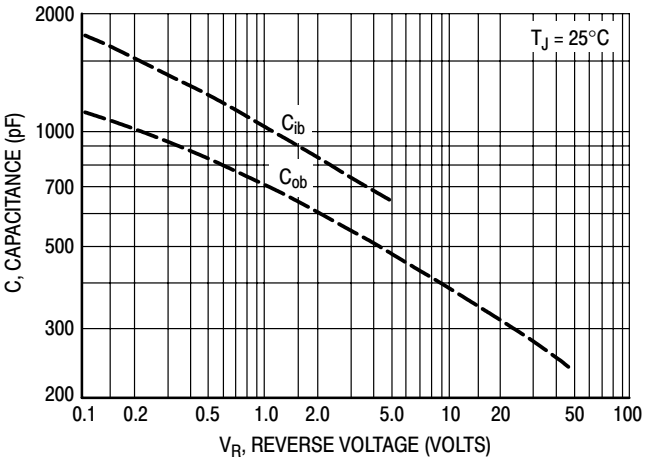


Figure 7. Capacitance

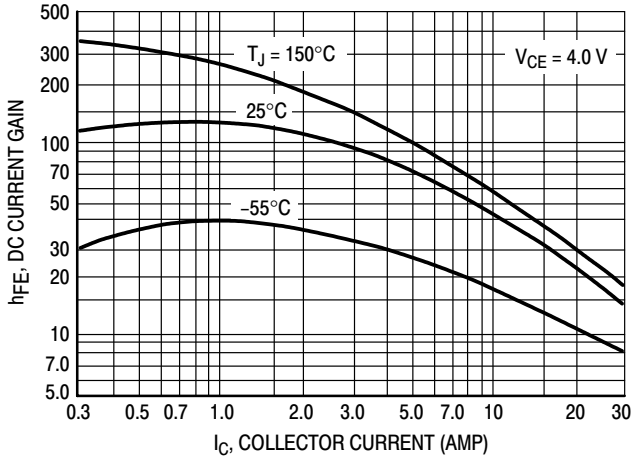


Figure 8. DC Current Gain

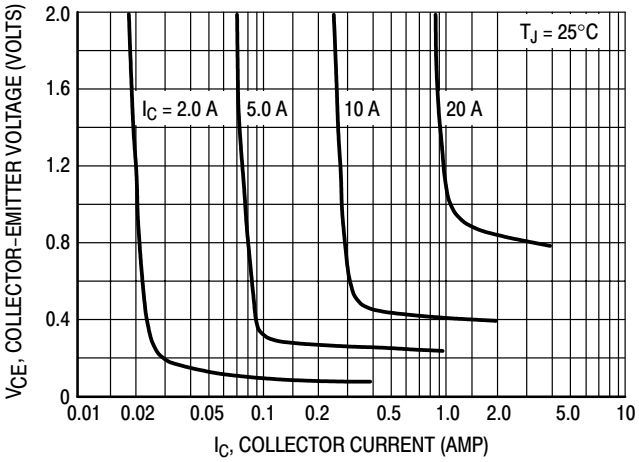


Figure 9. Collector Saturation Region

High Power NPN Silicon Power Transistors

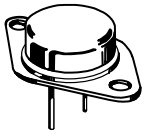
2N3771*
2N3772

*ON Semiconductor Preferred Device

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc — 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc — 2N3772

20 and 30 AMPERE POWER TRANSISTORS NPN SILICON 40 and 60 VOLTS 150 WATTS



CASE 1–07 TO–204AA (TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	Vdc
Collector–Emitter Voltage	V_{CEX}	50	80	Vdc
Collector–Base Voltage	V_{CB}	50	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current — Continuous Peak	I_C	30 30	20 30	Adc
Base Current — Continuous Peak	I_B	7.5 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

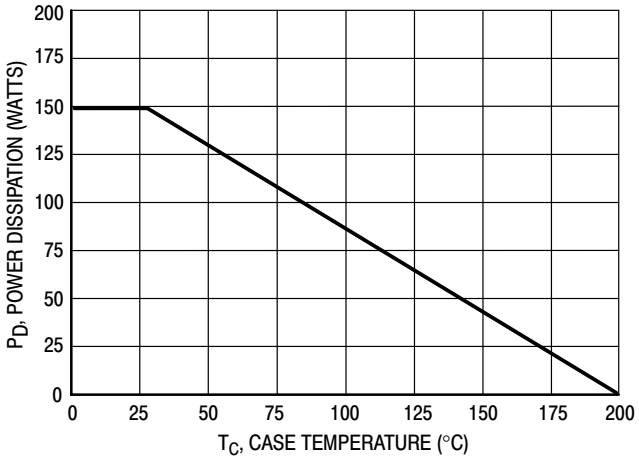


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N3771/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector–Emitter Sustaining Voltage (1) (I_C = 0.2 Adc, I_B = 0)	2N3771 2N3772	$V_{CEO(sus)}$	40 60	— —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CEX(sus)}$	50 80	— —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CER(sus)}$	45 70	— —	Vdc
*Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 25 Vdc, I_B = 0)	 2N3771 2N3772	I_{CEO}	 — —	 10 10	mAdc
*Collector Cutoff Current (V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N3771 2N3772 2N6257 2N3771 2N3772	I_{CEV}	 — — — — —	 2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 2N3771 2N3772	I_{CBO}	 — —	 2.0 5.0	mAdc
*Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0) (V_{BE} = 7.0 Vdc, I_C = 0)	 2N3771 2N3772	I_{EBO}	 — —	 5.0 5.0	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (1) (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc) (I_C = 20 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772 2N3771 2N3772	h_{FE}	 15 15 5.0 5.0	 60 60 — —	—
Collector–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 30 Adc, I_B = 6.0 Adc) (I_C = 20 Adc, I_B = 4.0 Adc)	 2N3771 2N3772 2N3771 2N3772	$V_{CE(sat)}$	 — — — —	 2.0 1.4 4.0 4.0	Vdc
Base–Emitter On Voltage (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772	$V_{BE(on)}$	 — —	 2.7 2.2	Vdc
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	—	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non–repetitive) (V_{CE} = 40 Vdc) (V_{CE} = 60 Vdc)	 2N3771 2N3772	$I_{S/b}$	 3.75 2.5	 — —	Adc

*Indicates JEDEC Registered Data.

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

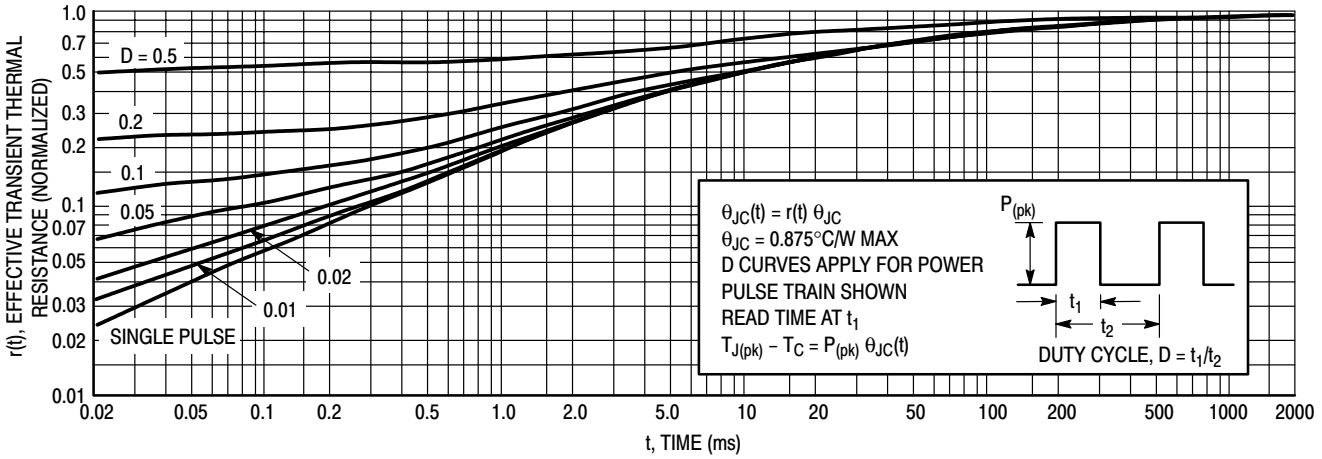


Figure 2. Thermal Response — 2N3771, 2N3772

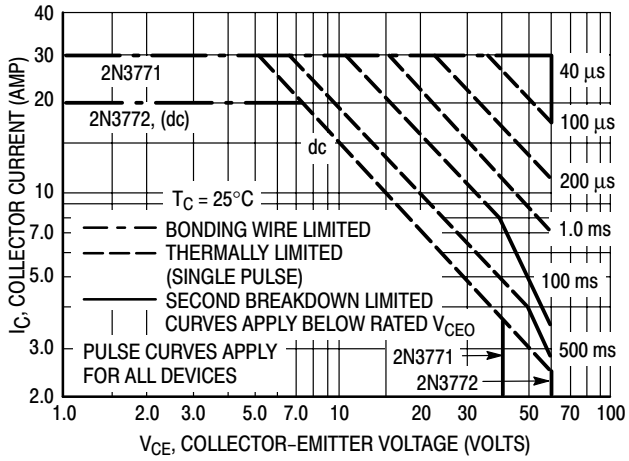


Figure 3. Active−Region Safe Operating Area — 2N3771, 2N3772

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

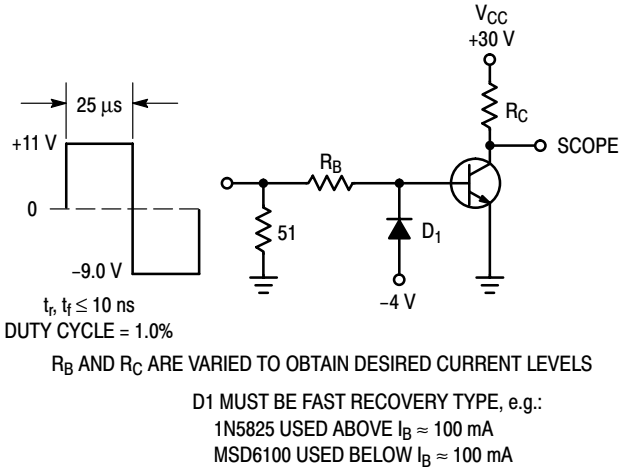


Figure 4. Switching Time Test Circuit

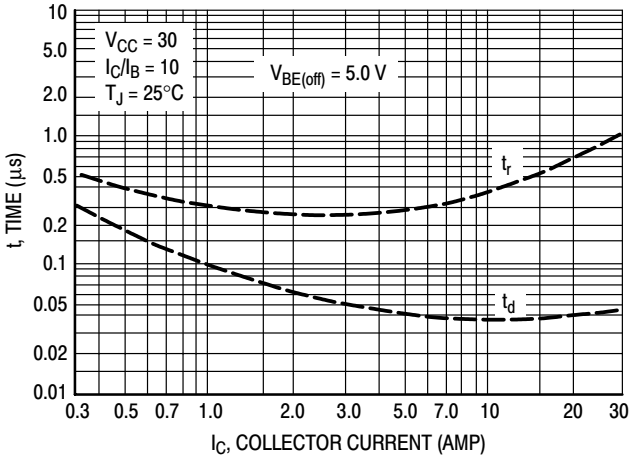


Figure 5. Turn−On Time

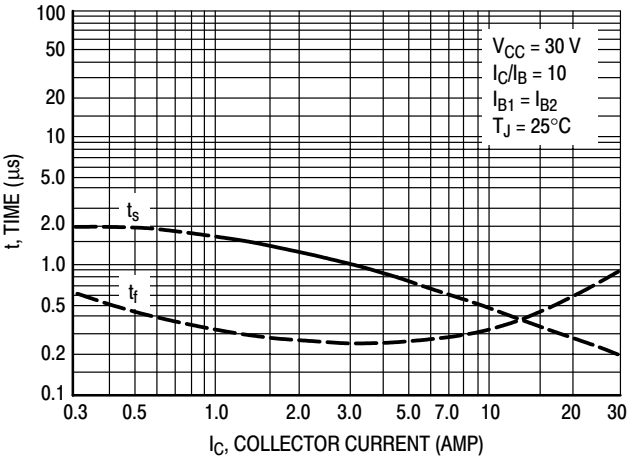


Figure 6. Turn–Off Time

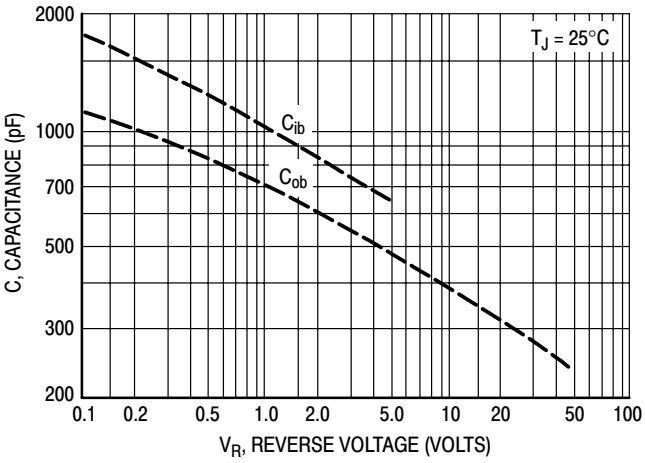


Figure 7. Capacitance

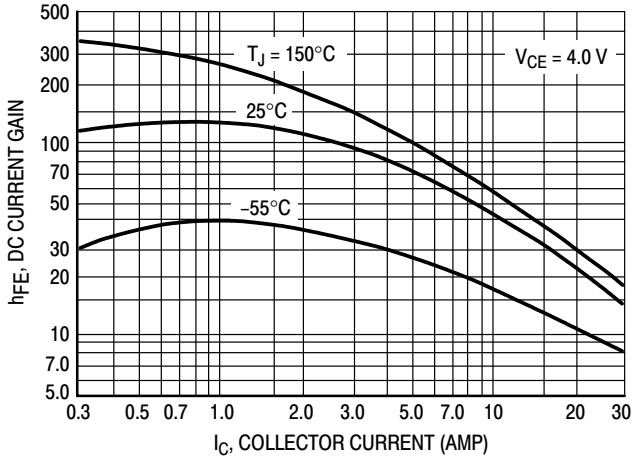


Figure 8. DC Current Gain

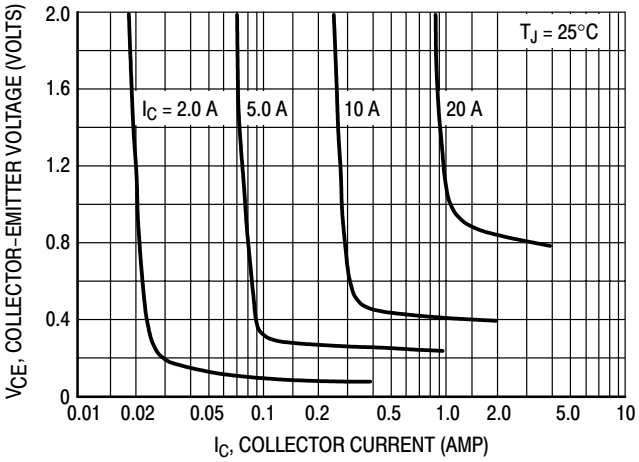


Figure 9. Collector Saturation Region

Complementary Silicon Power Transistors

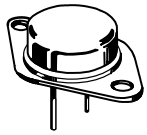
NPN
2N3773*
PNP
2N6609

*ON Semiconductor Preferred Device

The 2N3773 and 2N6609 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested) 150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE
COMPLEMENTARY
POWER TRANSISTORS
140 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector–Emitter Voltage	V_{CEX}	160	Vdc
Collector–Base Voltage	V_{CBO}	160	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 30	Adc
Base Current — Continuous — Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N3773/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (2)				
*Collector–Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
*Collector–Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	—	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	—	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	—	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	—	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	—	5	mAdc
ON CHARACTERISTICS (2)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60 —	—
Collector–Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 1.4 4	Vdc
*Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common–Emitter Small–Signal, Short–Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	—	—
*Small–Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	—	—
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non–repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	—	Adc

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data.

NPN

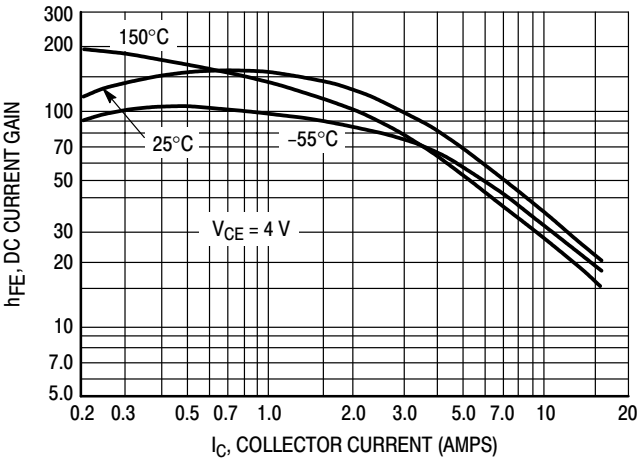


Figure 10. DC Current Gain

PNP

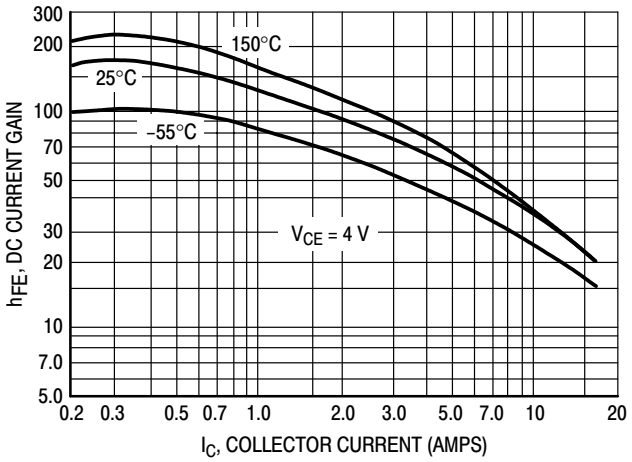


Figure 11. DC Current Gain

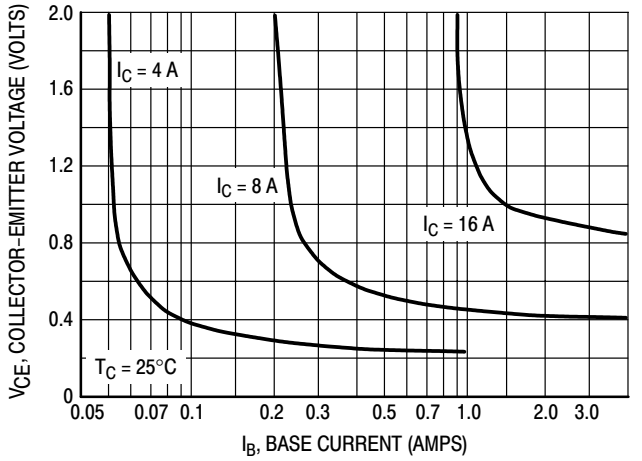


Figure 12. Collector Saturation Region

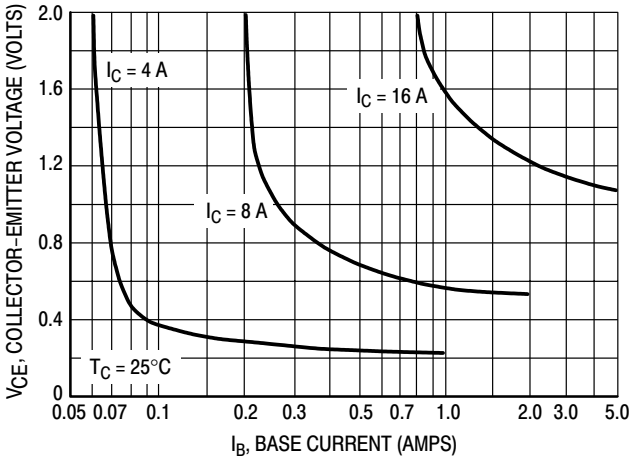


Figure 13. Collector Saturation Region

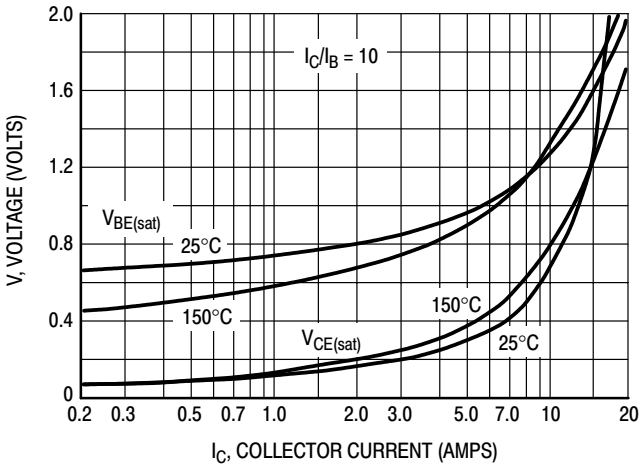


Figure 14. “On” Voltage

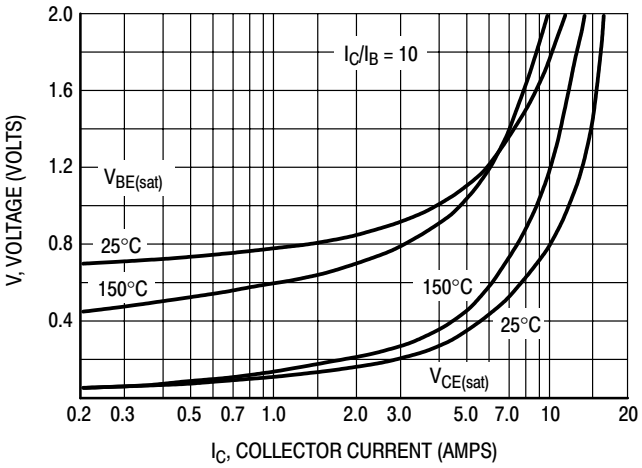


Figure 15. “On” Voltage

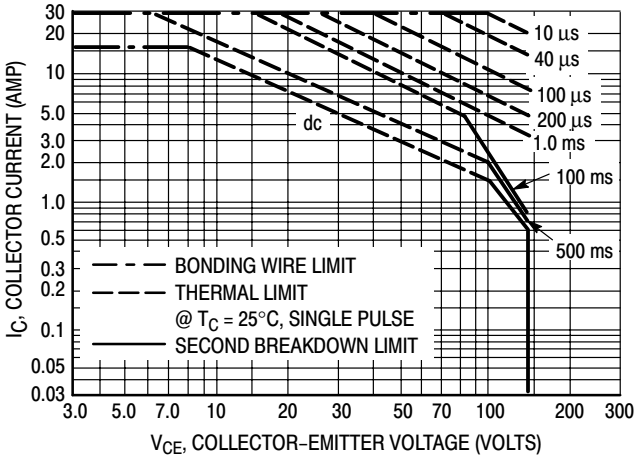


Figure 16. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

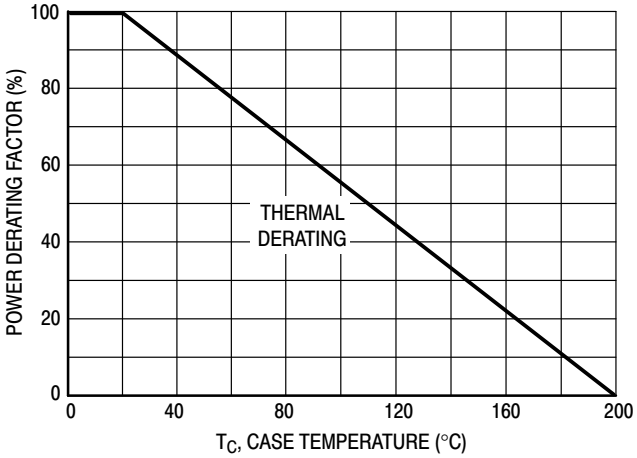


Figure 17. Power Derating

2N4918 thru 2N4920*

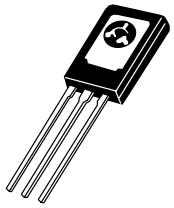
*ON Semiconductor Preferred Device

Medium-Power Plastic PNP Silicon Transistors

. . . designed for driver circuits, switching, and amplifier applications. These high–performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to NPN 2N4921, 2N4922, 2N4923

3 AMPERE GENERAL–PURPOSE POWER TRANSISTORS 40–80 VOLTS 30 WATTS



CASE 77–09 TO–225AA TYPE

***MAXIMUM RATINGS**

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous (1)	I_C*	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

*Indicates JEDEC Registered Data for 2N4918 Series.

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current–handling capability of the device (See Figure 5).

(2) Recommend use of thermal compound for lowest thermal resistance.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

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Publication Order Number: 2N4918/D

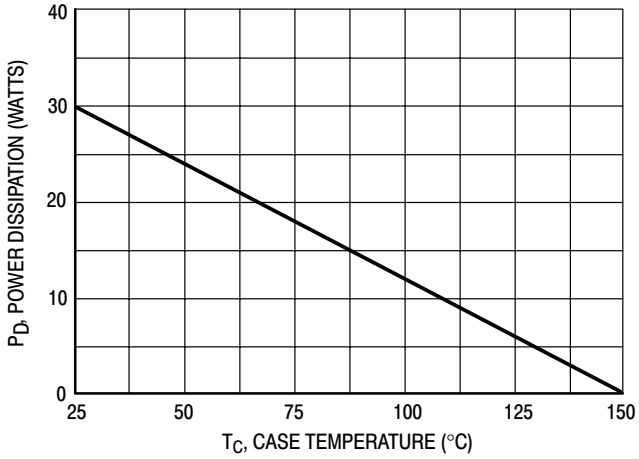


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N4918 2N4919 2N4920	$V_{CEO(sus)}$	 40 60 80	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N4918 2N4919 2N4920	I_{CEO}	 — — —	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	 — —	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30 10	 — 150 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	100	pF
Small–Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

*Indicates JEDEC Registered Data.
(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

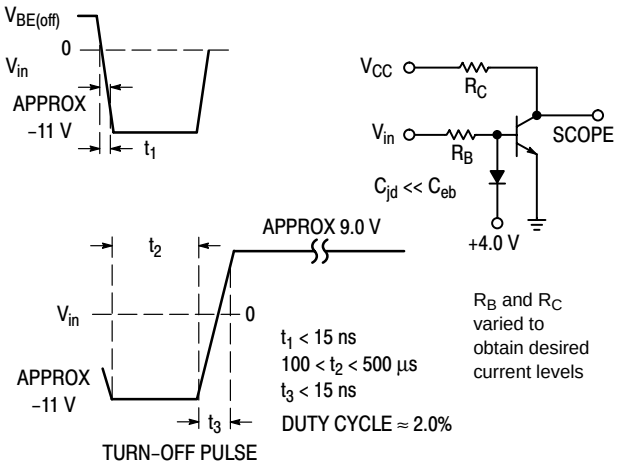


Figure 2. Switching Time Equivalent Test Circuit

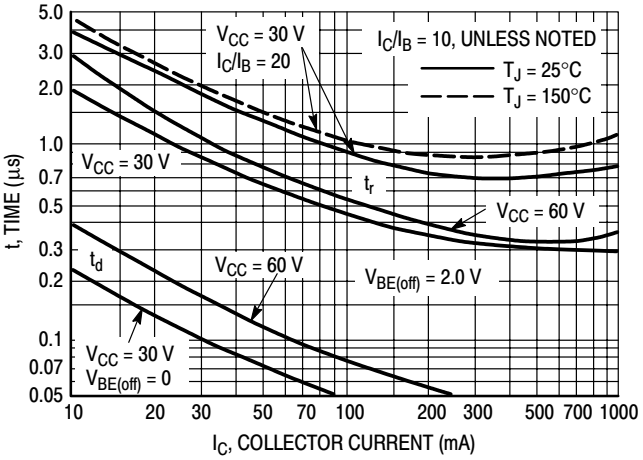


Figure 3. Turn–On Time

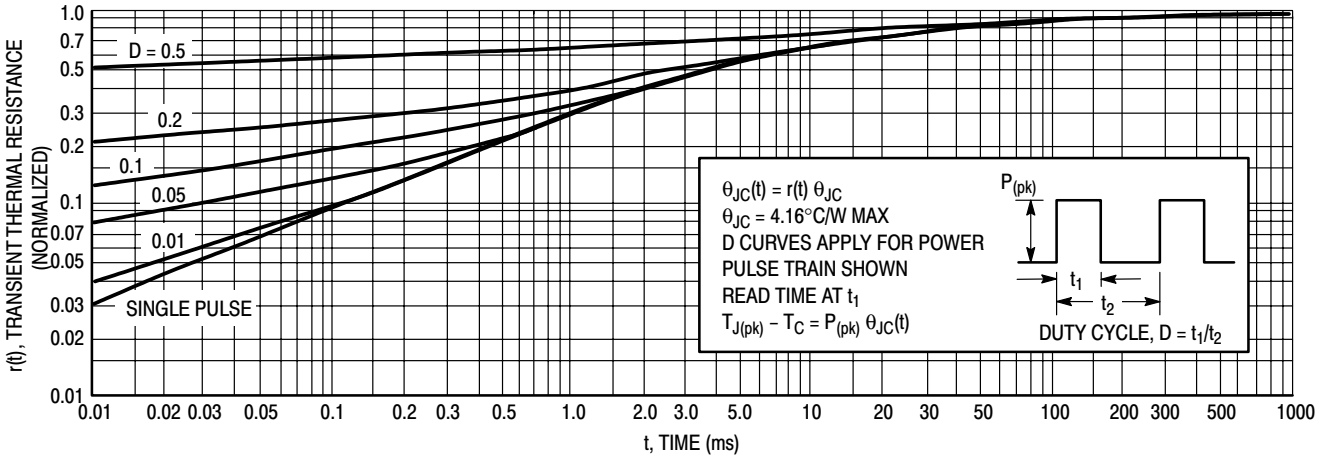


Figure 4. Thermal Response

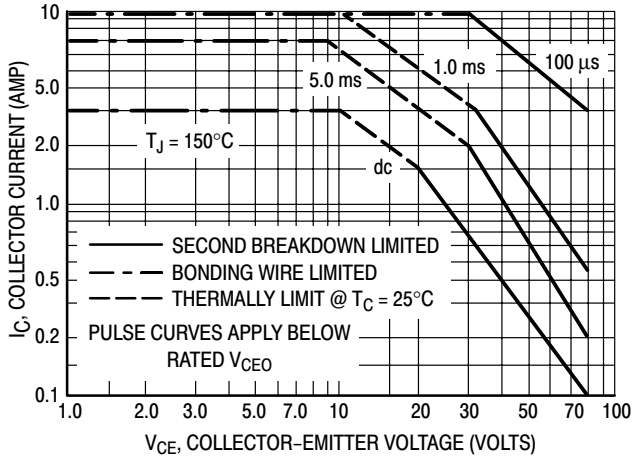


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

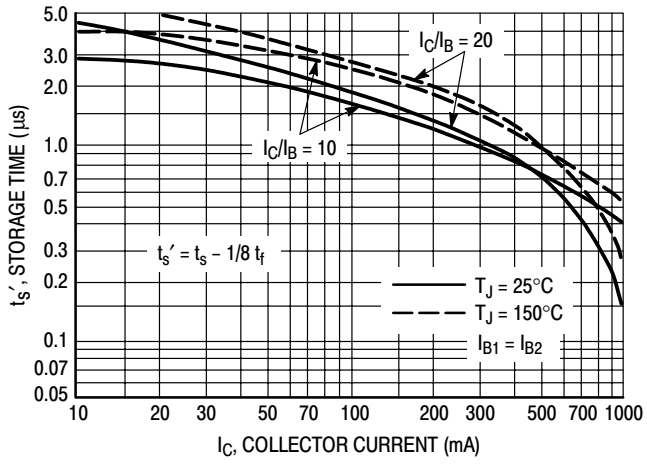


Figure 6. Storage Time

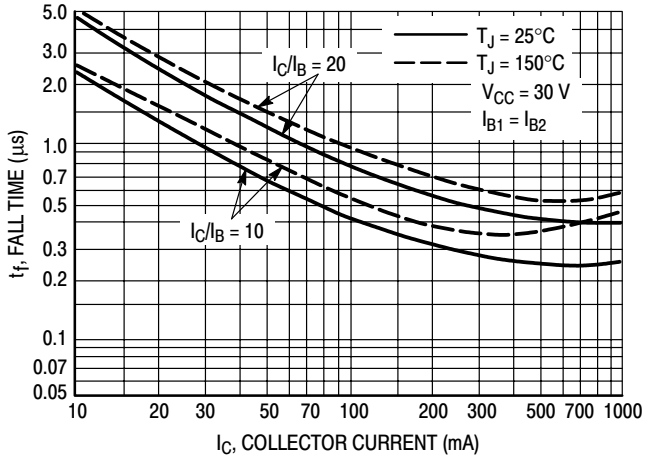


Figure 7. Fall Time

TYPICAL DC CHARACTERISTICS

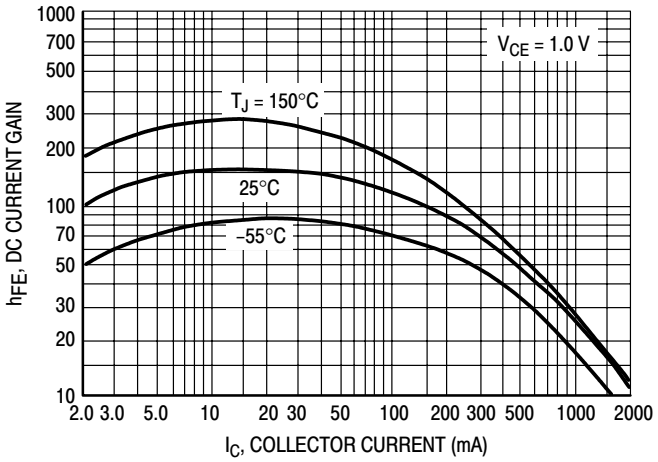


Figure 8. Current Gain

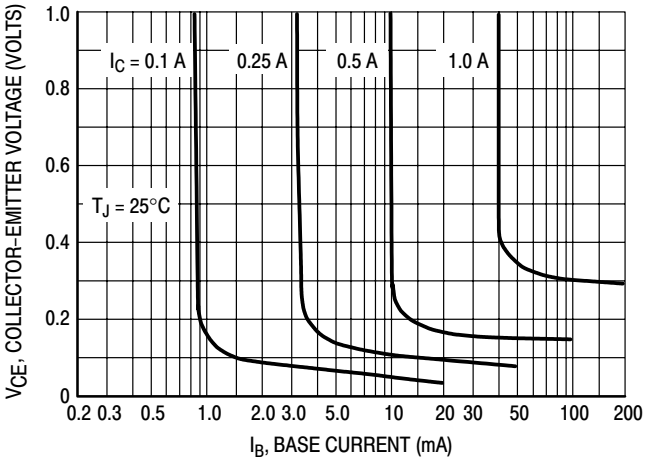


Figure 9. Collector Saturation Region

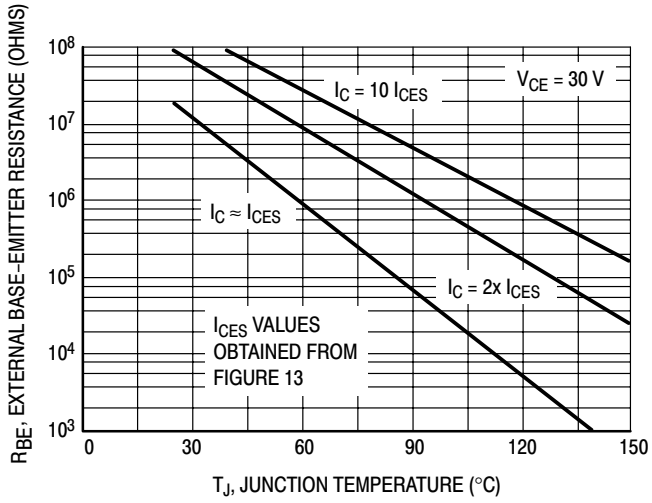


Figure 10. Effects of Base−Emitter Resistance

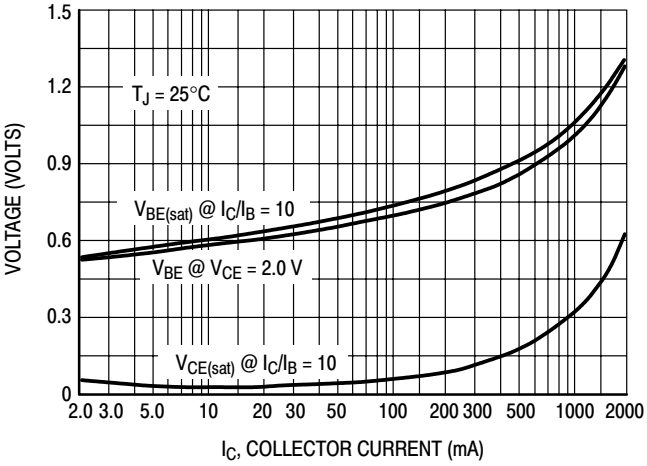


Figure 11. "On" Voltage

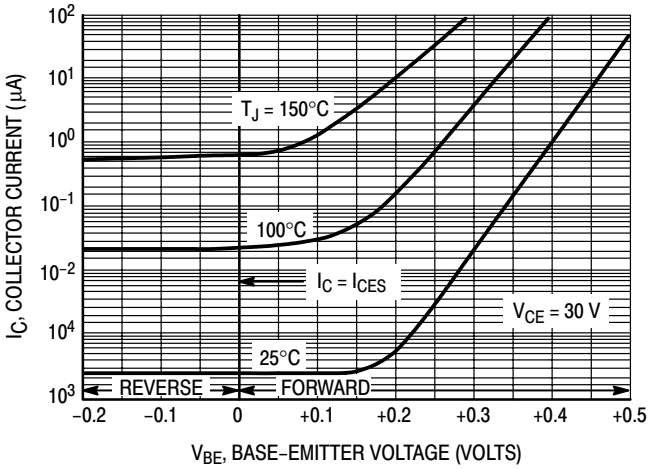


Figure 12. Collector Cut−Off Region

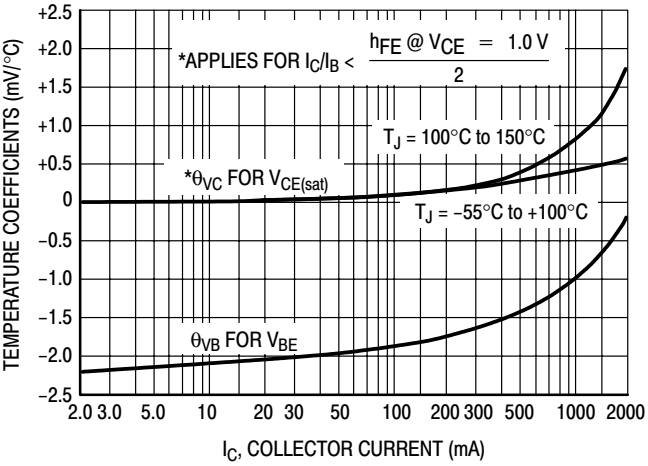


Figure 13. Temperature Coefficients

Medium-Power Plastic NPN Silicon Transistors

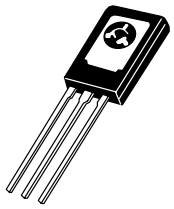
2N4921 thru 2N4923 *

*ON Semiconductor Preferred Device

. . . designed for driver circuits, switching, and amplifier applications. These high–performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920

1 AMPERE GENERAL–PURPOSE POWER TRANSISTORS 40–80 VOLTS 30 WATTS



CASE 77–09 TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous (1)	I_C	1.0 3.0			Adc
Base Current — Continuous	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current handling capability of the device (see Figures 5 and 6)

(2) Recommend use of thermal compound for lowest thermal resistance.

*Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N4921/D

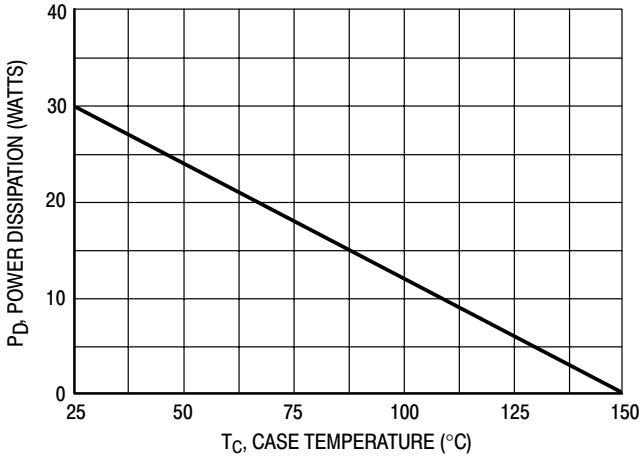


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (3) (I_C = 0.1 Adc, I_B = 0)	2N4921 2N4922 2N4923	$V_{CEO(sus)}$	 40 60 80	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N4921 2N4922 2N4923	I_{CEO}	 — — —	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	 — —	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (3) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30 10	 — 150 —	—
Collector–Emitter Saturation Voltage (3) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (3) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (3) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	100	pF
Small–Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(3) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.
*Indicates JEDEC Registered Data.

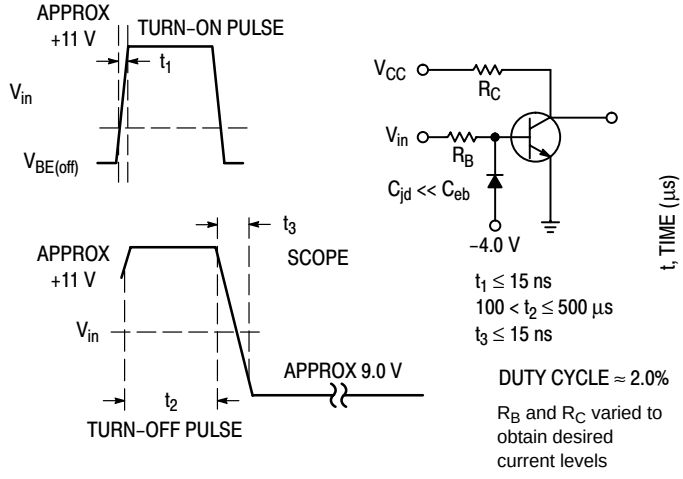


Figure 2. Switching Time Equivalent Circuit

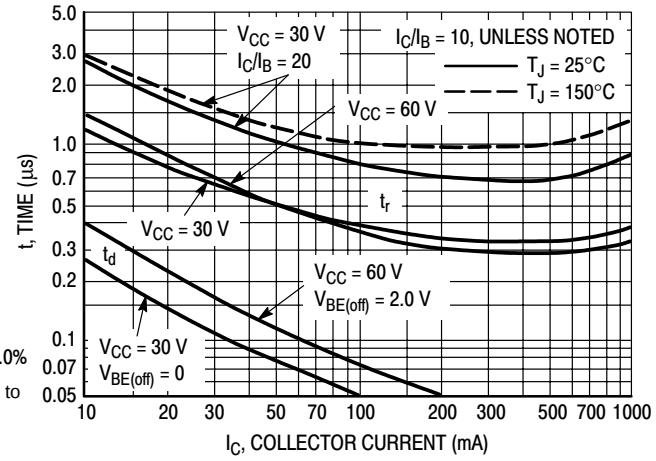


Figure 3. Turn–On Time

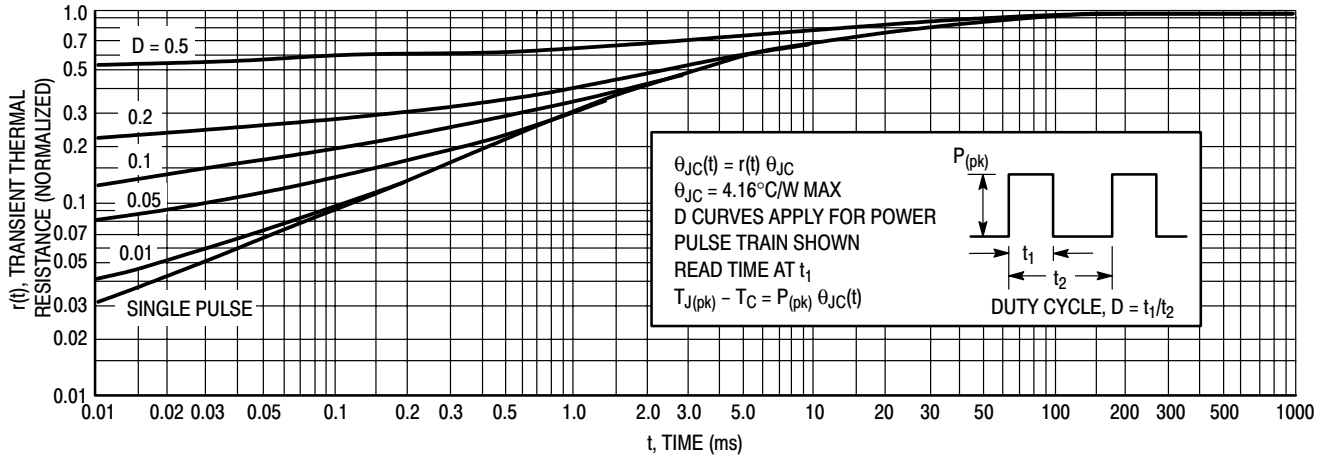


Figure 4. Thermal Response

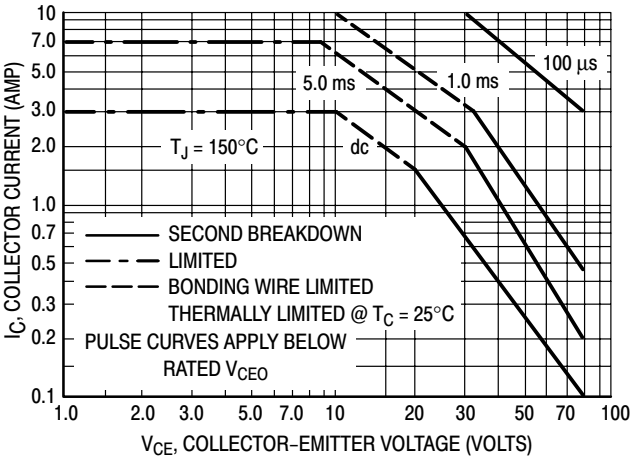


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

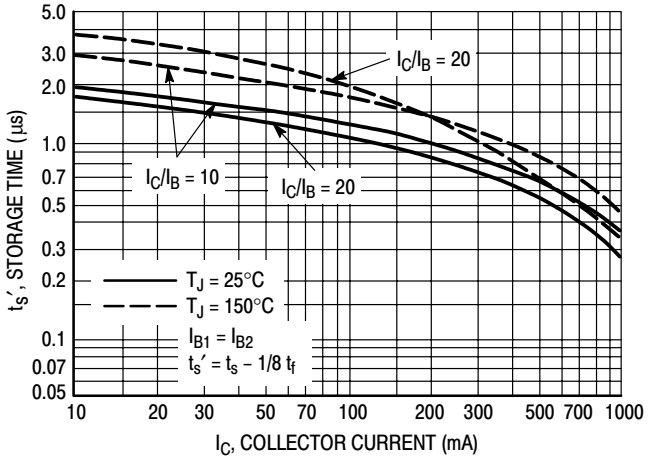


Figure 6. Storage Time

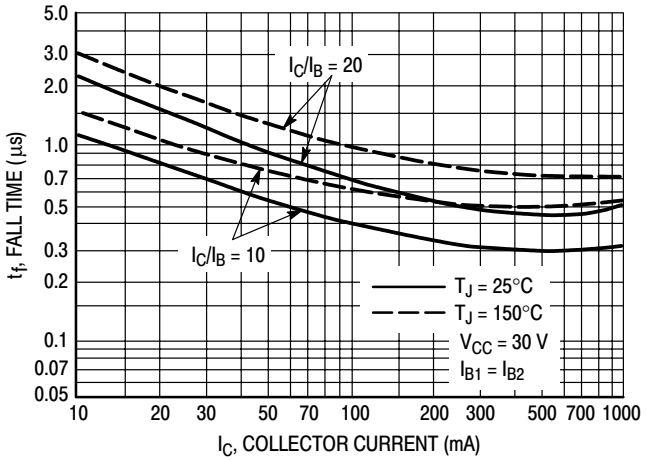


Figure 7. Fall Time

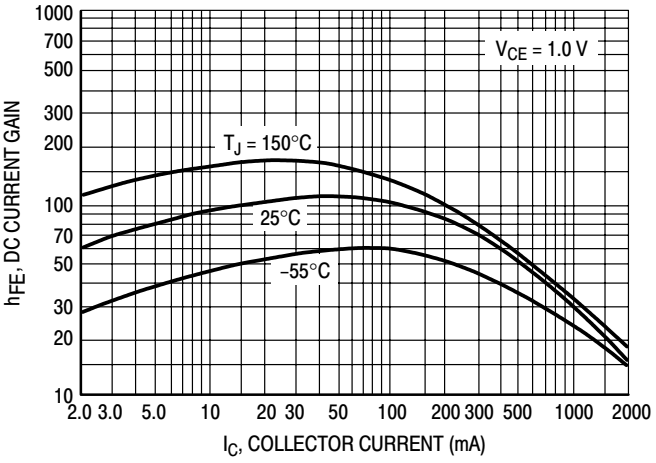


Figure 8. Current Gain

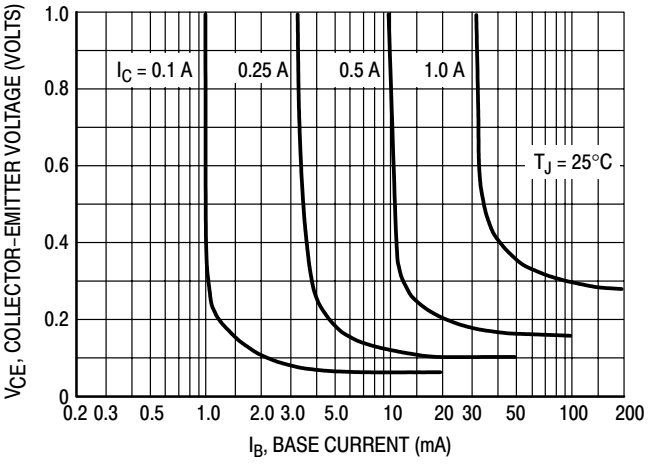


Figure 9. Collector Saturation Region

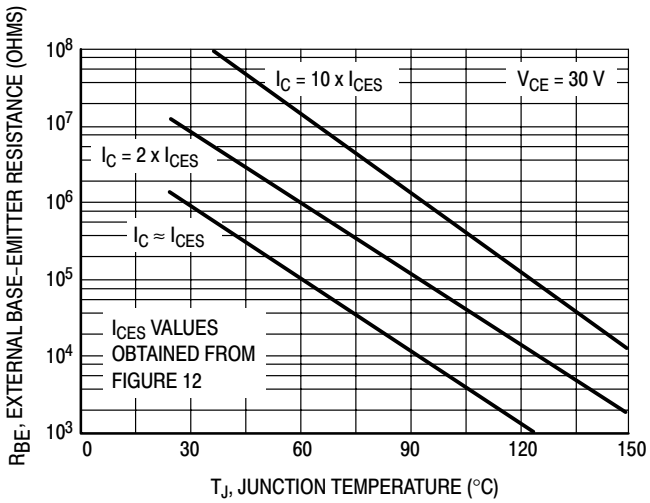


Figure 10. Effects of Base−Emitter Resistance

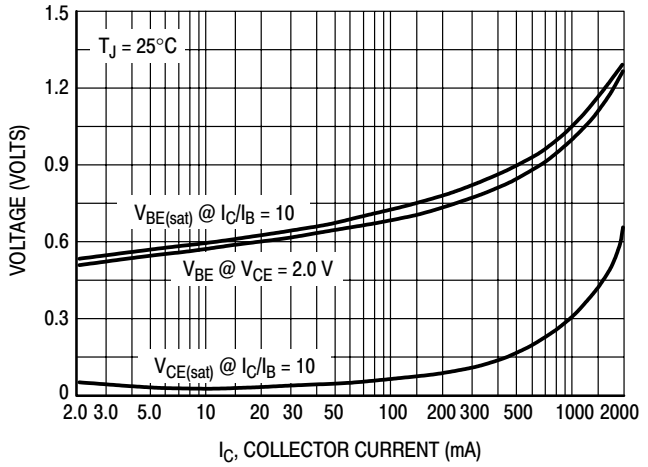


Figure 11. “On” Voltage

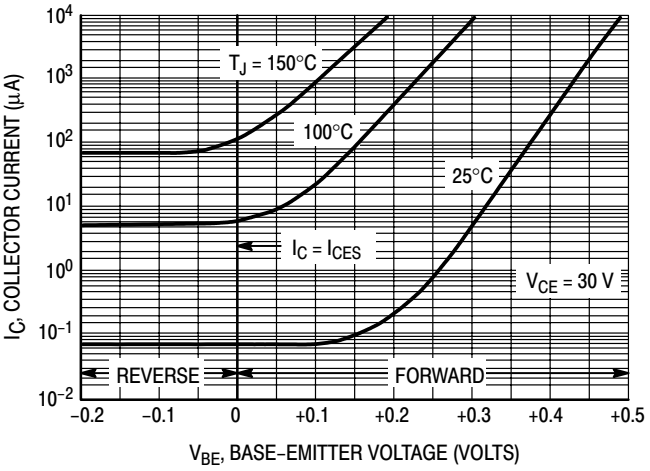


Figure 12. Collector Cut−Off Region

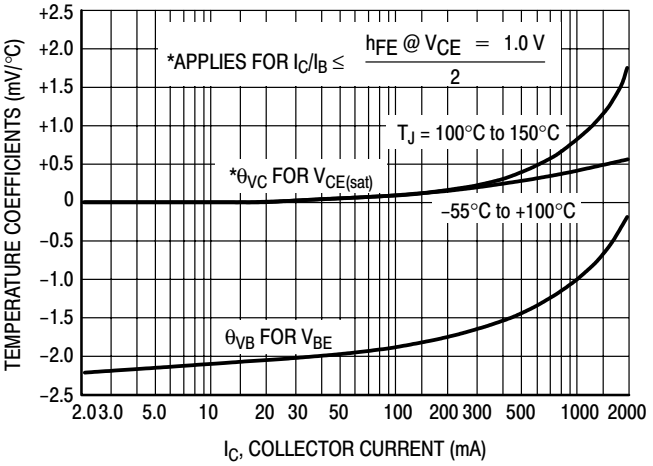


Figure 13. Temperature Coefficients

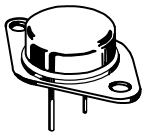
2N5038

NPN Silicon Transistors

. . . fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide–band amplifiers and power oscillators in industrial and commercial applications.

- High Speed – t_f = 0.5 μs (Max)
- High Current – $I_{C(max)}$ = 30 Amps
- Low Saturation – $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 20 Amps

20 AMPERE
NPN SILICON
POWER TRANSISTOR
90 VOLTS
140 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CBO}	150	Vdc
Collector–Emitter Voltage	V_{CEV}	150	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	20 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	140 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 10 ms, Duty Cycle ≤ 50%.

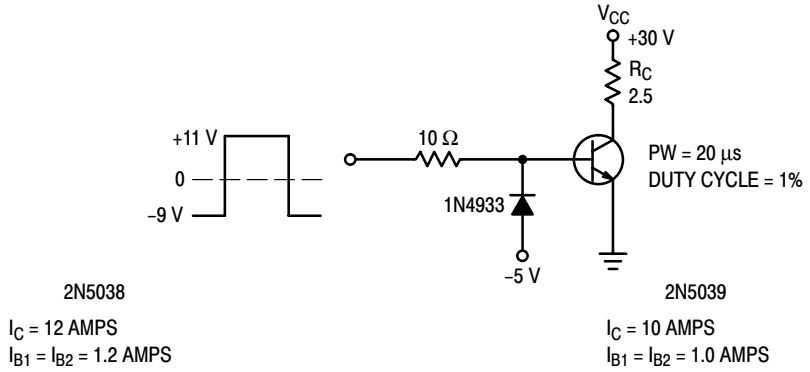


Figure 1. Switching Time Test Circuit

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	90	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	50 10	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0) (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}	– –	5 50	mAdc
ON CHARACTERISTICS (2)				
DC Current Gain (I_C = 12 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	100	–
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)	$V_{CE(sat)}$	–	2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)	$V_{BE(sat)}$	–	3.3	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common–Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio (I_C = 2 Adc, V_{CE} = 10 Vdc, f = 5 MHz)	$\|h_{fe}\|$	12	–	–
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD				
Rise Time (V_{CC} = 30 Vdc)	t_r	–	0.5	μs
Storage Time (I_C = 12 Adc, I_{B1} = I_{B2} = 1.2 Adc)	t_s	–	1.5	μs

*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width ≤ 300, μs, Duty Cycle ≤ 2%.

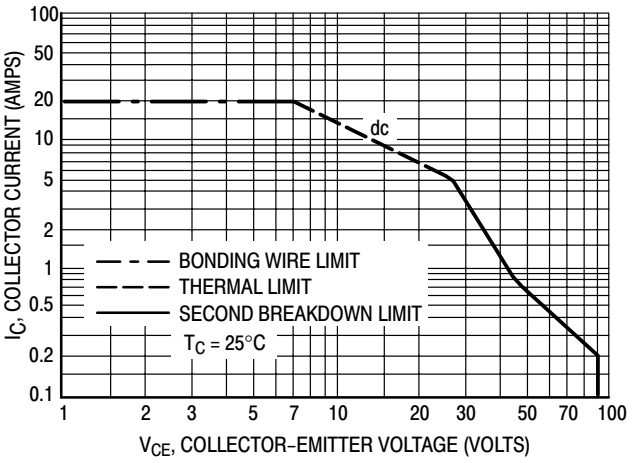


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

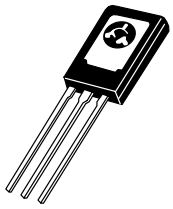
Silicon NPN Power Transistors

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5194, 2N5195.

2N5191
2N5192*

*ON Semiconductor Preferred Device

4 AMPERE
POWER TRANSISTORS
SILICON NPN
60–80 VOLTS
40 WATTS



CASE 77–09
TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N5191	2N5192	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	 2N5191 2N5192	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N5191 2N5192	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N5191 2N5192 2N5191 2N5192	I_{CEX}	 — — — —	 0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5191 2N5192	I_{CBO}	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
*Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N5191/D

***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (2)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5191		25	100	
	2N5192		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5191		10	—	
	2N5192		7.0	—	
Collector–Emitter Saturation Voltage (2)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			—	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			—	1.4	
Base–Emitter On Voltage (2)		$V_{BE(on)}$	—	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	2.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
*Indicates JEDEC Registered Data.

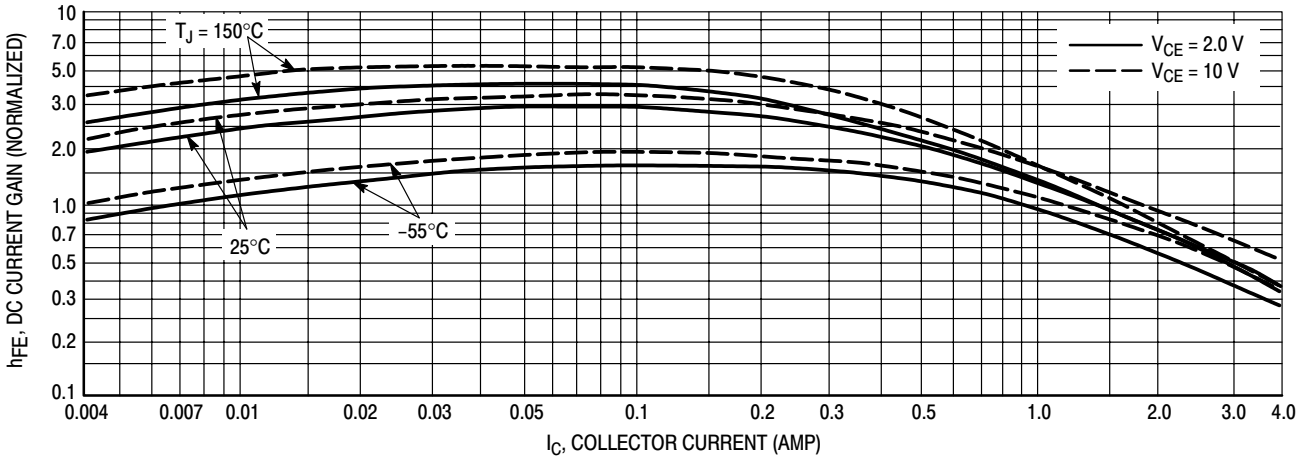


Figure 1. DC Current Gain

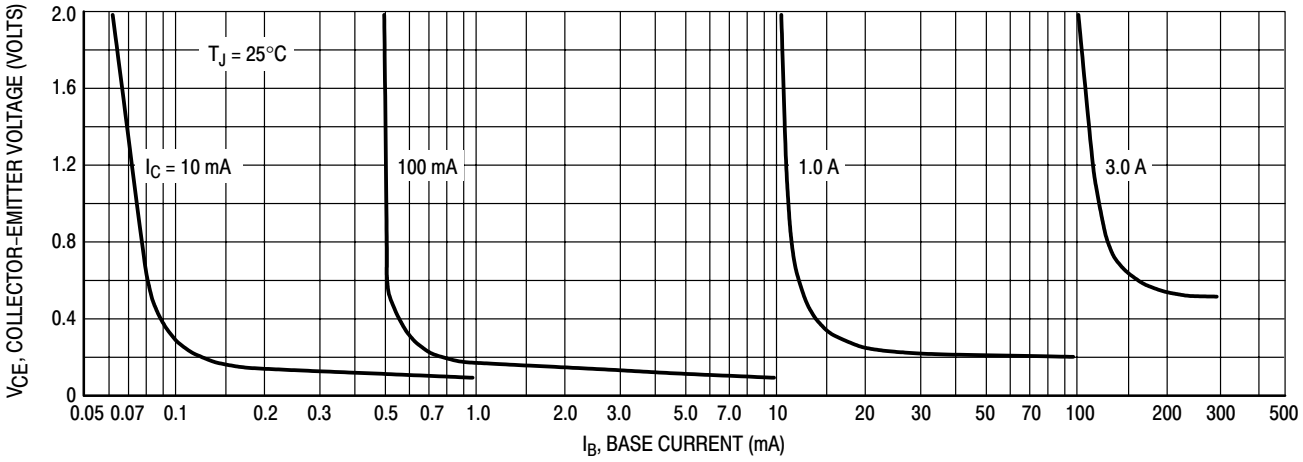


Figure 2. Collector Saturation Region

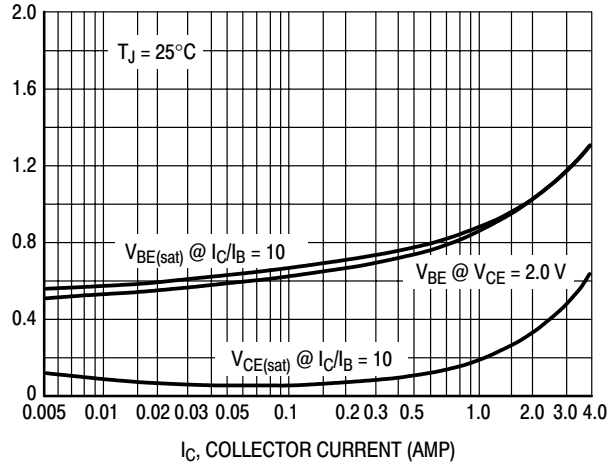


Figure 3. “On” Voltages

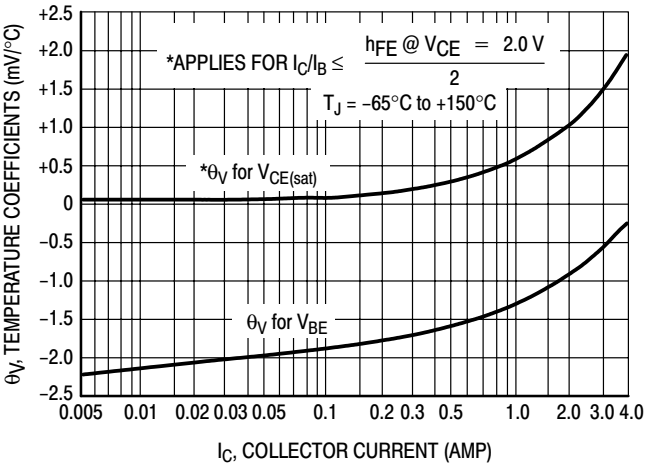


Figure 4. Temperature Coefficients

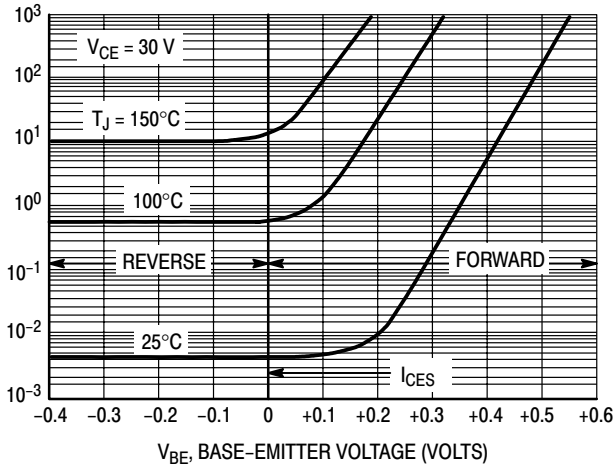


Figure 5. Collector Cut−Off Region

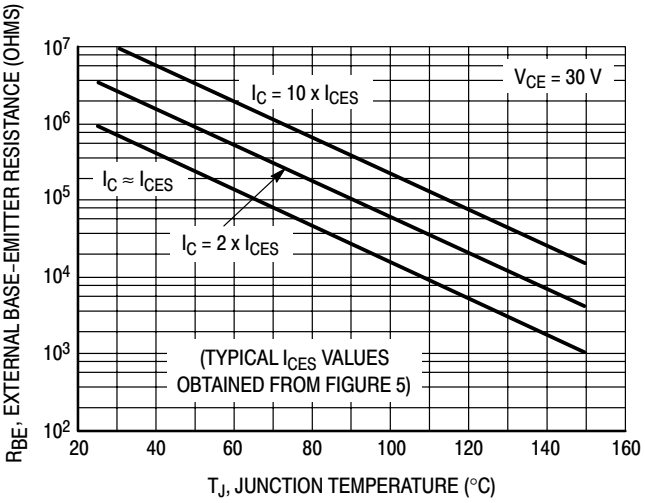


Figure 6. Effects of Base−Emitter Resistance

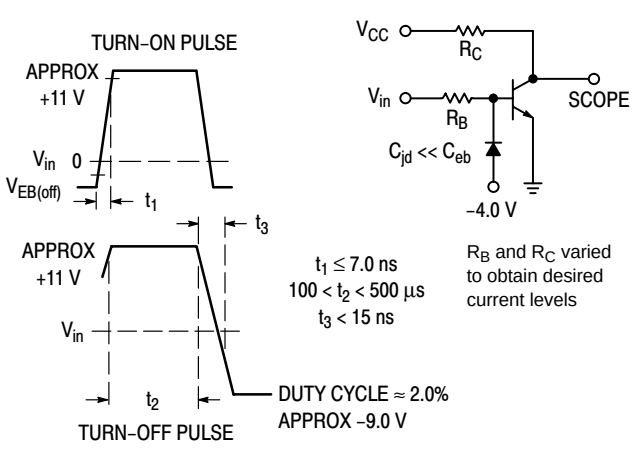


Figure 7. Switching Time Equivalent Test Circuit

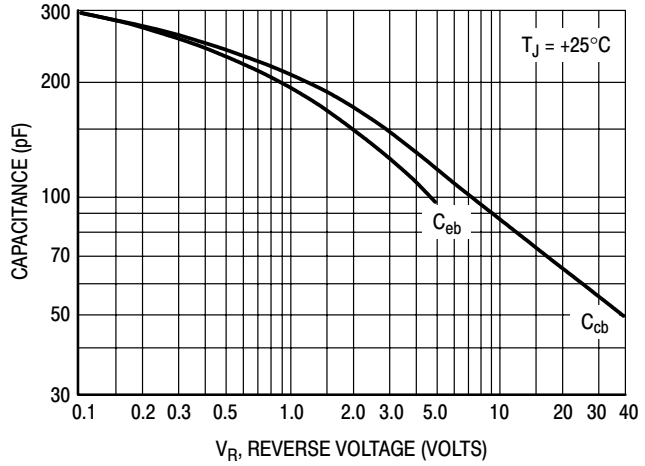


Figure 8. Capacitance

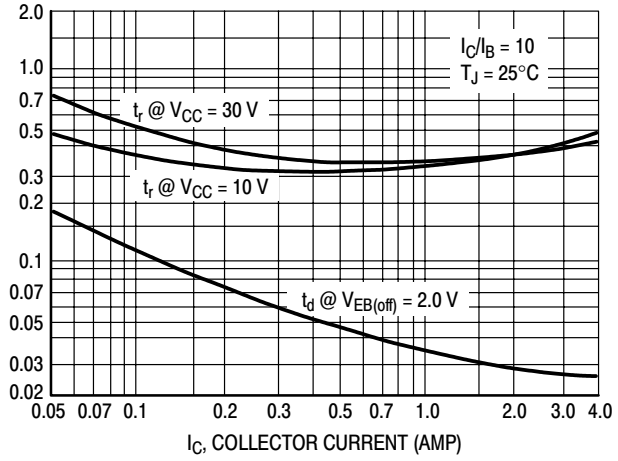


Figure 9. Turn–On Time

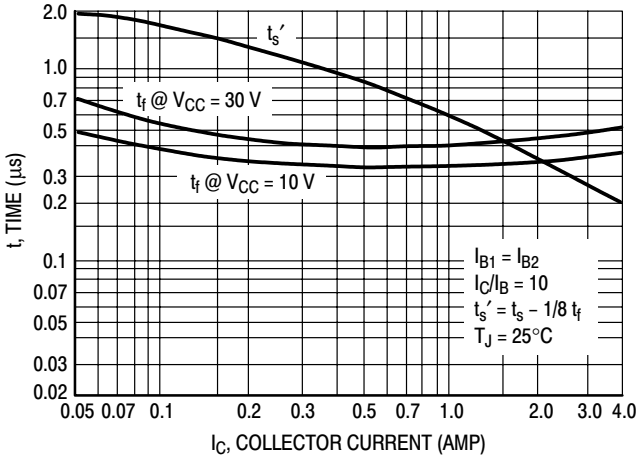


Figure 10. Turn–Off Time

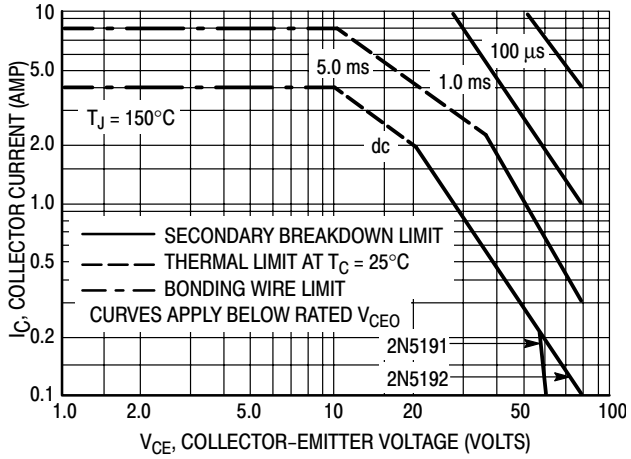


Figure 11. Rating and Thermal Data
Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

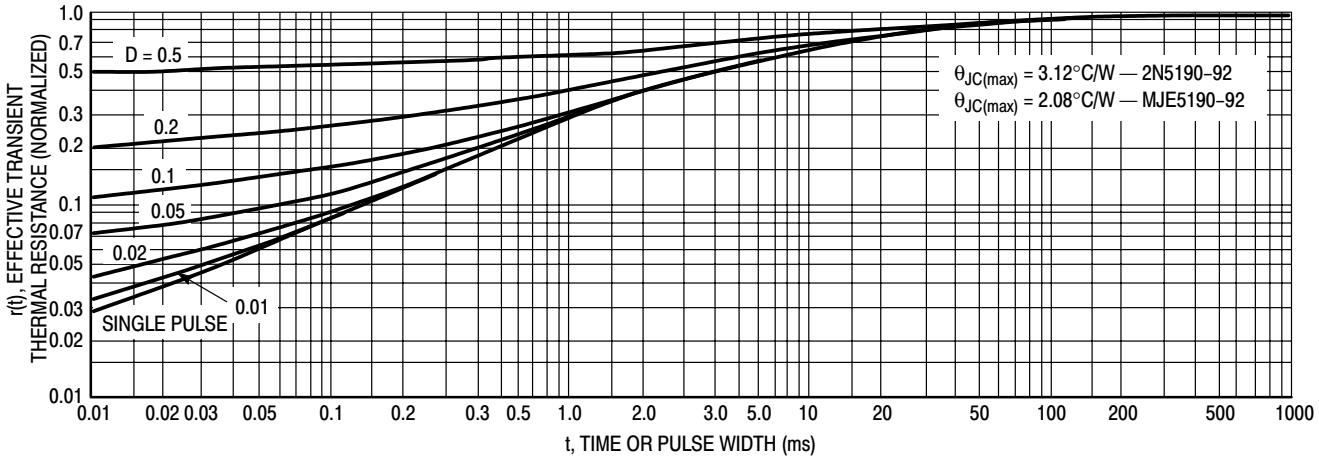
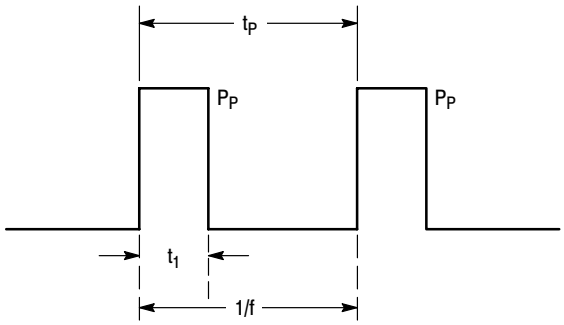


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE, $D = t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

Figure A

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5190 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in function temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

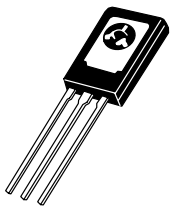
Silicon PNP Power Transistors

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5191, 2N5192

2N5194
2N5195*

*ON Semiconductor Preferred Device

4 AMPERE
POWER TRANSISTORS
SILICON PNP
60–80 VOLTS



CASE 77–09
TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N5194	2N5195	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	 2N5194 2N5195	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N5194 2N5195	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N5194 2N5195 2N5194 2N5195	I_{CEX}	 — — — —	 0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5194 2N5195	I_{CBO}	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N5194/D

***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (2)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5194		25	100	
	2N5195		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5194		10	—	
	2N5195		7.0	—	
Collector–Emitter Saturation Voltage (2)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			—	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			—	1.4	
Base–Emitter On Voltage (2)		$V_{BE(on)}$	—	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	2.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					

*Indicates JEDEC Registered Data.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

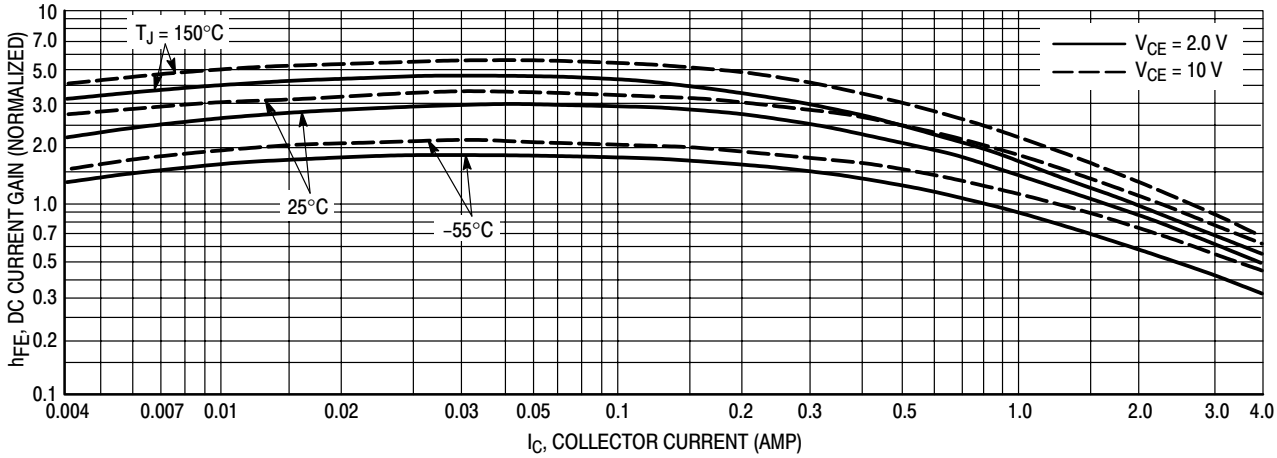


Figure 1. DC Current Gain

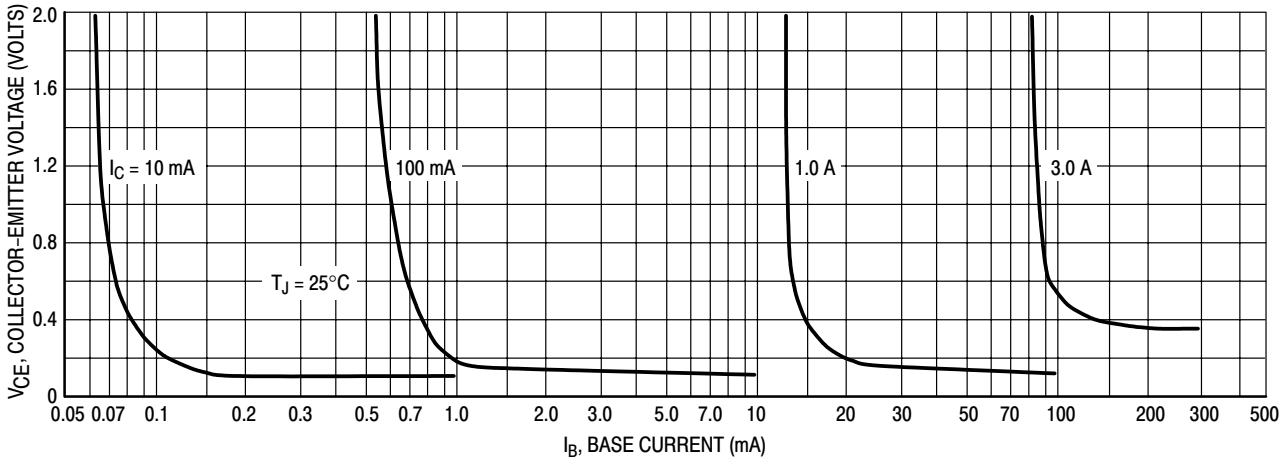


Figure 2. Collector Saturation Region

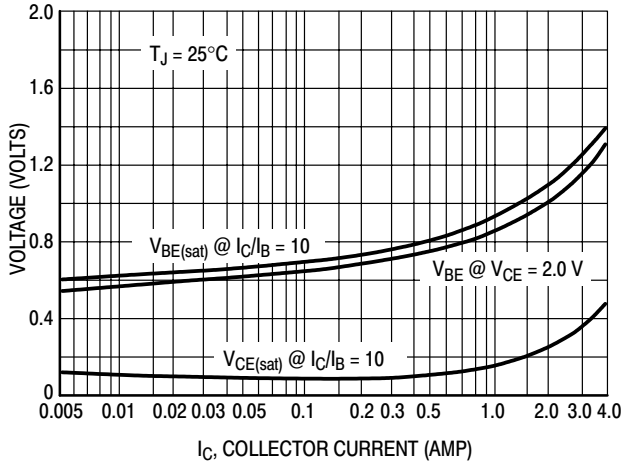


Figure 3. “On” Voltage

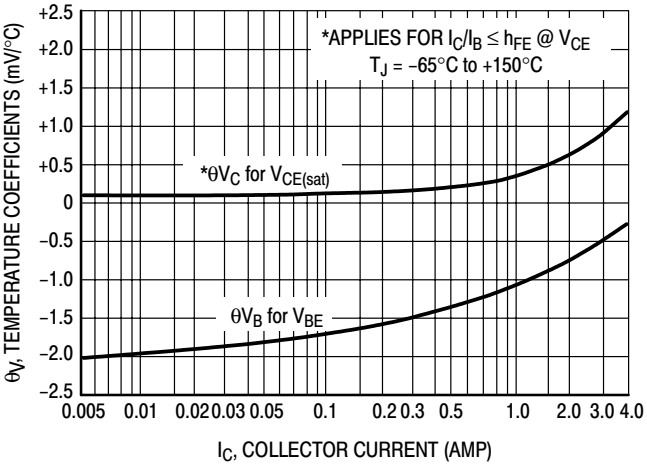


Figure 4. Temperature Coefficients

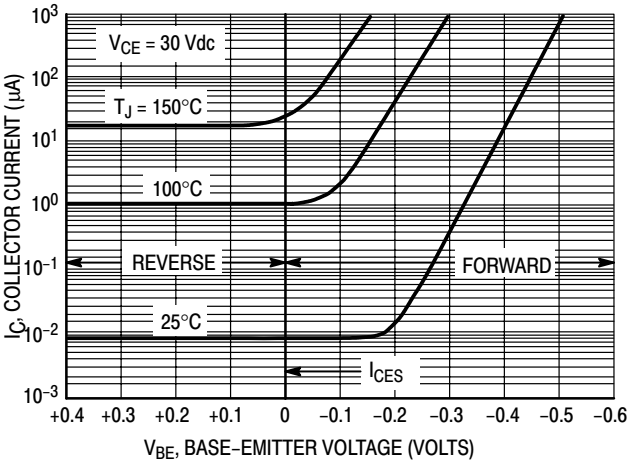


Figure 5. Collector Cut−Off Region

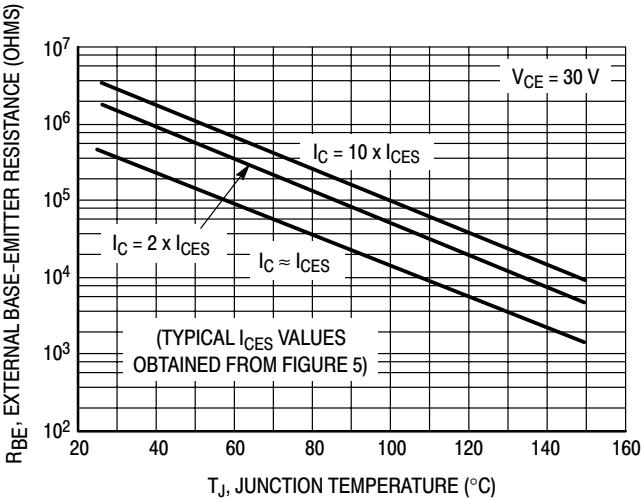


Figure 6. Effects of Base−Emitter Resistance

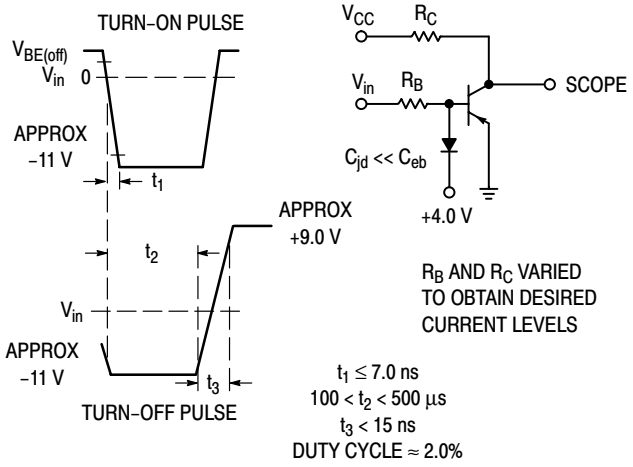


Figure 7. Switching Time Equivalent Test Circuit

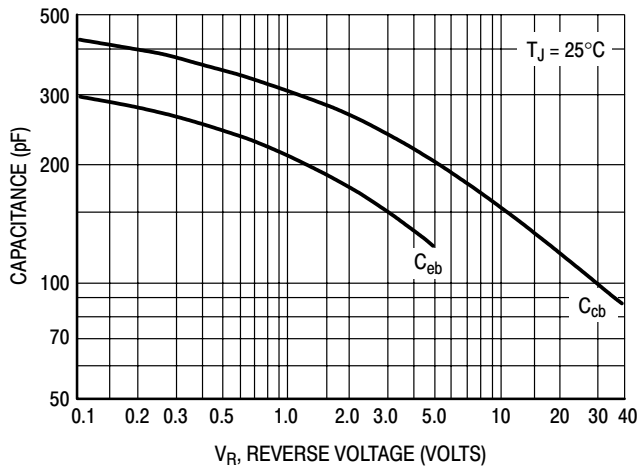


Figure 8. Capacitance

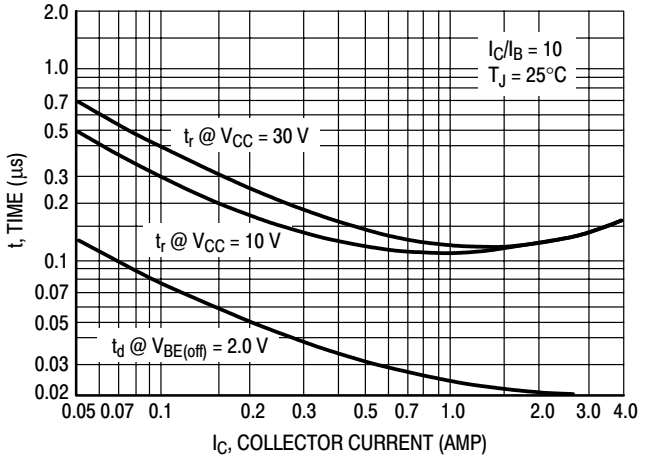


Figure 9. Turn–On Time

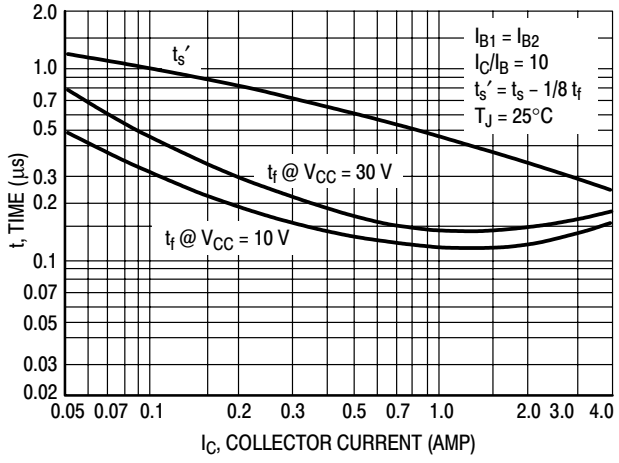


Figure 10. Turn–Off Time

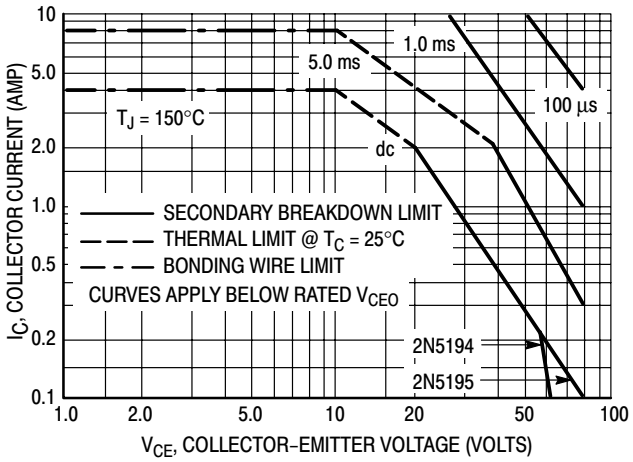


Figure 11. Rating and Thermal Data
Active–Region Safe Operating Area

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high–case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

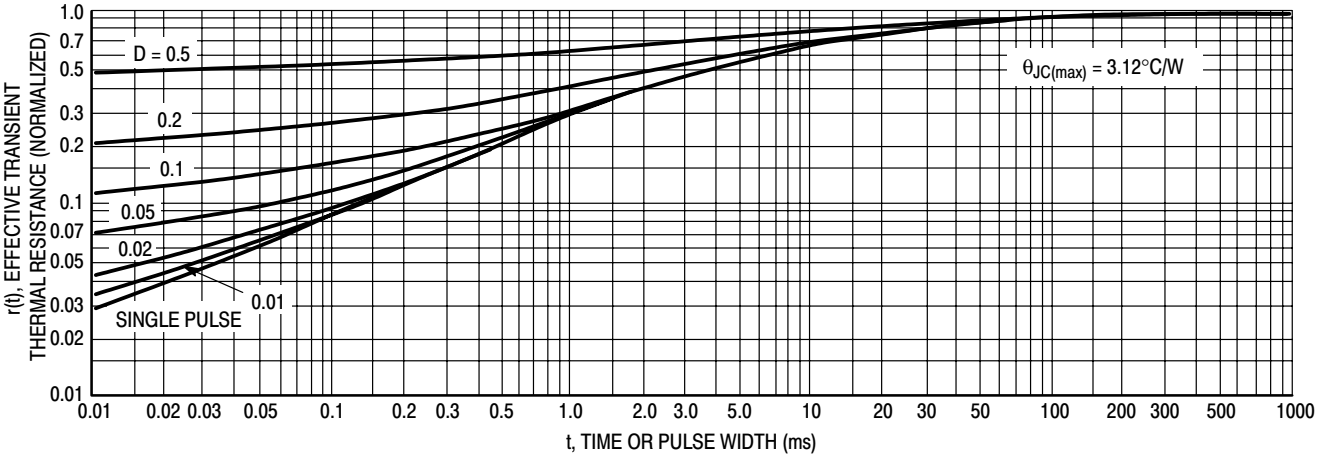


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

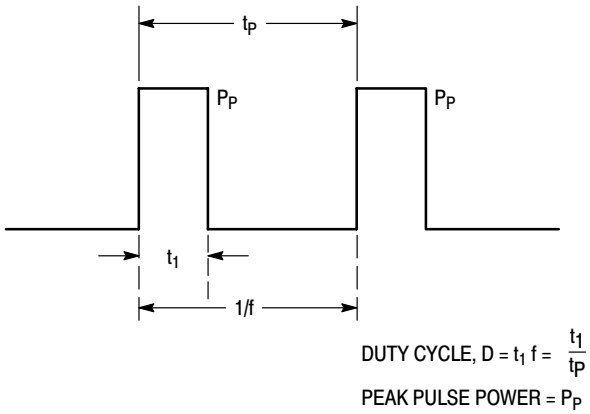


Figure 13.

A train of periodical power pulses can be represented by the model shown in Figure 13. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

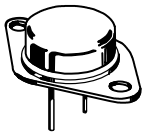
High–Power NPN Silicon Transistor

2N5302

. . . for use in power amplifier and switching circuits applications.

- Low Collector–Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc

30 AMPERE
POWER TRANSISTOR
NPN SILICON
60 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N5302	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CB}	60	Vdc
Collector Current – Continuous	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

*Indicates JEDEC Registered Data.

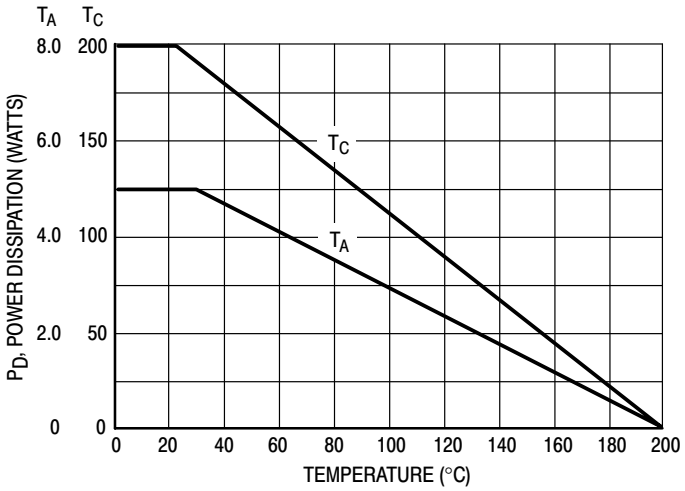


Figure 1. Power Temperature Derating Curve

May, 2001 – Rev. 0
Publication Order Number:
2N5302/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector–Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	–	5.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	–	10	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 1) *(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc) *(I_C = 15 Adc, V_{CE} = 2.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 40 15 5.0	 – 60 –	–
*Collector–Emitter Saturation Voltage (Note 1) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 20 Adc, I_B = 2.0 Adc)2 (I_C = 30 Adc, I_B = 6.0 Adc)	$V_{CE(sat)}$	 – – –	 0.75 2.0 3.0	Vdc
*Base Emitter Saturation Voltage (Note 1) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 20 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 – – –	 1.7 1.8 2.5	Vdc
*Base–Emitter On Voltage (Note 1) (I_C = 15 Adc, V_{CE} = 2.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	 – –	 1.7 3.0	Vdc
***DYNAMIC CHARACTERISTICS**				
Current–Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	40	–	–
***SWITCHING CHARACTERISTICS**				
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	1.0	μs
Storage Time		t_s	–	2.0	μs
Fall Time		t_f	–	1.0	μs

*Indicates JEDEC Registered Data.

Note 1: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

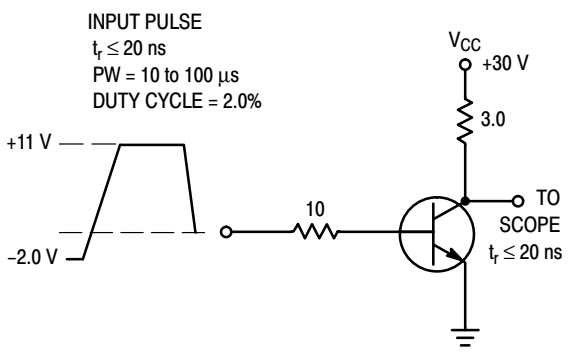


Figure 2. Turn–On time

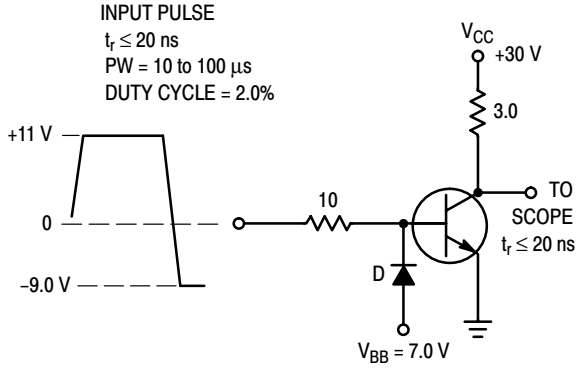


Figure 3. Turn–Off time

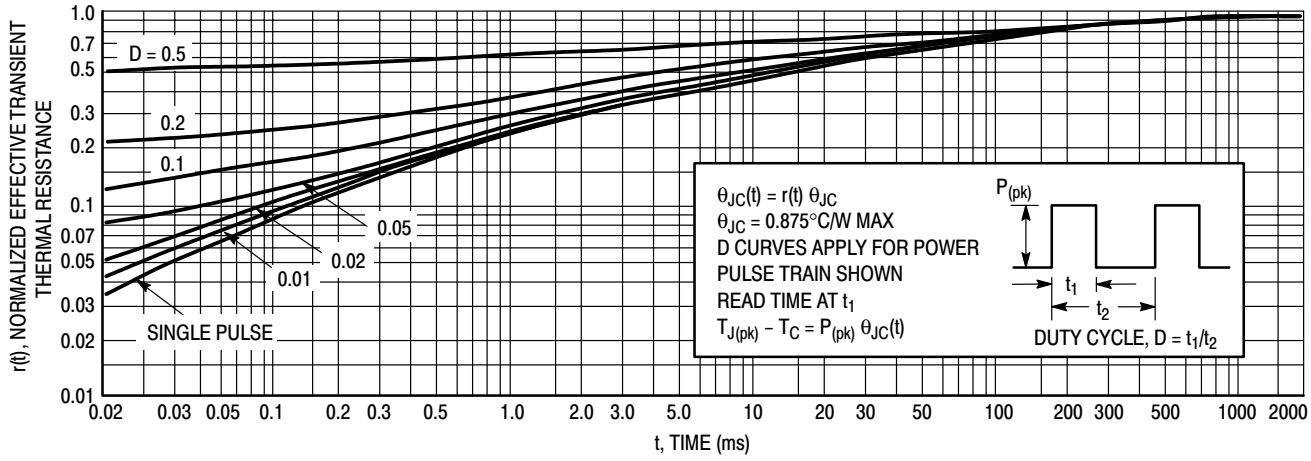


Figure 4. Thermal Response

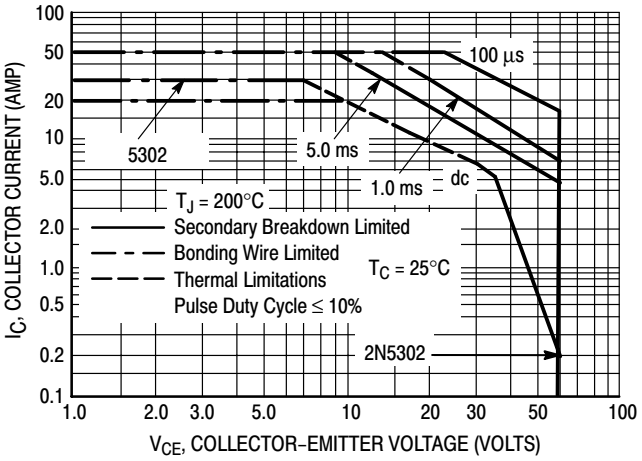


Figure 5. Active−Region Safe Operating Area

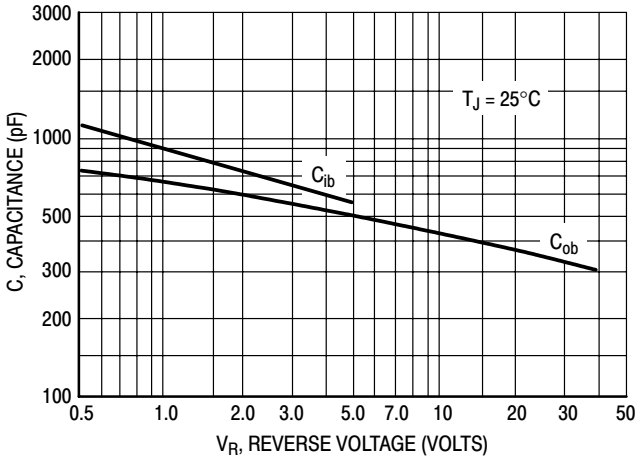


Figure 6. Capacitance versus Voltage

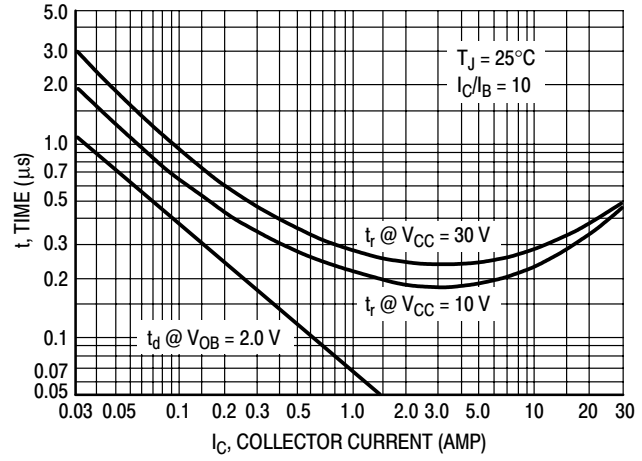


Figure 7. Turn−On Time

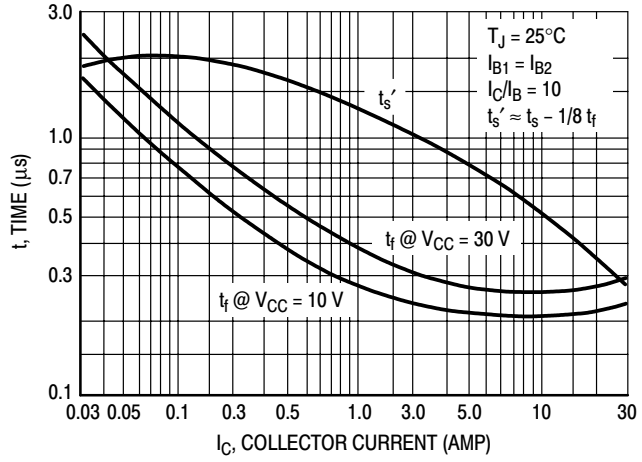


Figure 8. Turn−Off Time

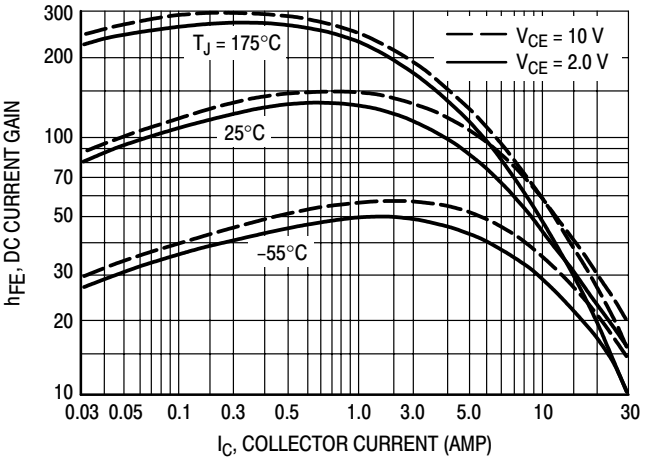


Figure 9. DC Current Gain

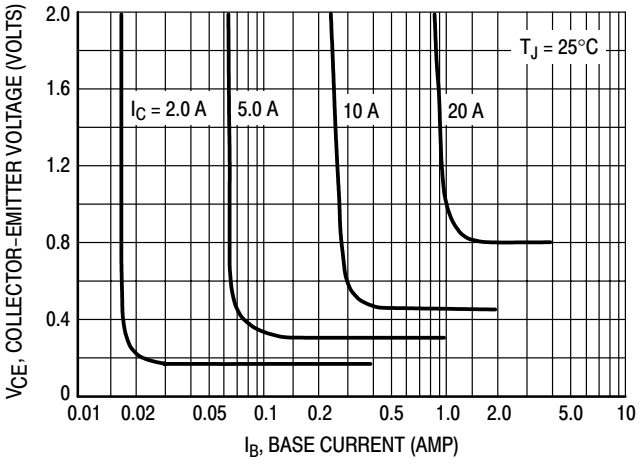


Figure 10. Collector Saturation Region

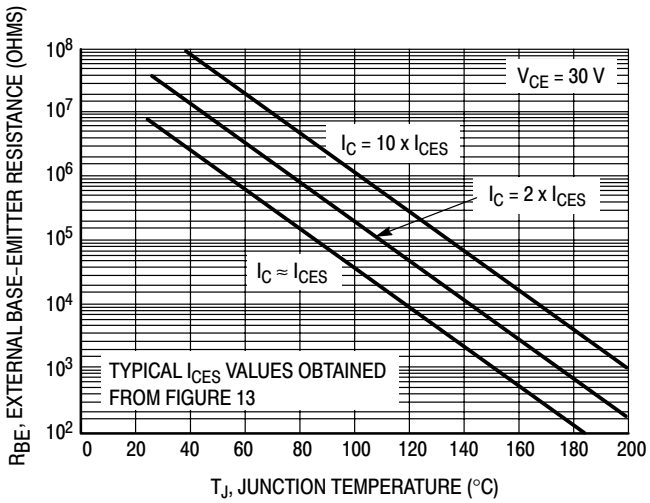


Figure 11. Effects of Base−Emitter Resistance

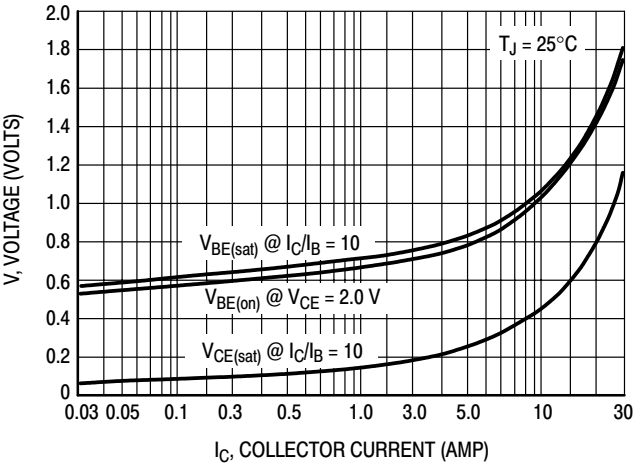


Figure 12. “On” Voltages

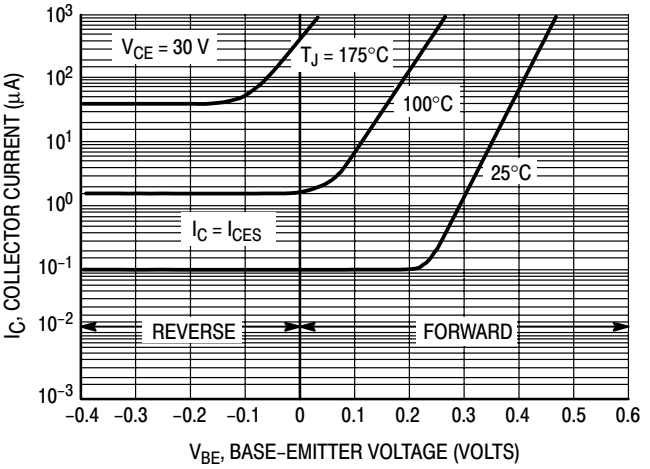


Figure 13. Collector Cut−Off Region

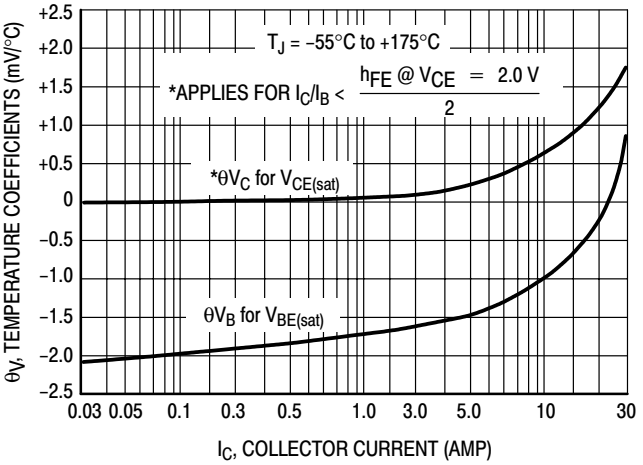


Figure 14. Temperature Coefficients

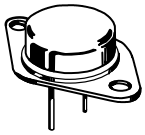
High-Voltage - High Power Transistors

NPN
2N5631
PNP
2N6031

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 140 Vdc
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 15 (Min)
- Low Collector–Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CB}	140	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current – Continuous Peak	I_C	16 20	Adc
Base Current – Continuous	I_B	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

(1) Indicates JEDEC Registered Data.

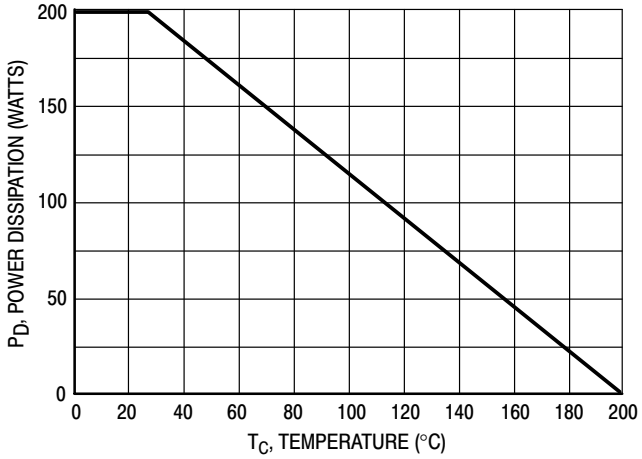


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

May, 2001 – Rev. 0
Publication Order Number:
2N5631/D

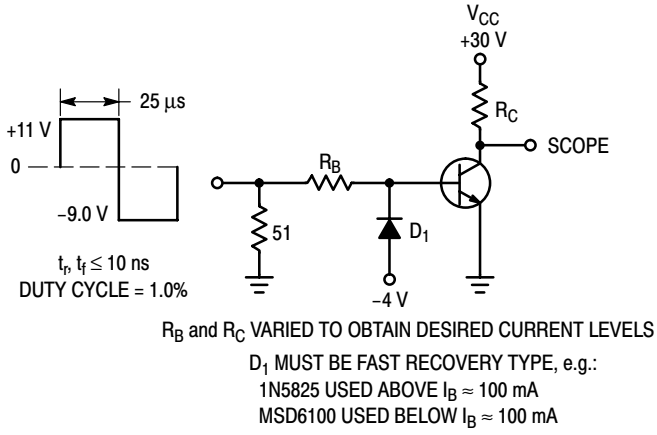
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)		$V_{CEO(sus)}$	140	–	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 70 Vdc, I_B = 0)		I_{CEO}	–	2.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	2.0 7.0	mAdc
Collector–Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	2.0	mAdc
Emitter–Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 8 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	15 4.0	60 –	–
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 16 Adc, I_B = 4.0 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.8	Vdc
Base–Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (3) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5631 2N6031	C_{ob}	– –	500 1000	pF
Small–Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$



For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Times Test Circuit

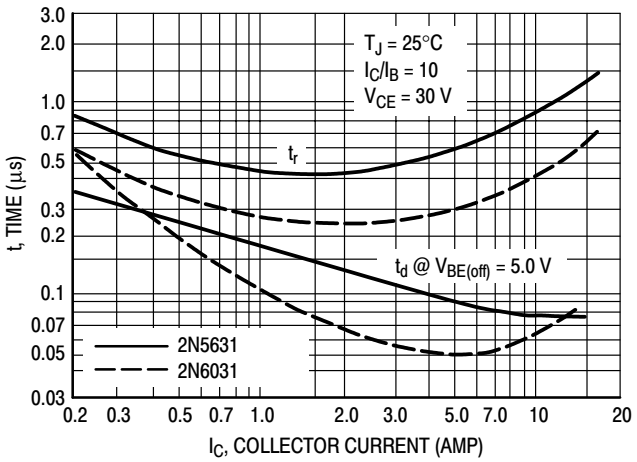


Figure 3. Turn–On Time

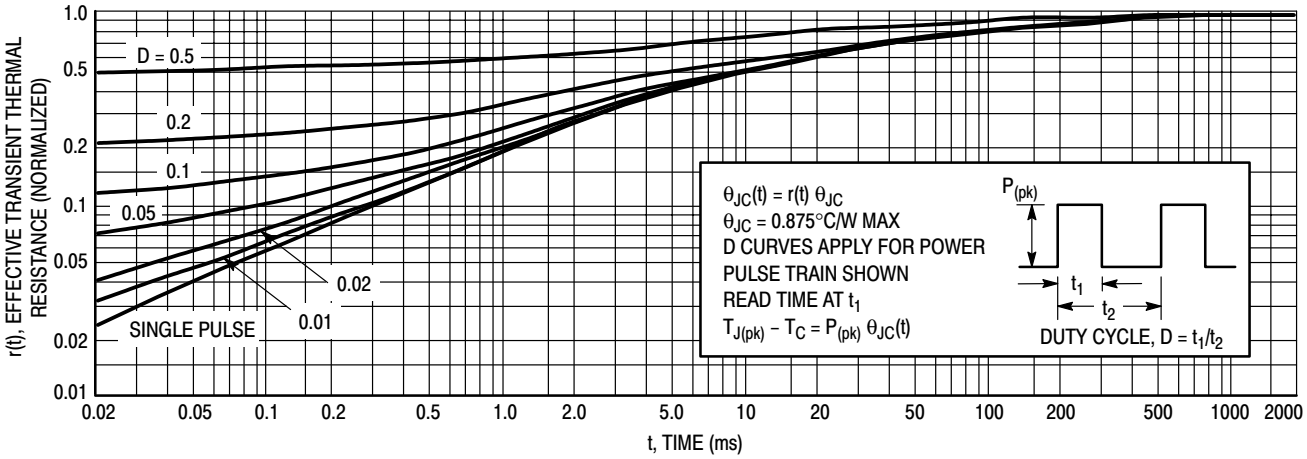


Figure 4. Thermal Response

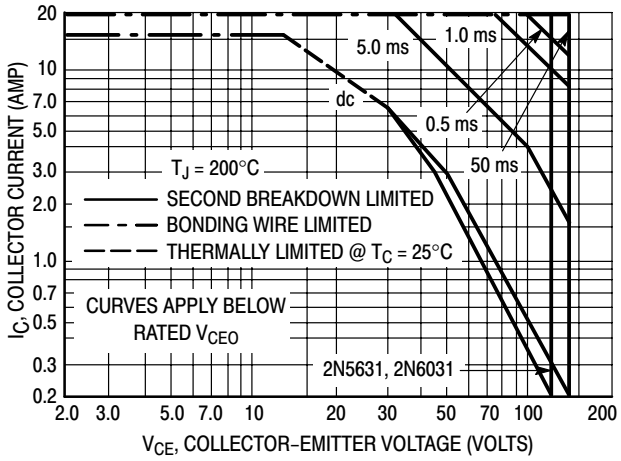
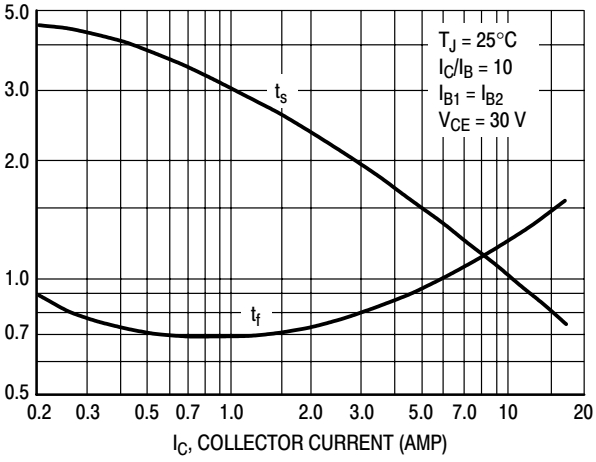


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5631



PNP
2N6031

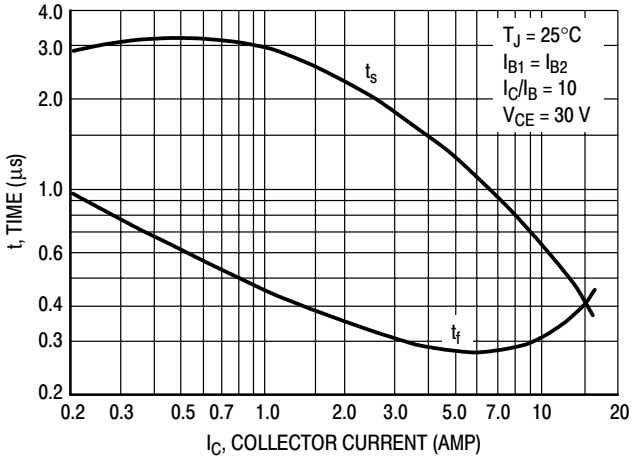
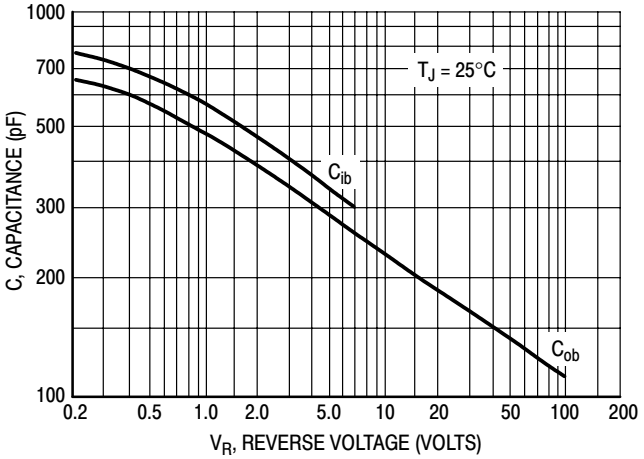


Figure 6. Turn−Off Time

NPN
2N5631



PNP
2N6031

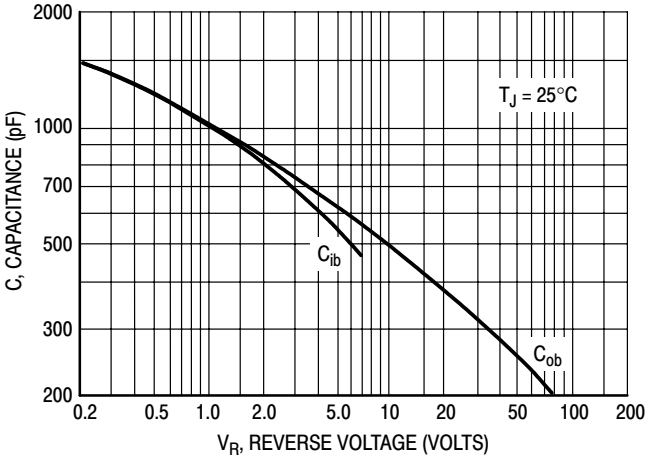
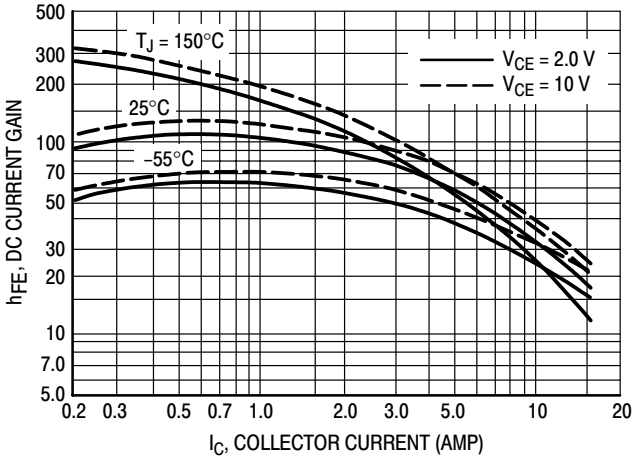


Figure 7. Capacitance



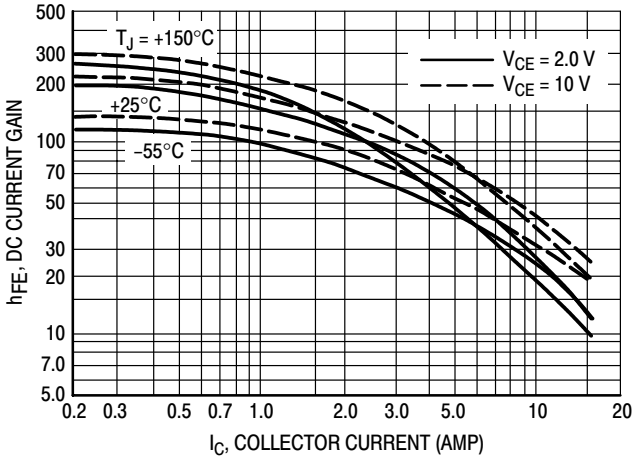
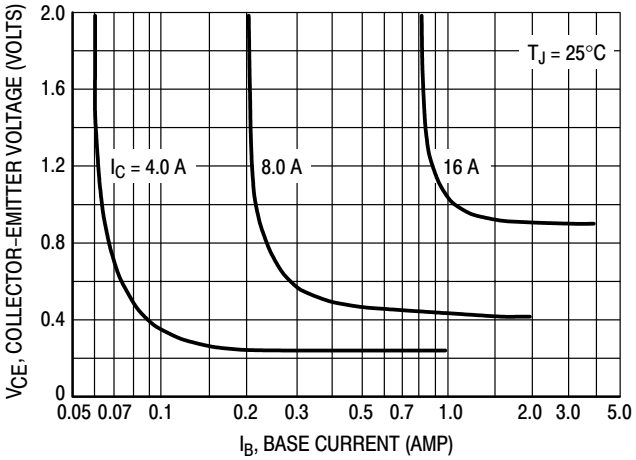


Figure 8. DC Current Gain



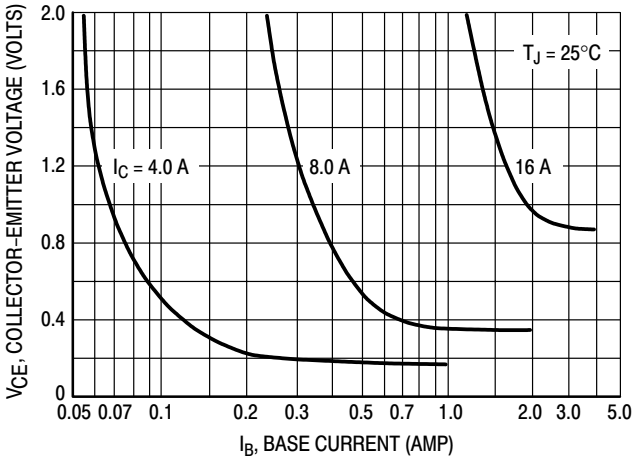


Figure 9. Collector Saturation Region

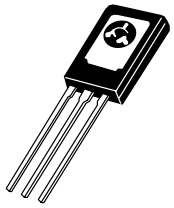
Plastic NPN Silicon High-Voltage Power Transistor

2N5655
2N5657

. . . designed for use in line–operated equipment such as audio output amplifiers; low–current, high–voltage converters; and AC line relays.

- Excellent DC Current Gain –
  h_{FE} = 30–250 @ I_C = 100 mAdc
- Current–Gain – Bandwidth Product –
  f_T = 10 MHz (Min) @ I_C = 50 mAdc

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
250–350 VOLTS
20 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS (1)

Rating	Symbol	2N5655	2N5657	Unit
Collector–Emitter Voltage	V_{CEO}	250	350	Vdc
Collector–Base Voltage	V_{CB}	275	375	Vdc
Emitter–Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous Peak	I_C	0.5 1.0		Adc
Base Current	I_B	0.25		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

(1) Indicates JEDEC Registered Data.

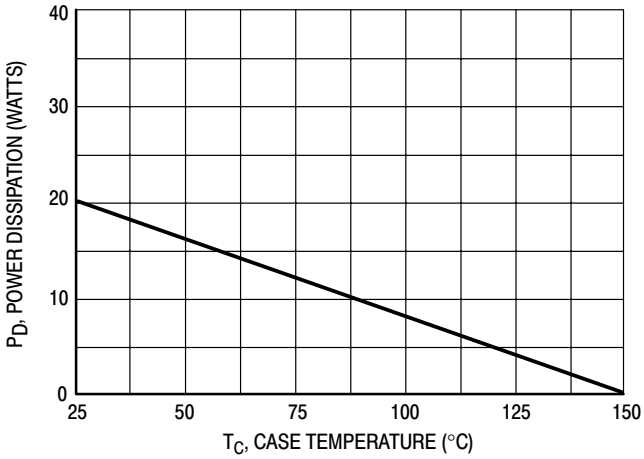


Figure 1. Power Derating

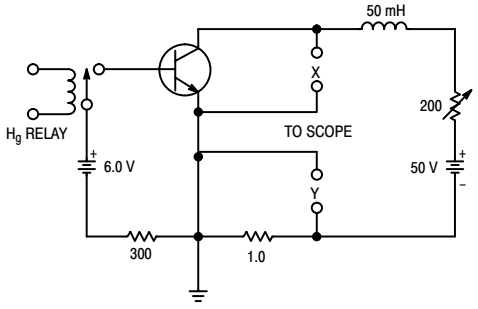


Figure 2. Sustaining Voltage Test Circuit

Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

May, 2001 – Rev. 6
Publication Order Number:
2N5655/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655 2N5657	$V_{CEO(sus)}$	250 350	– –	Vdc
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655 2N5657	$V_{(BR)CEO}$	250 350	– –	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N5655		–	0.1	
(V_{CE} = 250 Vdc, I_B = 0)	2N5657		–	0.1	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5655		–	0.1	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5657		–	0.1	
(V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655		–	1.0	
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5657		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 275 Vdc, I_E = 0)	2N5655		–	10	
(V_{CB} = 375 Vdc, I_E = 0)	2N5657		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			30	250	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			15	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)			5.0	–	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)			–	1.0	
(I_C = 250 mAdc, I_B = 25 mAdc)			–	2.5	
(I_C = 500 mAdc, I_B = 100 mAdc)			–	10	
Base–Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	25	pF
Small–Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5655 Series.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

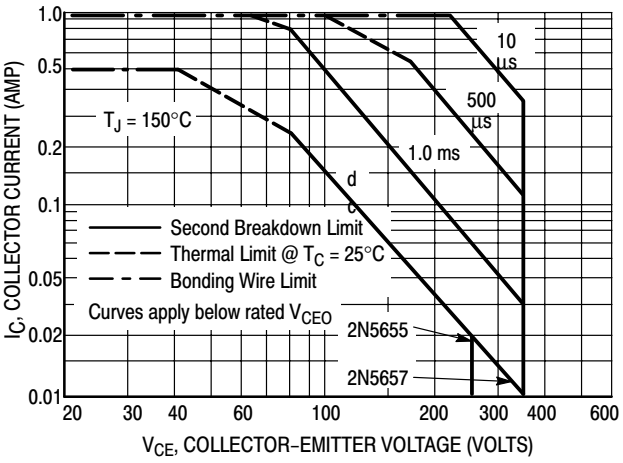


Figure 3. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

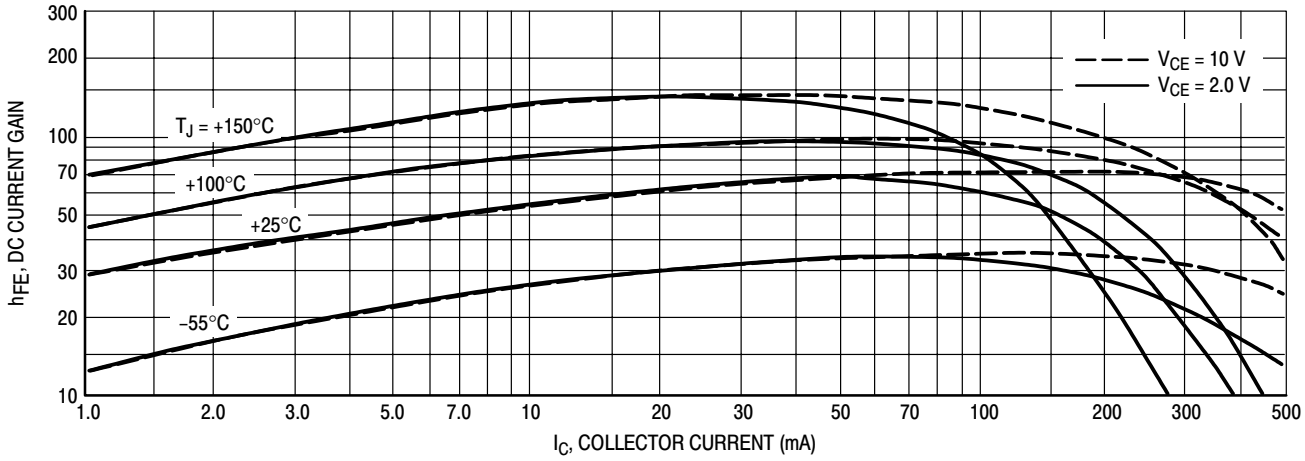


Figure 4. Current Gain

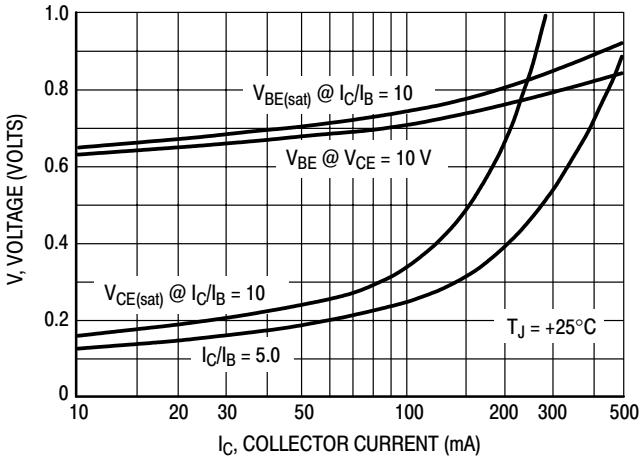


Figure 5. “On” Voltages

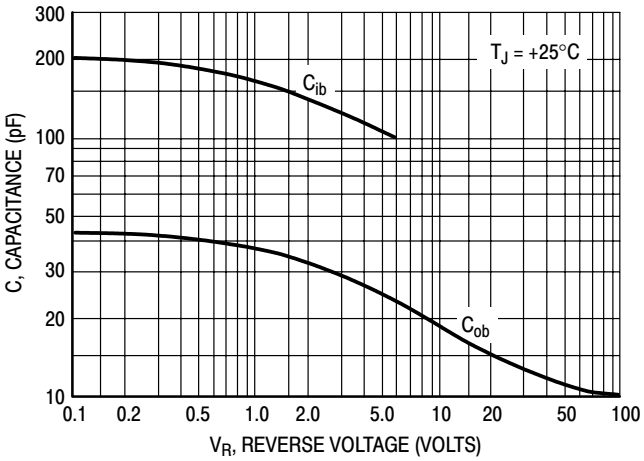


Figure 6. Capacitance

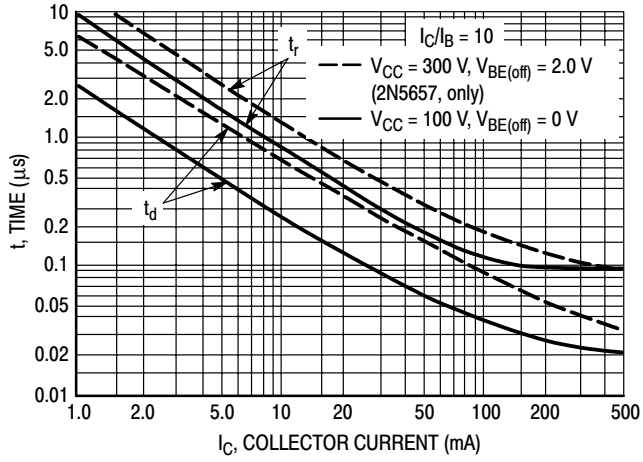


Figure 7. Turn−On Time

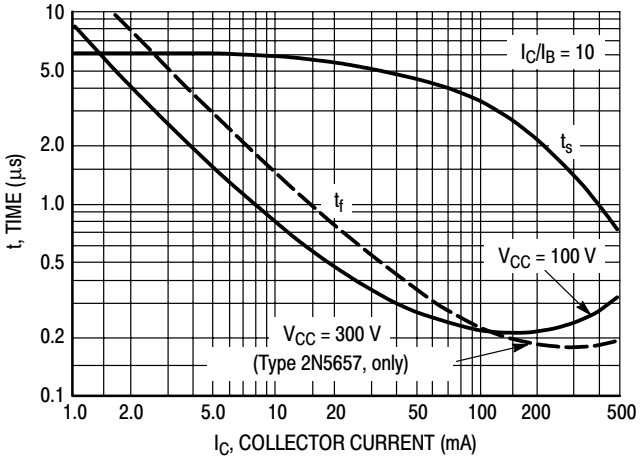


Figure 8. Turn−Off Time

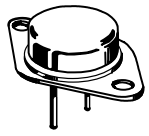
High-Current Complementary Silicon Power Transistors

. . . designed for use in high–power amplifier and switching circuit applications.

- High Current Capability – I_C Continuous = 50 Amperes.
- DC Current Gain – h_{FE} = 15–60 @ I_C = 25 Adc
- Low Collector–Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

PNP
2N5684
NPN
2N5686

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80 VOLTS 300 WATTS



CASE 197A–05 TO–204AE

MAXIMUM RATINGS (1)

Rating	Symbol	2N5684 2N5686	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CB}	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	50	Adc
Base Current	I_B	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	°C/W

(1) Indicates JEDEC Registered Data.

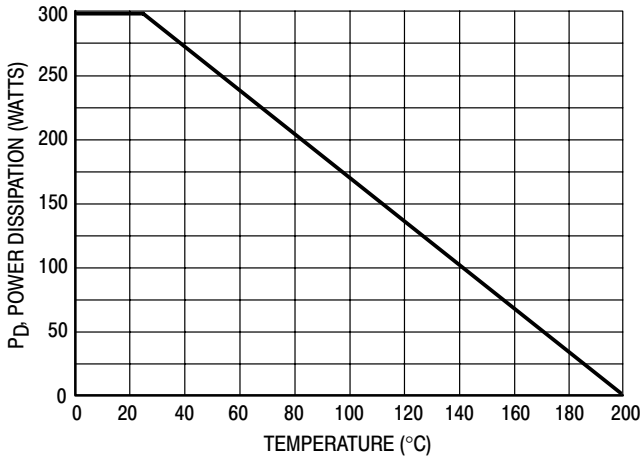


Figure 1. Power Derating

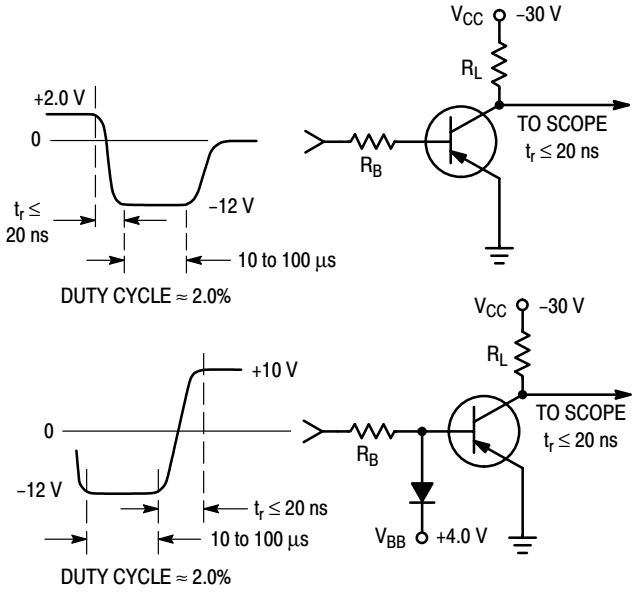
Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 2) (I_C = 0.2 Adc, I_B = 0)		$V_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)		I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	2.0 10	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)		I_{CBO}	–	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2) (I_C = 25 Adc, V_{CE} = 2.0 Vdc) (I_C = 50 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	15 5.0	60 –	–
Collector–Emitter Saturation Voltage (Note 2) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	– –	1.0 5.0	Vdc
Base–Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	–	2.0	Vdc
Base–Emitter On Voltage (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5684 2N5686	C_{ob}	– –	2000 1200	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	15	–	

*Indicates JEDEC Registered Data.

Note 2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

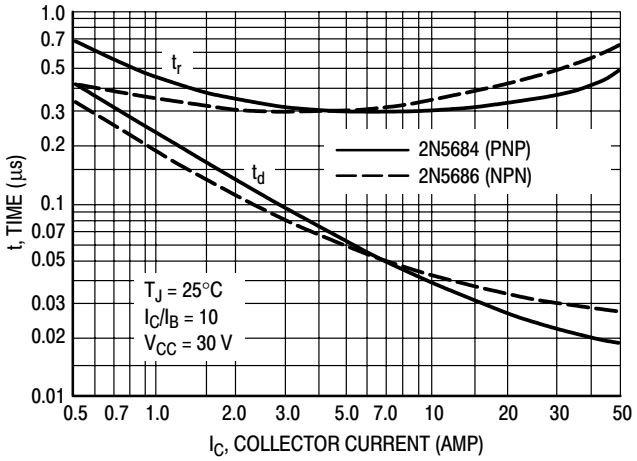


Figure 3. Turn–On Time

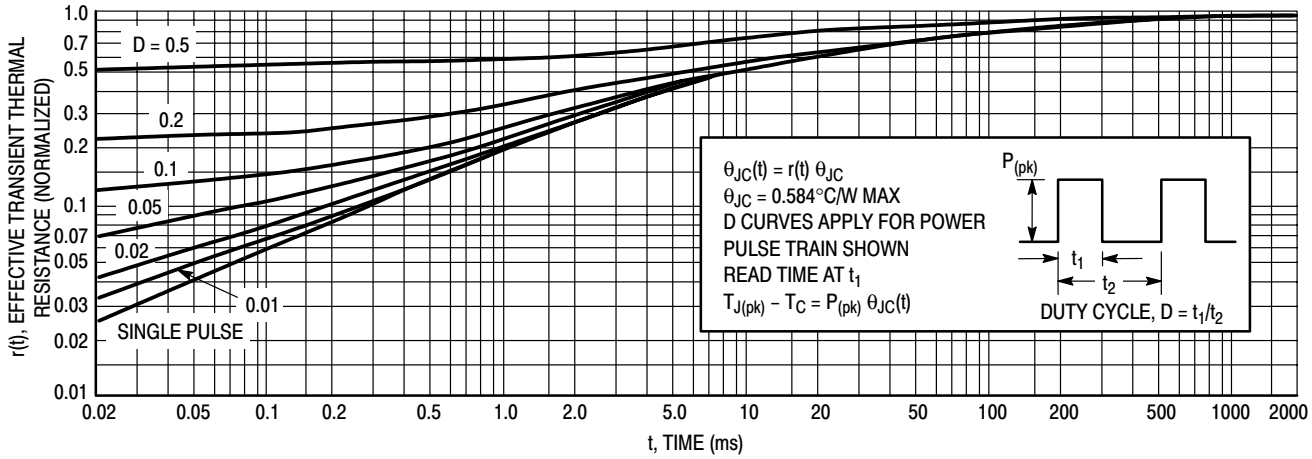


Figure 4. Thermal Response

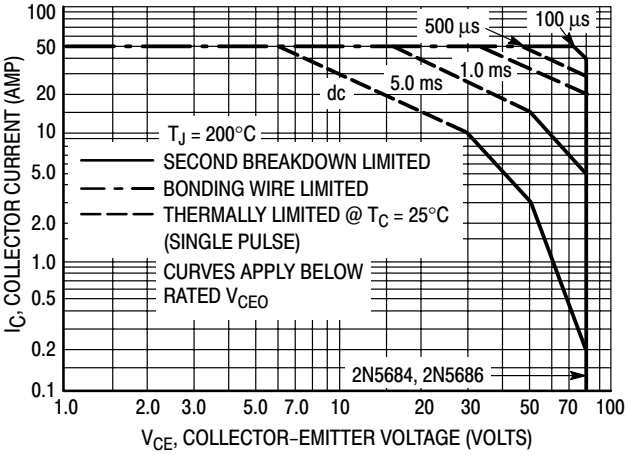


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

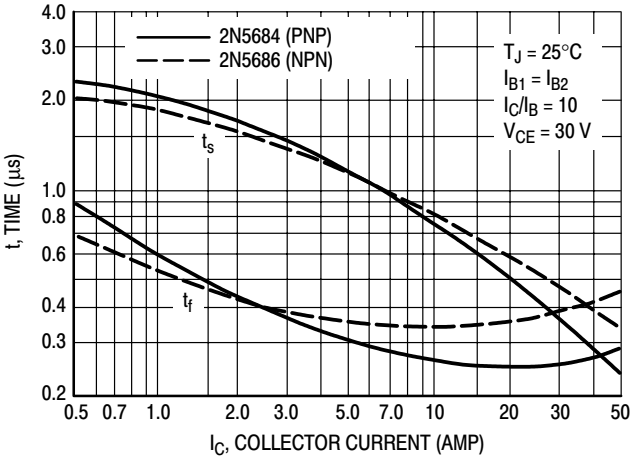


Figure 6. Turn−Off Time

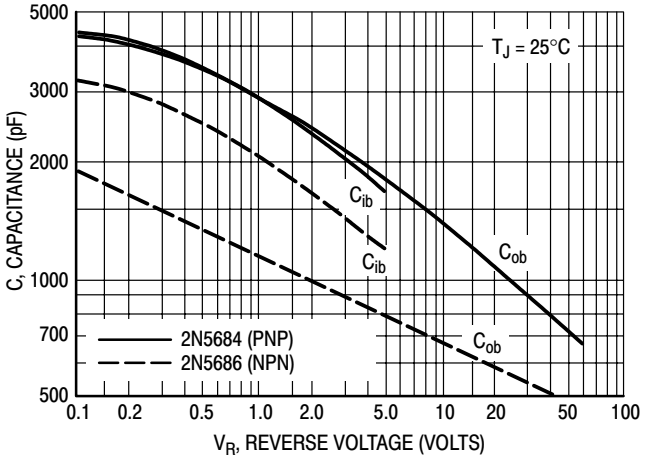
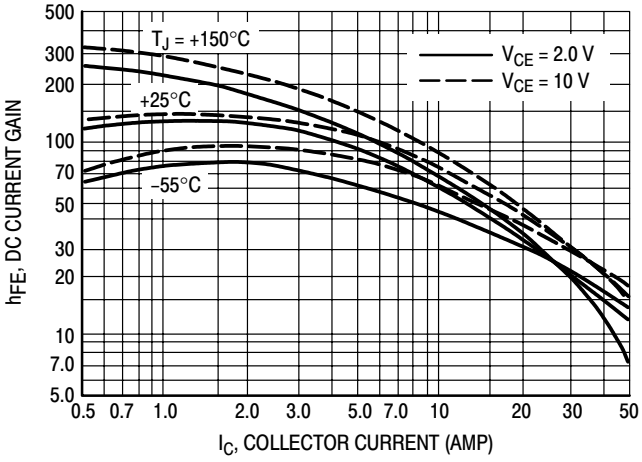


Figure 7. Capacitance

PNP
2N5684



NPN
2N5686

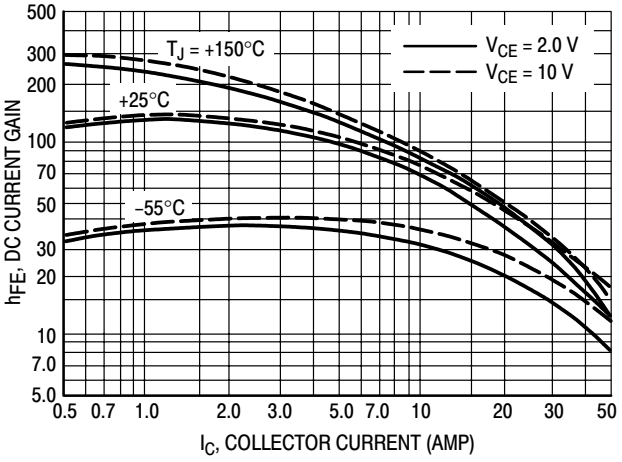
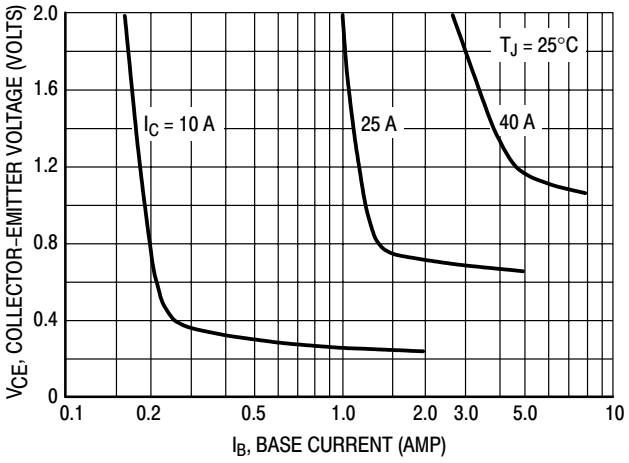


Figure 8. DC Current Gain



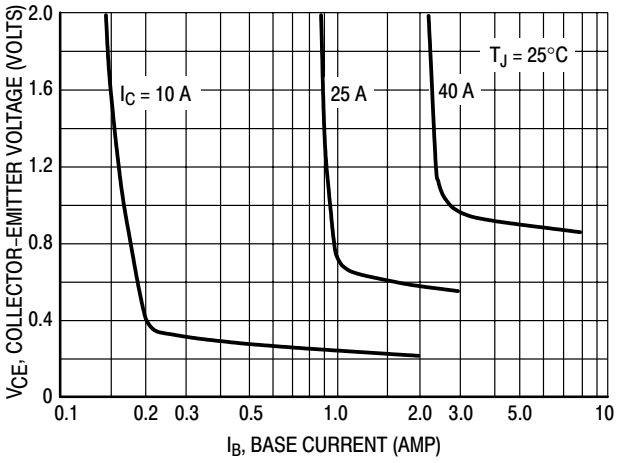
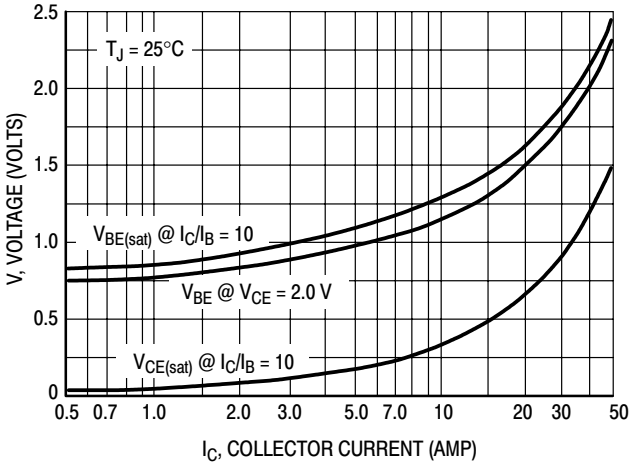


Figure 9. Collector Saturation Region



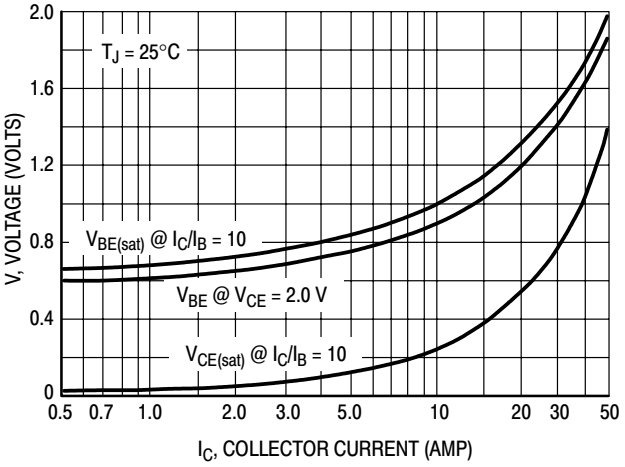


Figure 10. “On” Voltages

Complementary Silicon High-Power Transistors

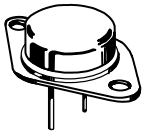
. . . designed for general–purpose power amplifier and switching applications.

- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current
  I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain —
  h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product —
  f_τ = 4.0 MHz (min) at I_C = 1.0 Adc

PNP
2N5883
2N5884*
NPN
2N5885
2N5886*

*ON Semiconductor Preferred Device

25 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–80 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

(1) Indicates JEDEC registered data. Units and conditions differ on some parameters and re–registration reflecting these changes has been requested. All above values most or exceed present JEDEC registered data.

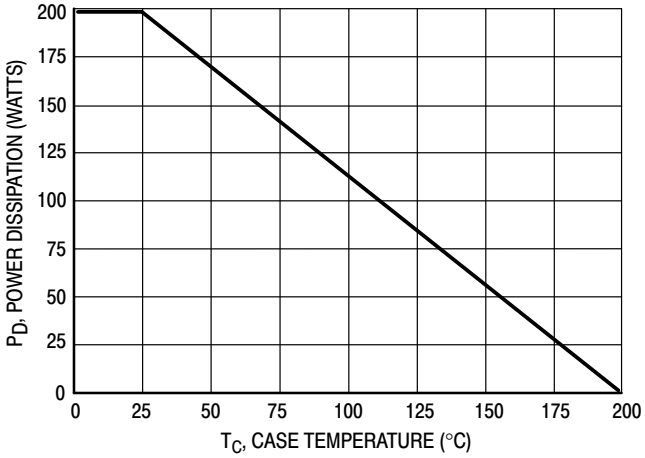


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

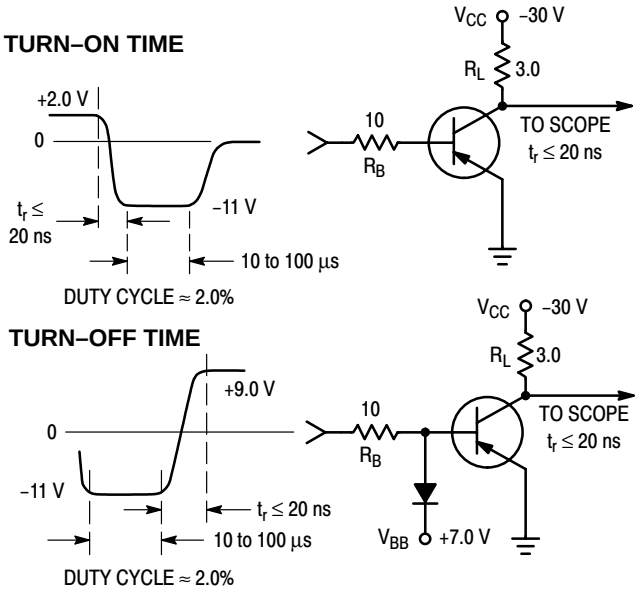
March, 2001 – Rev. 9
Publication Order Number:
2N5883/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5883, 2N5885 2N5984, 2N5886	I_{CEO}	— —	2.0 2.0	mAdc
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5883, 2N5885		—	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5884, 2N5886		—	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5883, 2N5885			10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5884, 2N5886		—	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5883, 2N5885		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5884, 2N5886		—	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (2) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 25 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35 20 4.0	— 100	—
Collector–Emitter Saturation Voltage (2) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{CE(sat)}$	— —	1.0 4.0	Vdc
Base–Emitter Saturation Voltage (2) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (2) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (3) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884 2N5885, 2N5886	C_{ob}	— —	1000 500	pF
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)		h_{fe}	20	—	—
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	—	0.7	μs
Storage Time		t_s	—	1.0	μs
Fall Time		t_f	—	0.8	μs

*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%. (3) $f_T = |h_{fe}| \bullet f_{test}$.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

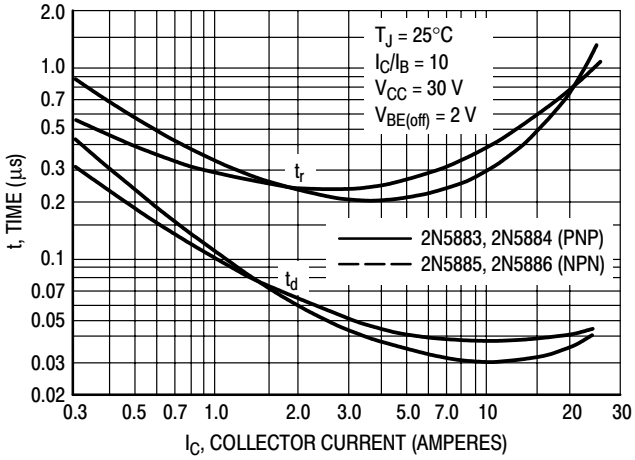


Figure 3. Turn–On Time

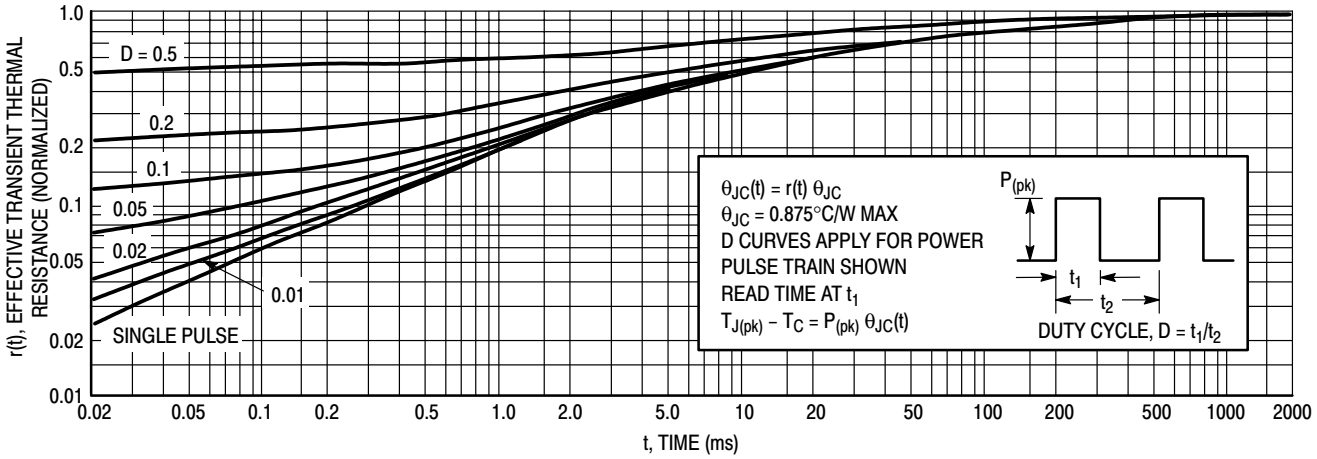


Figure 4. Thermal Response

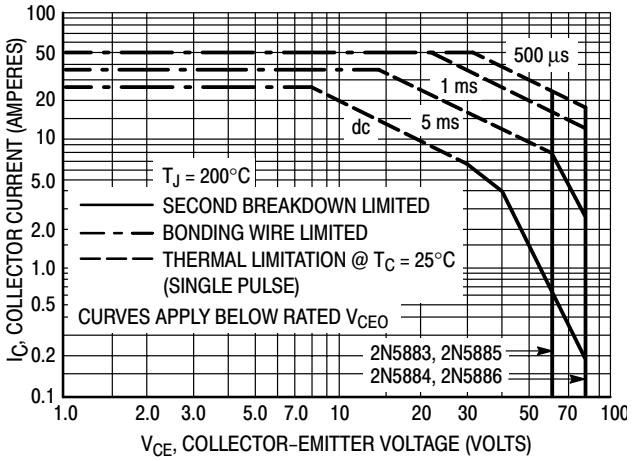


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

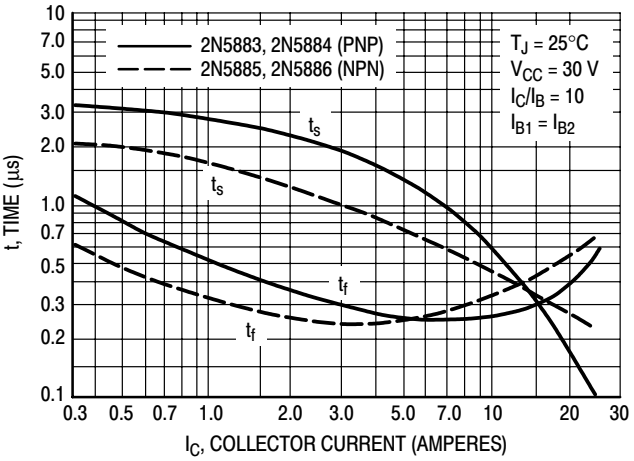


Figure 6. Turn−Off Time

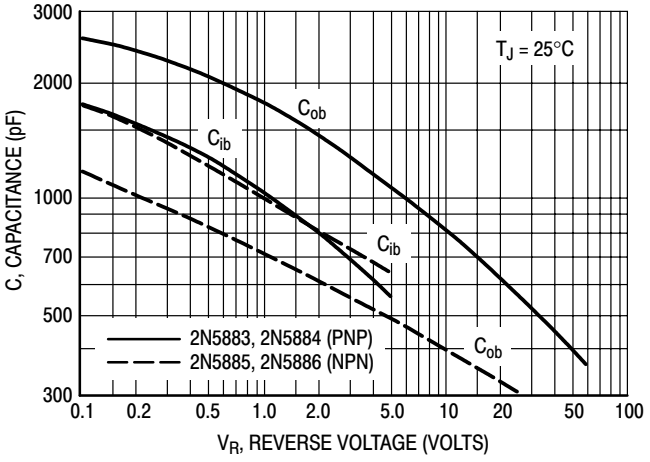


Figure 7. Capacitance

PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

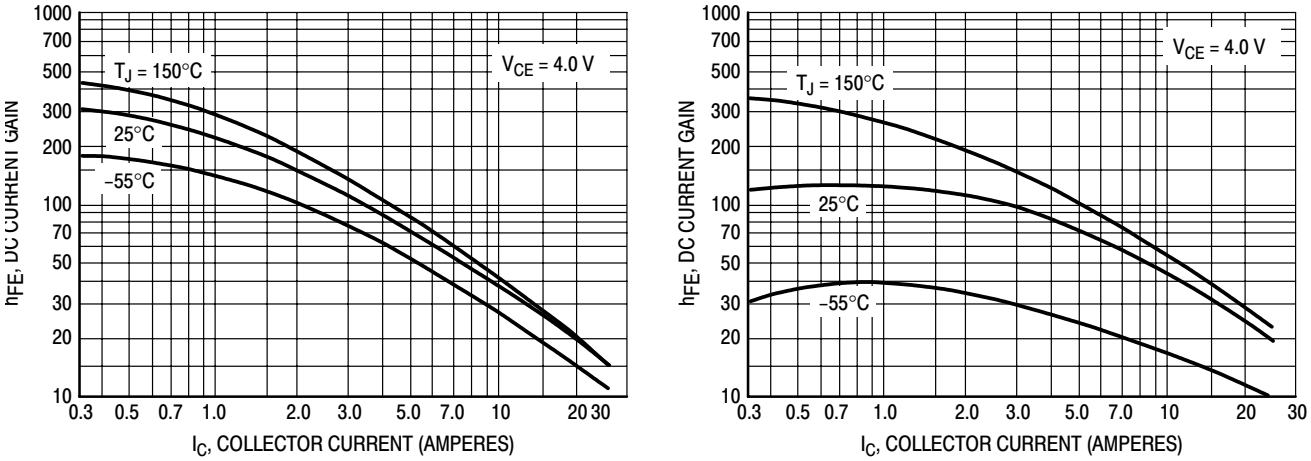


Figure 8. DC Current Gain

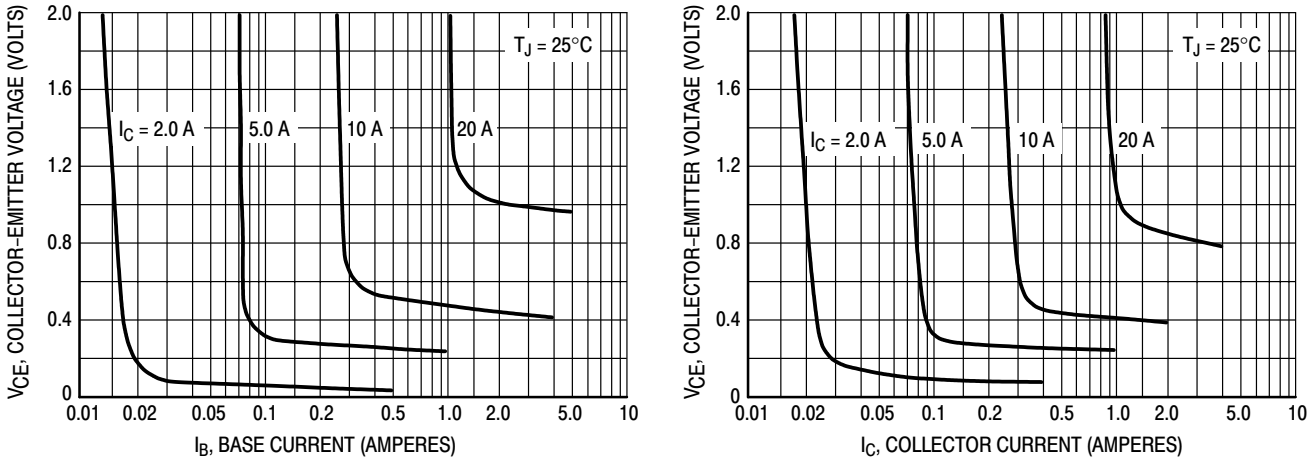


Figure 9. Collector Saturation Region

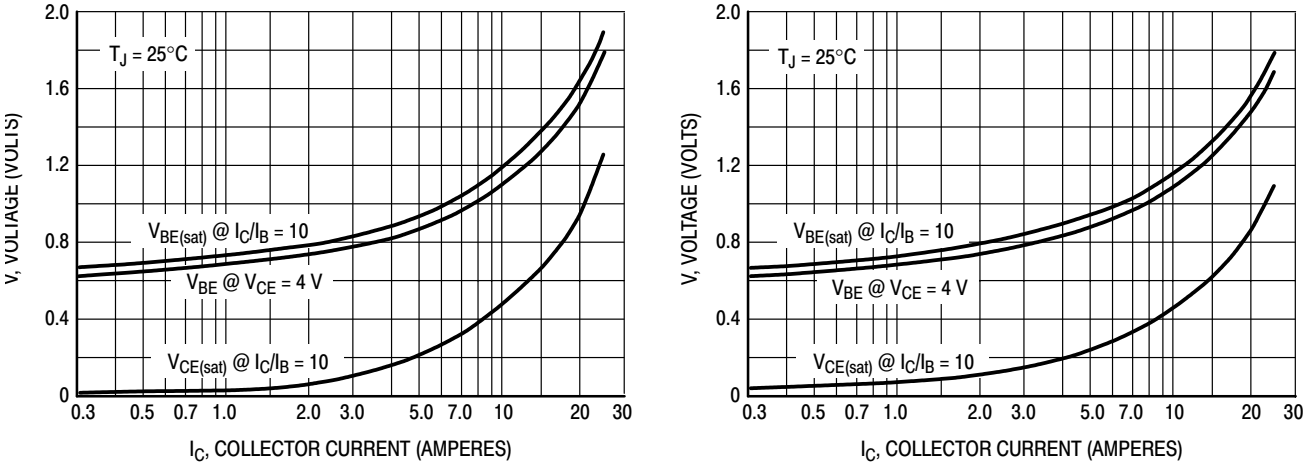


Figure 10. “On” Voltages

Plastic Darlington Complementary Silicon Power Transistors

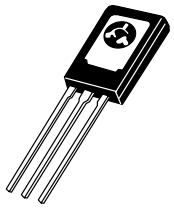
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6035, 2N6038 = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built–In Base–Emitter Resistors to Limit Leakage Multiplication
- Space–Saving High Performance–to–Cost Ratio TO–225AA Plastic Package

PNP
2N6035
2N6036*
NPN
2N6038
2N6039*

***ON Semiconductor Preferred Device**

DARLINGTON
4–AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 80 VOLTS
40 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS (1)

Rating	Symbol	2N6035 2N6038	2N6036 2N6039	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	100		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.3	°C/W

(1) Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N6035/D

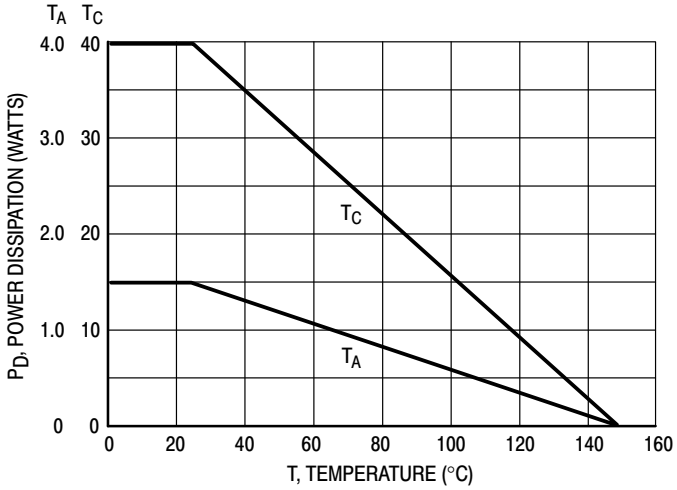


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6035, 2N6038 2N6036, 2N6039	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector–Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N6035, 2N6038 2N6036, 2N6039	I_{CEO}	 — —	 100 100	μA
Collector–Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6035, 2N6038 2N6036, 2N6039 2N6035, 2N6038 2N6036, 2N6039	I_{CEX}	 — — — —	 100 100 500 500	μA
Collector–Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N6035, 2N6038 2N6036, 2N6039	I_{CBO}	 — —	 0.5 0.5	mAdc
Emitter–Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 500 750 100	 — 15,000 —	—
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc) (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current–Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 2N6035, 2N6036 2N6038, 2N6039	C_{ob}	 — —	 200 100	pF

*Indicates JEDEC Registered Data.

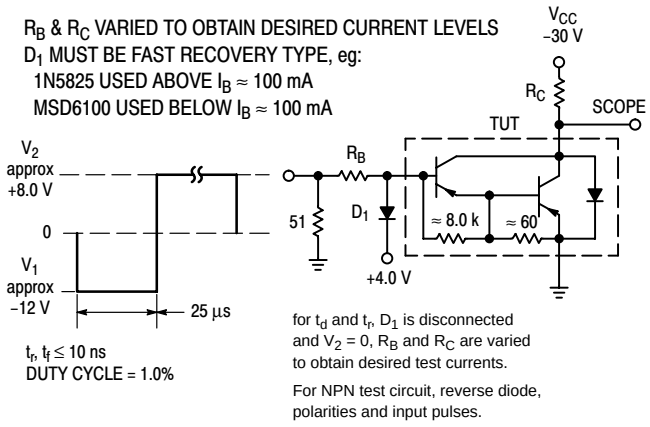


Figure 2. Switching Times Test Circuit

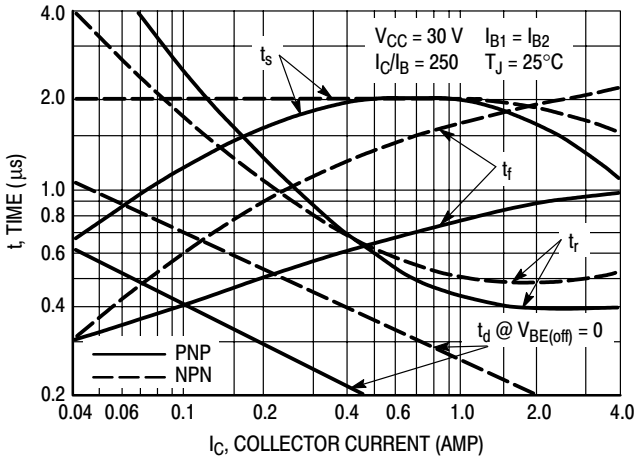


Figure 3. Switching Times

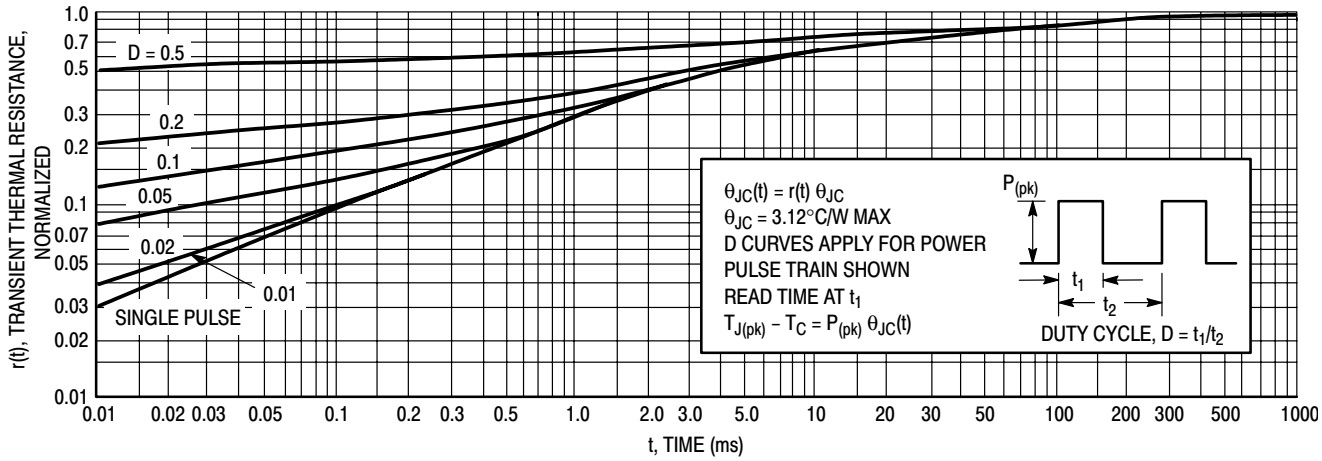


Figure 4. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

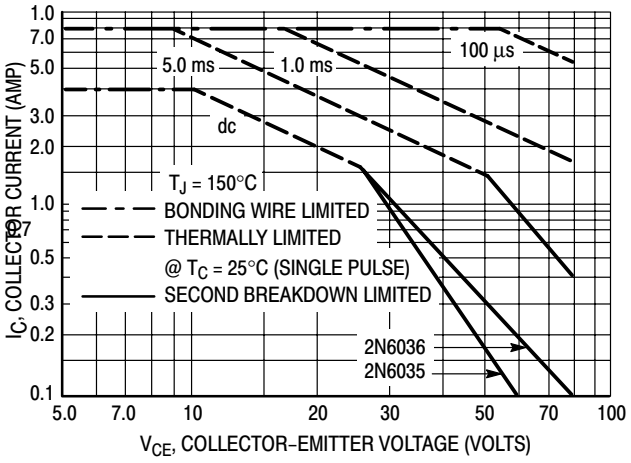


Figure 5. 2N6035, 2N6036

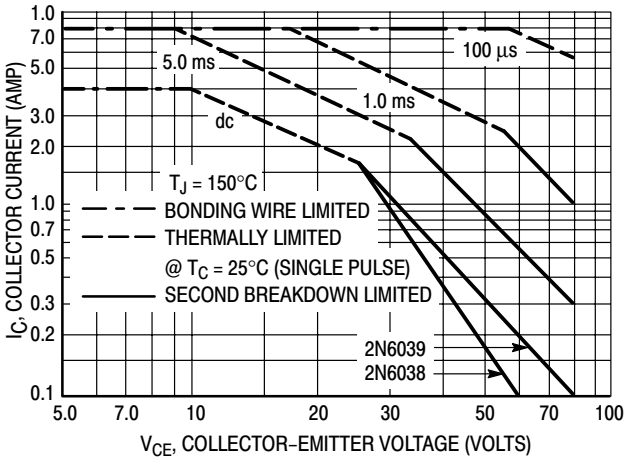


Figure 6. 2N6038, 2N6039

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

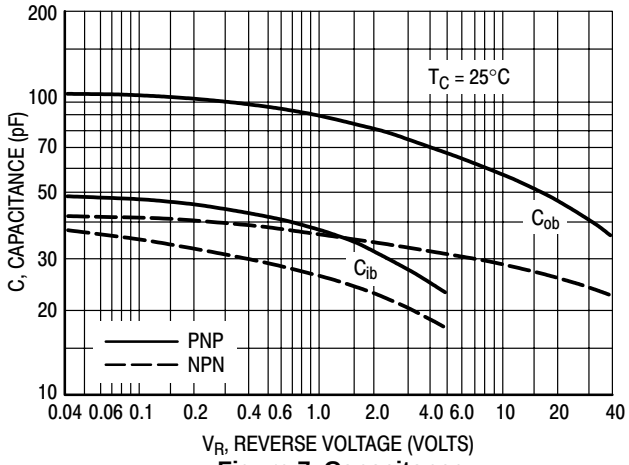


Figure 7. Capacitance

PNP
2N6035, 2N6036

NPN
2N6038, 2N6039

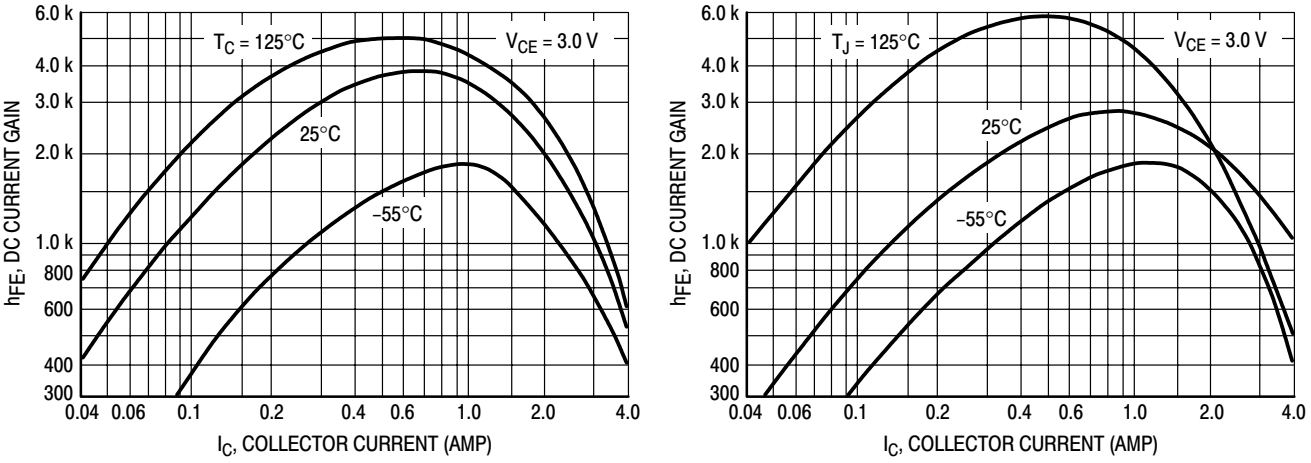


Figure 8. DC Current Gain

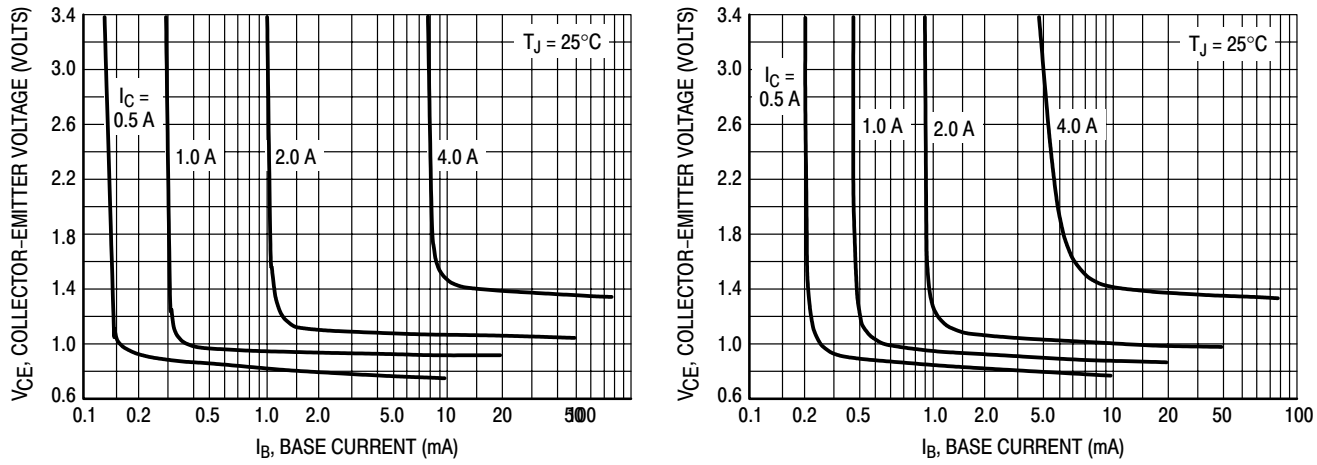


Figure 9. Collector Saturation Region

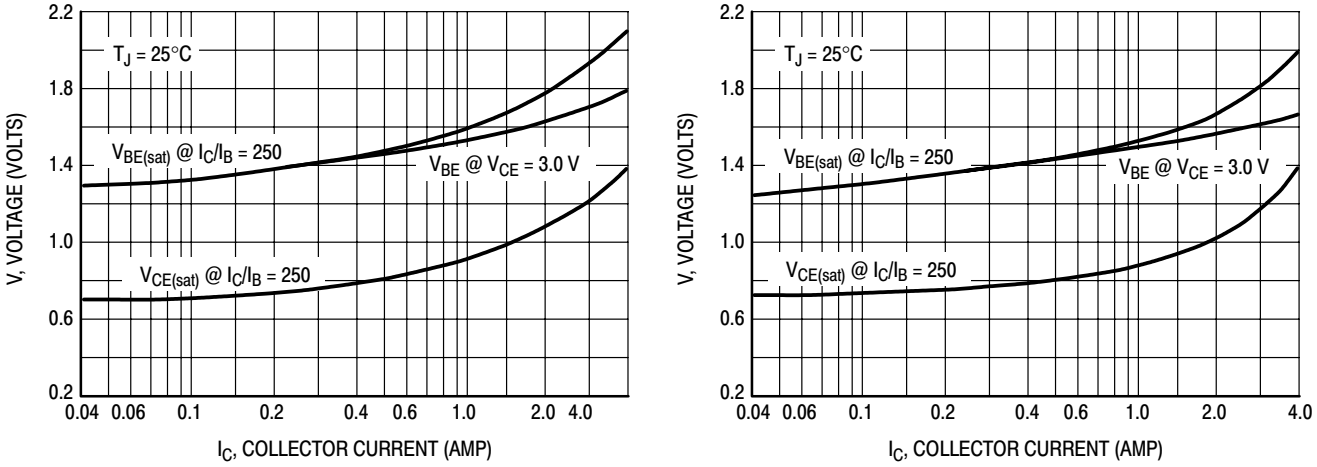


Figure 10. “On” Voltages

Plastic Medium-Power Complementary Silicon Transistors

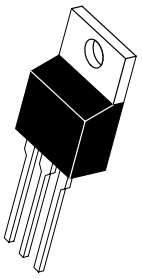
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage – @ 100 mAdc –
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6040, 2N6043
  = 100 Vdc (Min) – 2N6042, 2N6045
- Low Collector–Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc – 2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc – 2N6042, 2N6045
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

PNP
2N6040
2N6042
2N6043*
NPN
2N6045*

*ON Semiconductor Preferred Device

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–100 VOLTS
75 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6040 2N6043	2N6042 2N6045	Unit
Collector–Emitter Voltage	V_{CEO}	60	100	Vdc
Collector–Base Voltage	V_{CB}	60	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	120		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

(1) Indicates JEDEC Registered Data.

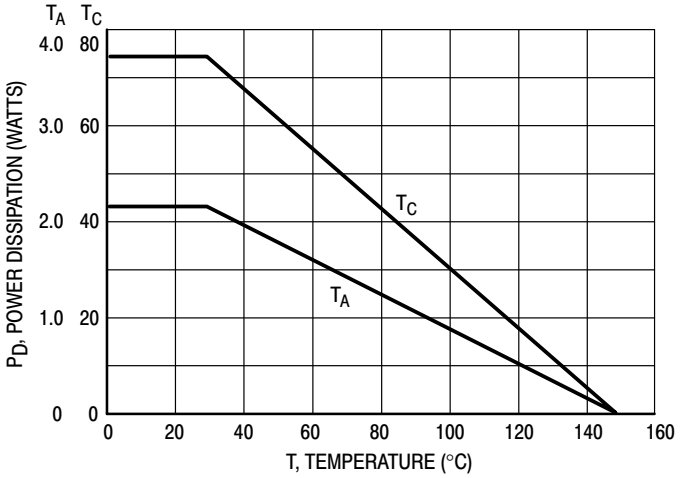


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 4
Publication Order Number:
2N6040/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043	$V_{CEO(sus)}$	60	–	Vdc
	2N6042, 2N6045		100	–	
Collector Cutoff Current		I_{CEO}			μA
(V_{CE} = 60 Vdc, I_B = 0)	2N6040, 2N6043		–	20	
(V_{CE} = 100 Vdc, I_B = 0)	2N6042, 2N6045		–	20	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6040, 2N6043		–	20	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6042, 2N6045		–	20	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6041, 2N6044		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6042, 2N6045		–	200	
Collector Cutoff Current		I_{CBO}			μA
(V_{CB} = 60 Vdc, I_E = 0)	2N6040, 2N6043		–	20	
(V_{CB} = 100 Vdc, I_E = 0)	2N6042, 2N6045		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	2N6040, 2N6043,		1000	20.000	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6042, 2N6045		1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	All Types		100	–	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)	2N6040, 2N6043,		–	2.0	
(I_C = 3.0 Adc, I_B = 12 mAdc)	2N6042, 2N6045		–	2.0	
(I_C = 8.0 Adc, I_B = 80 Adc)	All Types		–	4.0	
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.5	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	
Output Capacitance	2N6040/2N6042	C_{ob}	–	300	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6043/2N6045		–	200	
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

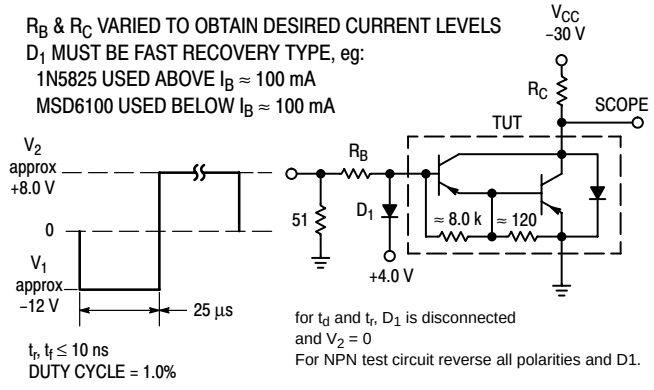


Figure 2. Switching Times Equivalent Circuit

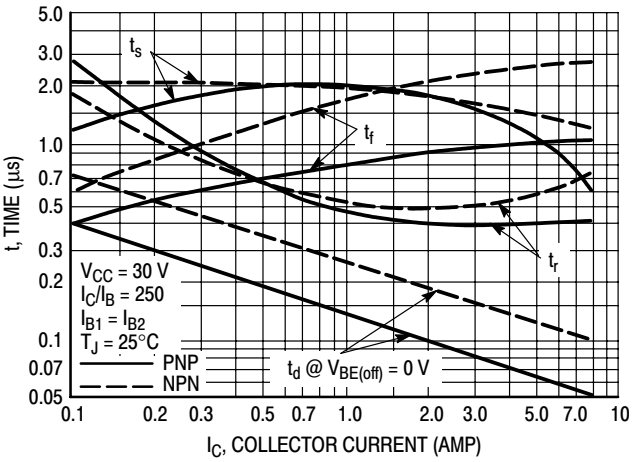


Figure 3. Switching Times

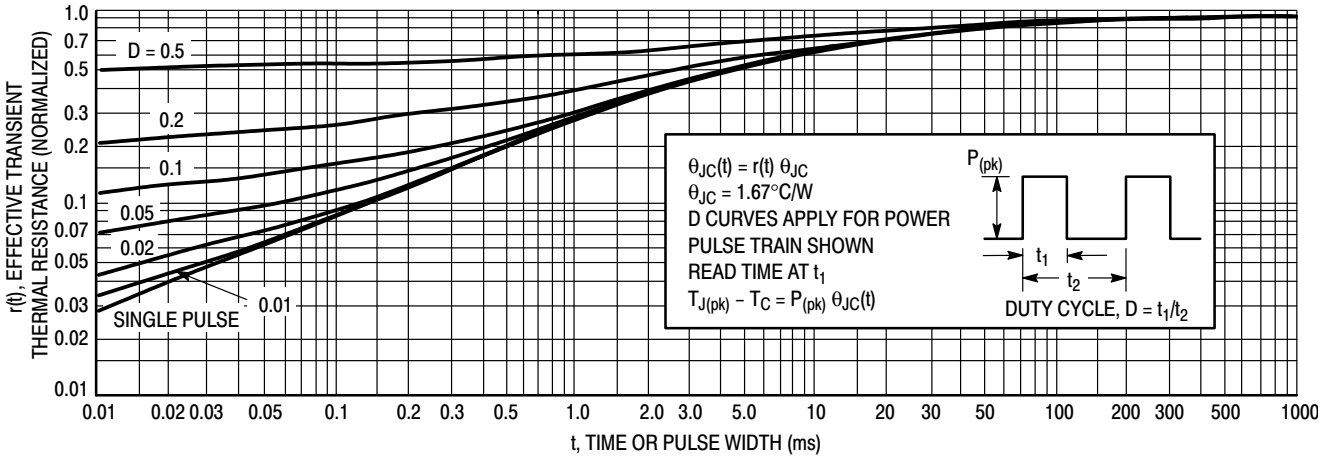


Figure 4. Thermal Response

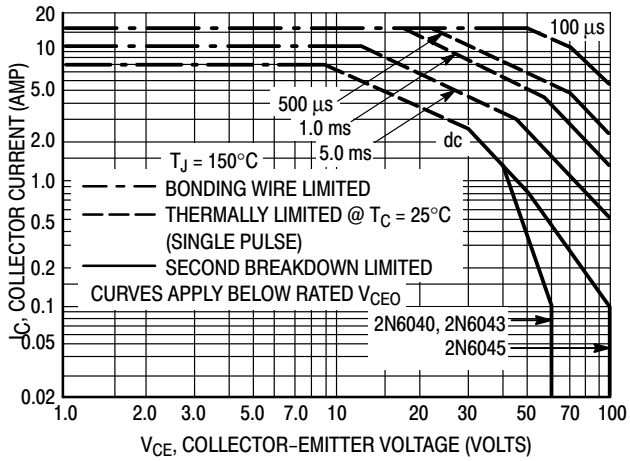


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

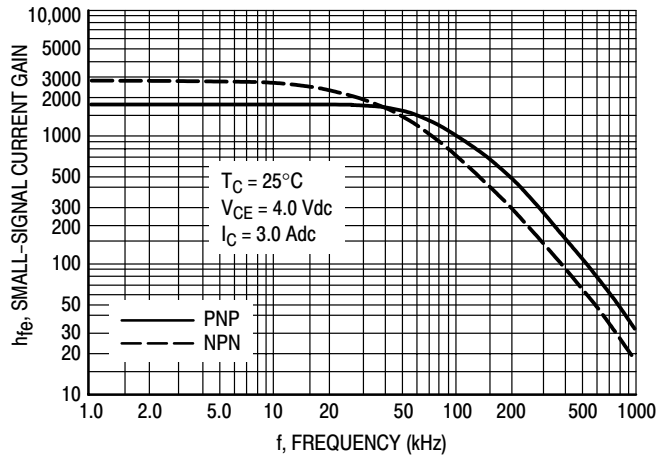


Figure 6. Small−Signal Current Gain

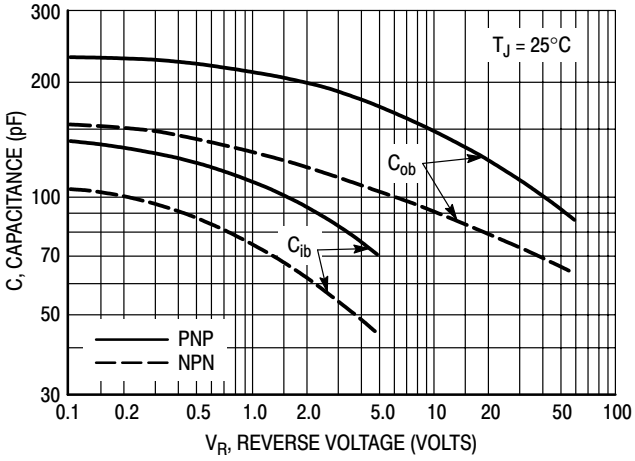
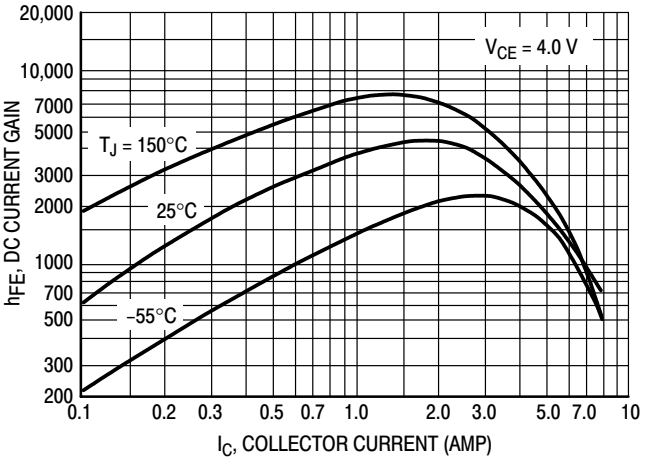


Figure 7. Capacitance

PNP
2N6040, 2N6042



NPN
2N6043, 2N6045

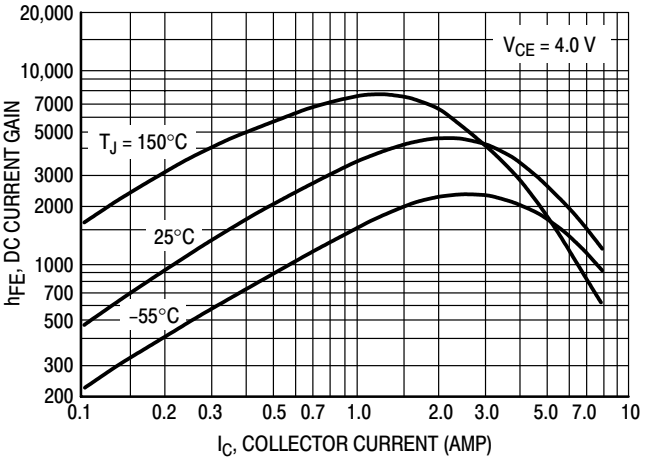
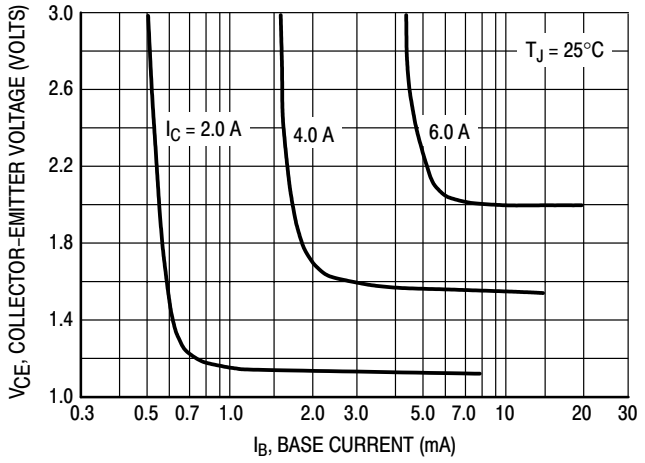


Figure 8. DC Current Gain



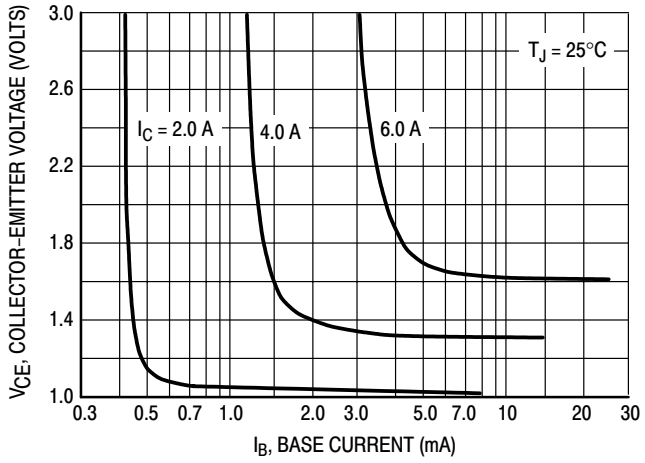
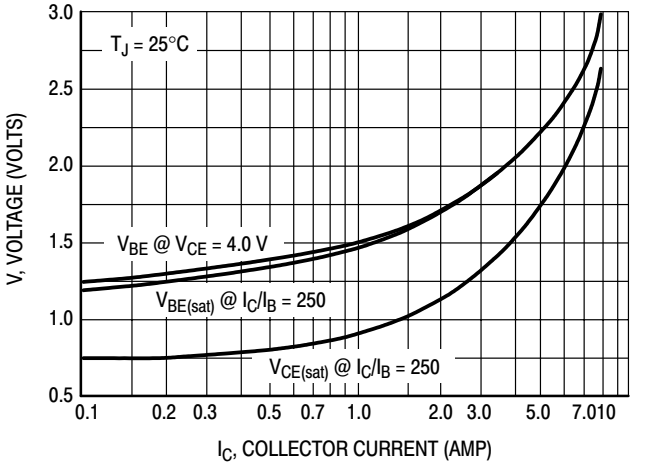


Figure 9. Collector Saturation Region



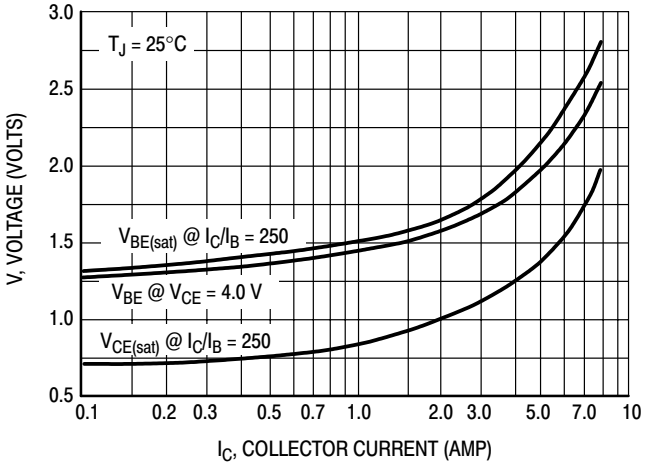


Figure 10. “On” Voltages

Darlington Complementary Silicon Power Transistors

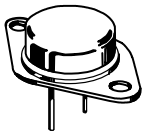
. . . designed for general–purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

PNP
2N6052*
NPN
2N6058
2N6059*

***ON Semiconductor Preferred Device**

DARLINGTON
12 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6058	2N6052 2N6059	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	12 20		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200°C		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

(1) Indicates JEDEC Registered Data.

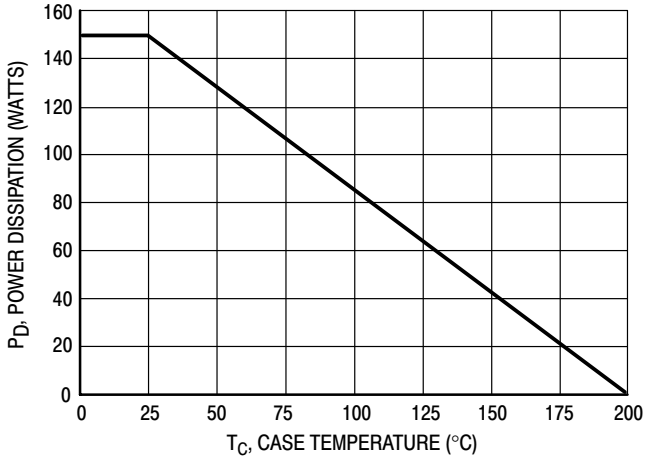


Figure 1. Power Derating

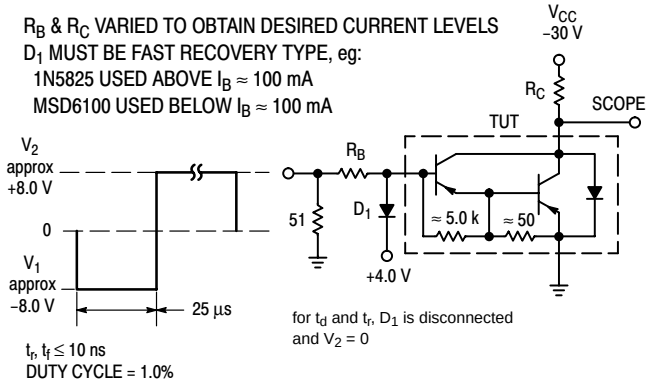
Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (2) (I_C = 100 mAdc, I_B = 0)	2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 2N6058 2N6052, 2N6059	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 —	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small–Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6052 2N6058/2N6059	C_{ob}	— —	500 300	pF
Small–Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

*Indicates JEDEC Registered Data.

(2) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

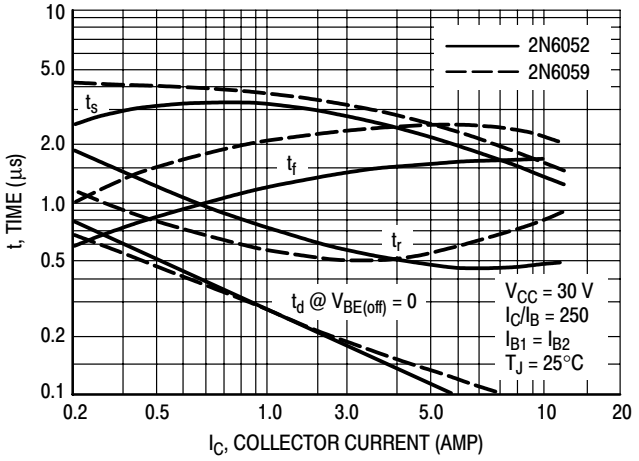


Figure 3. Switching Times

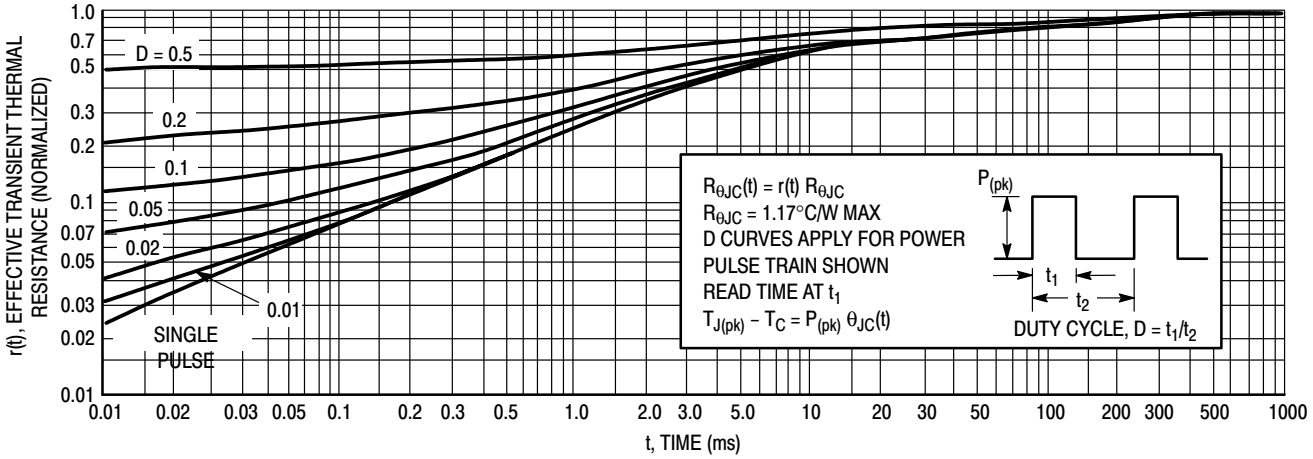


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

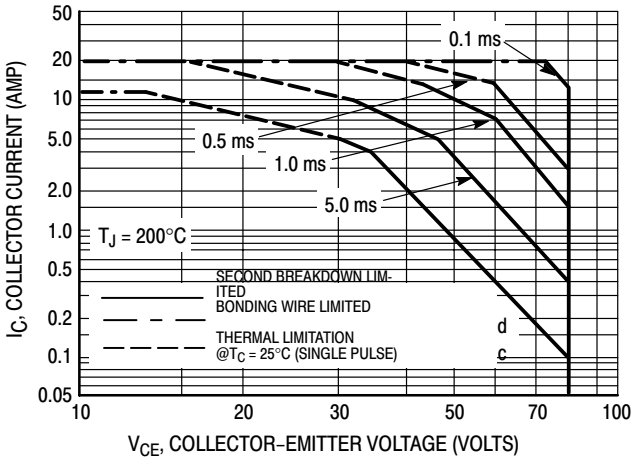


Figure 5. 2N6058

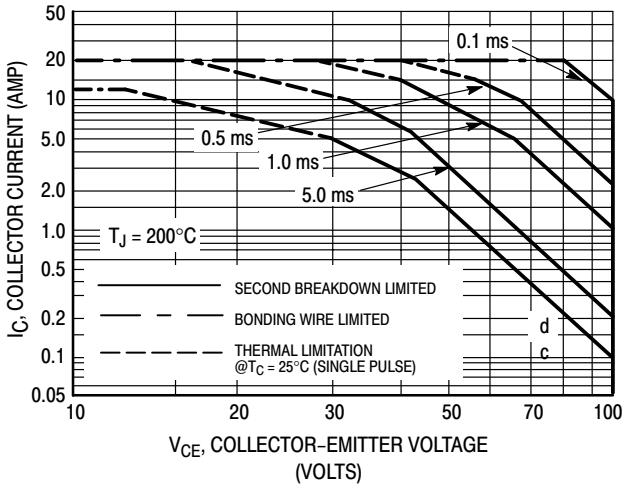


Figure 6. 2N6052, 2N6059

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6, and 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$; $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

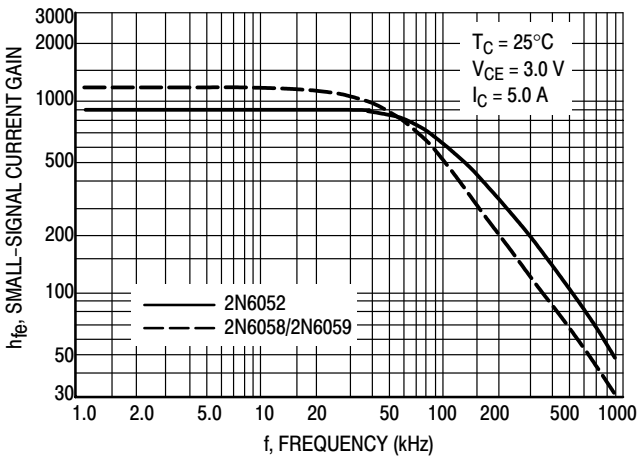


Figure 7. Small−Signal Current Gain

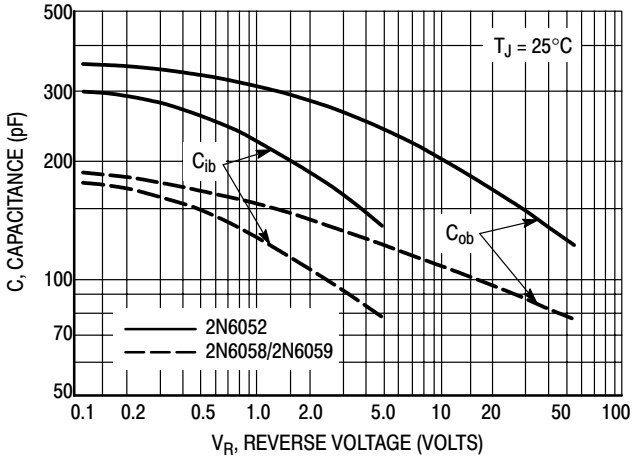


Figure 8. Capacitance

PNP
2N6052

NPN
2N6058, 2N6059

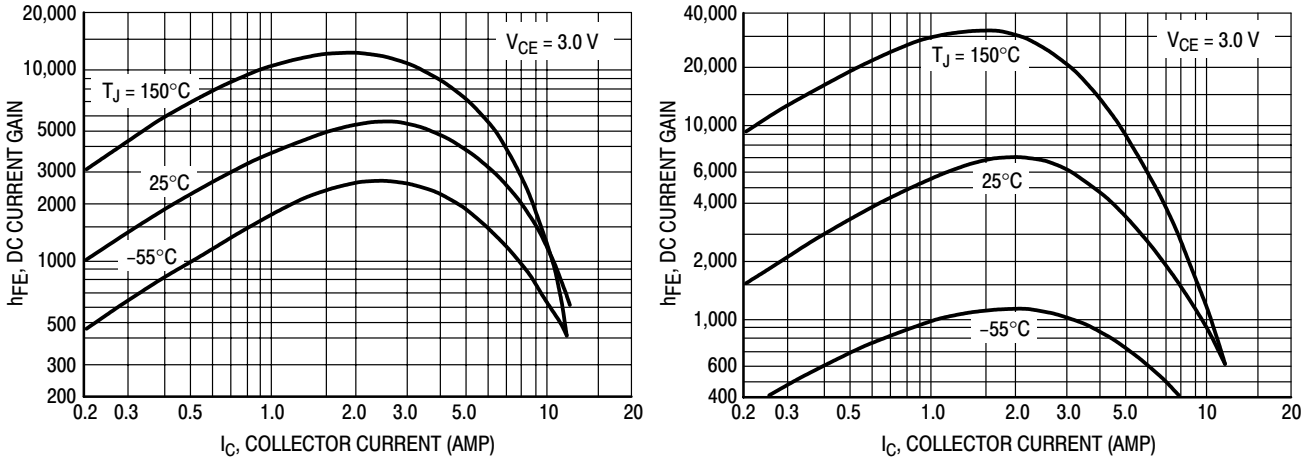


Figure 9. DC Current Gain

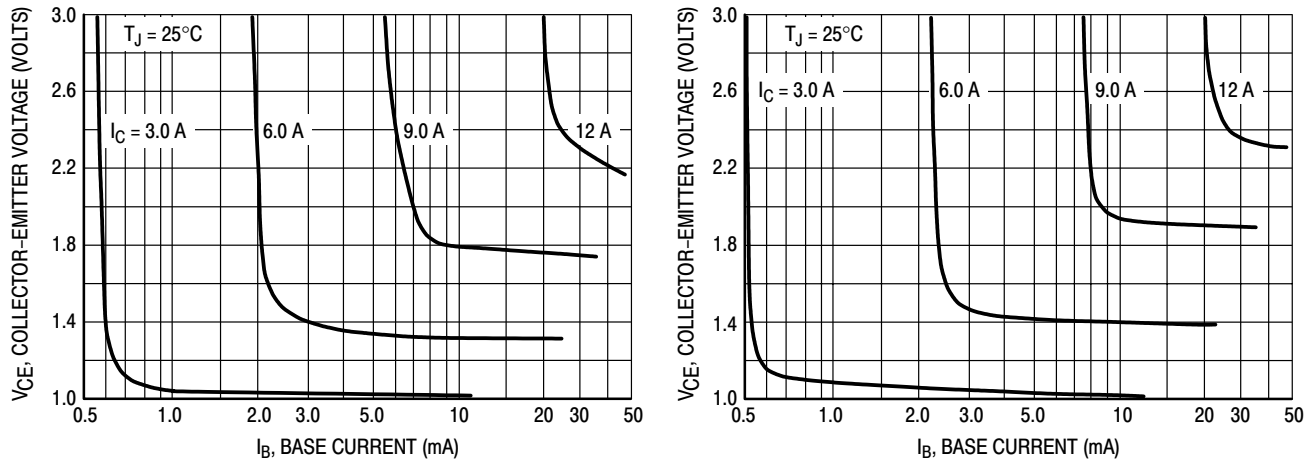


Figure 10. Collector Saturation Region

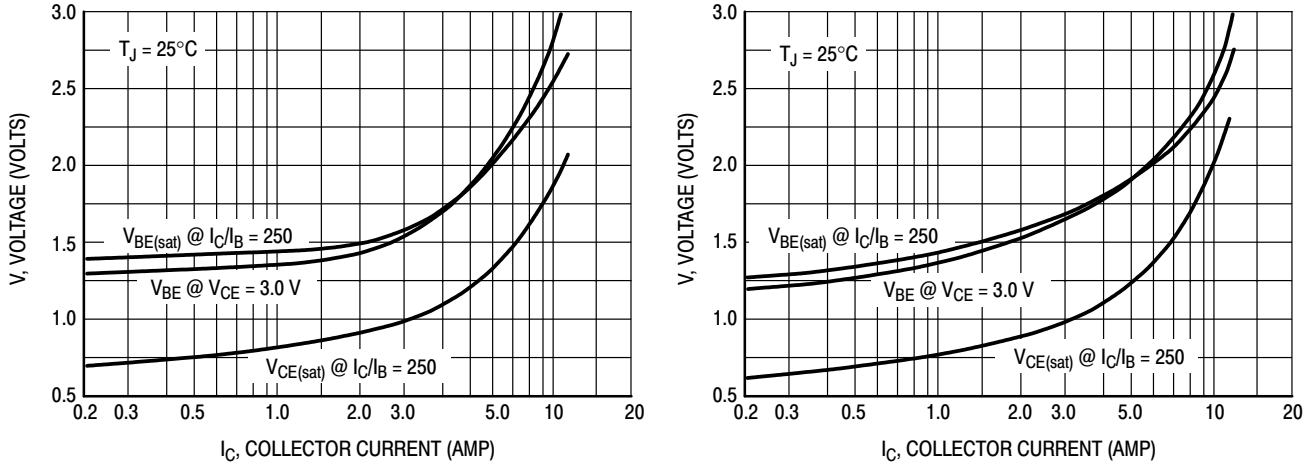


Figure 11. “On” Voltages

Complementary Silicon Plastic Power Transistors

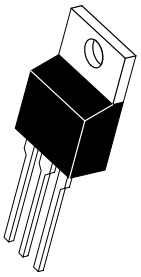
. . . designed for use in general–purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
  h_{FE} = 30–150 @ I_C
  = 3.0 Adc — 2N6111, 2N6288
  = 2.3 (Min) @ I_C = 7.0 Adc — All Devices
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) — 2N6111, 2N6288
  = 50 Vdc (Min) — 2N6109
  = 70 Vdc (Min) — 2N6107, 2N6292
- High Current Gain — Bandwidth Product
  f_T = 4.0 MHz (Min) @ I_C = 500 mAdc — 2N6288, 90, 92
  = 10 MHz (Min) @ I_C = 500 mAdc — 2N6107, 09, 11
- TO–220AB Compact Package

PNP
2N6107
2N6109*
2N6111
NPN
2N6288
2N6292*

***ON Semiconductor Preferred Device**

7 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
30–50–70 VOLTS
40 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector–Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	7.0 10			Adc
Base Current	I_B	3.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

*Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 4
Publication Order Number:
2N6107/D

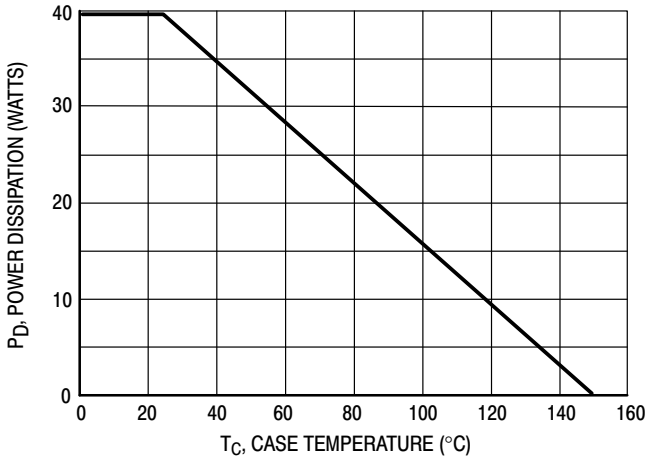


Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6111, 2N6288		30	—	
	2N6109		50	—	
	2N6107, 2N6292		70	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6111, 2N6288		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6109		—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6107, 2N6292		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6111, 2N6288		—	100	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6109		—	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6107, 2N6292		—	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6111, 2N6288		—	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6109		—	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6107, 2N6292		—	2.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N6107, 2N6292		30	150	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)	2N6109		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)	All Devices		2.3	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	3.5	Vdc
(I_C = 7.0 Adc, I_B = 3.0 Adc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	3.0	Vdc
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)	2N6288, 92		4.0	—	
	2N6107, 09, 11		10	—	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	250	pF
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)		h_{fe}	20	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

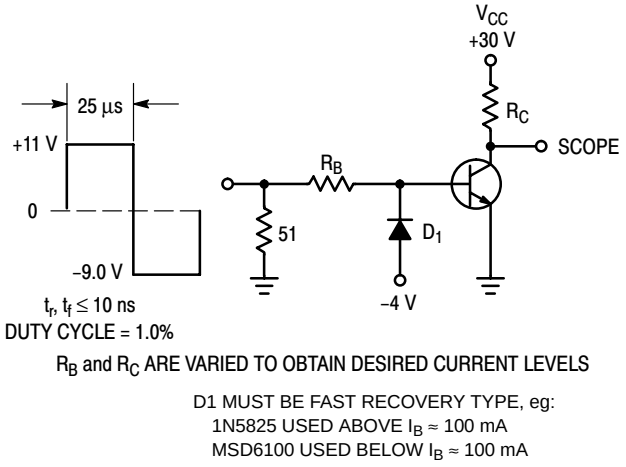


Figure 2. Switching Time Test Circuit

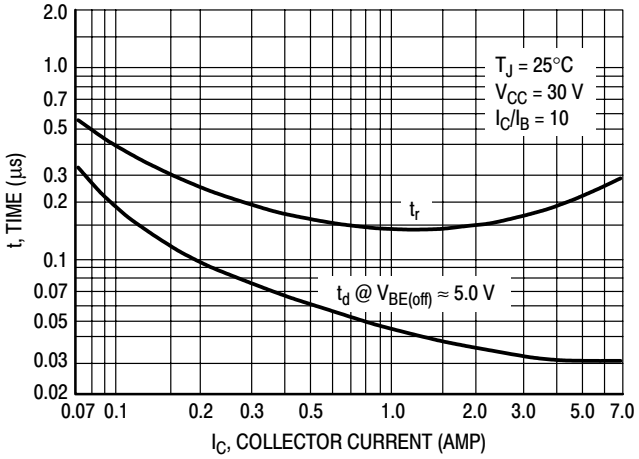


Figure 3. Turn–On Time

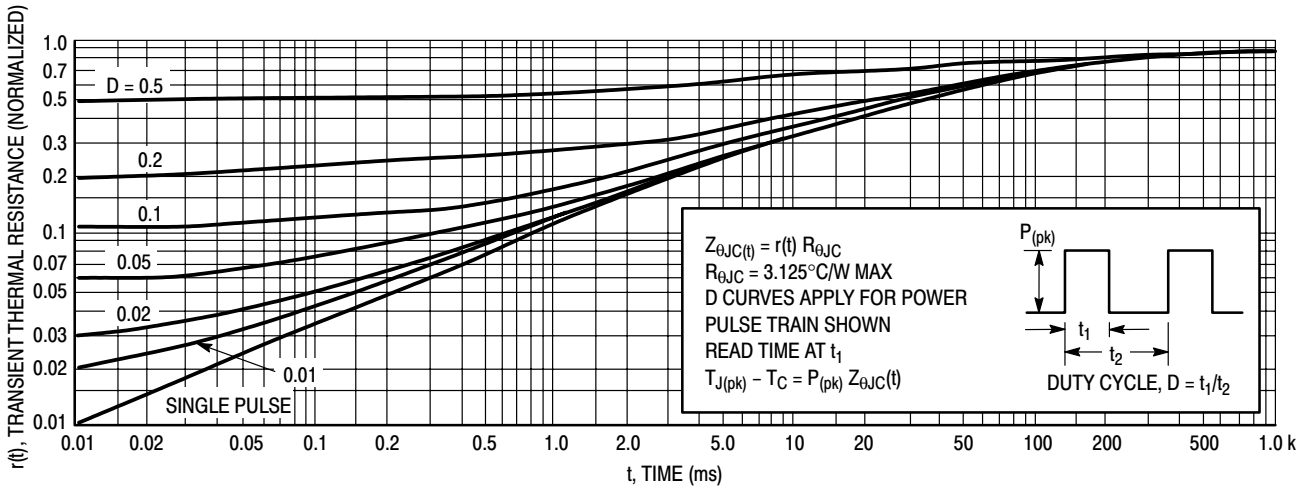


Figure 4. Thermal Response

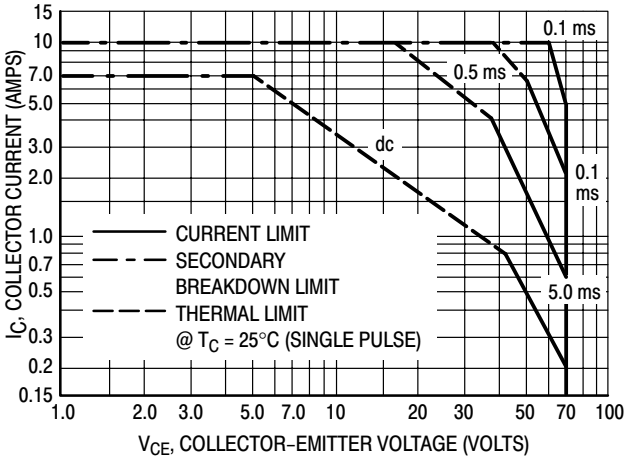


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

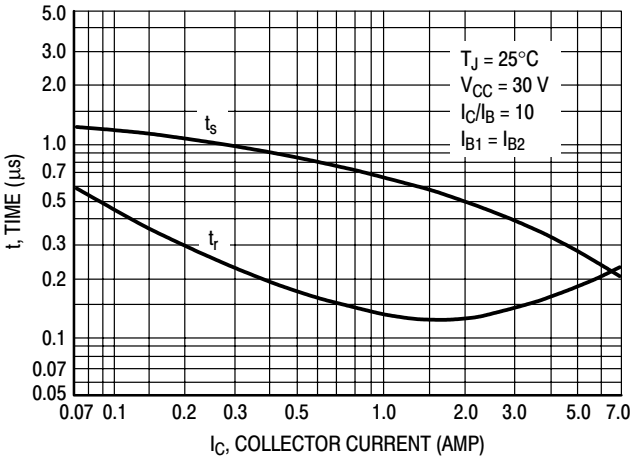


Figure 6. Turn–Off Time

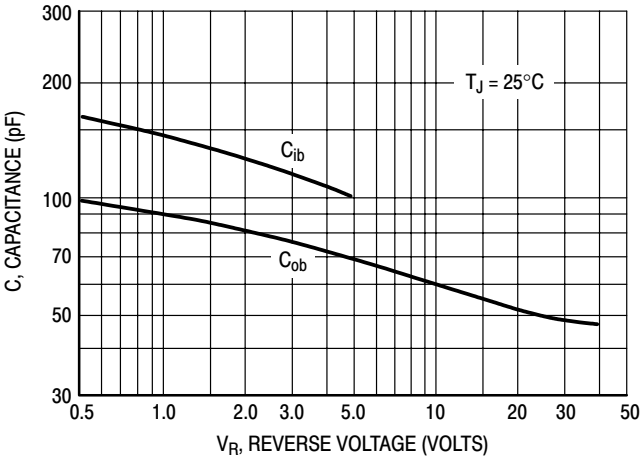


Figure 7. Capacitance

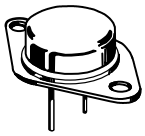
Darlington Complementary Silicon Power Transistors

. . . designed for general–purpose amplifier and low–frequency switching applications.

- High DC Current Gain @ I_C = 10 Adc –
  h_{FE} = 2400 (Typ) – 2N6284
  = 4000 (Typ) – 2N6287
- Collector–Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

NPN
2N6283
2N6284
PNP
2N6286
2N6287

DARLINGTON
20 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
100 VOLTS
160 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6283 2N6286	2N6284 2N6287	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	20 40		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to +200		°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	°C/W

*Indicates JEDEC Registered Data.

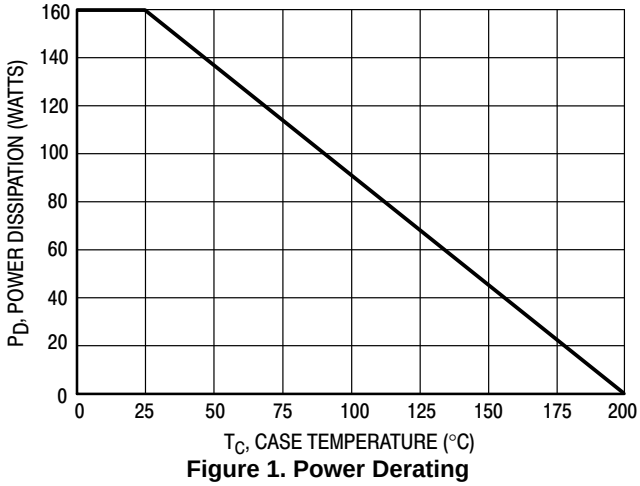


Figure 1. Power Derating

May, 2001 – Rev. 1
Publication Order Number:
2N6284/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	2N6283, 2N6286 2N6284, 2N6287	$V_{CEO(sus)}$	**80** 100	– –	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	 – –	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 – –	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 –	–
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	 – –	 2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6283, 2N6284 2N6286, 2N6287	C_{ob}	 – –	 400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

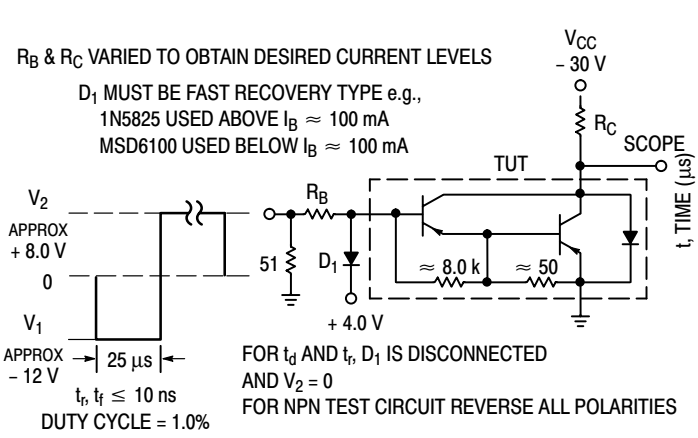


Figure 2. Switching Times Test Circuit

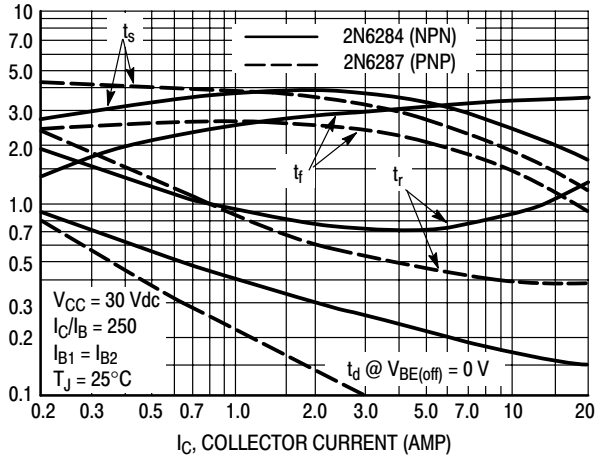


Figure 3. Switching Times

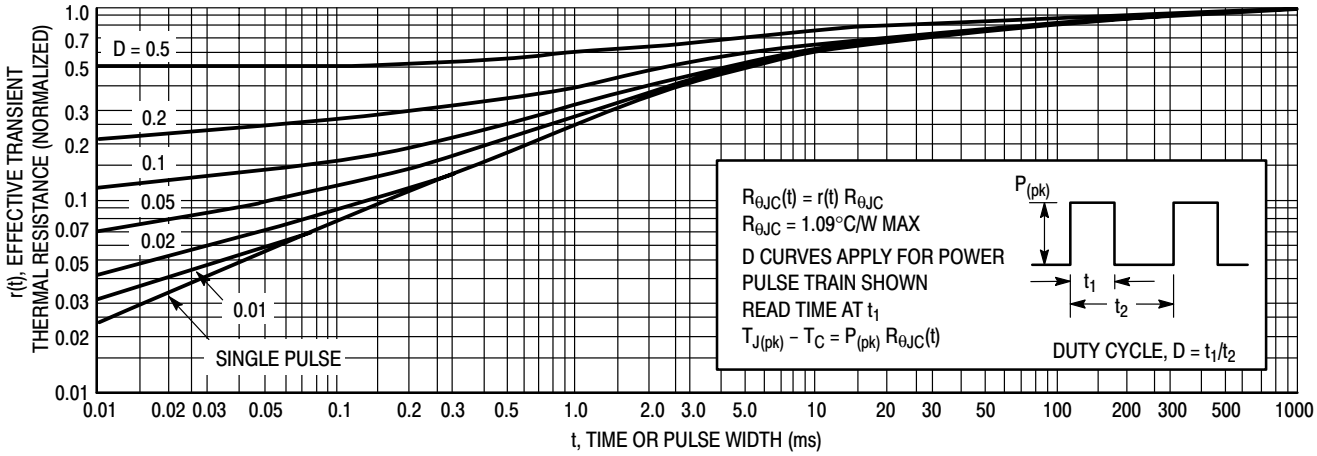


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

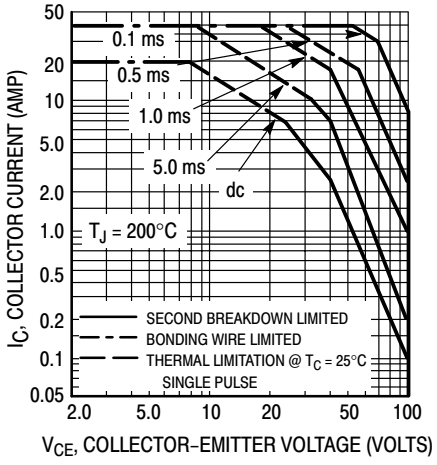


Figure 5. 2N6284, 2N6287

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} <$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

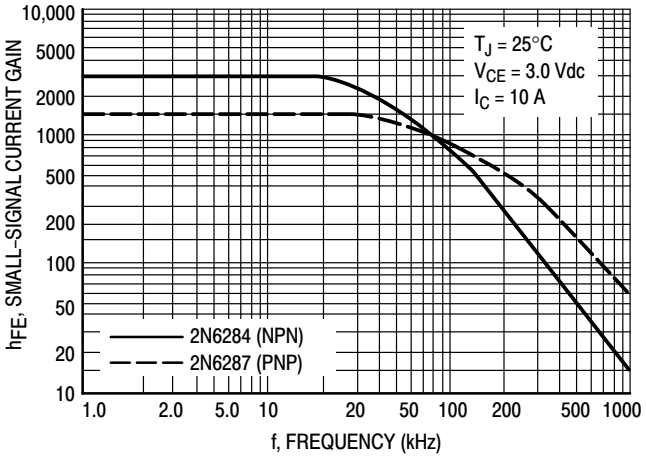


Figure 6. Small–Signal Current Gain

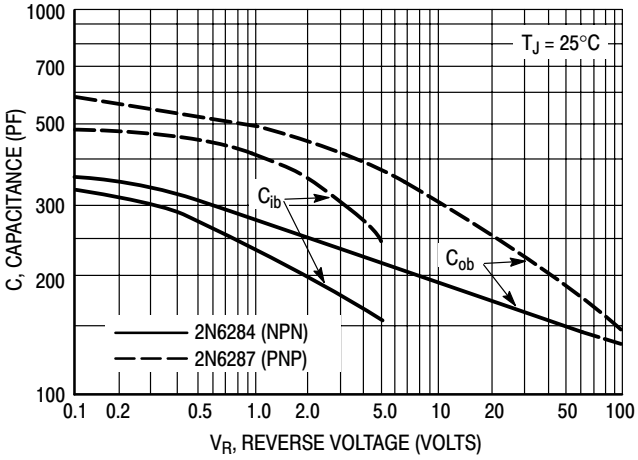
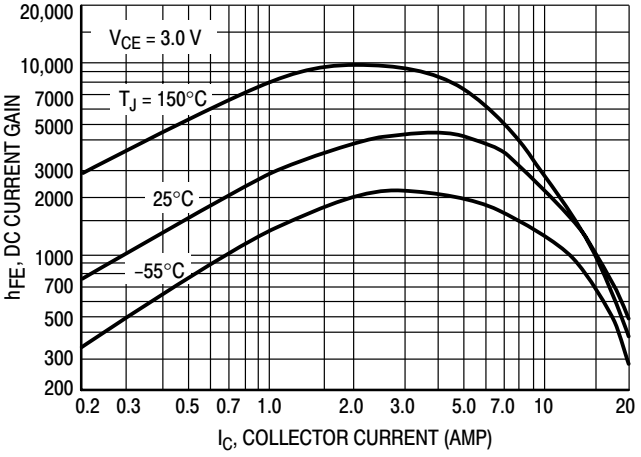


Figure 7. Capacitance

NPN
2N6284



PNP
2N6287

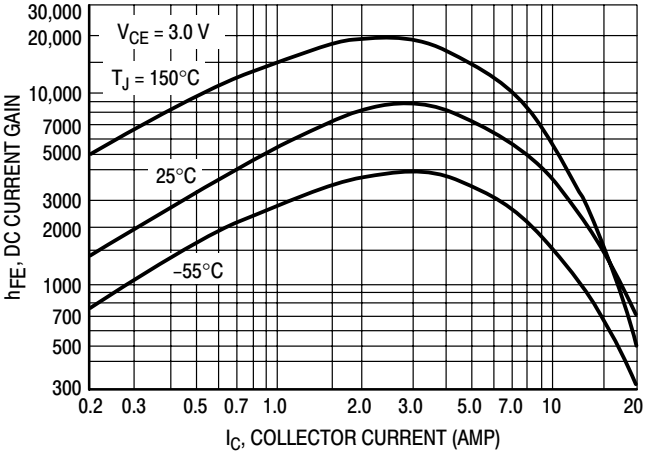
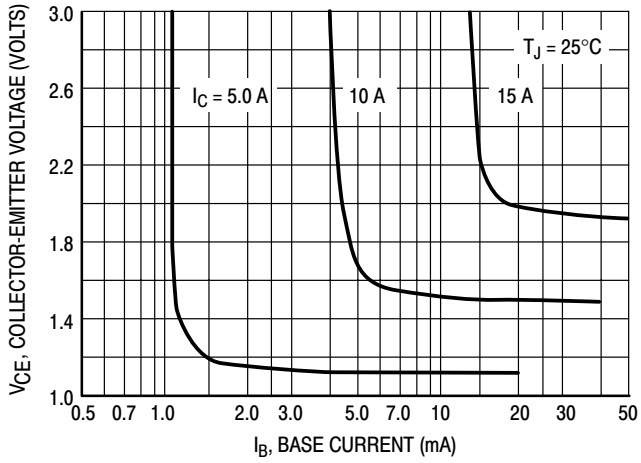


Figure 8. DC Current Gain



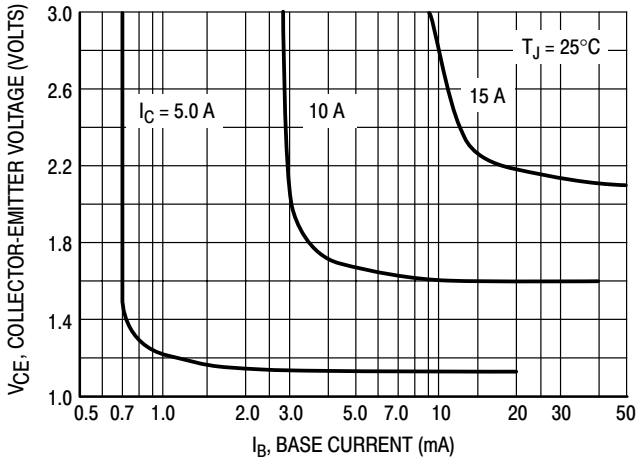
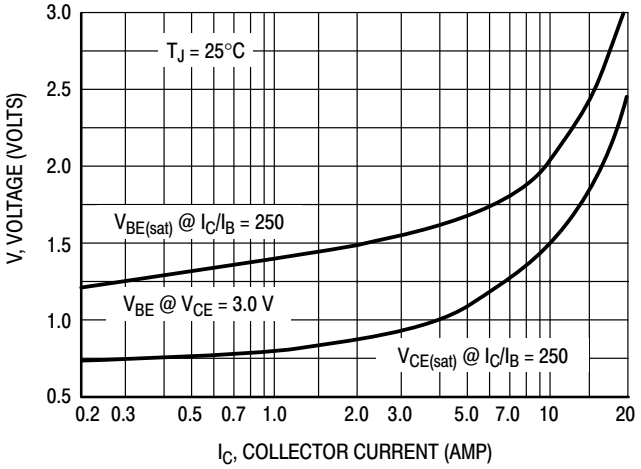


Figure 9. Collector Saturation Region



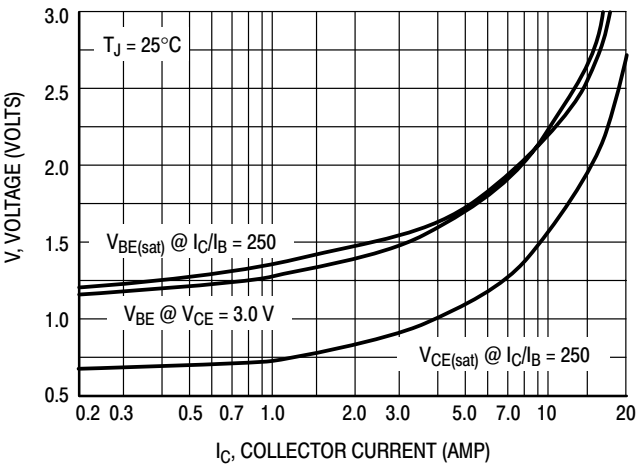


Figure 10. “On” Voltages

NPN
2N6284

PNP
2N6287

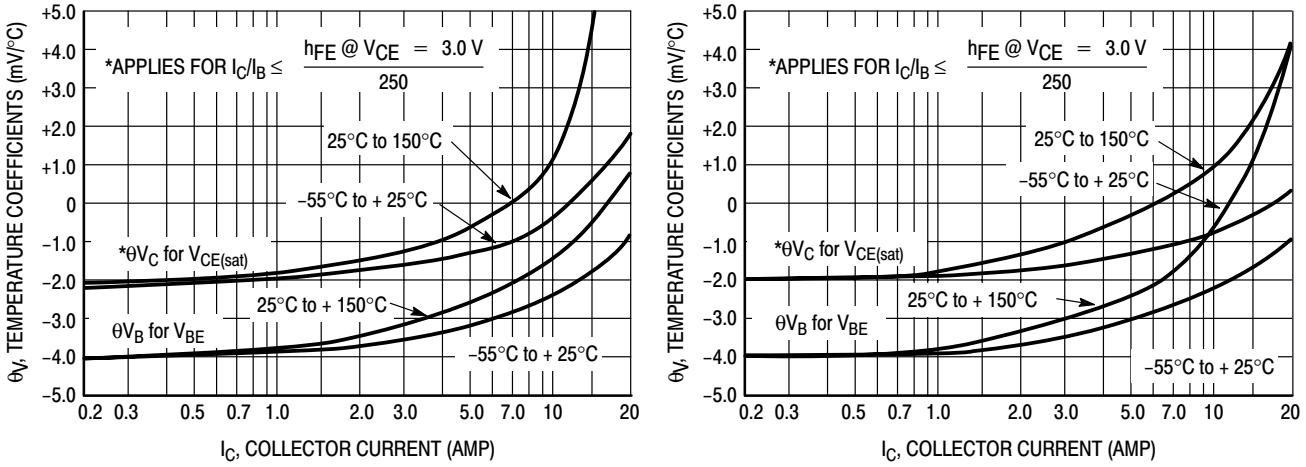


Figure 11. Temperature Coefficients

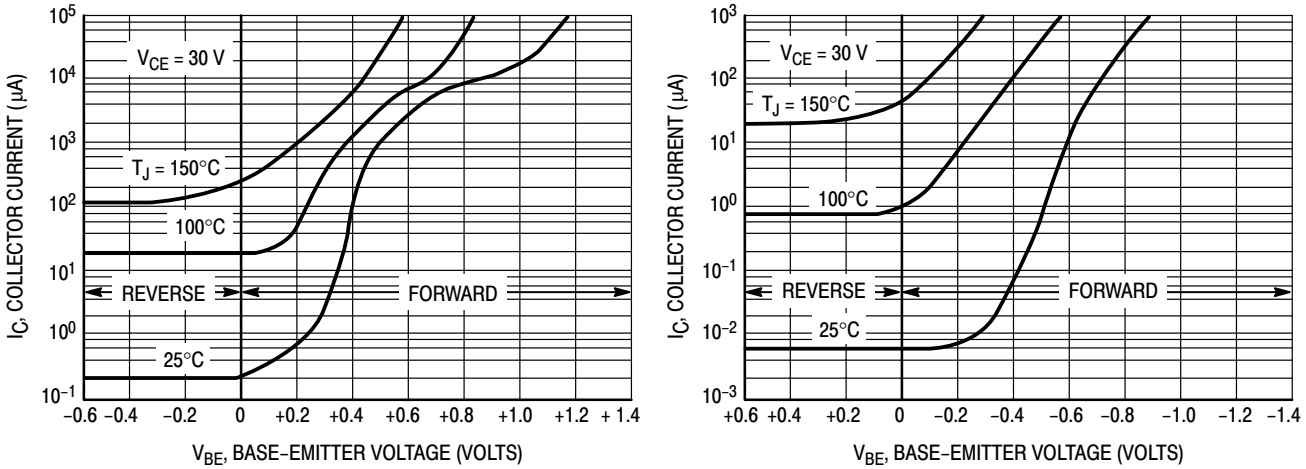


Figure 12. Collector Cut−Off Region

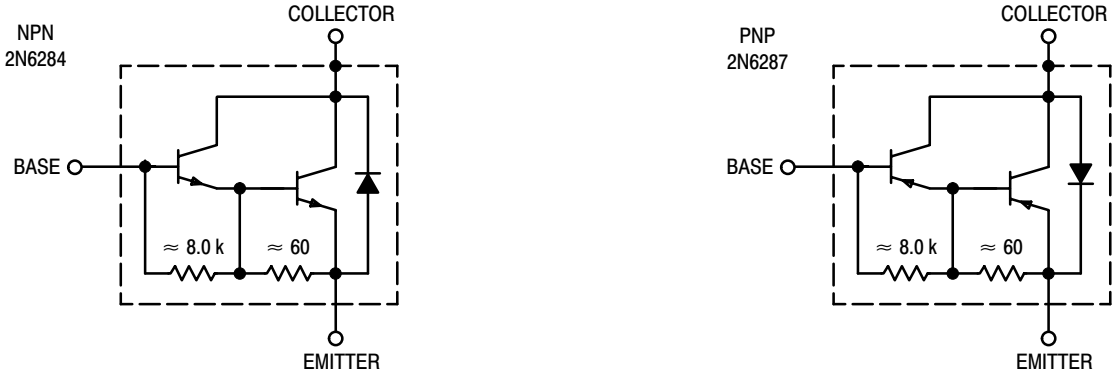


Figure 13. Darlington Schematic

High-Power NPN Silicon Transistors

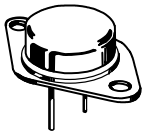
. . . designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector–Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6338
  = 150 Vdc (Min) – 2N6341
- High DC Current Gain –
  h_{FE} = 30 – 120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector–Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 ms (Max)
  t_s = 1.0 ms (Max)
  t_f = 0.25 ms (Max)

2N6338
2N6341*

*ON Semiconductor Preferred Device

25 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6338	2N6341	Unit
Collector–Base Voltage	V_{CB}	120	180	Vdc
Collector–Emitter Voltage	V_{CEO}	100	150	Vdc
Emitter–Base Voltage	V_{EB}	6.0		Vdc
Collector Current Continuous Peak	I_C	 25 50		Adc
Base Current	I_B	10		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 200 1.14		 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

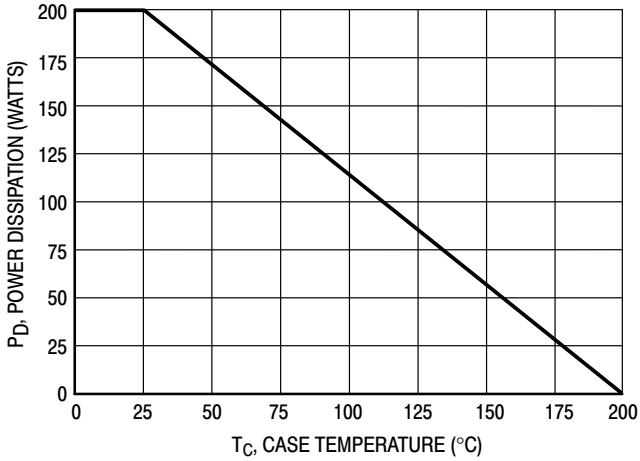


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 10
Publication Order Number:
2N6338/D

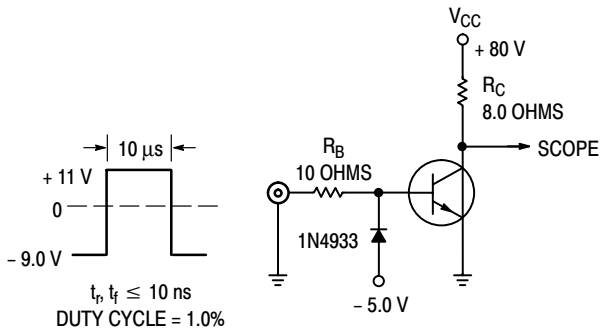
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6338 2N6341	$V_{CEO(sus)}$	100 150	– –	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 75 Vdc, I_B = 0)	 2N6338 2N6341	I_{CEO}	 – –	 50 50	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 – –	 10 1.0	 μAdc mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain) (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 50 30 12	 – 120 –	–
Collector Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{CE(sat)}$	 – –	 1.0 1.8	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	 – –	 1.8 2.5	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r	–	0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.



NOTE: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

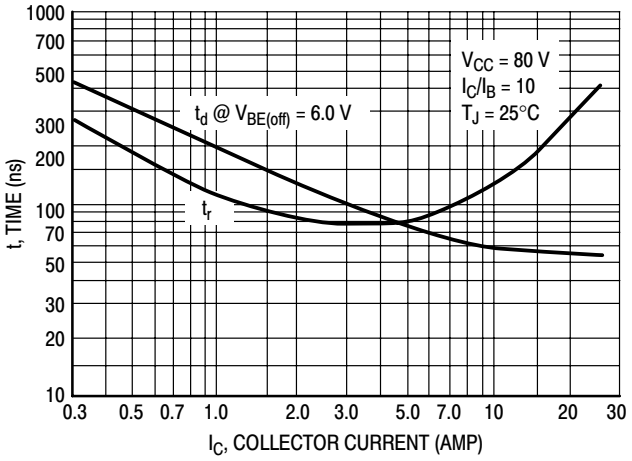


Figure 3. Turn–On Time

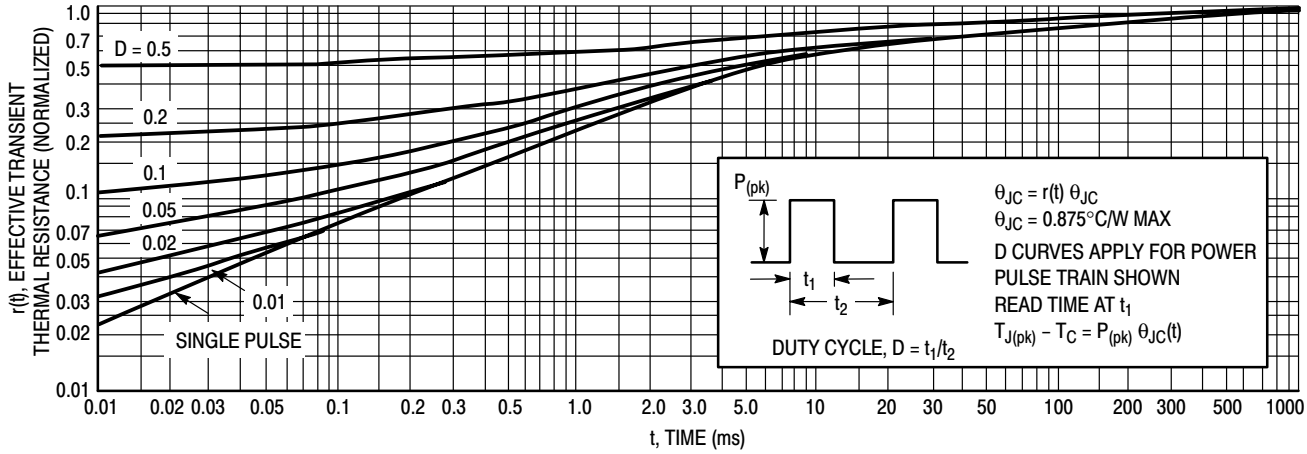


Figure 4. Thermal Response

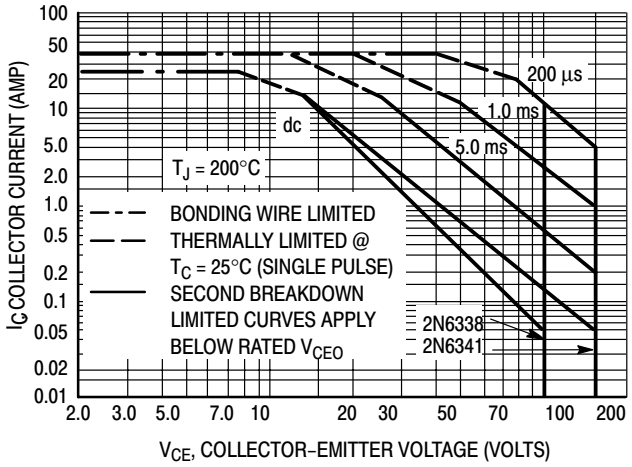


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

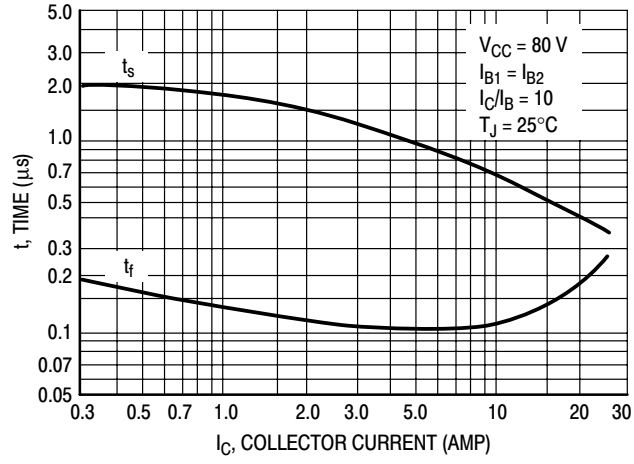


Figure 6. Turn–Off Time

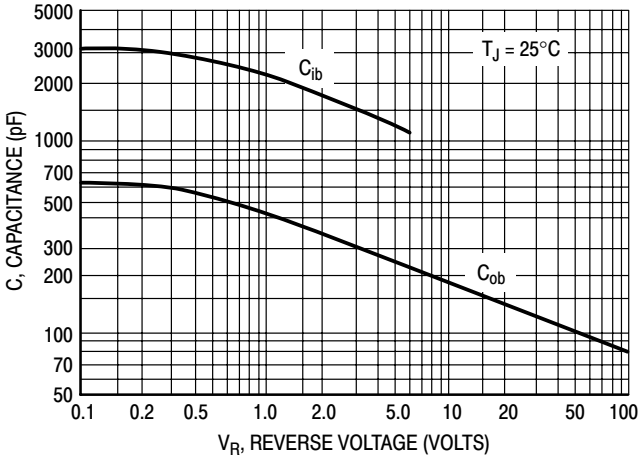


Figure 7. Capacitance

Plastic Medium-Power Silicon Transistors

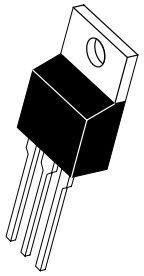
2N6387
2N6388*

*ON Semiconductor Preferred Device

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C
  = 4.0 Adc
- Collector–Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6387
  = 80 Vdc (Min) — 2N6388
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C
  = 5.0 Adc — 2N6387, 2N6388
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

DARLINGTON
8 AND 10 AMPERE
NPN SILICON
POWER TRANSISTORS
60–80 VOLTS
65 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6387	2N6388	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15	10 15	Adc
Base Current	I_B	250		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52		 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016		 Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N6387/D

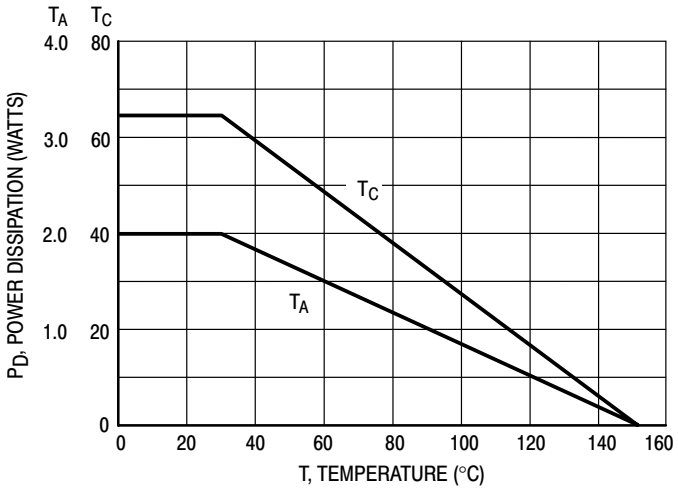


Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6387		60	—	
	2N6388		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N6387		—	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6388		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6387		—	300	
(V_{CE} – 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6388		—	300	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6387		—	3.0	mAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6388		—	3.0	
Emitter Cutoff Current		I_{EBO}	—	5.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		1000	20,000	
(I_C = 1 0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		100	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6387, 2N6388		—	2.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6387, 2N6388		—	3.0	
Base–Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	2.8	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	4.5	
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		$\|h_{fe}\|$	20	—	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	—	200	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)					
Small–Signal Current Gain		h_{fe}	1000	—	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

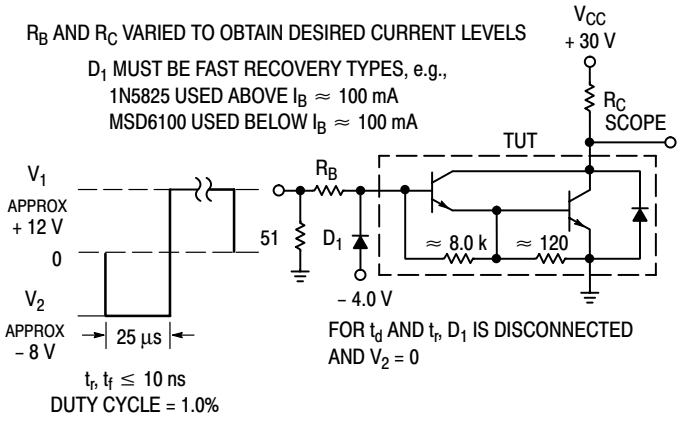


Figure 2. Switching Times Test Circuit

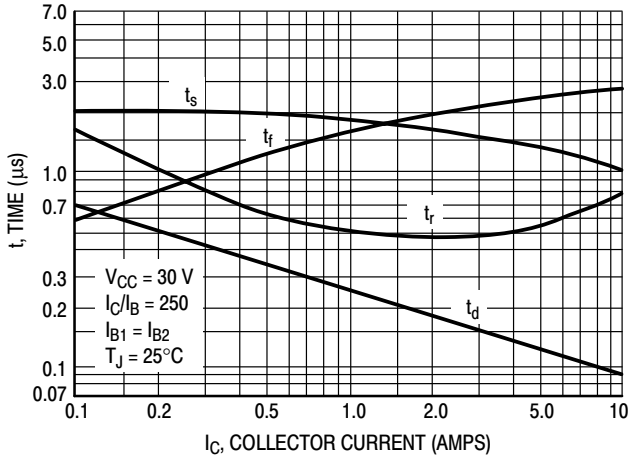


Figure 3. Switching Times

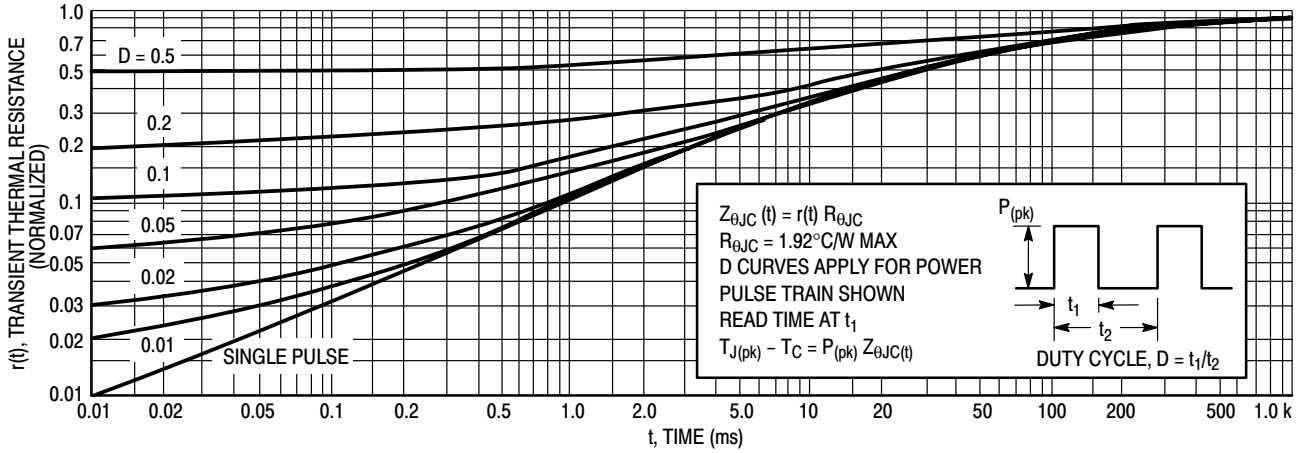


Figure 4. Thermal Response

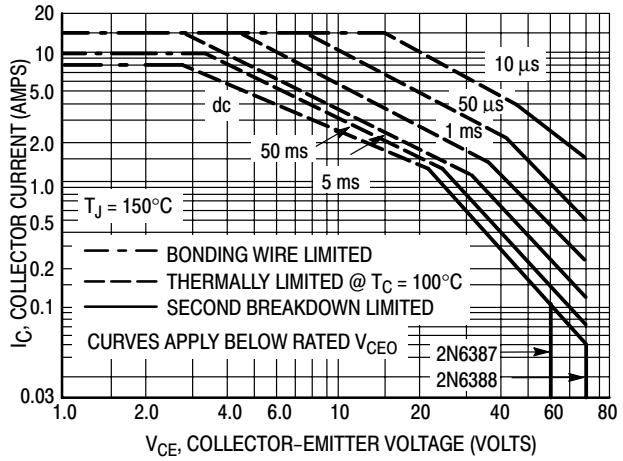


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

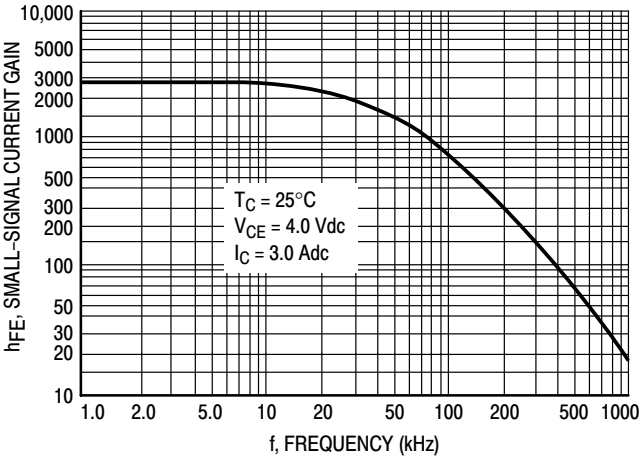


Figure 6. Small–Signal Current Gain

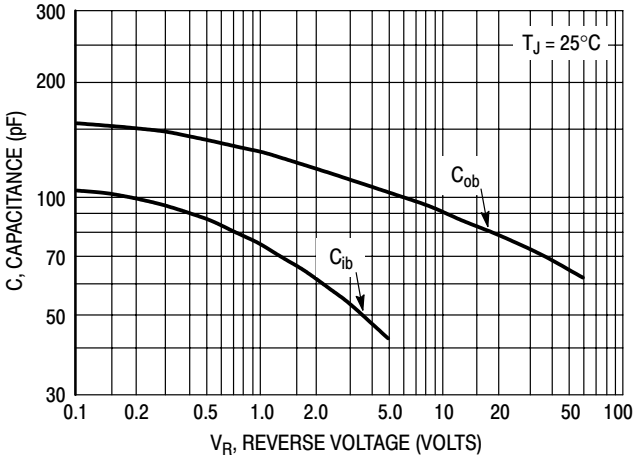


Figure 7. Capacitance

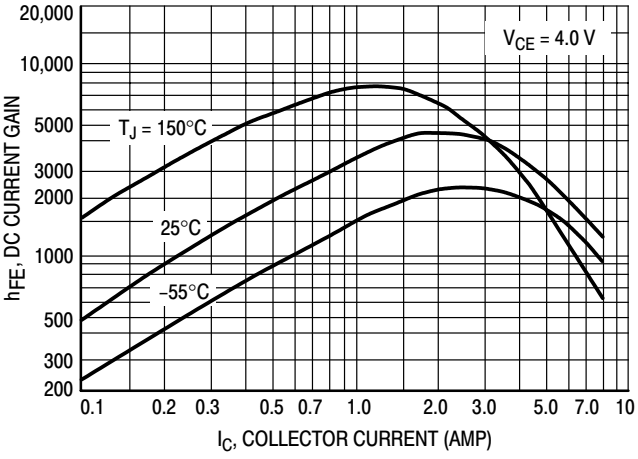


Figure 8. DC Current Gain

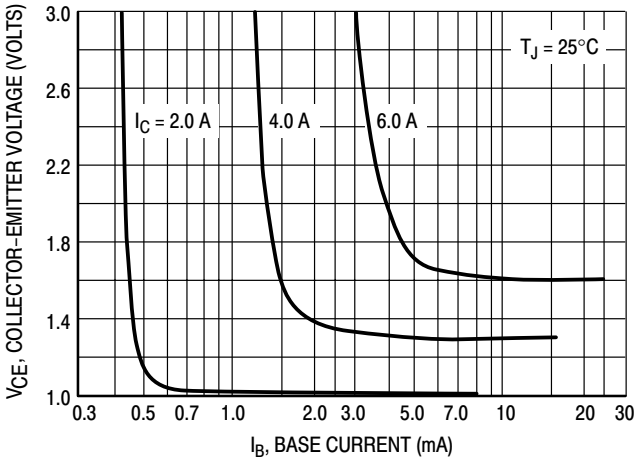


Figure 9. Collector Saturation Region

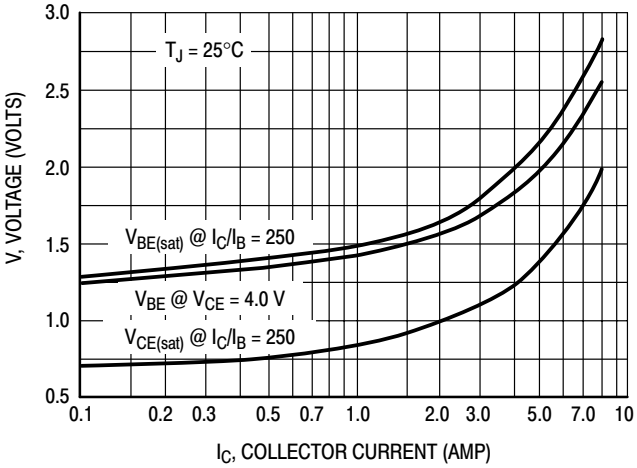


Figure 10. “On” Voltages

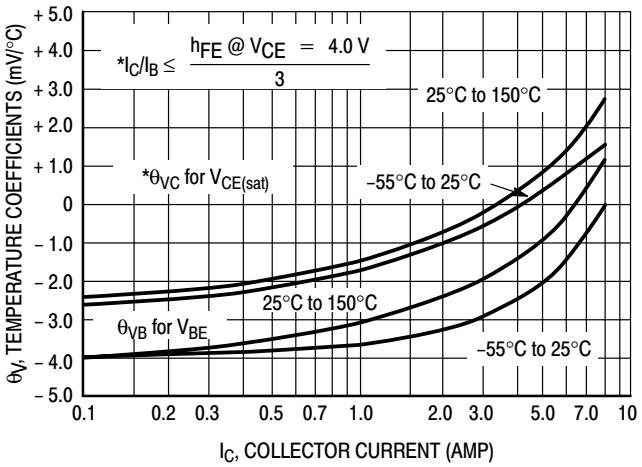


Figure 11. Temperature Coefficients

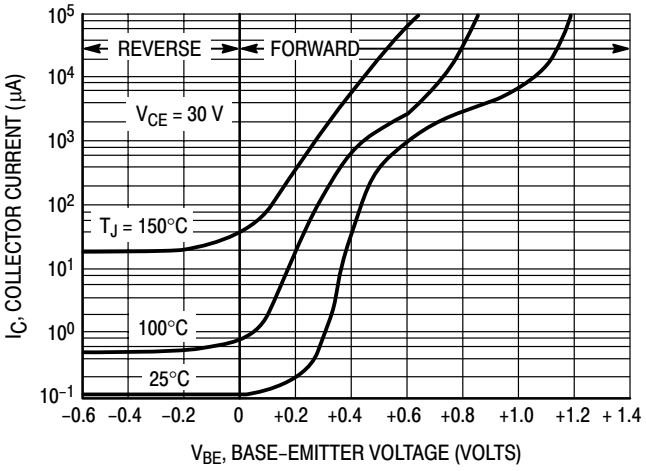


Figure 12. Collector Cut–Off Region

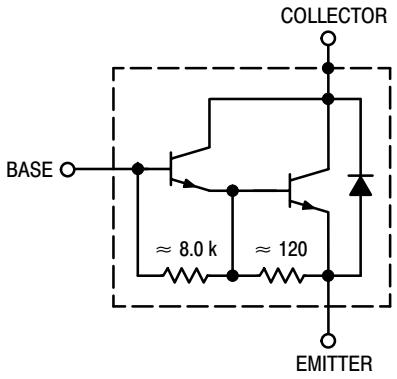


Figure 13. Darlington Schematic

Complementary Silicon Plastic Power Transistors

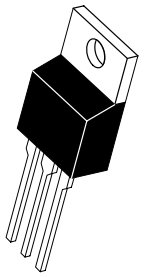
. . . designed for use in general–purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes —
  h_{FE} = 20–150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6487, 2N6490
  = 80 Vdc (Min) – 2N6488, 2N6491
- High Current Gain — Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO–220AB Compact Package

NPN
2N6487
2N6488*
PNP
2N6490
2N6491*

***ON Semiconductor Preferred Device**

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80 VOLTS 75 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6487 2N6490	2N6488 2N6491	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	70	90	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	5.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.8 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

(1) Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
2N6487/D

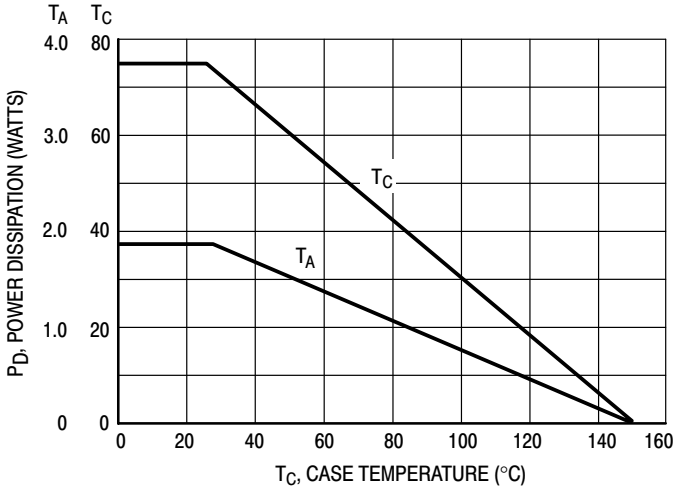


Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	 2N6487, 2N6490 2N6488, 2N6491	$V_{CEO(sus)}$	 60 80	 —	Vdc
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	 2N6487, 2N6490 2N6488, 2N6491	VCEX	 70 90	 — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N6487, 2N6490 2N6488, 2N6491	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N6487, 2N6490 2N6488, 2N6491 2N6487, 2N6490 2N6488, 2N6491	I_{CEX}	 — — — —	 500 500 5.0 5.0	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 20 5.0	 150 —	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 15 Adc, I_B = 5.0 Adc)		$V_{CE(sat)}$	 — —	 1.3 3.5	Vdc
Base–Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	 — —	 1.3 3.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)		f_T	5.0	—	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

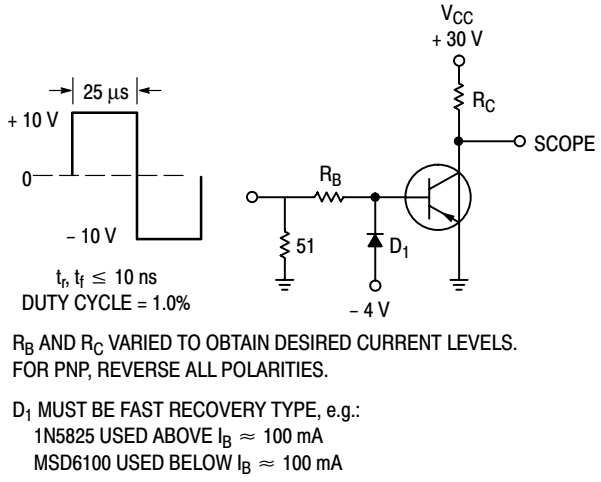


Figure 2. Switching Time Test Circuit

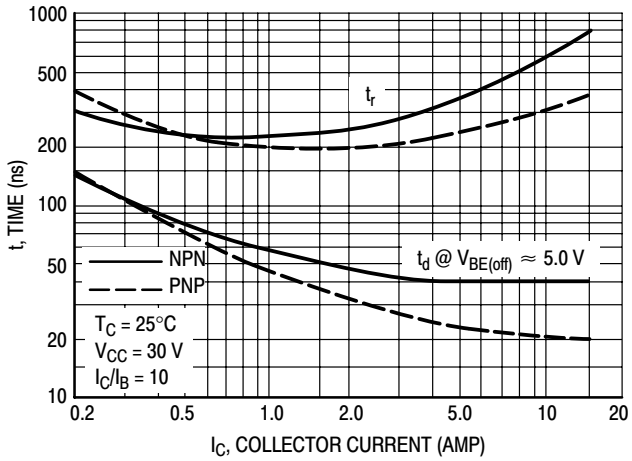


Figure 3. Turn–On Time

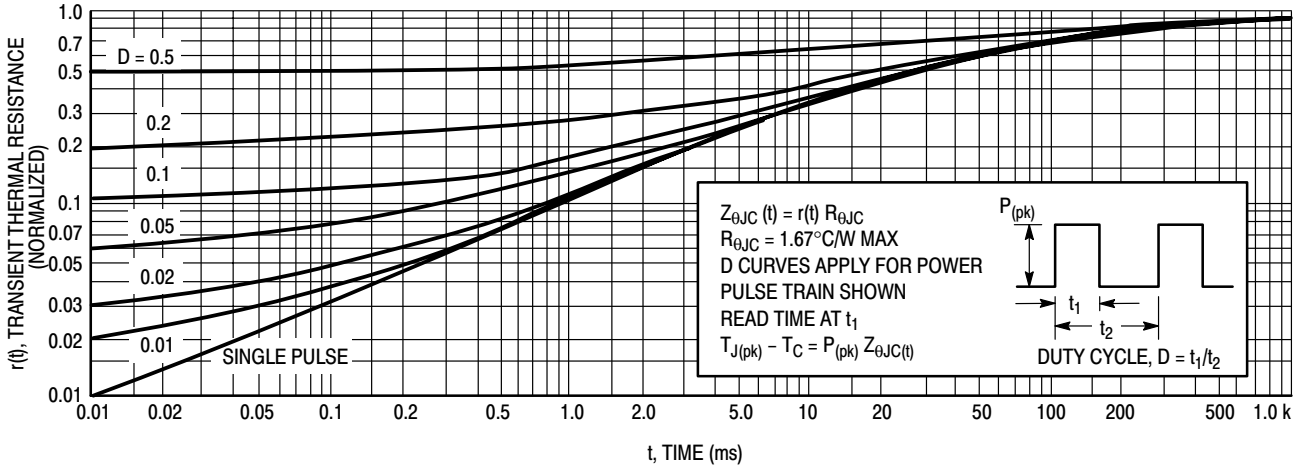


Figure 4. Thermal Response

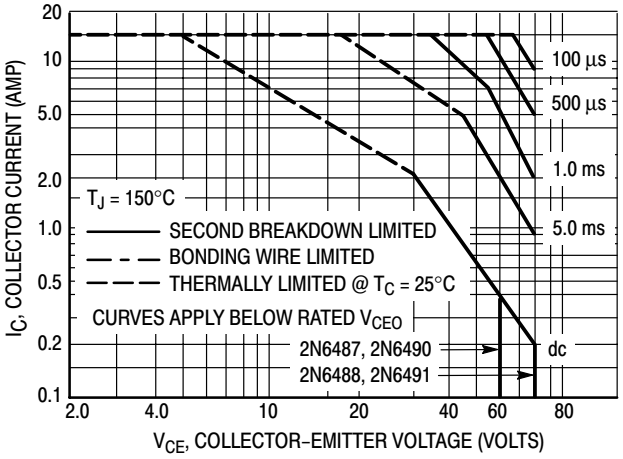


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

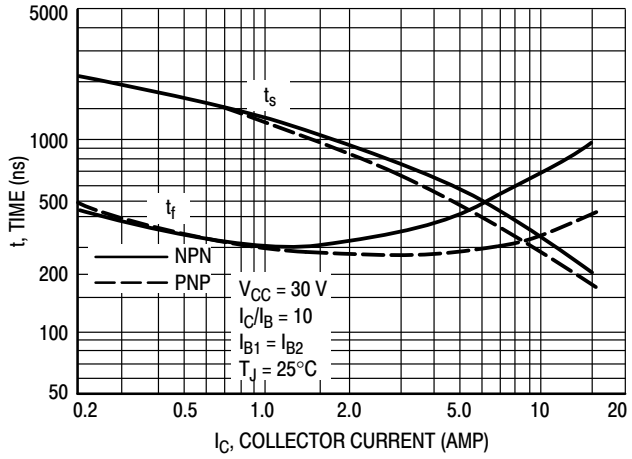


Figure 6. Turn–Off Time

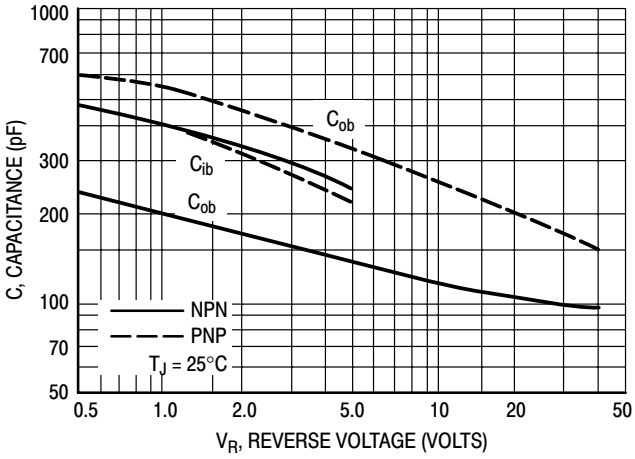


Figure 7. Capacitances

NPN
2N6487, 2N6488

PNP
2N6490, 2N6491

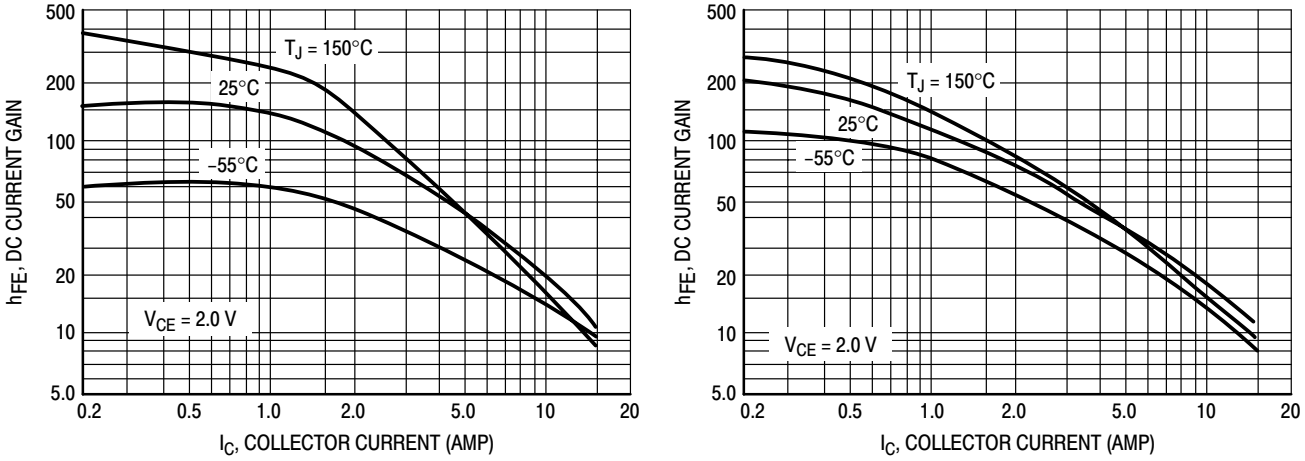


Figure 8. DC Current Gain

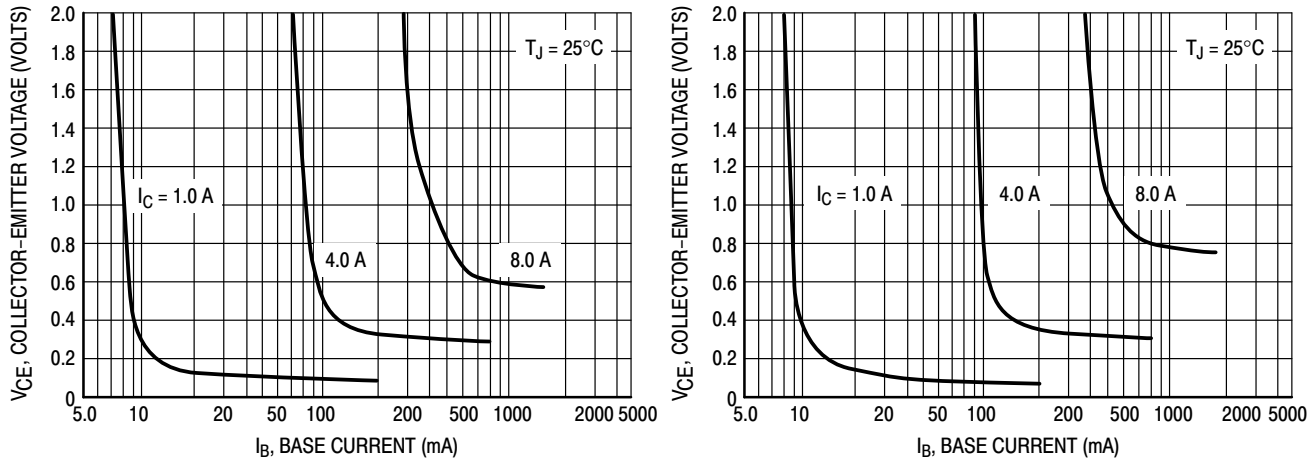


Figure 9. Collector Saturation Region

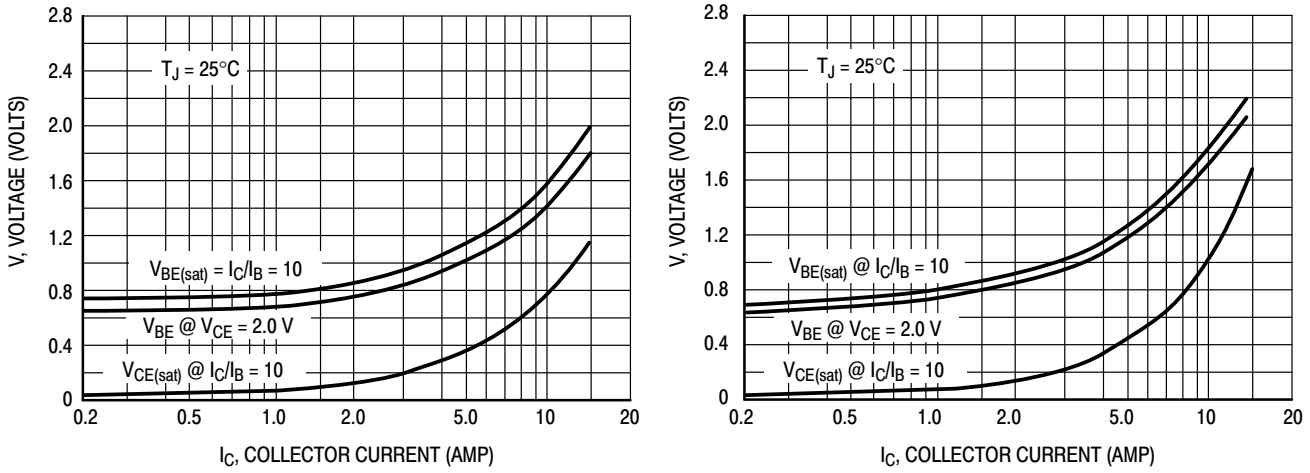


Figure 10. “On” Voltages

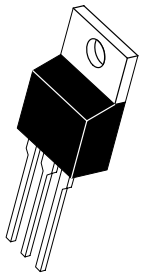
High Voltage NPN Silicon Power Transistors

2N6497

. . . designed for high voltage inverters, switching regulators and line–operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector–Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 250 Vdc (Min)
- Excellent DC Current Gain
  h_{FE} = 10–75 @ I_C = 2.5 Adc
- Low Collector–Emitter Saturation Voltage @ I_C = 2.5 Adc –
  $V_{CE(sat)}$ = 1.0 Vdc (Max)

5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 VOLT
80 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CB}	350	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous – Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

(1) Indicates JEDEC Registered Data.

May, 2001 – Rev. 10
Publication Order Number:
2N6497/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 25 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current (V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEX}	– –	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 10 Vdc) (I_C = 5.0 Adc, V_{CE} = 10 Vdc)	h_{FE}	10 3.0	– –	75 –	–
Collector–Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) (I_C = 5.0 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	– –	– –	1.0 5.0	Vdc
Base–Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) (I_C = 5.0 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	– –	– –	1.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	5.0	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)	t_r	–	0.4	1.0	μs
Storage Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)	t_s	–	1.4	2.5	μs
Fall Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	t_f	–	0.45	1.0	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

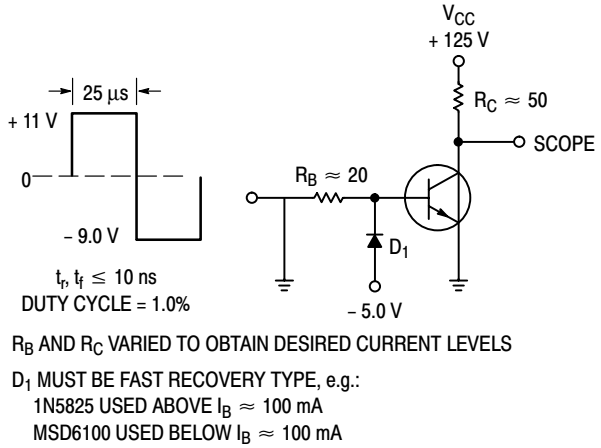


Figure 11. Switching Time Test Circuit

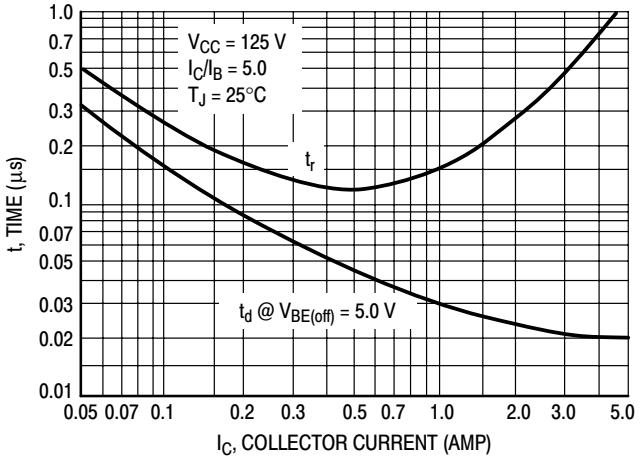


Figure 12. Turn–On Time

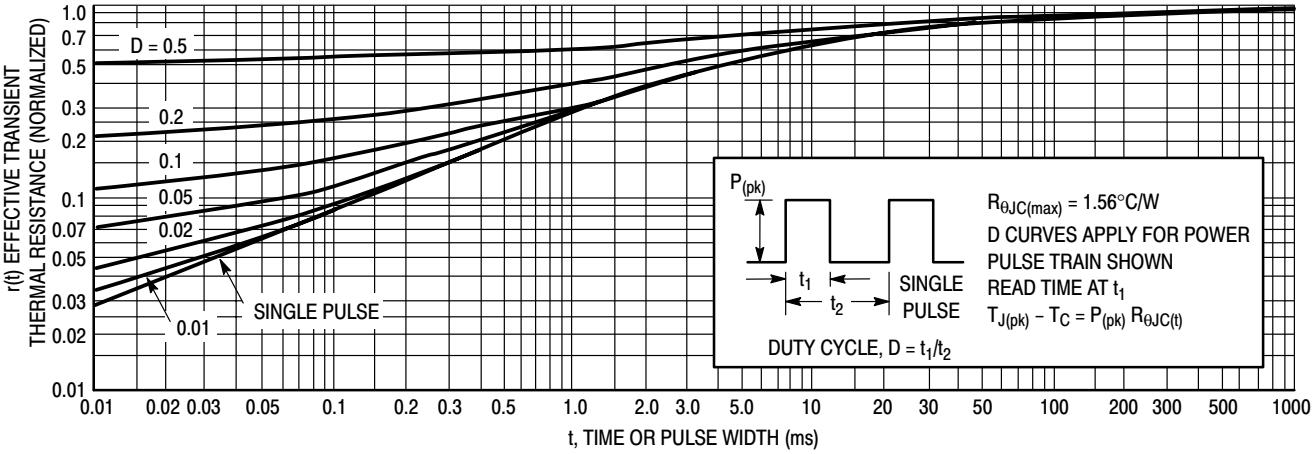


Figure 13. Thermal Response

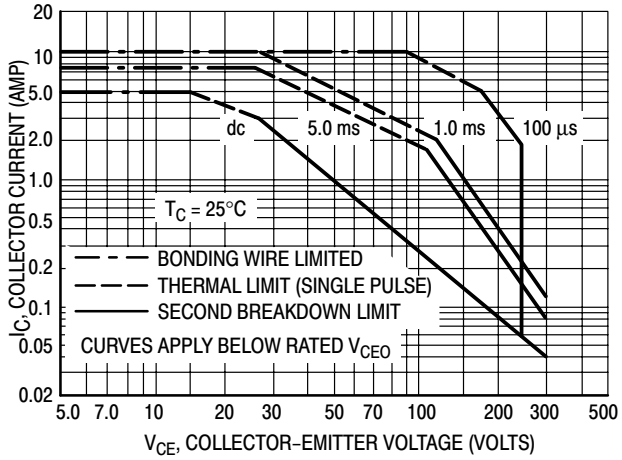


Figure 14. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

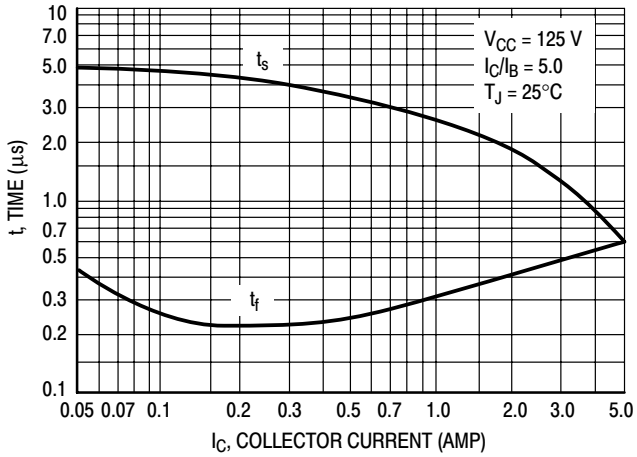


Figure 15. Turn−Off Time

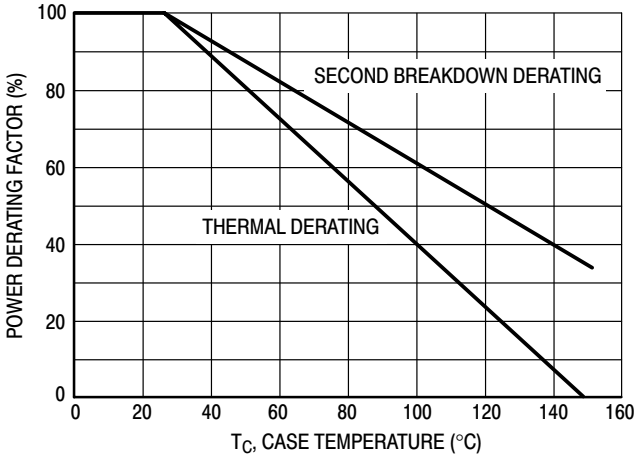


Figure 16. Power Derating

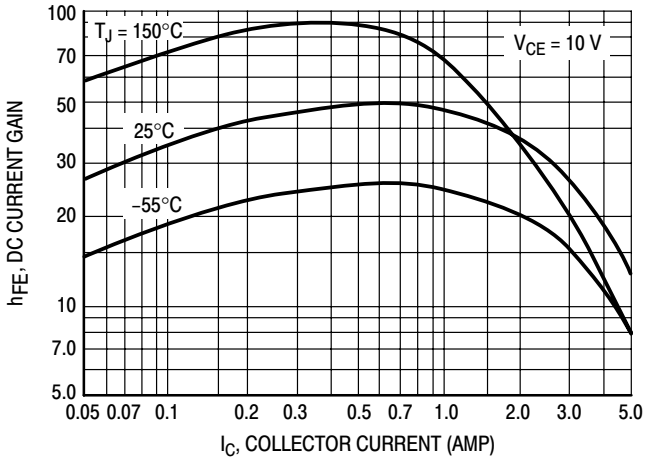


Figure 17. DC Current Gain

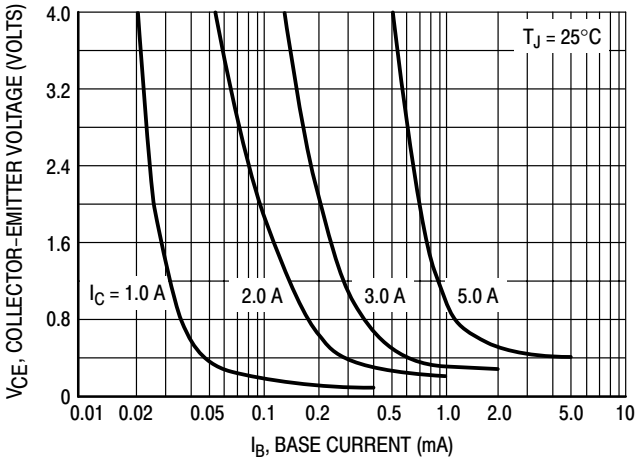


Figure 18. Collector Saturation Region

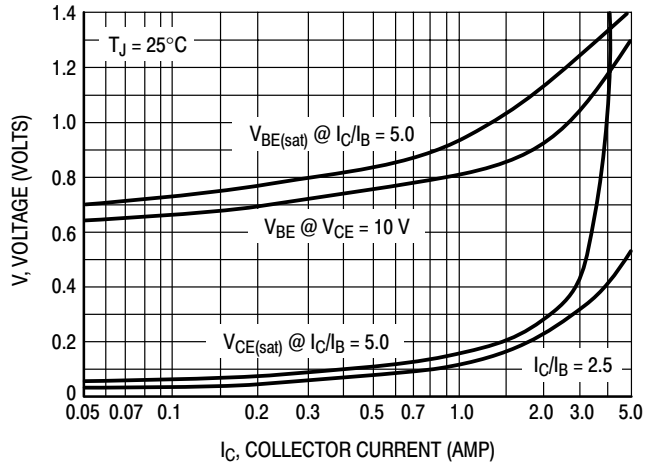


Figure 19. “On” Voltages

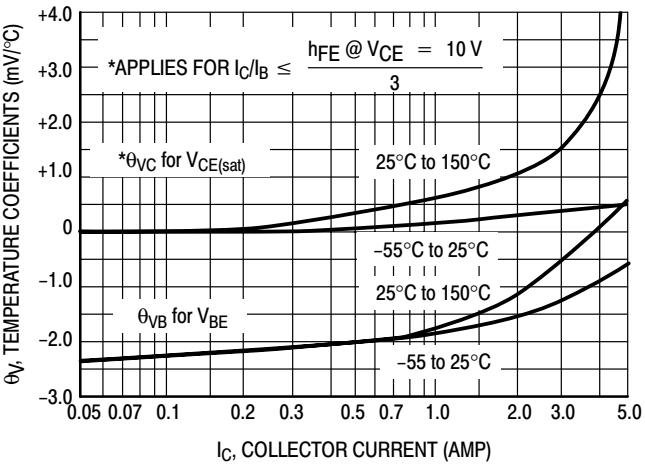


Figure 20. Temperature Coefficients

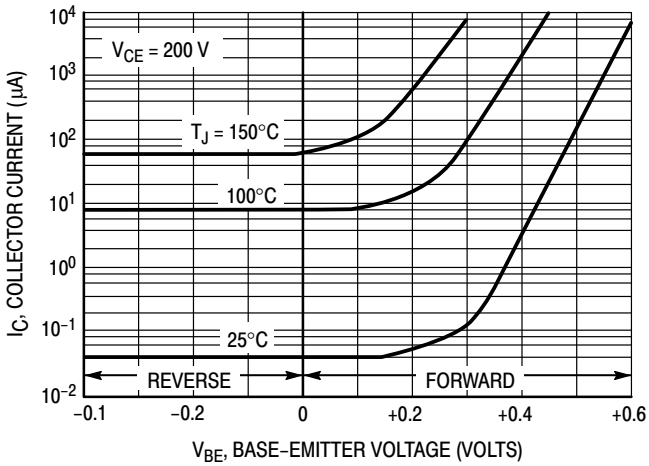


Figure 21. Collector Cutoff Region

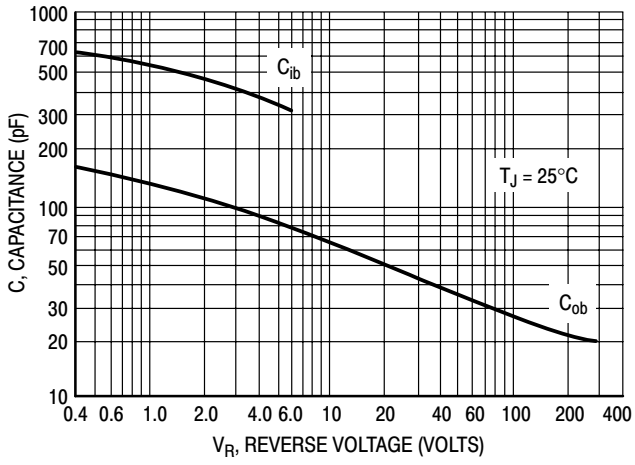


Figure 22. Capacitance

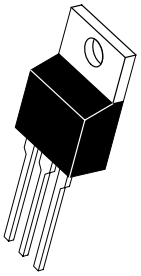
Darlington Silicon Power Transistors

2N6667
2N6668

PNP SILICON
DARLINGTON
POWER TRANSISTORS
10 AMPERES
60–80 VOLTS
65 WATTS

. . . designed for general–purpose amplifier and low speed switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 4 Adc
- Collector–Emitter Sustaining Voltage — @ 200 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6667
  = 80 Vdc (Min) — 2N6668
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2 Vdc (Max)@ I_C = 5 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package
- Complementary to 2N6387, 2N6388



CASE 221A–09
TO–220AB

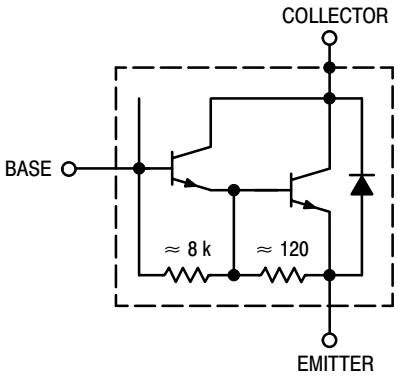


Figure 1. Darlington Schematic

MAXIMUM RATINGS (1)

Rating	Symbol	2N6667	2N6668	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous — Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52		watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

(1) Indicates JEDEC Registered Data.

March, 2001 – Rev. 3
Publication Order Number:
2N6667/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)	2N6667 2N6668	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N6667 2N6668	I_{CEO}	— —	1 1	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6667 2N6668 2N6667 2N6668	I_{CEX}	 — — — —	 300 300 3 3	 μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 3 Vdc) (I_C = 10 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 100	20000 —	—
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	— —	2 3	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	— —	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	200	pF
Small–Signal Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc, f = 1 kHz)		h_{fe}	1000	—	—

*Indicates JEDEC Registered Data

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

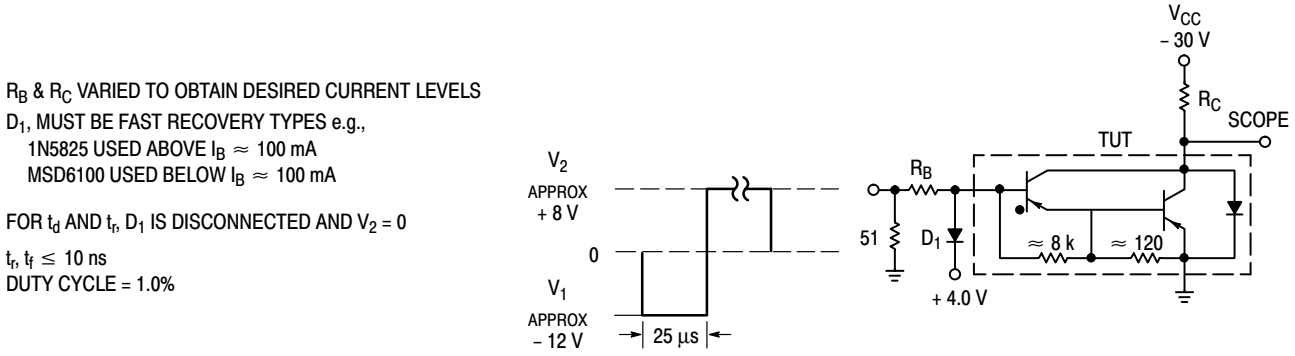


Figure 2. Switching Times Test Circuit

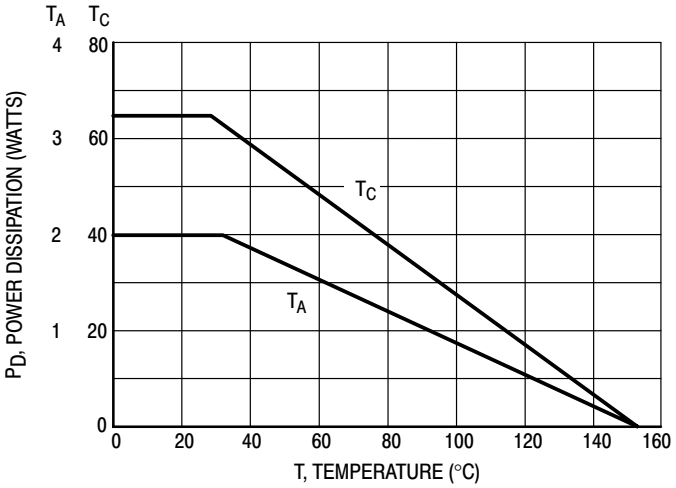


Figure 3. Power Derating

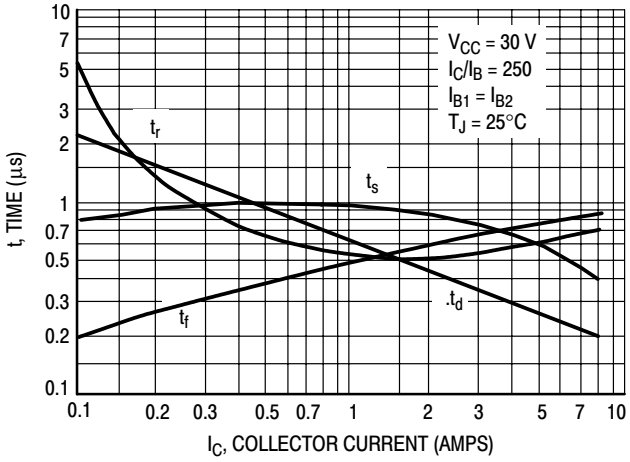


Figure 4. Typical Switching Times

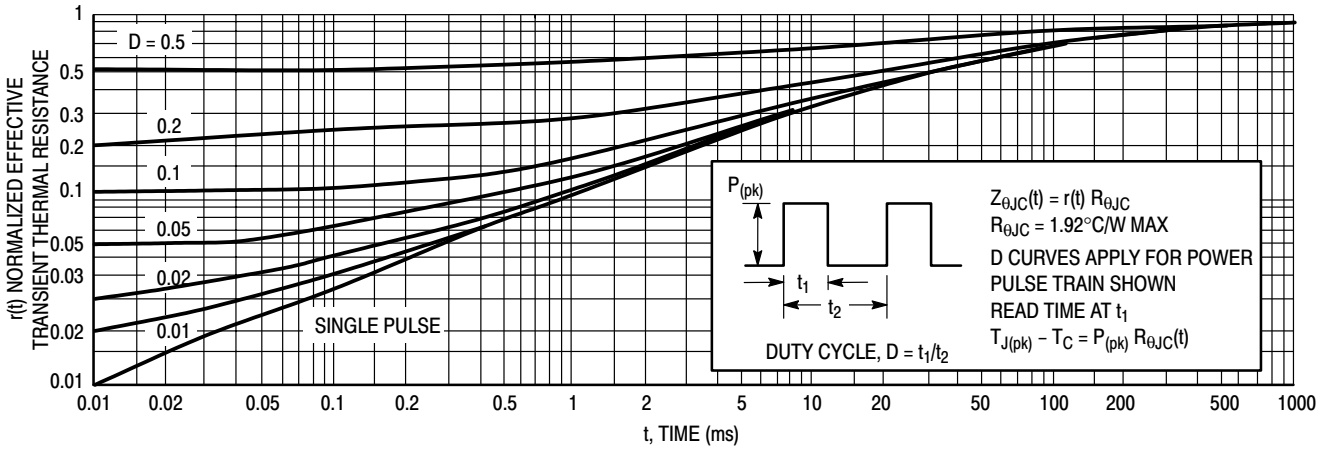


Figure 5. Thermal Response

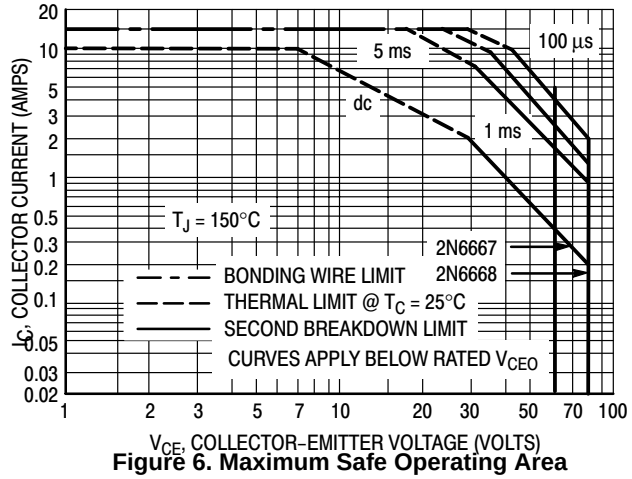


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

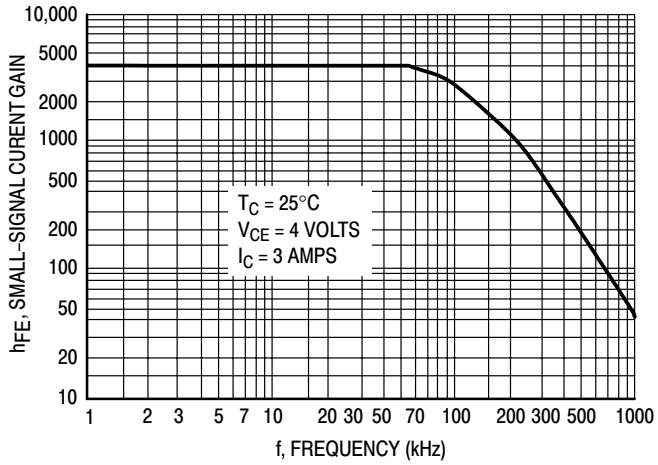


Figure 7. Typical Small−Signal Current Gain

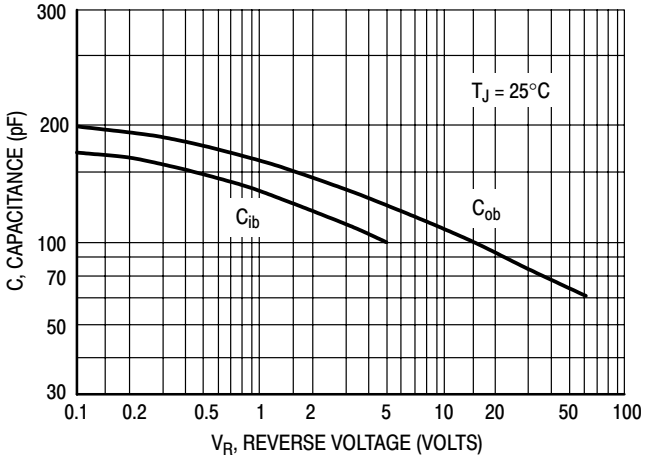


Figure 8. Typical Capacitance

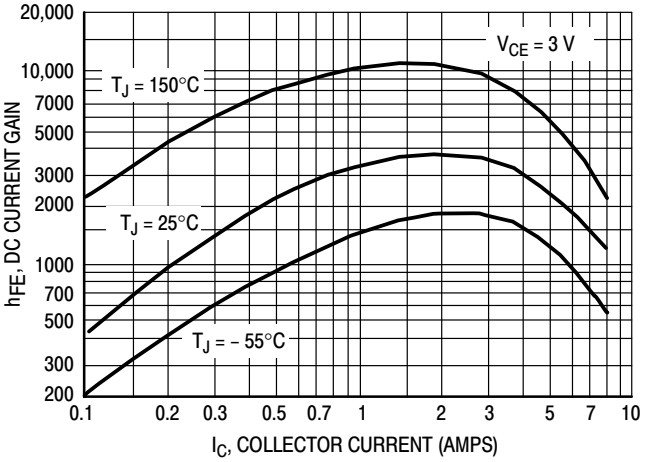


Figure 9. Typical DC Current Gain

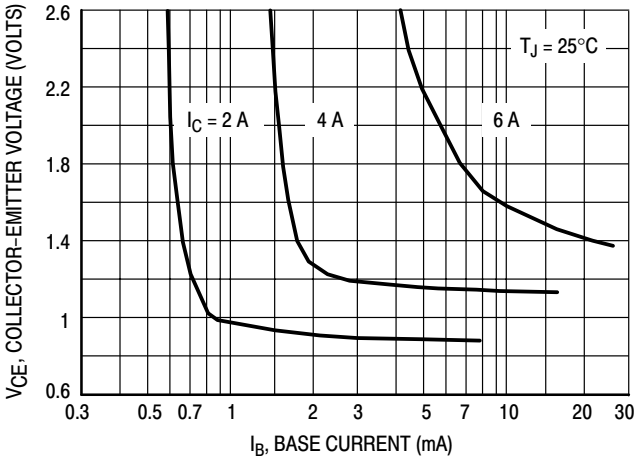


Figure 10. Typical Collector Saturation Region

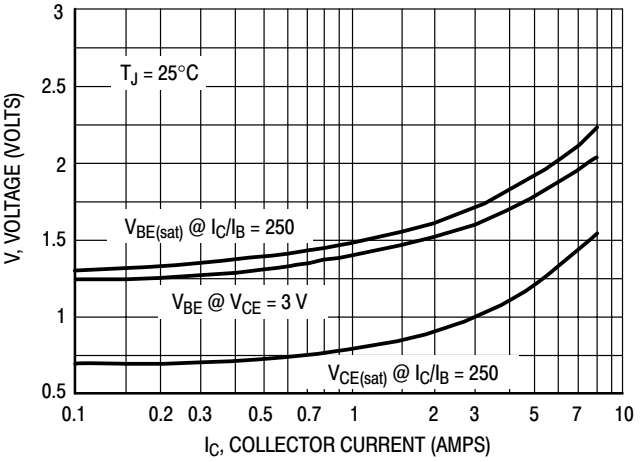


Figure 11. Typical “On” Voltages

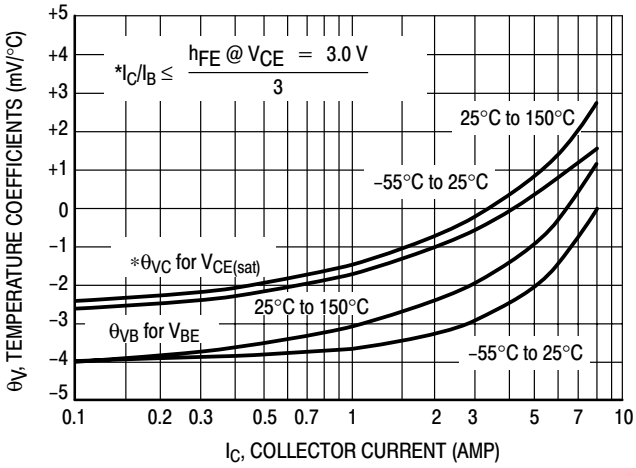


Figure 12. Typical Temperature Coefficients

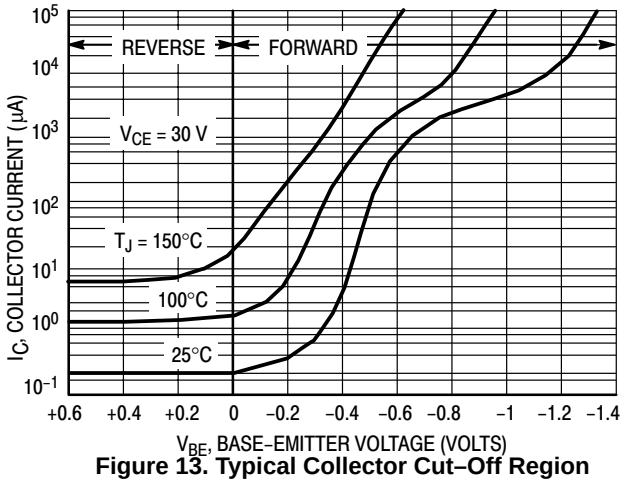


Figure 13. Typical Collector Cut−Off Region

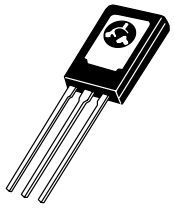
Plastic Medium Power Silicon NPN Transistor

BD135
BD137
BD139

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

1.5 AMPERE
POWER TRANSISTORS
NPN SILICON
45, 60, 80 VOLTS
10 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector–Base Voltage	V_{CBO}	BD 135 BD 137 BD 139	45 60 100	Vdc
Emitter–Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–55 to +150	°C

March, 2001 – Rev. 9
Publication Order Number:
BD135/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	UnIt
Collector–Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}		— —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

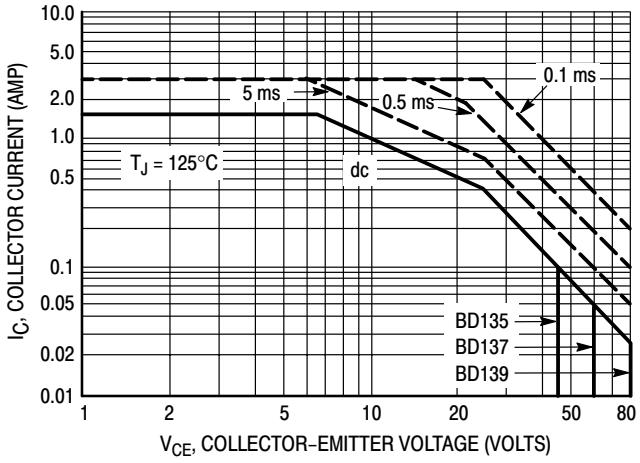


Figure 1. Active–Region Safe Operating Area

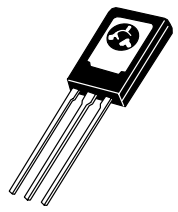
Plastic Medium Power Silicon PNP Transistor

BD136
BD138
BD140
BD140-10

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

1.5 AMPERE
POWER TRANSISTORS
PNP SILICON
45, 60, 80 VOLTS
10 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Collector–Base Voltage	V_{CBO}	BD 136 BD 138 BD 140	45 60 100	Vdc
Emitter–Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation@ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–55 to +150	°C

March, 2001 – Rev. 9
Publication Order Number:
BD136/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)		BV_{CEO}	BD 136 BD 138 BD 140	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125 °C)		I_{CBO}		— —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	 ALL ALL BD140–10	h_{FE}*		 25 40 63 25	 — 250 160 —	—
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)		$V_{CE(sat)}$*		—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$*		—	1	Vdc

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

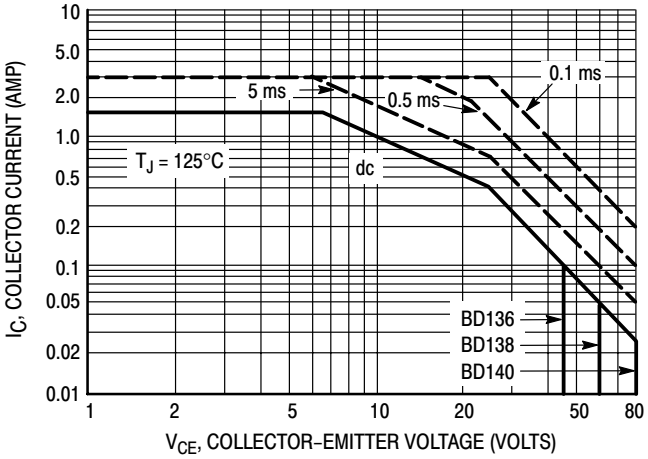


Figure 1. Active–Region Safe Operating Area

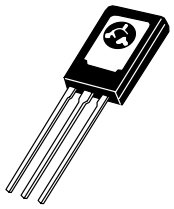
Plastic Medium Power NPN Silicon Transistor

BD159

. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line–Operated Equipment
- Thermopad™ Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
20 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V_{CEO}	350	Vdc
Collector–Base Voltage	V_{CB}	375	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	0.5 1.0	Adc
Base Current	I_B	0.25	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	350	—	Vdc
Collector Cutoff Current (At rated voltage)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

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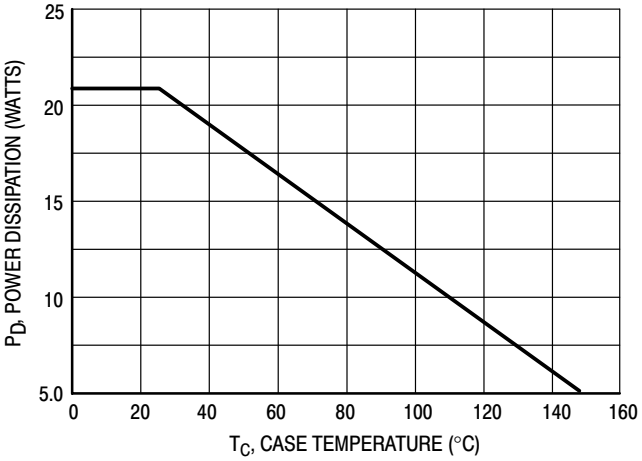


Figure 2. Power–Temperature Derating Curve

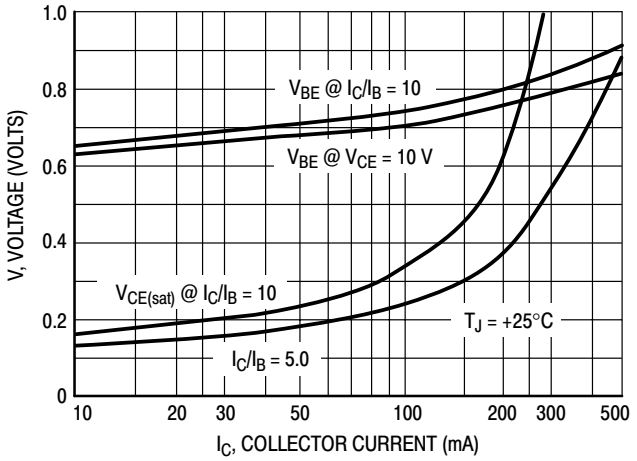


Figure 3. "On" Voltages

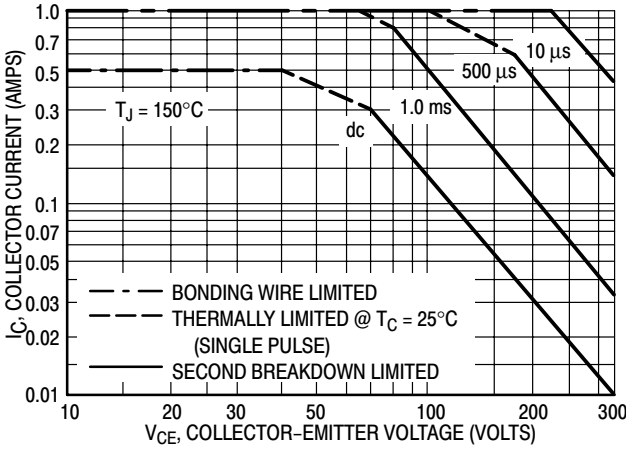


Figure 4. DC Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below, the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

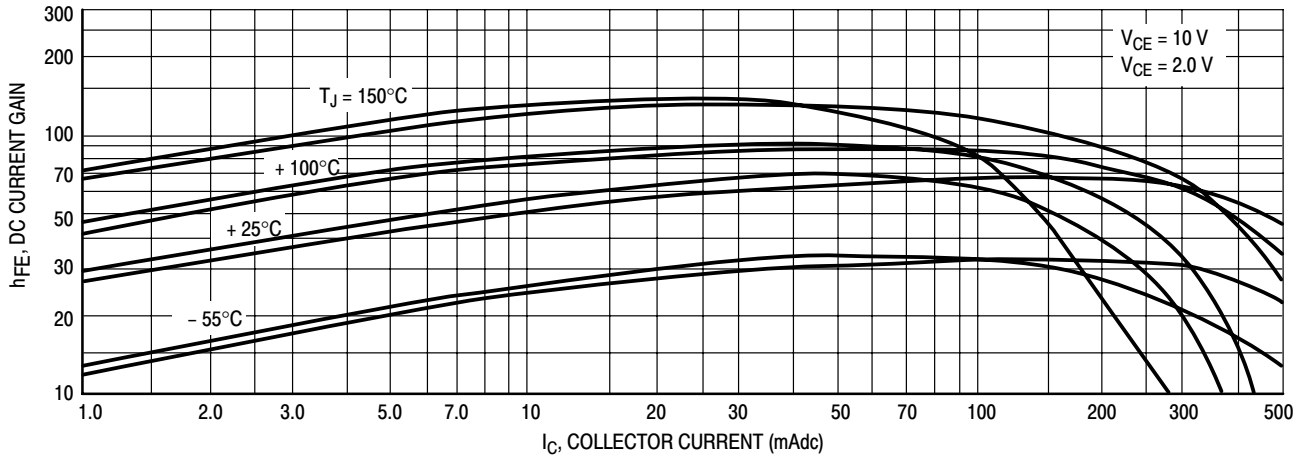


Figure 5. Current Gain

Plastic Medium Power Silicon NPN Transistor

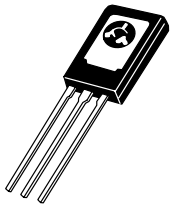
BD179
BD179-10

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD179 is complementary with BD180

3.0 AMPERES
POWER TRANSISTORS
NPN SILICON
80 VOLTS
30 WATTS

*ON Semiconductor Preferred Device



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 240	Watts mw/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) BD179–10 (I_C = 1.0 A, V_{CE} = 2.0 V) ALL	h_{FE}	 63 15	 160 —	
Collector–Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain – Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

*Pulse Test: Pulse Width ≦ 300 As, Duty Cycle ≦ 2.0%.

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Publication Order Number:
BD179/D

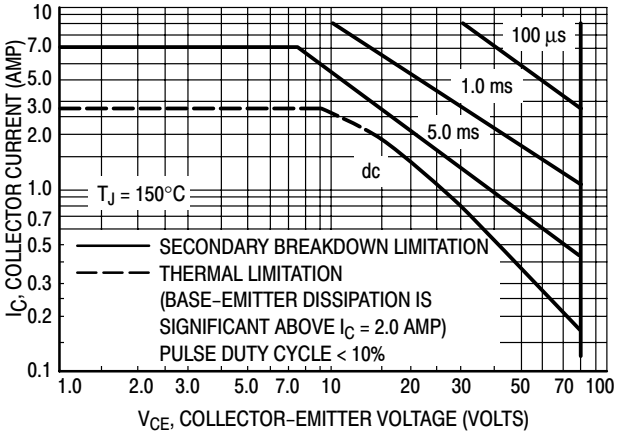


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

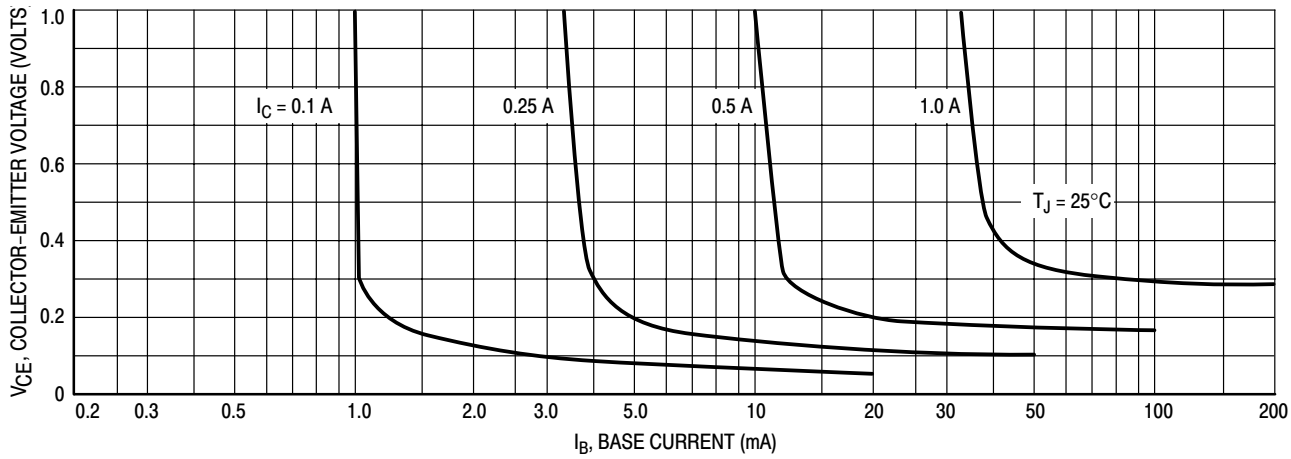


Figure 2. Collector Saturation Region

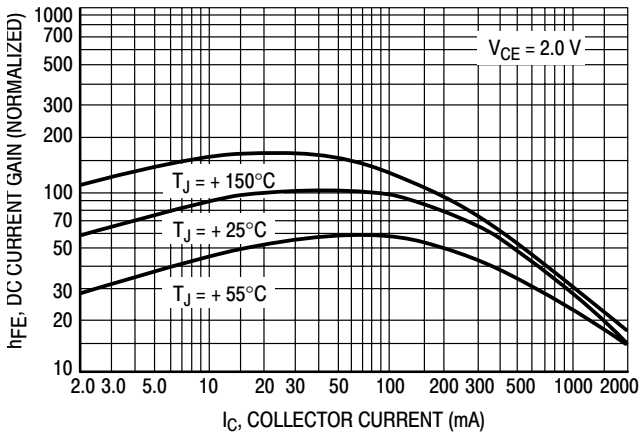


Figure 3. Current Gain

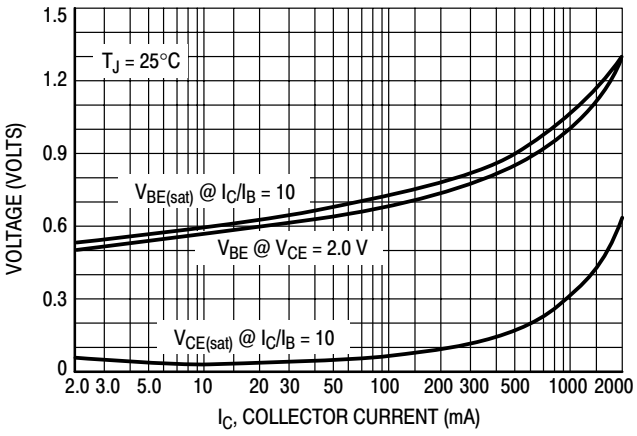


Figure 4. “On” Voltages

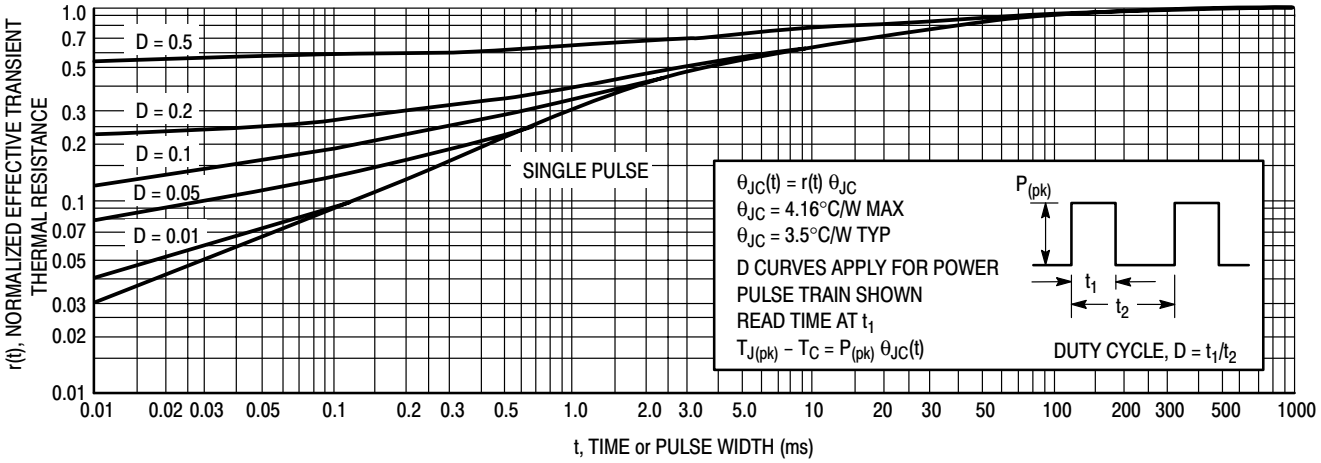


Figure 5. Thermal Response

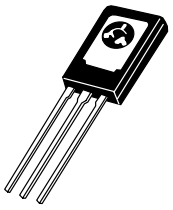
BD180

Plastic Medium Power Silicon PNP Transistor

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD180 is complementary with BD179

3.0 AMPERES
POWER TRANSISTOR
PNP SILICON
80 VOLTS
30 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) BD180	I_{CBO}	 — —	 — 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V)	h_{FE}	 40 15	 250 —	—
Collector–Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

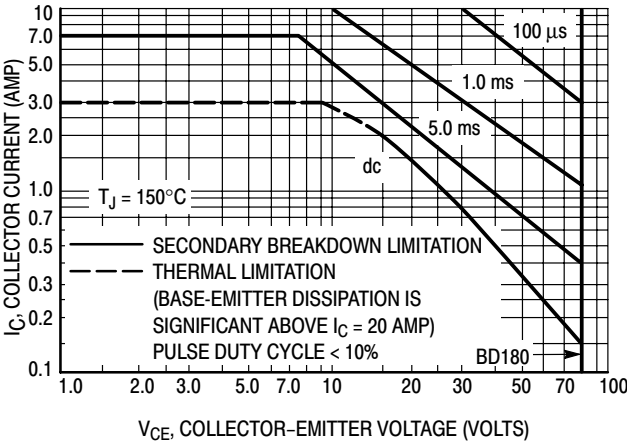


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

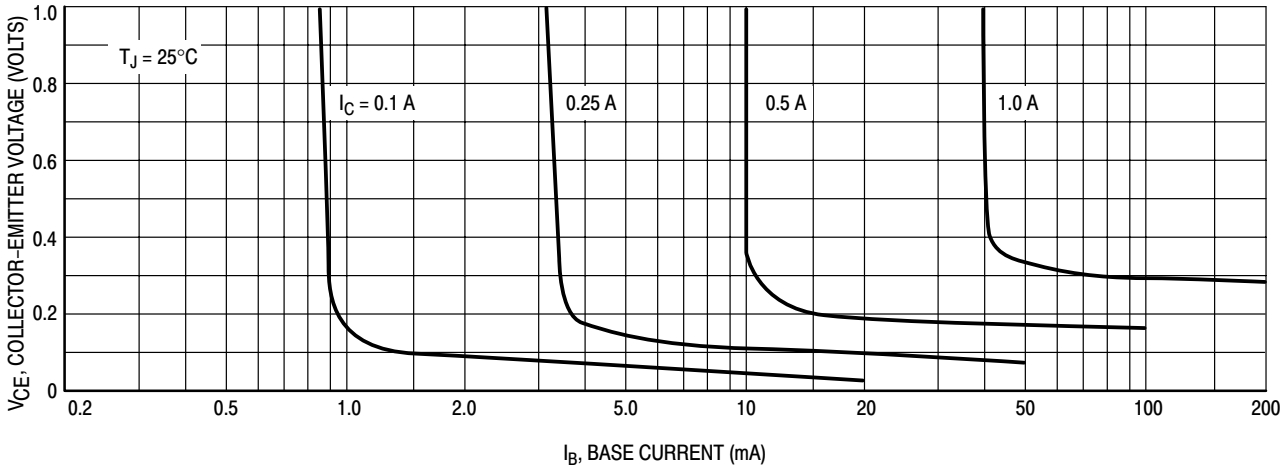


Figure 2. Collector Saturation Region

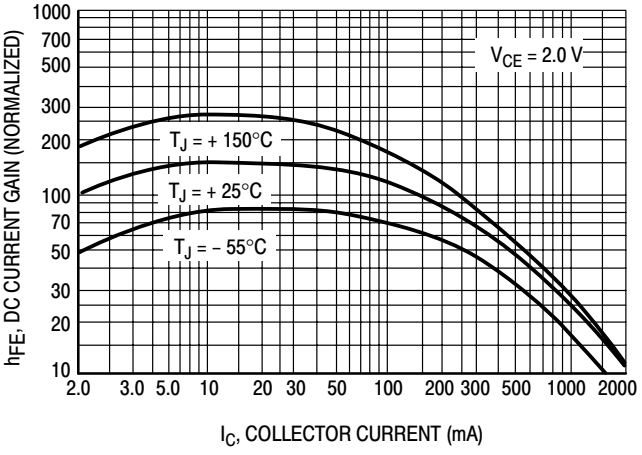


Figure 3. Current Gain

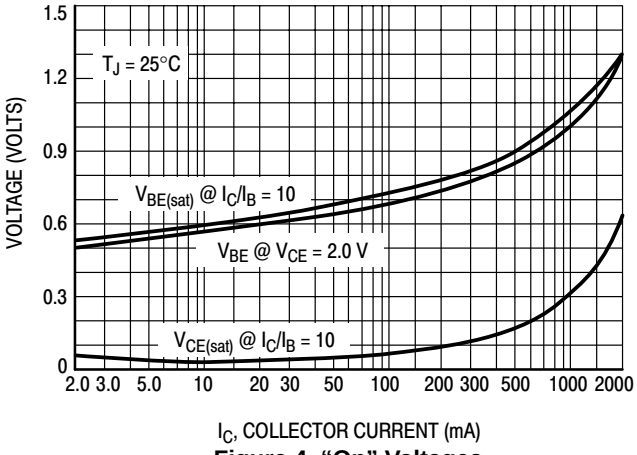


Figure 4. "On" Voltages

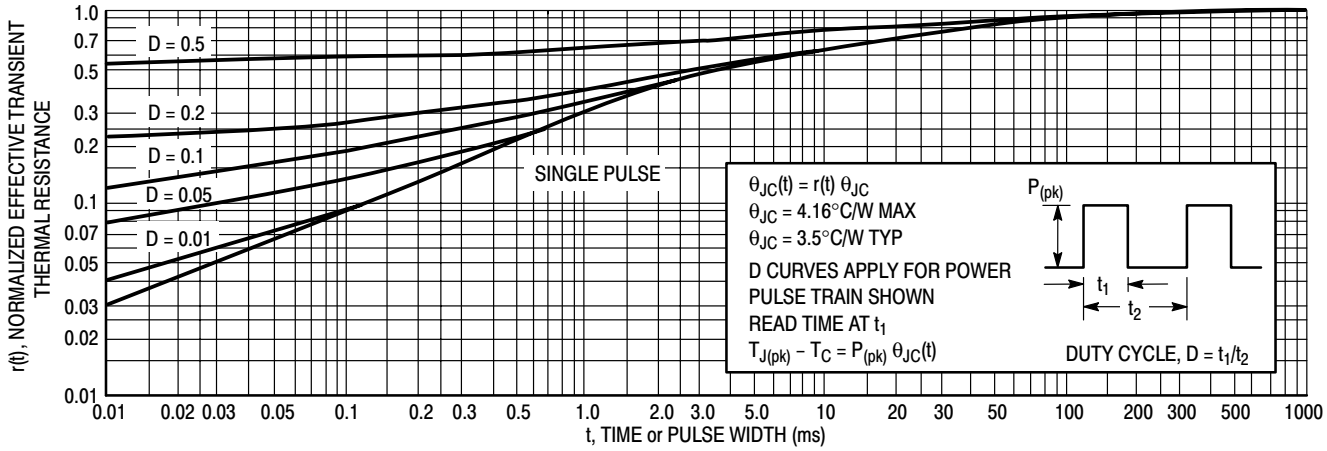


Figure 5. Thermal Response

Plastic Medium Power Silicon NPN Transistor

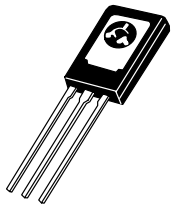
NPN
BD237
PNP
BD238

*ON Semiconductor Preferred Device

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 0.15 Adc

2.0 AMPERES
POWER TRANSISTORS
NPN SILICON
80 VOLTS
25 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	100	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	2.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V)	 h_{FE1} h_{FE2}	 40 25	 — —	
Collector–Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

April, 2001 – Rev. 10
Publication Order Number:
BD237/D

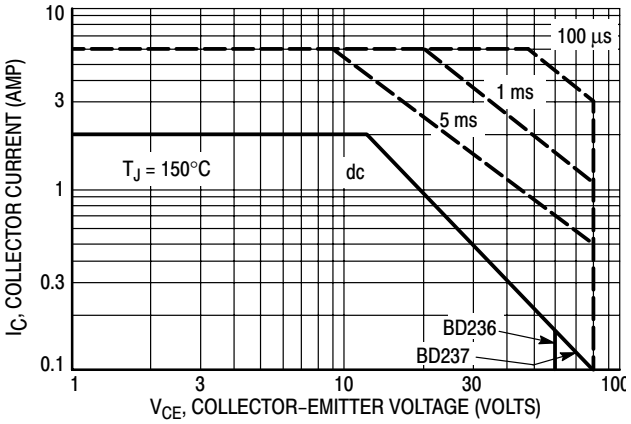


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

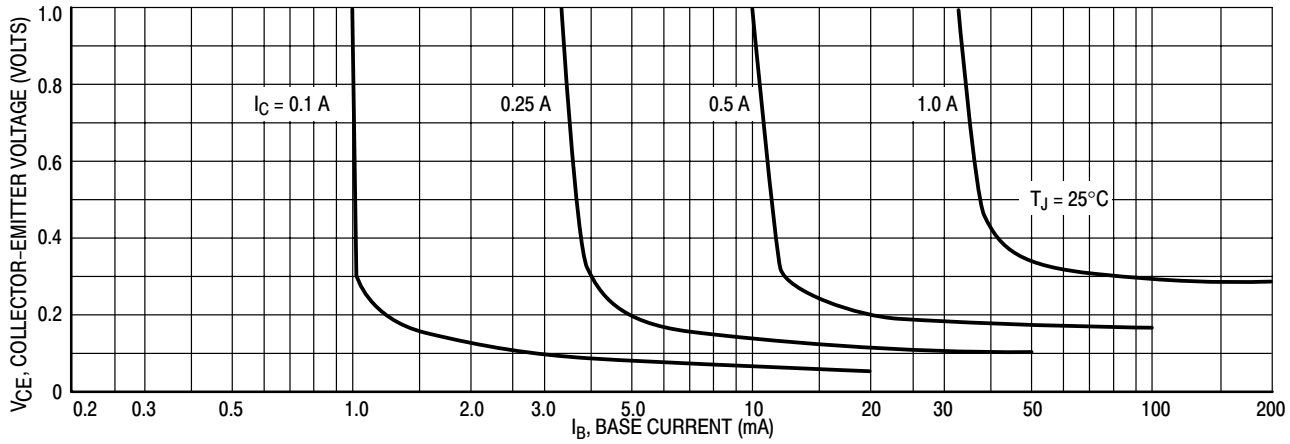


Figure 2. Collector Saturation Region

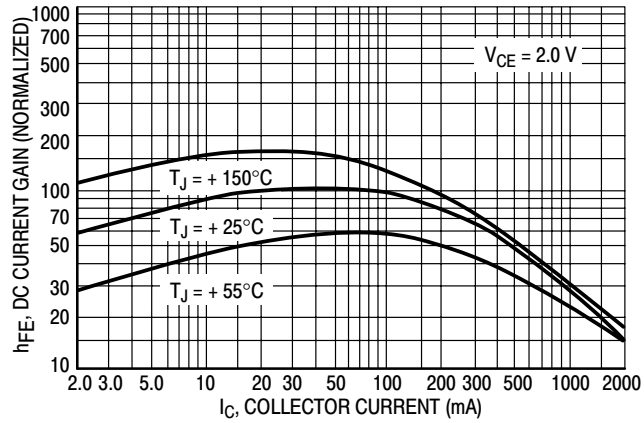


Figure 3. Current Gain

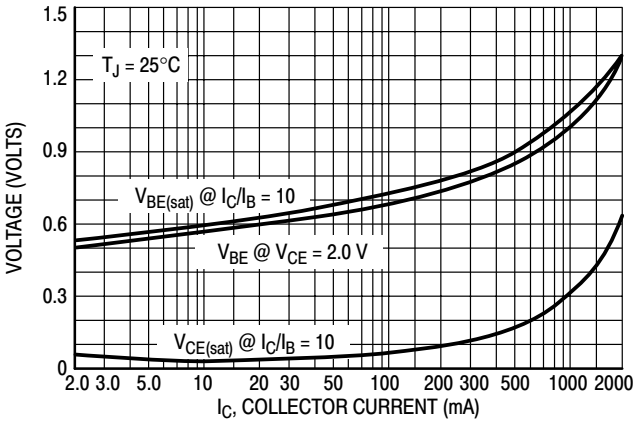


Figure 4. “On” Voltages

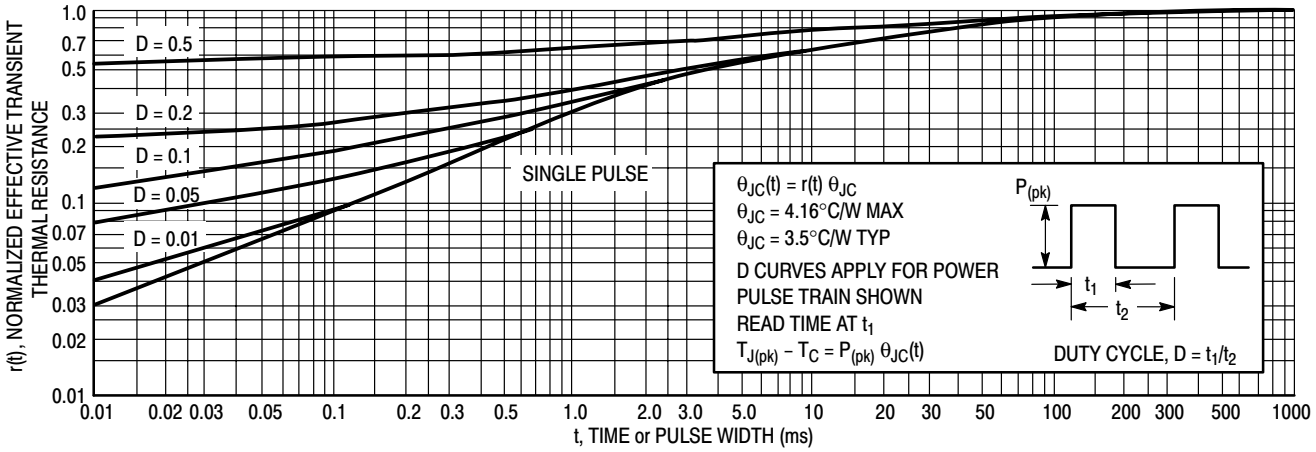


Figure 5. Thermal Response

Complementary Silicon Plastic Power Transistors

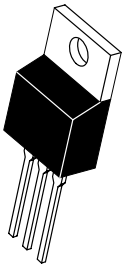
. . . designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
  V_{CE} = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min.) BD241C, BD242C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
BD241C*
PNP
BD242C*

***ON Semiconductor Preferred Device**

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80, 100 VOLTS
40 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BD241C BD242C	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Emitter Voltage	V_{CES}	115	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	3.0 5.0	Adc Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

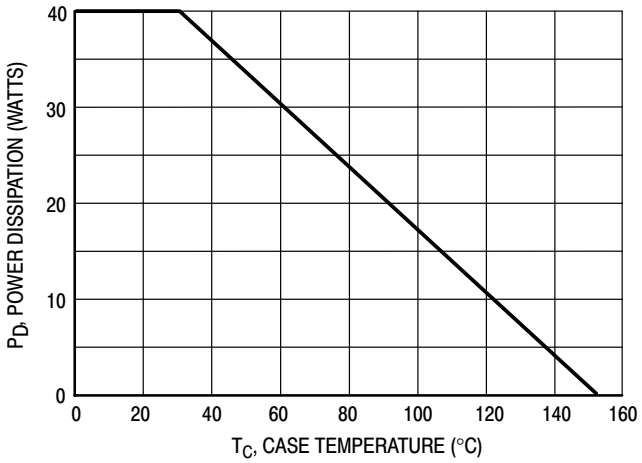


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage[1] (I_C = 30 mAdc, I_B = 0) BD241C, BD242C	V_{CEO}	100		Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) BD241C, BD242C	I_{CEO}		0.3	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0) BD241C, BD242C	I_{CES}		200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 10		
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 600 Adc)	$V_{CE(sat)}$		1.2	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product[2] (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3.0		MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	20		

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

[2] $f_T = |h_{fe}| \bullet f_{test}$.

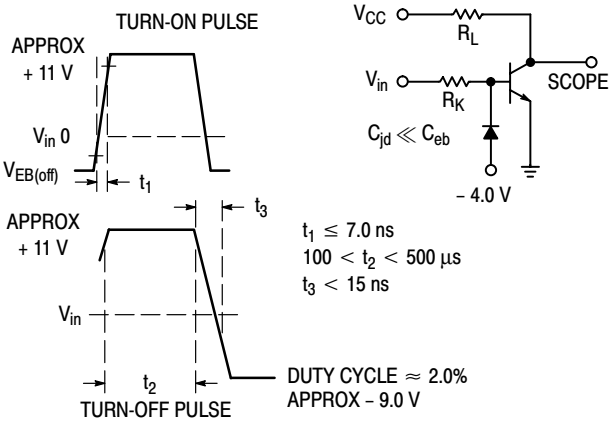


Figure 2. Switching Time Equivalent Circuit

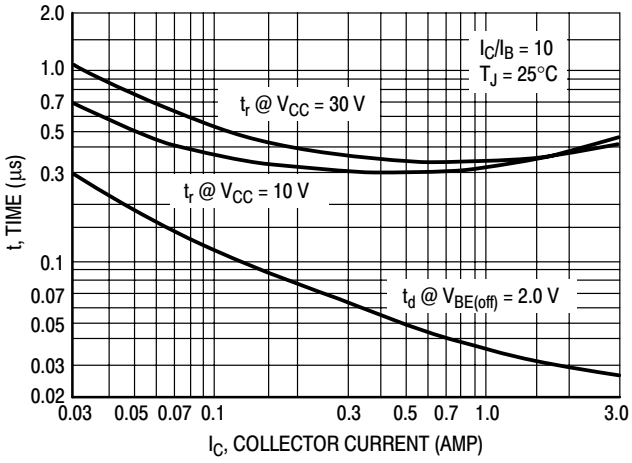


Figure 3. Turn–On Time

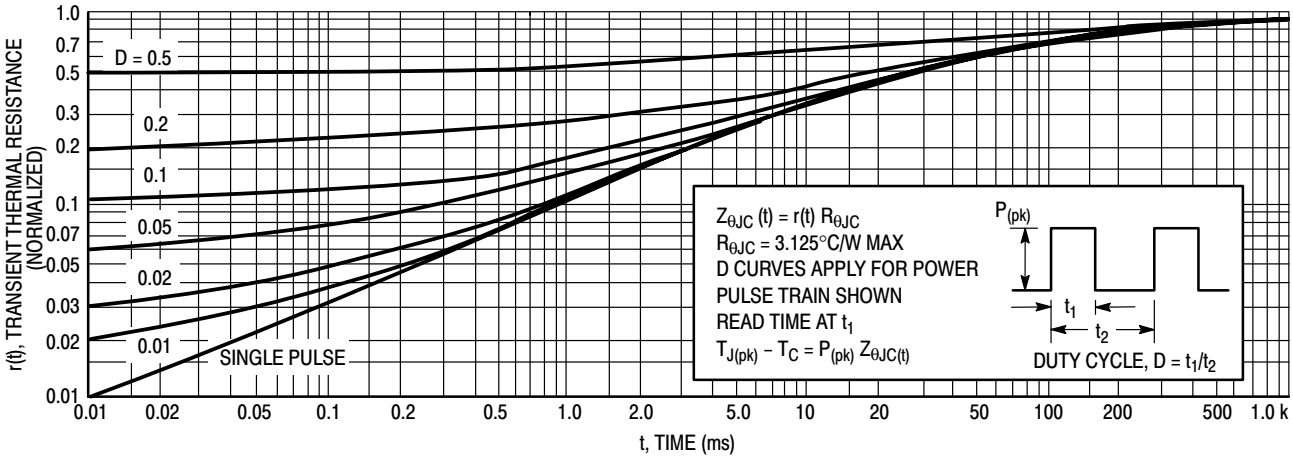


Figure 4. Thermal Response

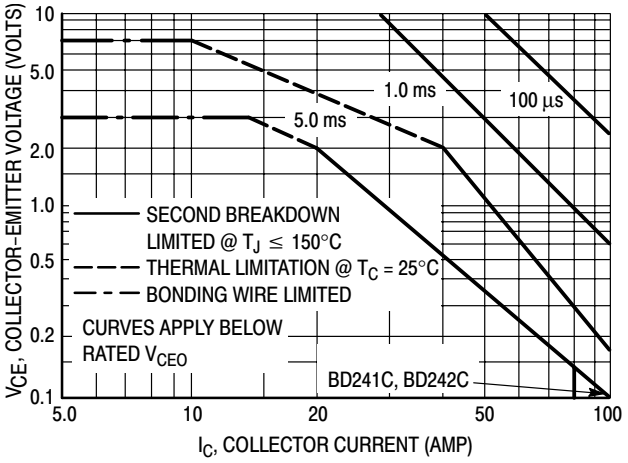


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

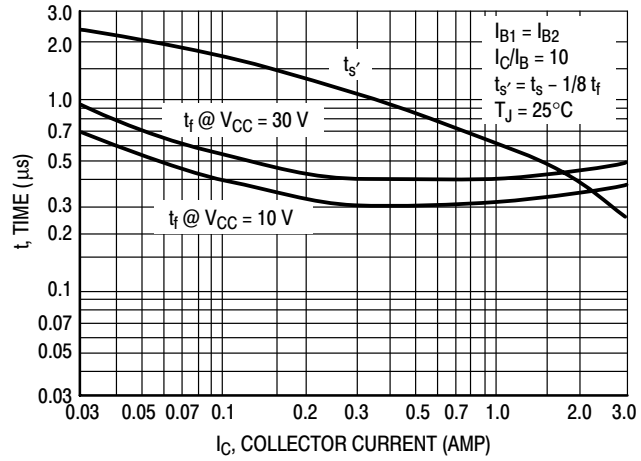


Figure 6. Turn–Off Time

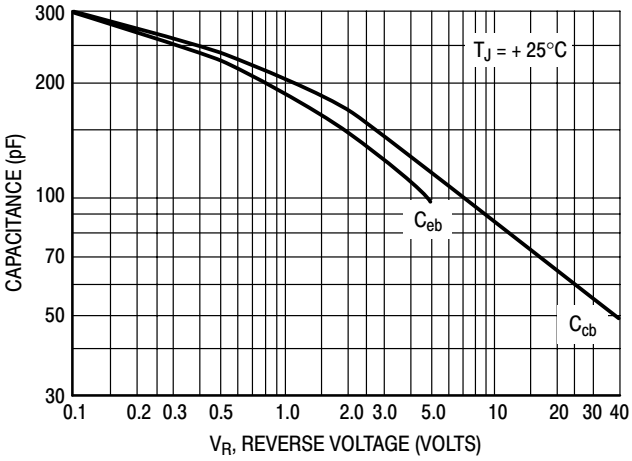


Figure 7. Capacitance

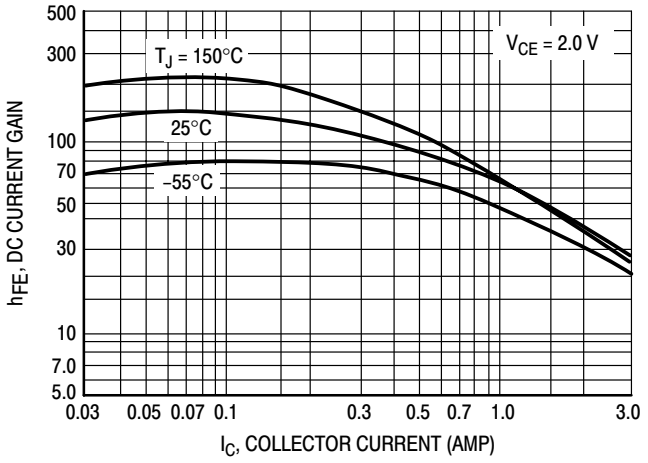


Figure 8. DC Current Gain

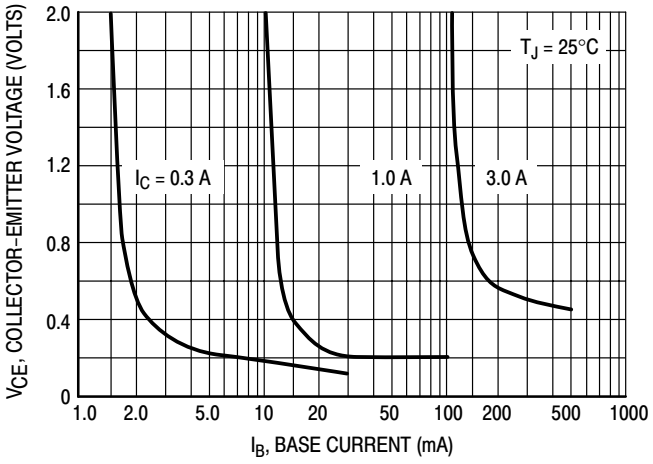


Figure 9. Collector Saturation Region

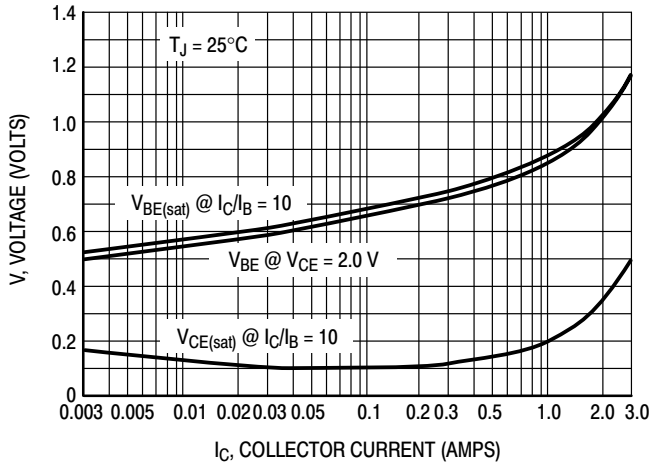


Figure 10. “On” Voltages

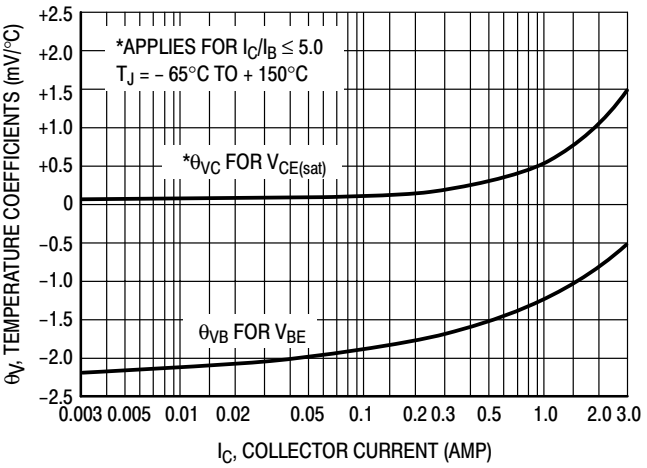


Figure 11. Temperature Coefficients

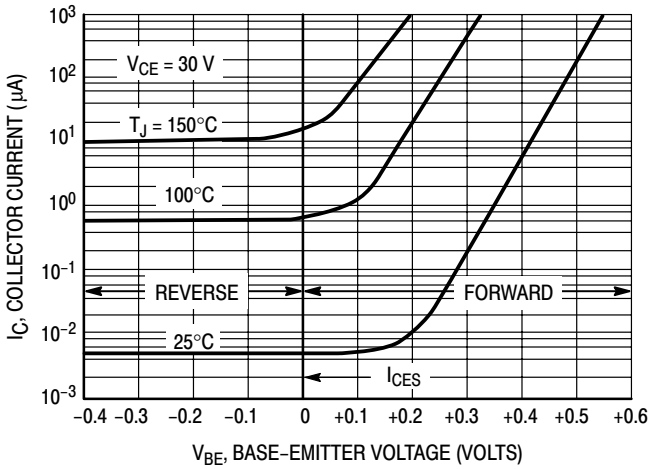


Figure 12. Collector Cut−Off Region

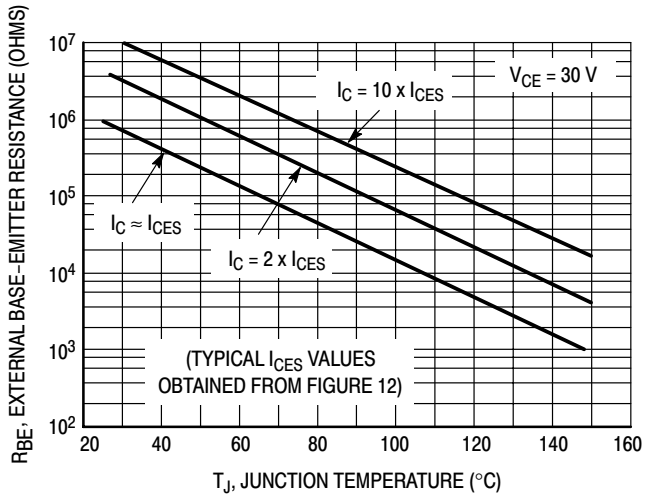


Figure 13. Effects of Base−Emitter Resistance

Complementary Silicon Plastic Power Transistors

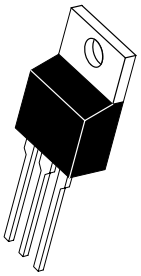
. . . designed for use in general purpose amplifier and switching applications.

- Collector – Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BD243B, BD244B
  = 100 Vdc (Min) — BD243C, BD244C
- High Current Gain Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
BD243B
BD243C*
PNP
BD244B
BD244C*

*ON Semiconductor Preferred Device

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80–100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BD243B BD244B	BD243C BD244C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	6 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

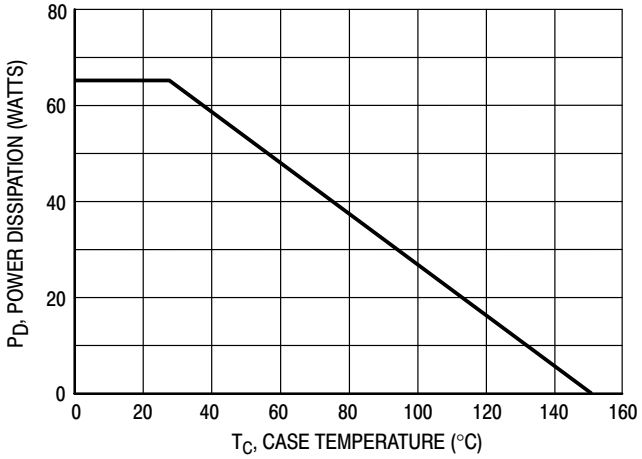


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD243B, BD244B BD243C, BD244C	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	BD243B, BD243C, BD244B, BD244C	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	 BD243B, BD244B BD243C, BD244C	I_{CES}	 — —	 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 30 15	 — —	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = h_{fe} \bullet f_{test}$

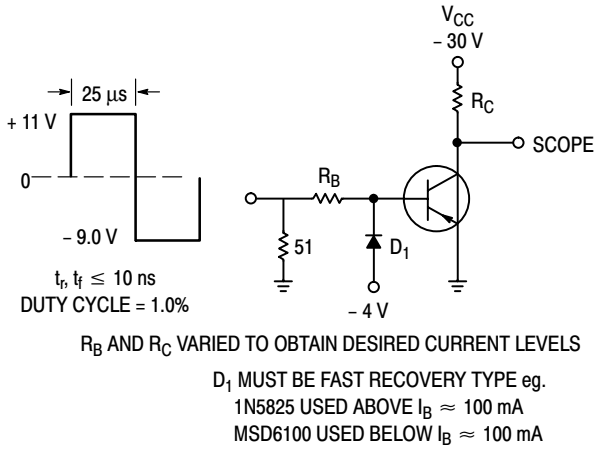


Figure 2. Switching Time Test Circuit

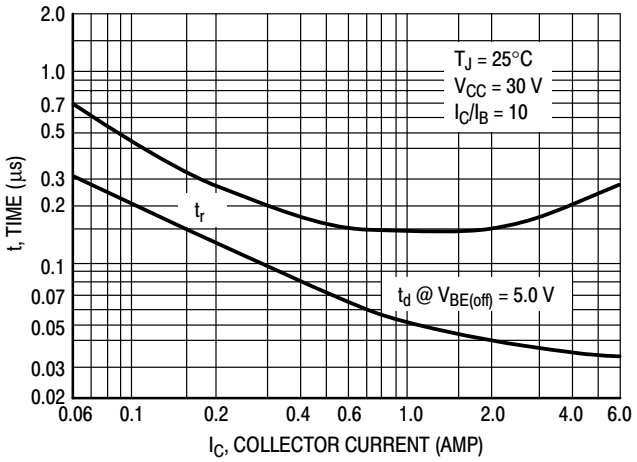


Figure 3. Turn–On Time

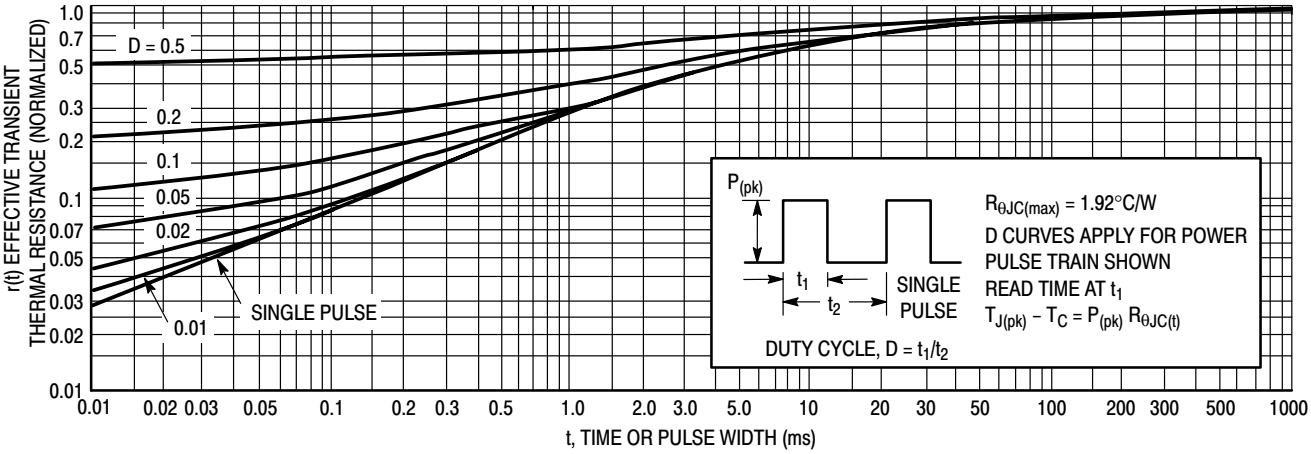


Figure 4. Thermal Response

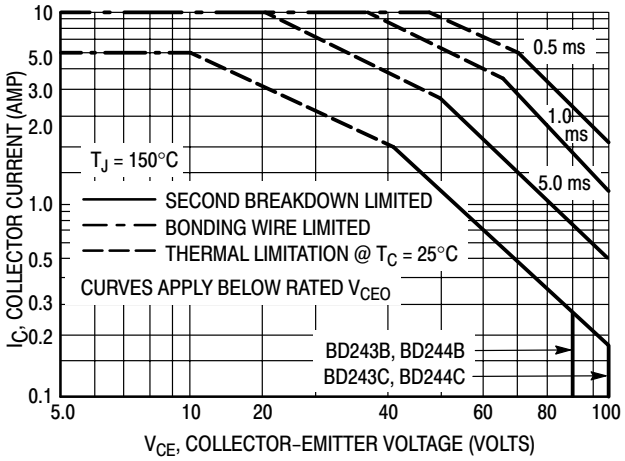


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

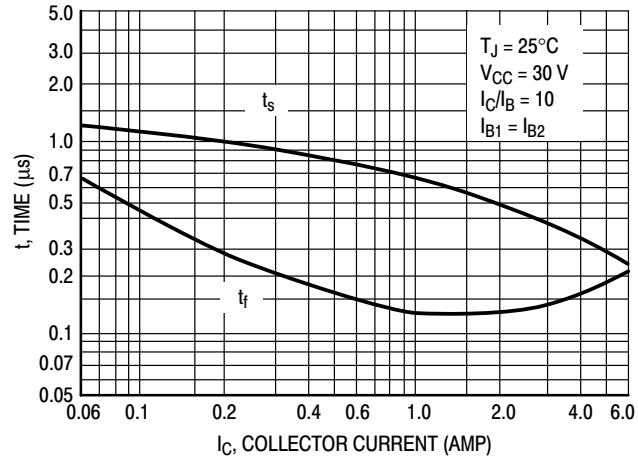


Figure 6. Turn-Off Time

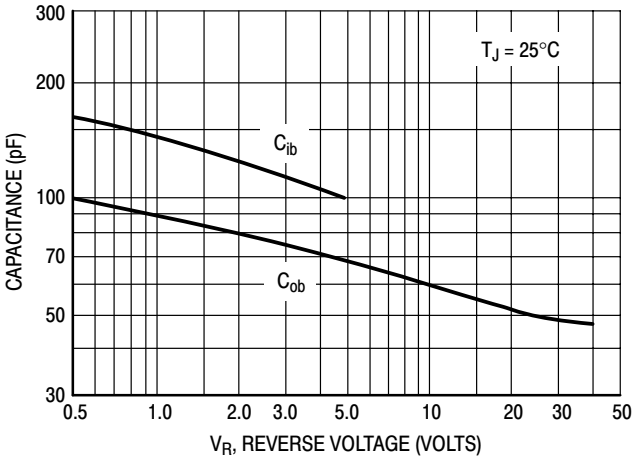


Figure 7. Capacitance

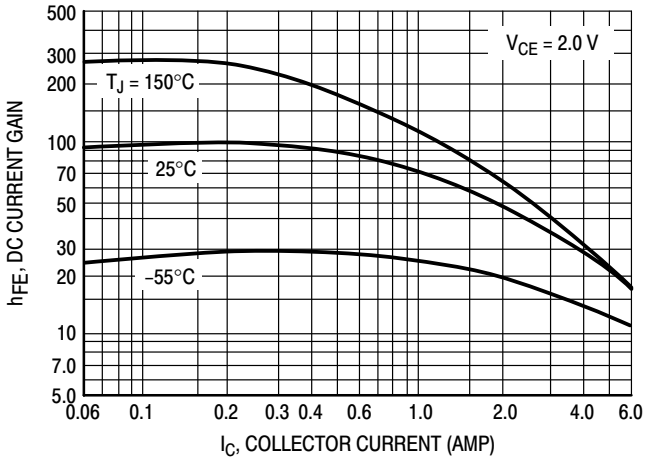


Figure 8. DC Current Gain

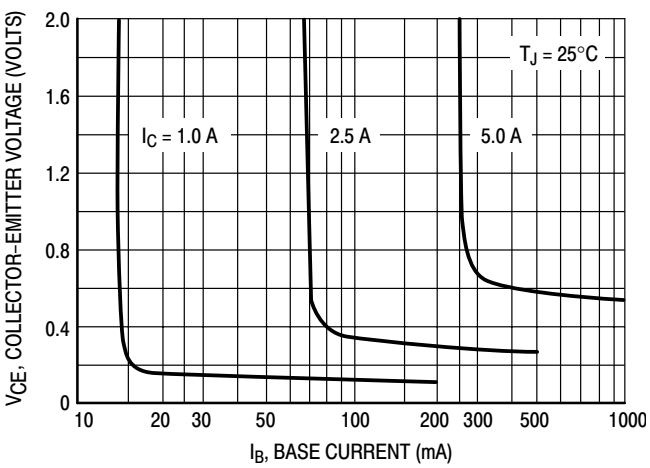


Figure 9. Collector Saturation Region

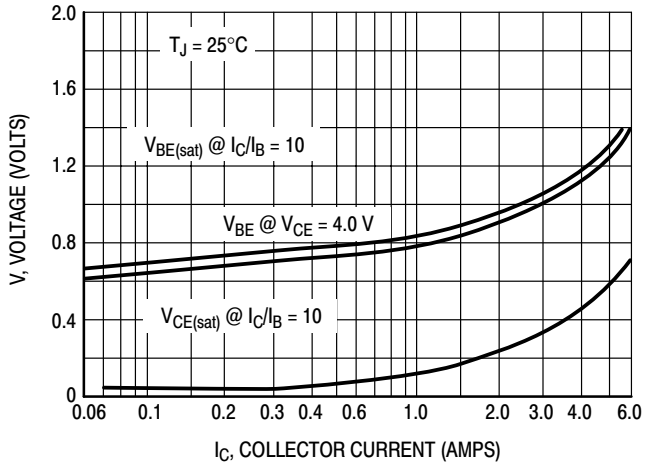


Figure 10. “On” Voltages

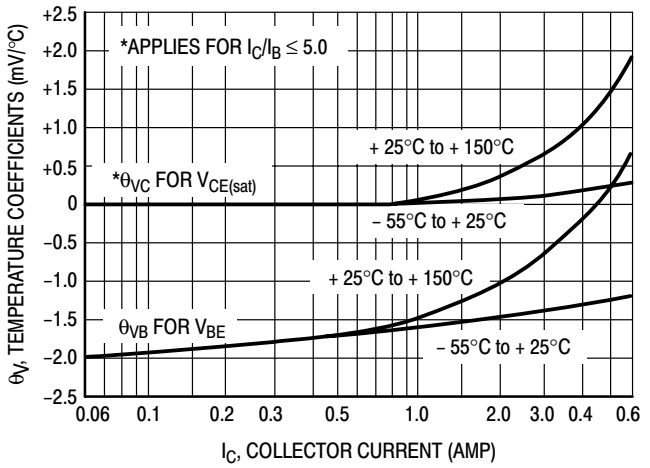


Figure 11. Temperature Coefficients

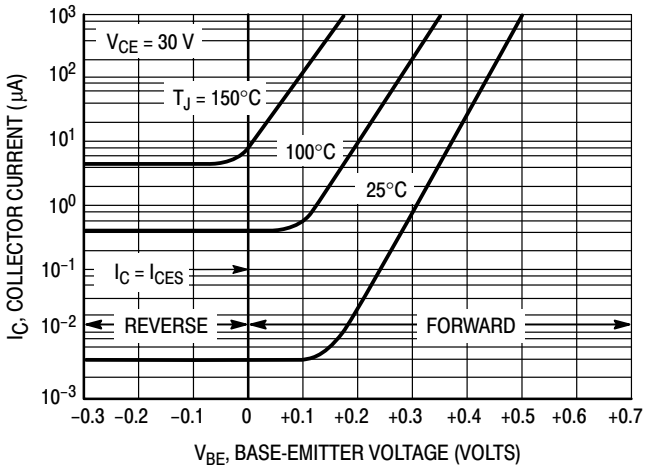


Figure 12. Collector Cut-Off Region

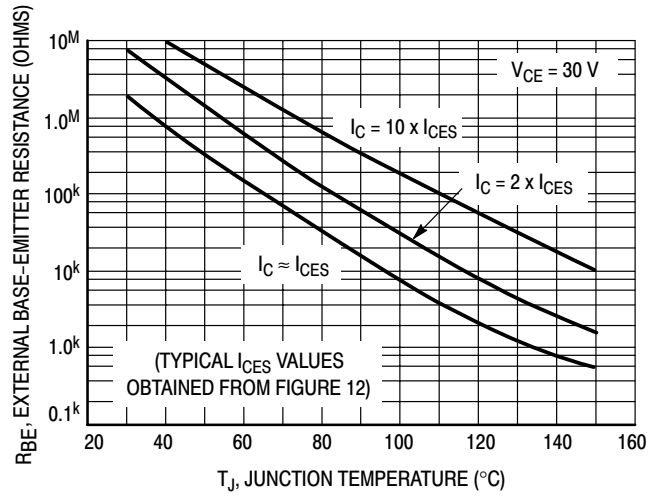


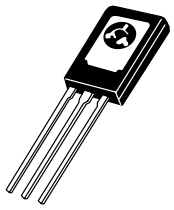
Figure 13. Effects of Base−Emitter Resistance

Plastic Medium Power Silicon NPN Transistor

BD437
BD439
BD441

. . . for amplifier and switching applications. Complementary types are BD438 and BD442.

4.0 AMPERES
POWER TRANSISTORS
NPN SILICON



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage	BD437 BD439 BD441	V_{CEO}	45 60 80	Vdc
Collector–Base Voltage	BD437 BD439 BD441	V_{CBO}	45 60 80	Vdc
Emitter–Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	36 288	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

May, 2001 – Rev. 10
Publication Order Number:
BD437/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector–Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD437 BD439 BD441	$V_{(BR)CEO}$	 45 60 80	 – – –	 – – –	Vdc
Collector–Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD437 BD439 BD441	$V_{(BR)CBO}$	 45 60 80	 – –	 – –	Vdc
Emitter–Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		$V_{(BR)EBO}$	5.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 45 V, I_E = 0) (V_{CB} = 60 V, I_E = 0) (V_{CB} = 80 V, I_E = 0)	 BD437 BD439 BD441	I_{CBO}	 – – –	 – – –	 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 V)		I_{EBO}	–	–	1.0	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5.0 V)	BD437 BD439 BD441	h_{FE}	 30 20 15	 – – –	 – – –	
DC Current Gain (I_C = 500 mA, V_{CE} = 1.0 V)	BD437 BD439, BD441	h_{FE}	 85 40	 – –	 375 475	
DC Current Gain (I_C = 2.0 A, V_{CE} = 1.0 V)	BD437 BD439 BD441	h_{FE}	 40 25 15	 – – –	 – – –	
Collector Saturation Voltage (I_C = 3.0 A, I_B = 0.3 A)	BD437, BD439, BD441	$V_{CE(sat)}$	 –	 –	 0.8	Vdc
Base–Emitter On Voltage (I_C = 2.0 A, V_{CE} = 1.0 V)		$V_{BE(on)}$	–	–	1.1	Vdc
Current–Gain – Bandwidth Product (V_{CE} = 1.0 V, I_C = 250 mA, f = 1.0 MHz)		f_T	3.0	–	–	MHz

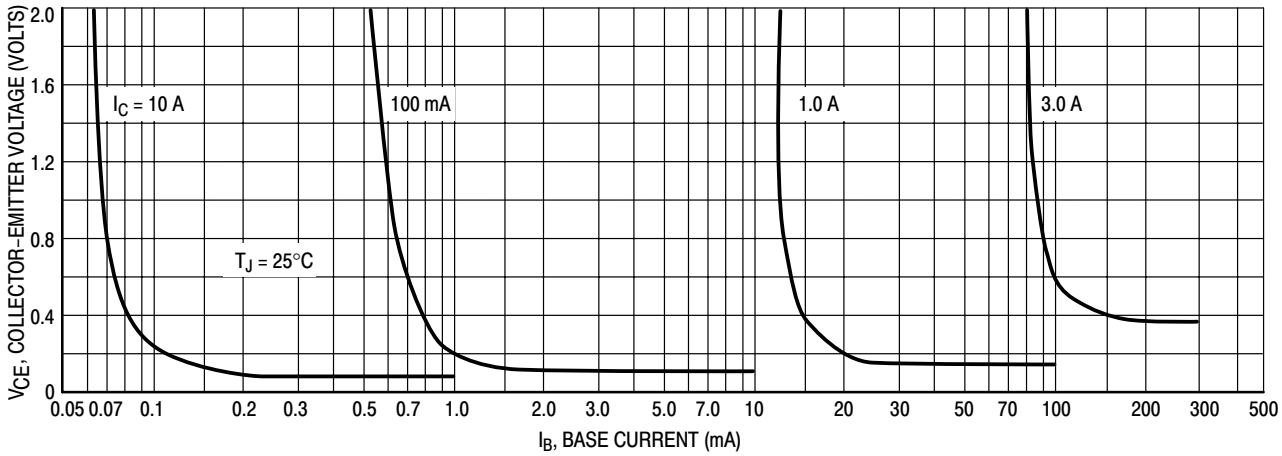


Figure 1. Collector Saturation Region

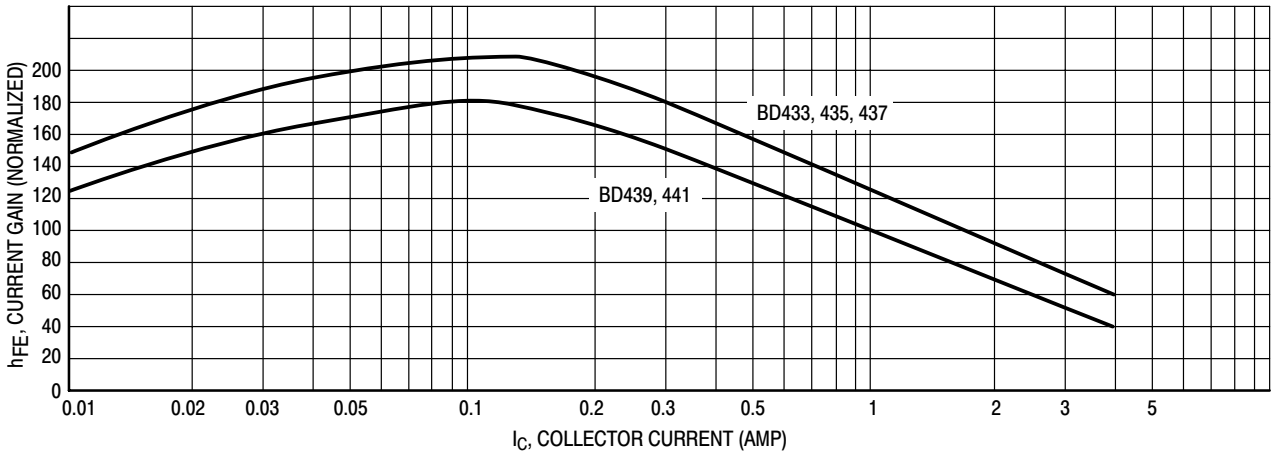


Figure 2. Current Gain

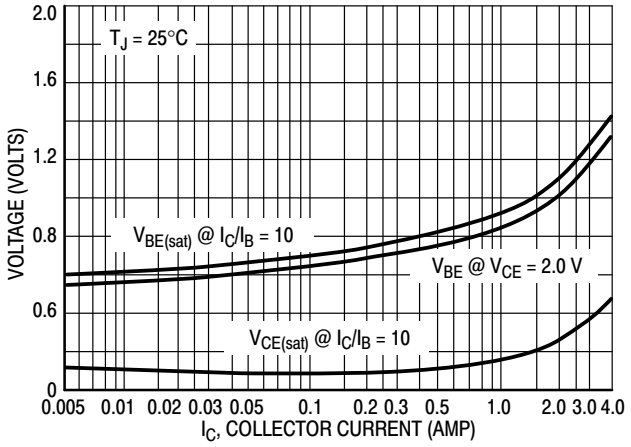


Figure 3. “On” Voltage

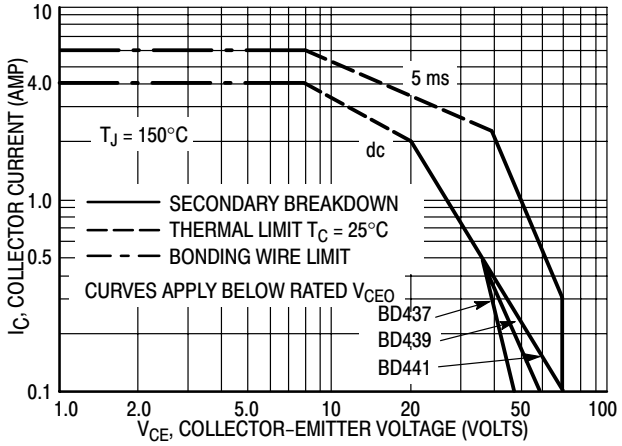


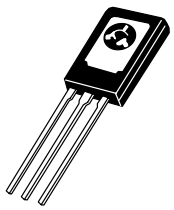
Figure 4. Active Region Safe Operating Area

Plastic Medium Power Silicon PNP Transistor

BD438
BD440
BD442

. . . for amplifier and switching applications. Complementary types are BD437 and BD441.

4.0 AMPERES
POWER TRANSISTORS
PNP SILICON



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage	BD438 BD440 BD442	V_{CEO}	45 60 80	Vdc
Collector–Base Voltage	BD438 BD440 BD442	V_{CBO}	45 60 80	Vdc
Emitter–Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	36 288	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector–Emitter Breakdown Voltage		$V_{(BR)CEO}$				Vdc
(I_C = 100 mA, I_B = 0)	BD438		45	—	—	
	BD440		60	—	—	
	BD442		80	—	—	
Collector–Base Breakdown Voltage		$V_{(BR)CBO}$				Vdc
(I_C = 100 μA, I_B = 0)	BD438		45	—	—	
	BD440		60	—	—	
	BD442		80	—	—	
Emitter–Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 45 V, I_E = 0)	BD438		—	—	0.1	
(V_{CB} = 60 V, I_E = 0)	BD440		—	—	0.1	
(V_{CB} = 80 V, I_E = 0)	BD442		—	—	0.1	
Emitter Cutoff Current (V_{EB} = 5.0 V)		I_{EBO}	—	—	1.0	mAdc
DC Current Gain		h_{FE}				
(I_C = 10 mA, V_{CE} = 5.0 V)	BD438		30	—	—	
	BD440		20	—	—	
	BD442		15	—	—	
DC Current Gain		h_{FE}				
(I_C = 500 mA, V_{CE} = 1.0 V)	BD438		85	—	375	
	BD440		40	—	475	
	BD442		40	—	475	
DC Current Gain		h_{FE}				
(I_C = 2.0 A, V_{CE} = 1.0 V)	BD438		40	—	—	
	BD440		25	—	—	
	BD442		15	—	—	
Collector Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 3.0 A, I_B = 0.3 A)	BD438		—	—	0.7	
	BD440		—	—	0.8	
	BD442		—	—	0.8	
Base–Emitter On Voltage	BD438	$V_{BE(ON)}$	—	—	1.1	Vdc
(I_C = 2.0 A, V_{CE} = 1.0 V)	BD440/442		—	—	1.5	
Current–Gain — Bandwidth Product (V_{CE} = 1.0 V, I_C = 250 mA, f = 1.0 MHz)		f_T	3.0	—	—	MHz

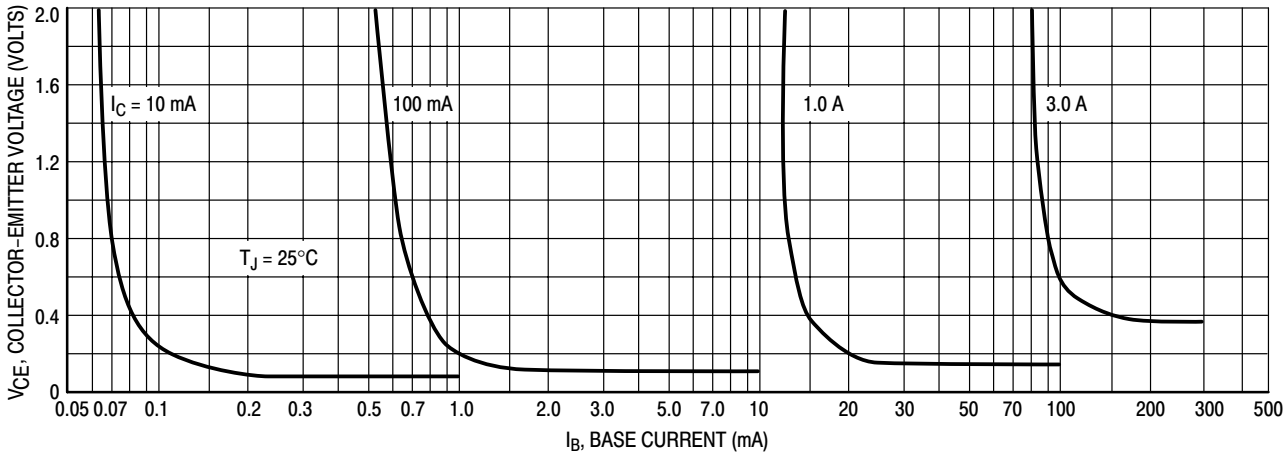


Figure 1. Collector Saturation Region

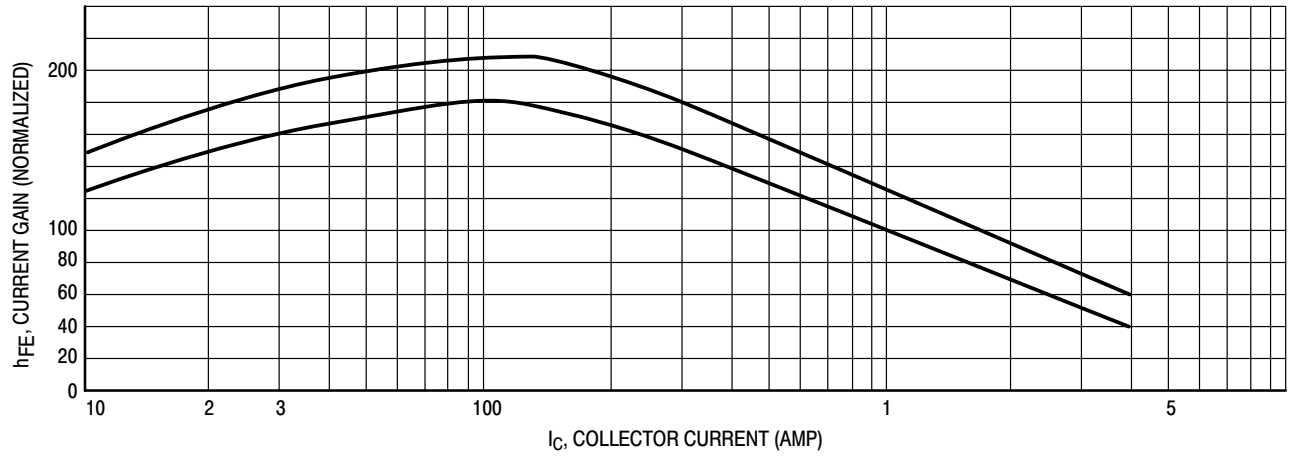


Figure 2. Current Gain

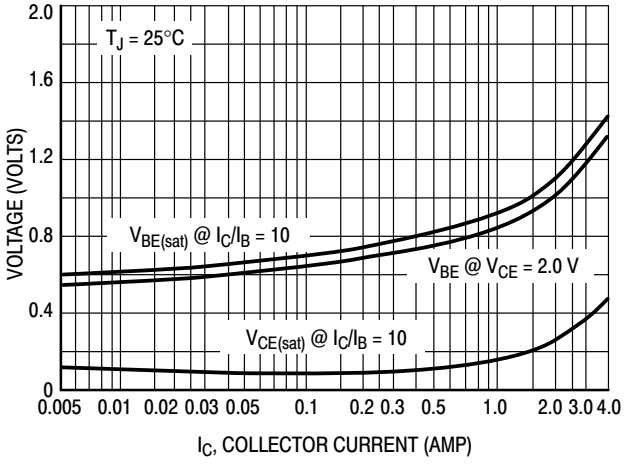


Figure 3. “On” Voltage

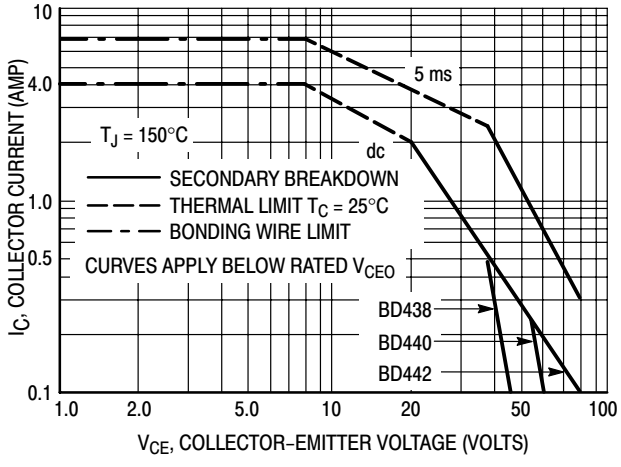


Figure 4. Active Region Safe Operating Area

Plastic Medium-Power Silicon NPN Darlingtons

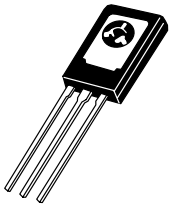
. . . for use as output devices in complementary general–purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 750 (Min) @ I_C
  = 1.5 and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

BD675
BD675A
BD677
BD677A
BD679
BD679A
BD681*

***ON Semiconductor Preferred Device**

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
NPN SILICON
60, 80, 100 VOLTS
40 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD675 BD675A	BD677 BD677A	BD679 BD679A	BD681	Unit
Collector–Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	–55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

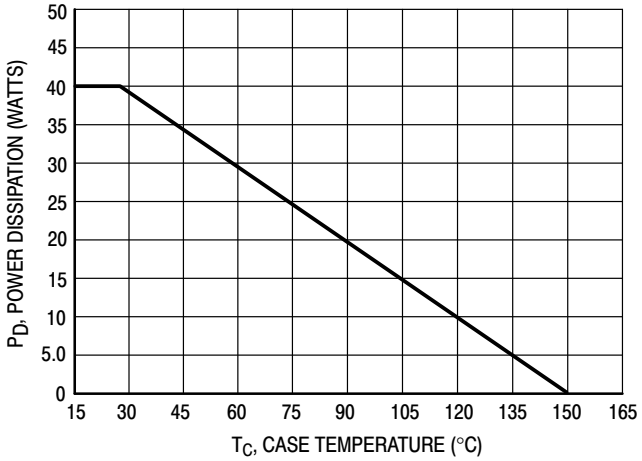


Figure 1. Power Temperature Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev.9
Publication Order Number:
BD675/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	—	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100'C)		I_{CBO}	 — —	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Currert Gain(1) (I_C = 1.5 Adc,V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD675, 677, 679, 681 BD675A, 677A, 679A	h_{FE}	 750 750	 — —	—
Collector–Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD677, 679, 681 BD675A, 677A, 679A	$V_{CE(sat)}$	 — —	 2.5 2.8	Vdc
Base–Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3 0 Vdc)	 BD677, 679, 681 BD675A, 677A, 679A	$V_{BE(on)}$	 — —	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

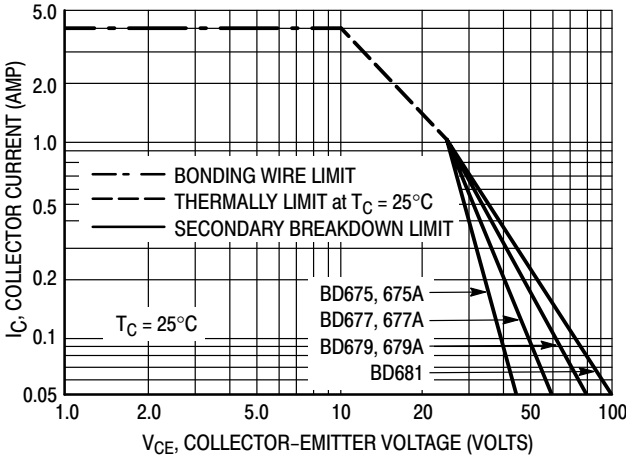


Figure 2. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

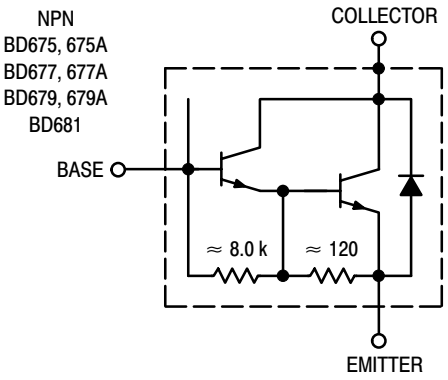


Figure 3. Darlington Circuit Schematic

BD676, BD676A, BD678, BD678A, BD680, BD680A, BD682

Plastic Medium-Power Silicon PNP Darlingtons

...for use as output devices in complementary general–purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BD676, BD676A BD678, BD678A BD680, BD680A BD682	V_{CEO}	 45 60 80 100	Vdc
Collector-Base Voltage BD676, BD676A BD678, BD678A BD680, BD680A BD682	V_{CB}	 45 60 80 100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	4.0	Adc
Base Current	I_B	0.1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 0.32	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

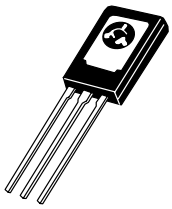
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case	$R_{\theta JC}$	3.13	°C/W

ON Semiconductor™

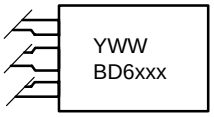
http://onsemi.com

4.0 AMPERE DARLINGTON POWER TRANSISTORS PNP SILICON 45, 60, 80, 100 VOLTS 40 WATTS



TO–225AA
CASE 77
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week
BD6xxx = Specific Device Code
xxx = 76, 76A, 78, 78A, 80, 80A or 82

ORDERING INFORMATION

Device	Package	Shipping
BD676	TO–225AA	500 Units/Box
BD676A	TO–225AA	500 Units/Box
BD678	TO–225AA	500 Units/Box
BD678A	TO–225AA	500 Units/Box
BD680	TO–225AA	500 Units/Box
BD680A	TO–225AA	500 Units/Box
BD682	TO–225AA	500 Units/Box

March, 2001 – Rev. 9

Publication Order Number:
BD676/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 1.) (I_C = 50 mAdc, I_B = 0)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}. I_E = 0, T_C = 100°C)		I_{CBO}	 – –	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1.) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD676, 678, 680, 682 BD676A, 678A, 680A	h_{FE}	 750 750	 – –	
Collector–Emitter Saturation Voltage (Note 1.) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD678, 680, 682 BD676A, 678A, 680A	$V_{CE(sat)}$	 – –	 2.5 2.8	Vdc
Base–Emitter On Voltage (Note 1.) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD678, 680, 682 BD676A, 678A, 680A	$V_{BE(on)}$	 – –	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

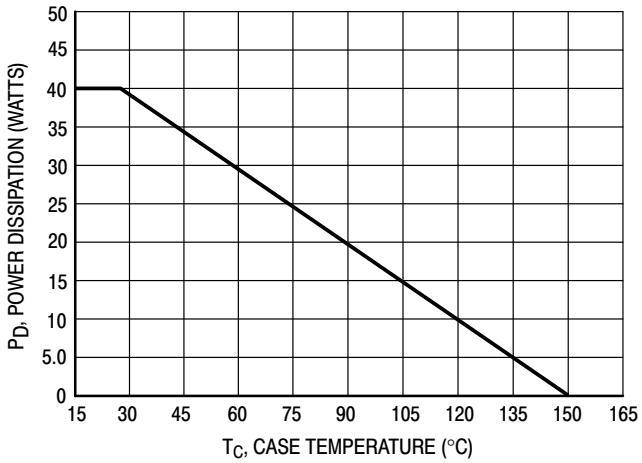


Figure 1. Power Temperature Derating

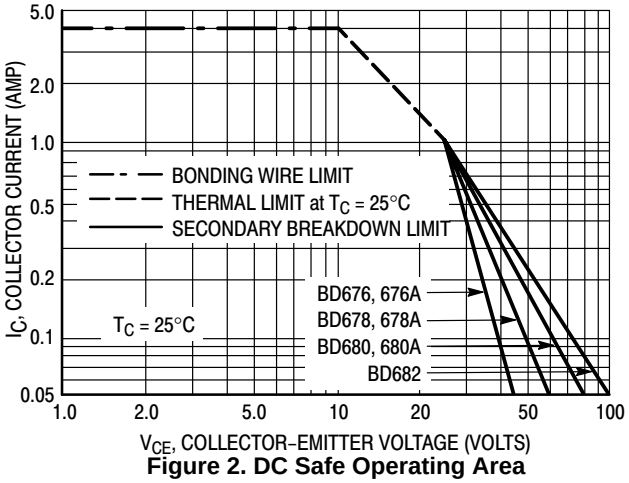


Figure 2. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

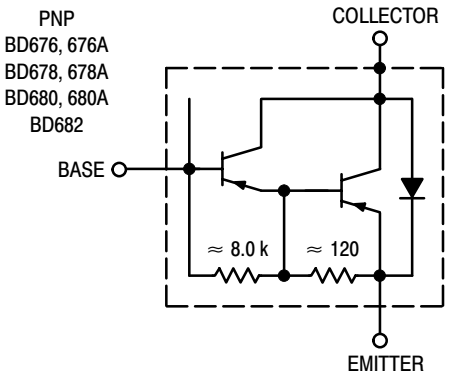


Figure 3. Darlington Circuit Schematic

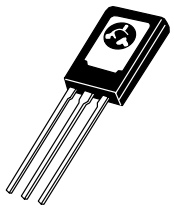
NPN
BD787
PNP
BD788

Complementary Plastic Silicon Power Transistors

. . . designed for lower power audio amplifier and low current, high–speed switching applications.

- Low Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ 60 Vdc (Min) — BD787, BD788
- High Current–Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Collector–Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
15 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD787 BD788	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

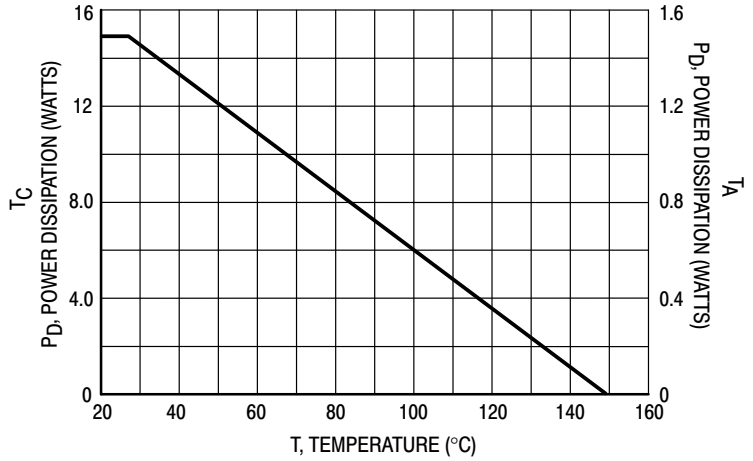


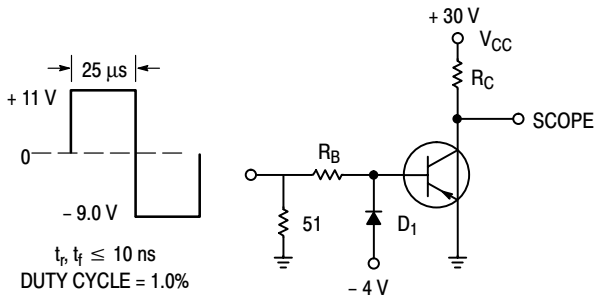
Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)		$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0)		I_{CEO}	—	100	μAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	 — —	 1.0 0.1	 μAdc mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 40 25 20 5.0	 250 — — —	—
Collector–Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)		$V_{CE(sat)}$	 — — — —	 0.4 0.6 0.8 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	2.0	Vdc
Base–Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0) (f = 0.1 MHz)	 BD787 BD788	C_{ob}	 — —	 50 70	pF
Small–Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	—	—

*Indicates JEDEC Registered Data

(1) Pulse Test; Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

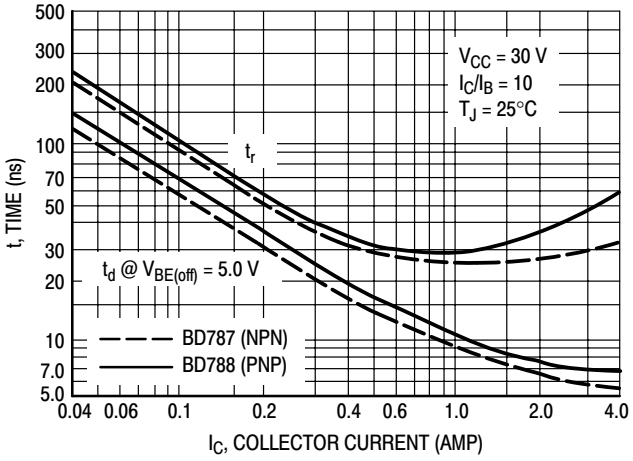


Figure 3. Turn–On Time

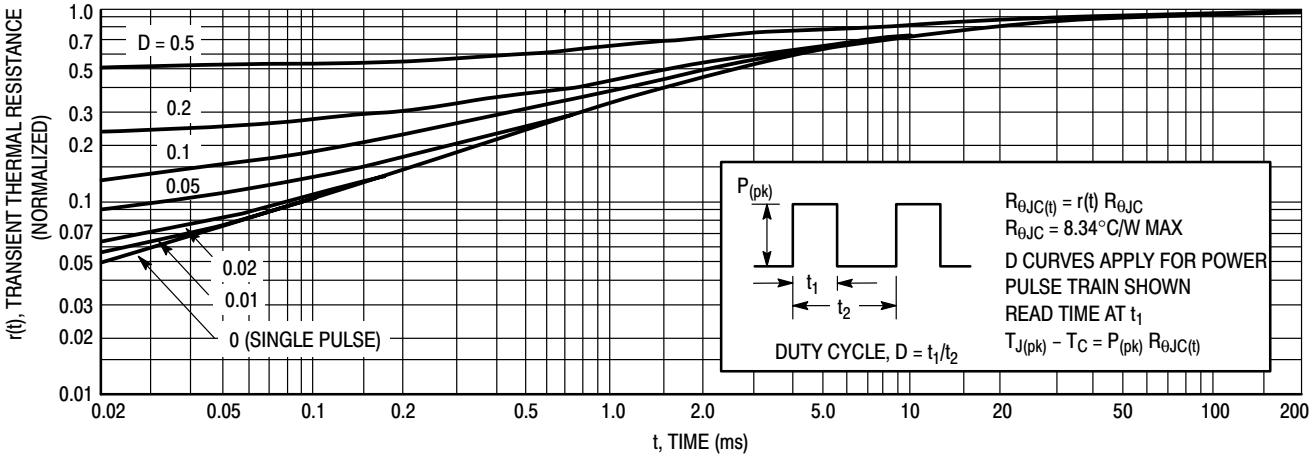


Figure 4. Thermal Response

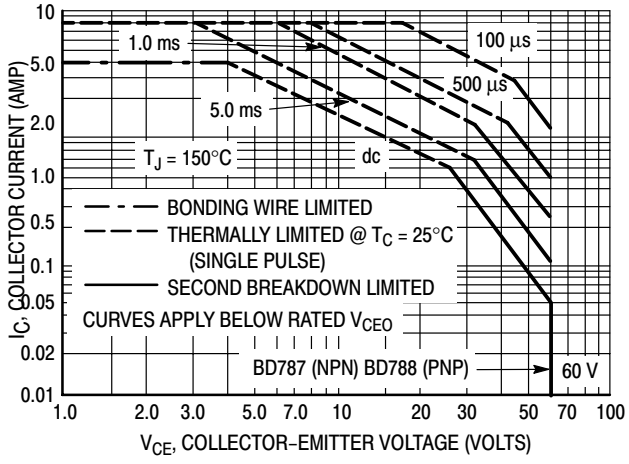


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

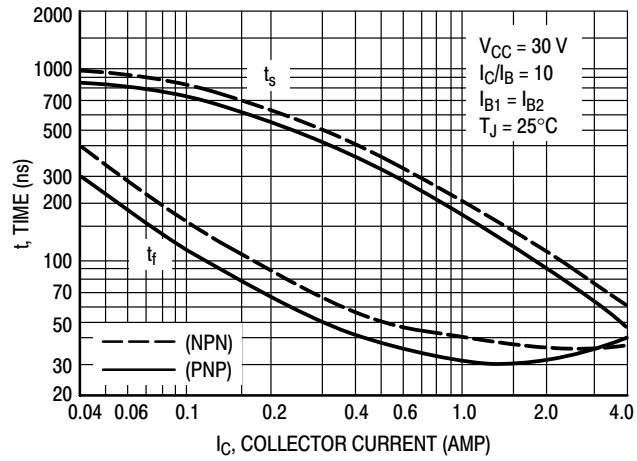


Figure 6. Turn–Off Time

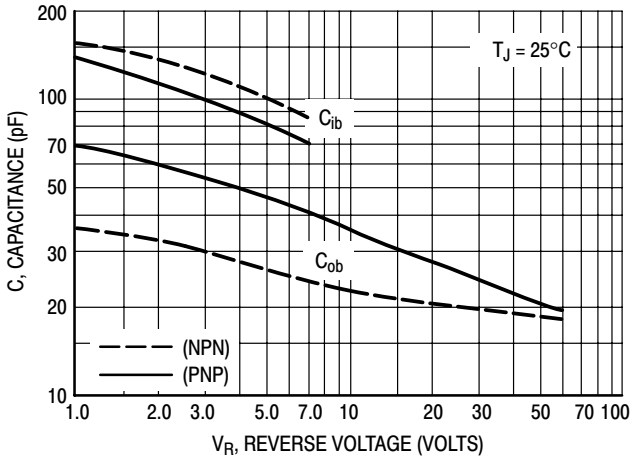
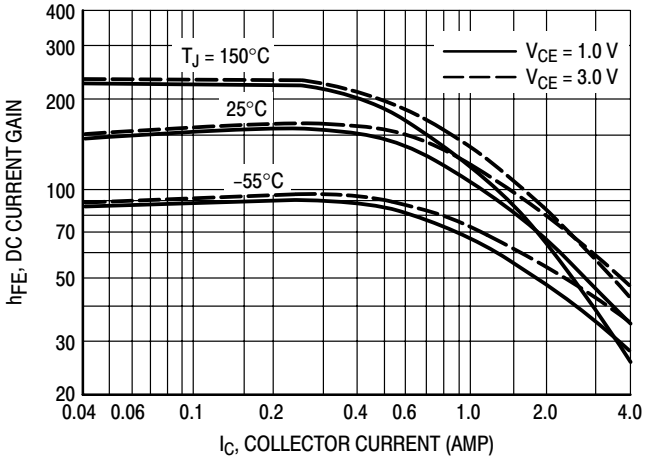


Figure 7. Capacitance

NPN
BD787



NPN
BD788

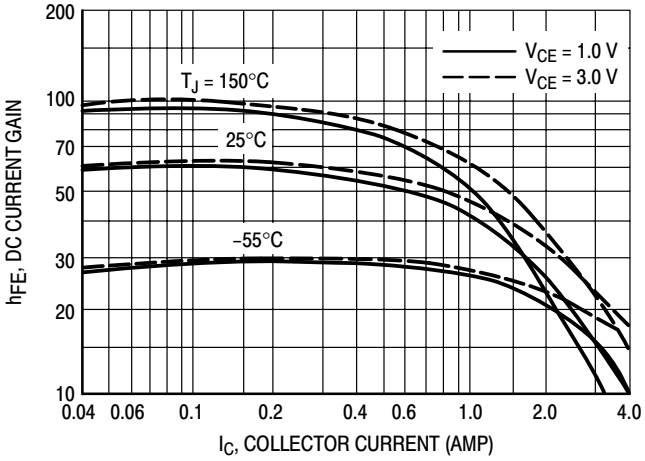
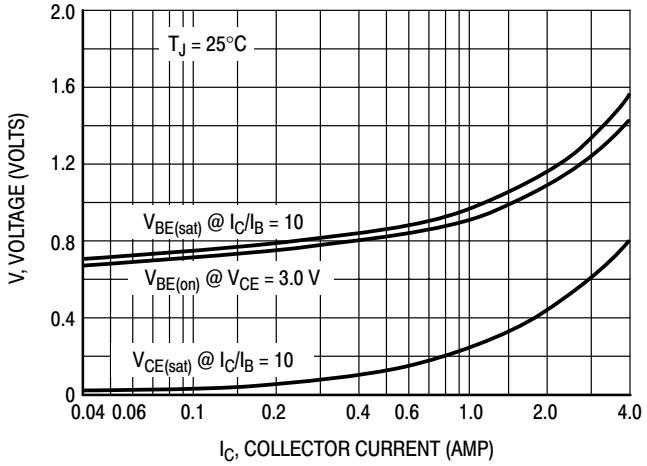


Figure 8. DC Current Gain



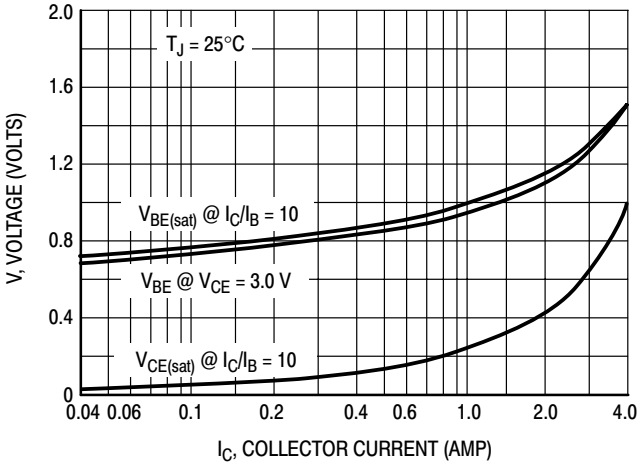


Figure 9. “On” Voltages

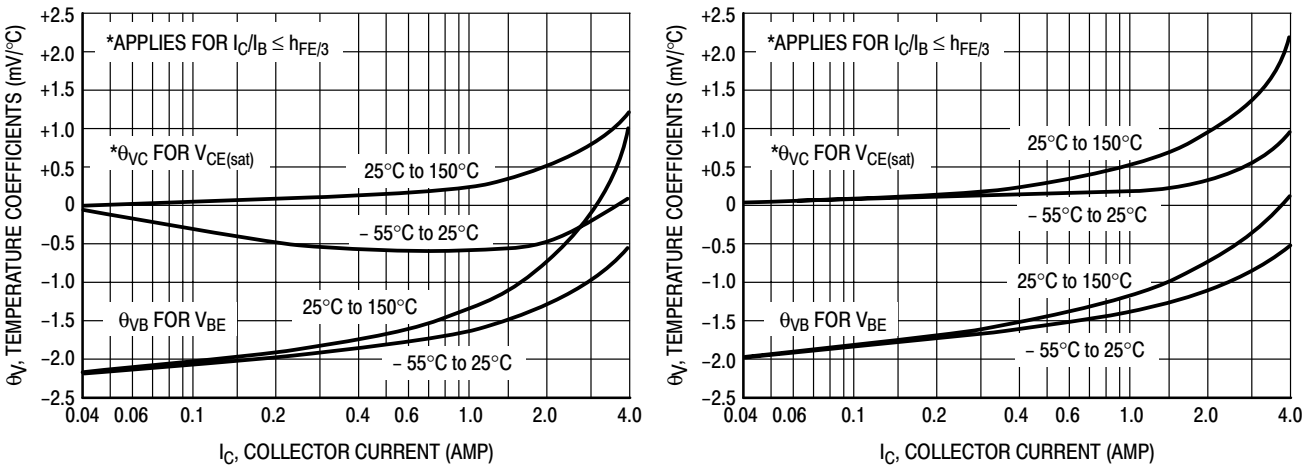


Figure 10. Temperature Coefficients

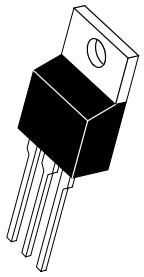
NPN
BD809
PNP
BD810

Plastic High Power Silicon Transistor

. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 2.0 Adc

10 AMPERE
POWER TRANSISTORS
PNP SILICON
60, 80 VOLTS
90 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

May, 2001 – Rev. 0
Publication Order Number:
BD809/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	 80	— —	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	 —	 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
DC Current Gain (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 4.0 A, V_{CE} = 2.0 V)	h_{FE}	 30 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	—	1.1	Vdc
Base–Emitter On Voltage* (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
Current–Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	1.5	—	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

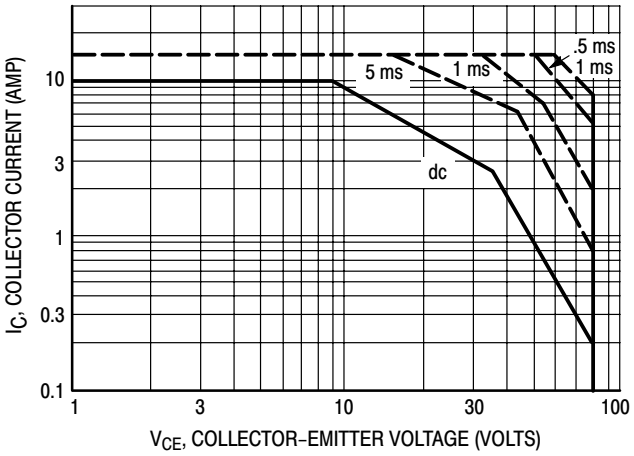


Figure 1. Active Region DC Safe Operating Area (see Note 1)

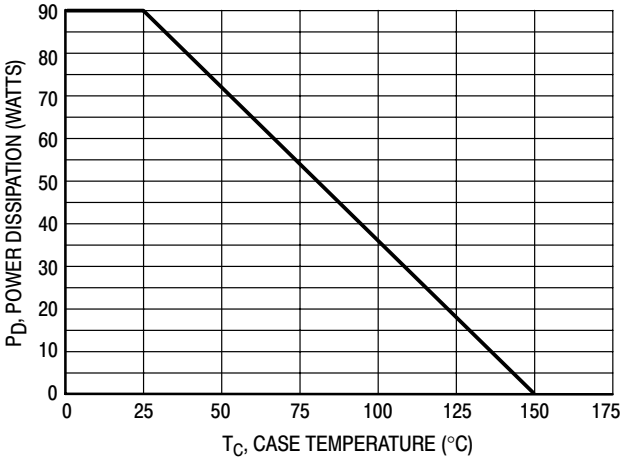
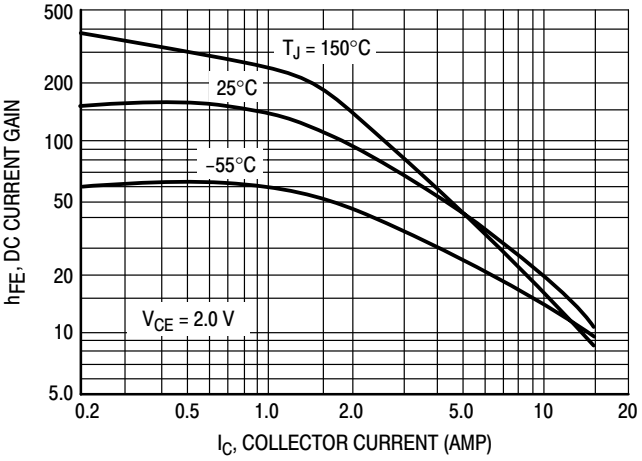


Figure 2. Power–Temperature Derating Curve

NPN
BD809



PNP
BD810

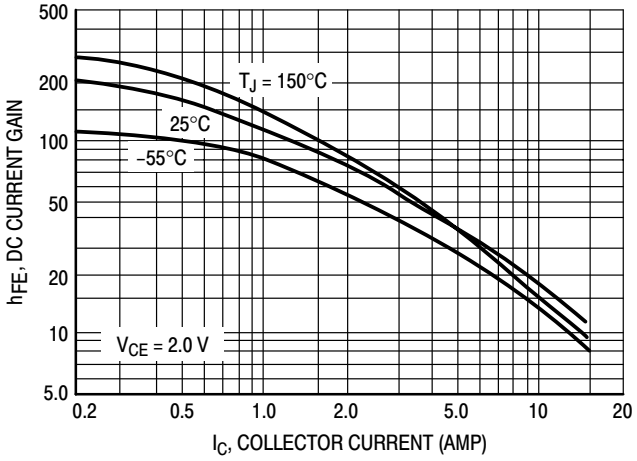
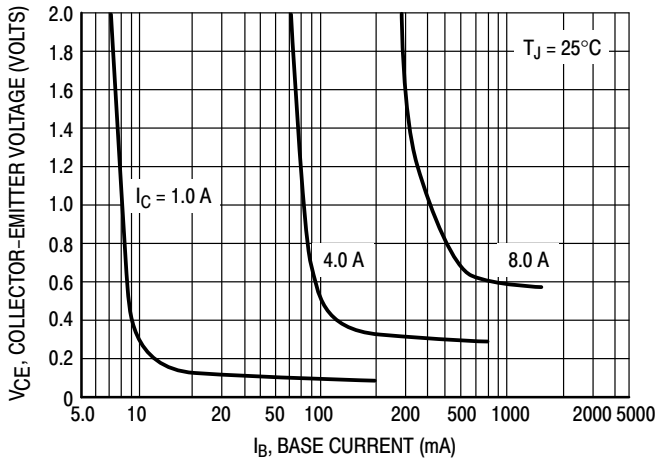


Figure 3. DC Current Gain



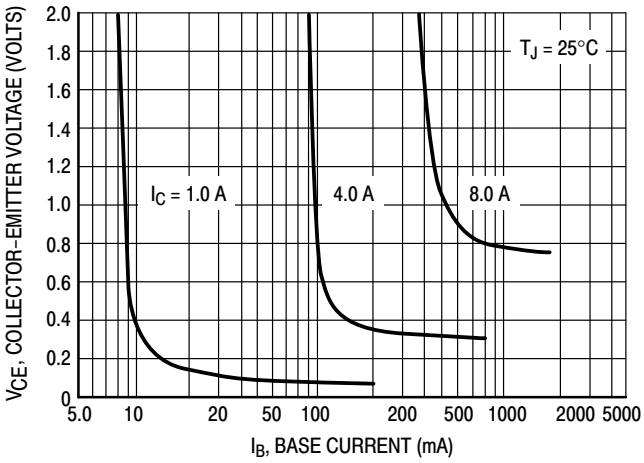
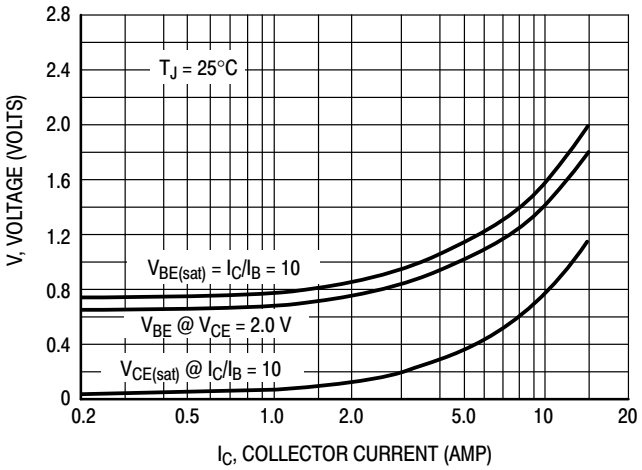


Figure 4. Collector Saturation Region



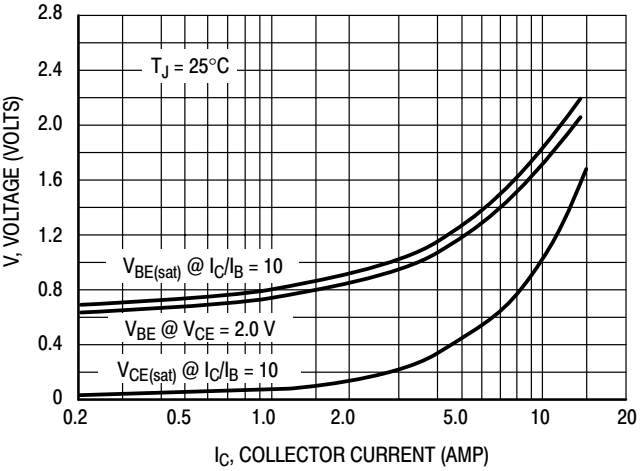


Figure 5. “On” Voltages

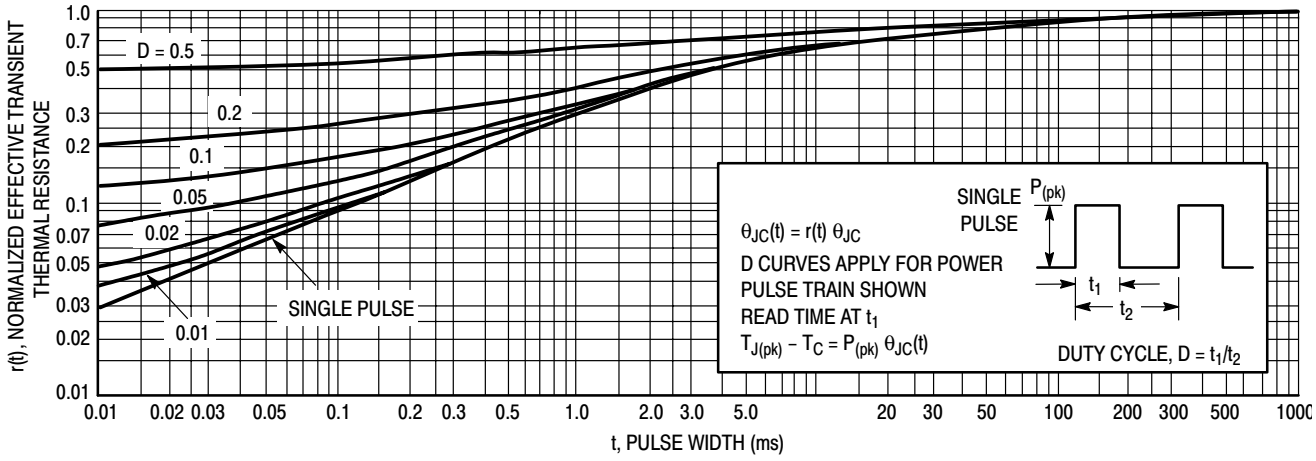


Figure 6. Thermal Response

Note 1:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

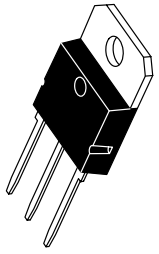
Complementary Silicon Plastic Power Darlingtons

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
  HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built–in Base Emitter Shunt Resistors

NPN
BDV65B
PNP
BDV64B

DARLINGTONS
10 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–80–100–120 VOLTS
125 WATTS



CASE 340D–02
SOT 93, TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	10 20	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

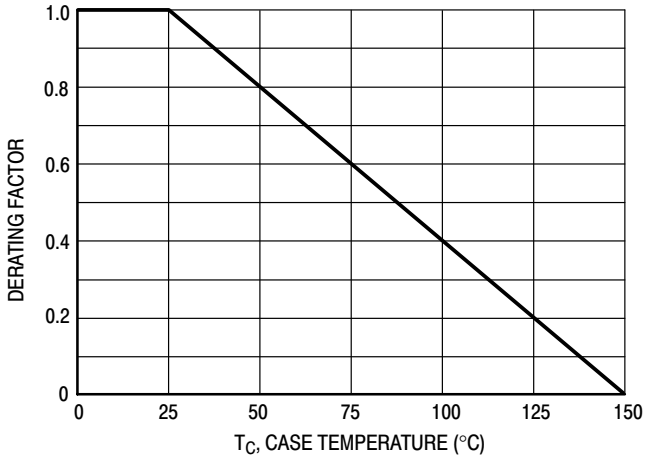


Figure 1. Power Derating

March, 2001 – Rev. 10
Publication Order Number:
BDV65B/D

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.4	mAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	—	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	1000	—	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.02 Adc)	$V_{CE(sat)}$	—	2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc

NPN

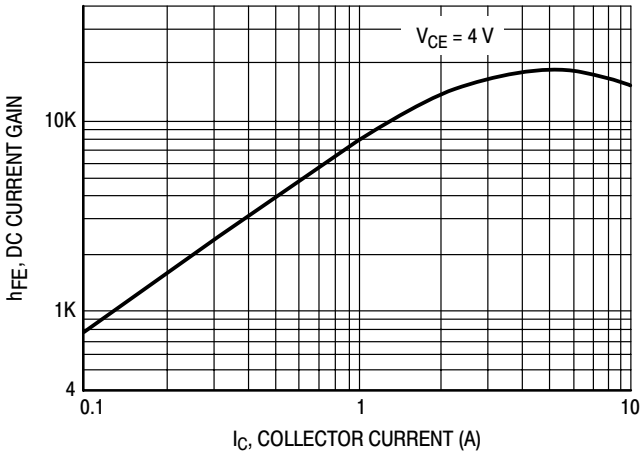


Figure 2. DC Current Gain

PNP

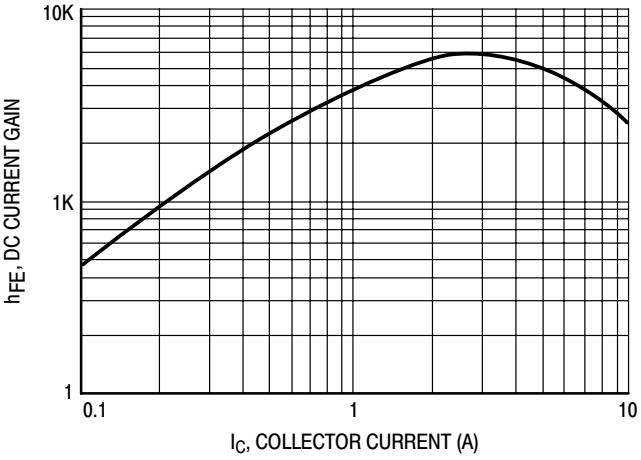


Figure 3. DC Current Gain

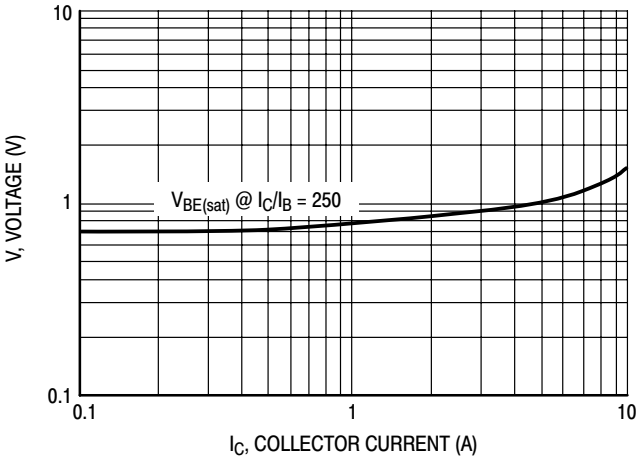


Figure 4. "On" Voltages

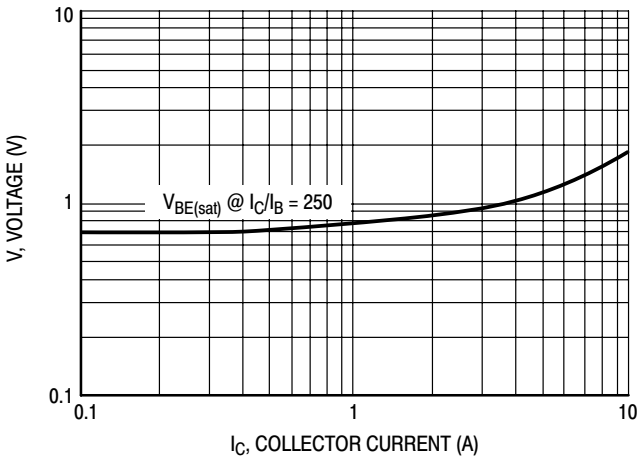


Figure 5. "On" Voltages

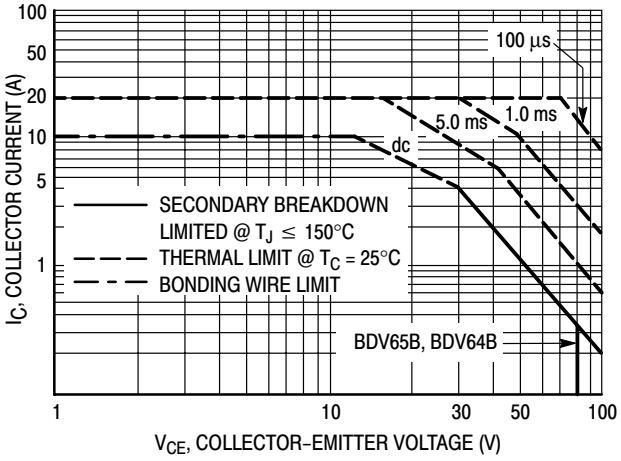


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

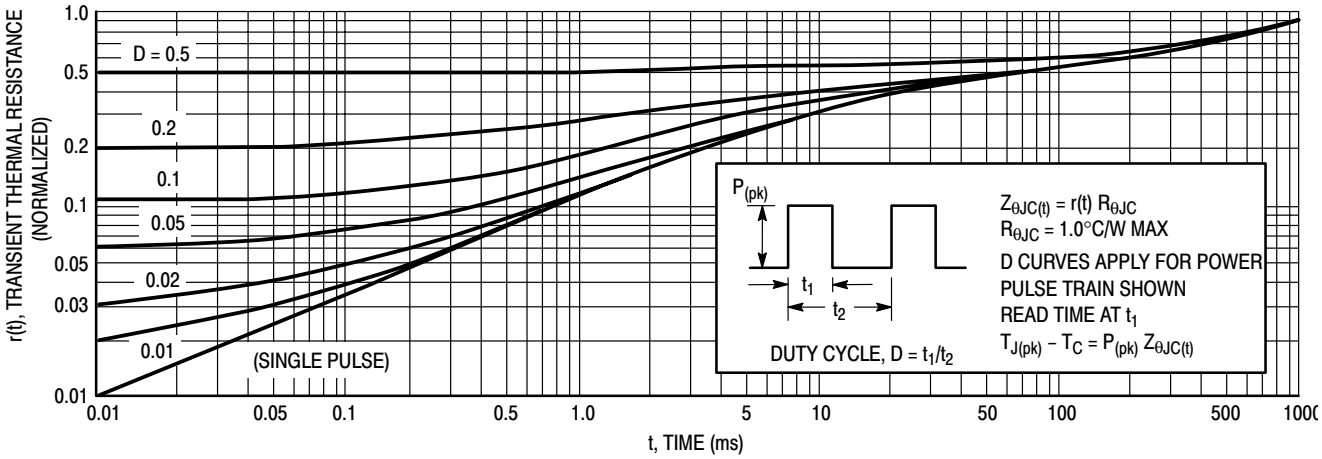


Figure 7. Thermal Response

Darlington Complementary Silicon Power Transistors

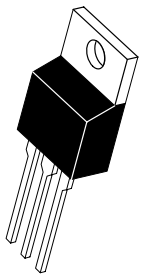
. . . designed for general purpose and low speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (typ.) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDW46
  100 Vdc (min.) — BDW42/BDW47
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.0 Vdc (max.) @ I_C = 5.0 Adc
  3.0 Vdc (max.) @ I_C = 10.0 Adc
- Monolithic Construction with Built–In Base Emitter Shunt resistors
- TO–220AB Compact Package

NPN
BDW42*
PNP
BDW46
BDW47*

***ON Semiconductor Preferred Device**

DARLINGTON
15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
85 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDW46	BDW42 BDW47	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	85 0.68		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

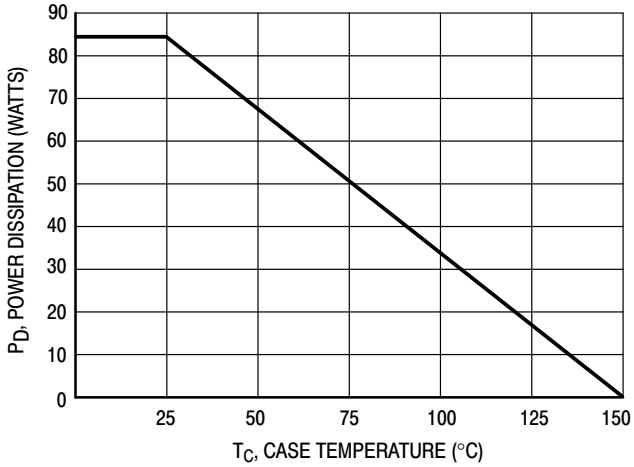


Figure 1. Power Temperature Derating Curve

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	BDW46		80	—	
	BDW42/BDW47		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	BDW46		—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	BDW42/BDW47		—	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 80 Vdc, I_E = 0)	BDW41/BDW46		—	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	BDW42/BDW47		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			1000	—	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			250	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 10 mAdc)			—	2.0	
(I_C = 10 Adc, I_B = 50 mAdc)			—	3.0	
Base–Emitter On Voltage		$V_{BE(on)}$	—	3.0	Vdc
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)					
SECOND BREAKDOWN (2)					
Second Breakdown Collector		$I_{S/b}$			Adc
Current with Base Forward Biased					
BDW42	V_{CE} = 28.4 Vdc		3.0	—	
	V_{CE} = 40 Vdc		1.2	—	
BDW46/BDW47	V_{CE} = 22.5 Vdc		3.8	—	
	V_{CE} = 36 Vdc		1.2	—	
DYNAMIC CHARACTERISTICS					
Magnitude of common emitter small signal short circuit current transfer ratio		f_T	4.0	—	MHz
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDW42		—	200	
	BDW46/BDW47		—	300	
Small–Signal Current Gain		h_{fe}	300	—	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Pulse Test non repetitive: Pulse Width = 250 ms.

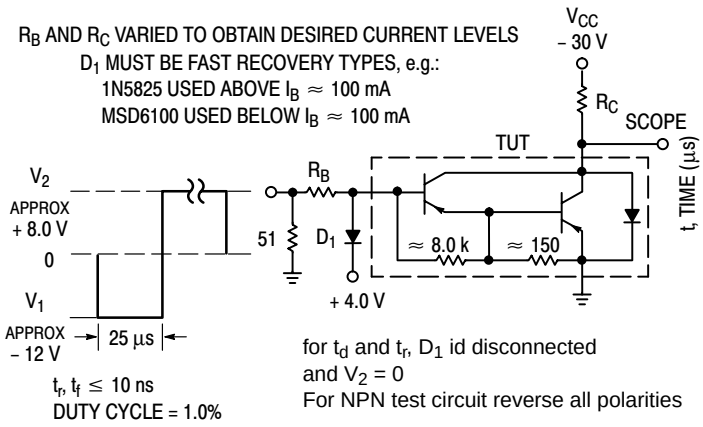


Figure 2. Switching Times Test Circuit

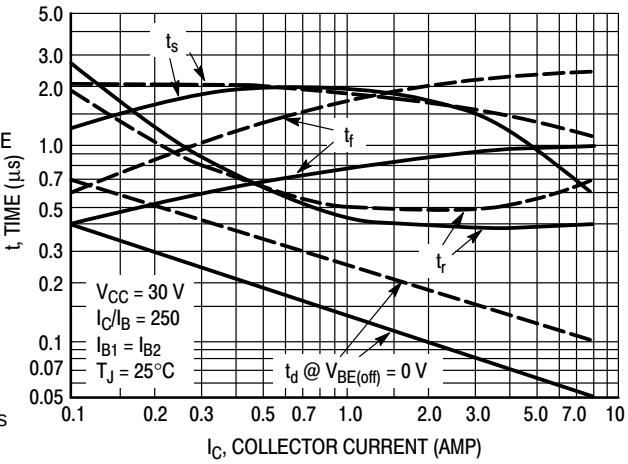


Figure 3. Switching Times

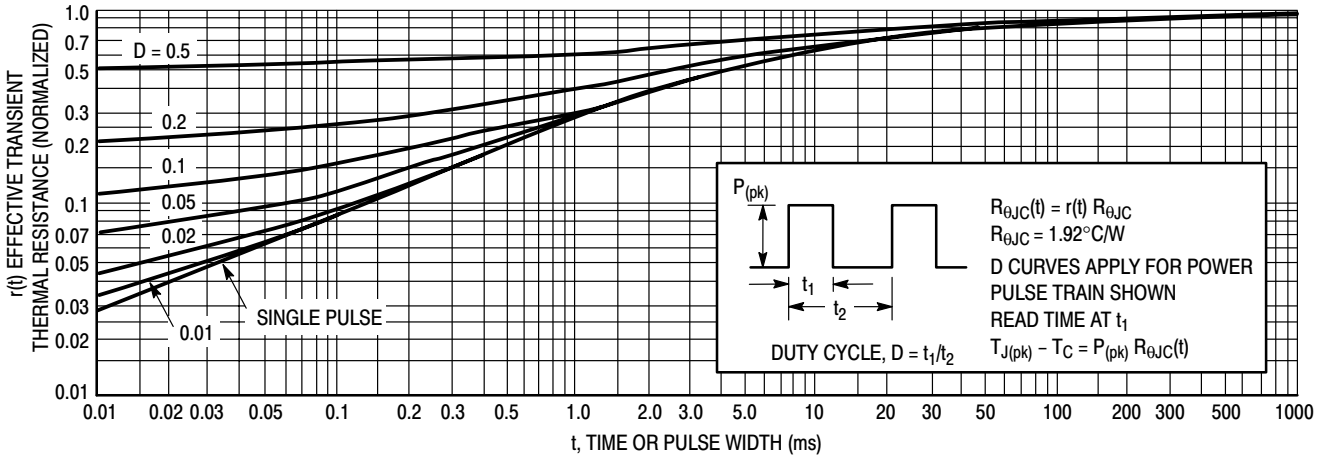


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

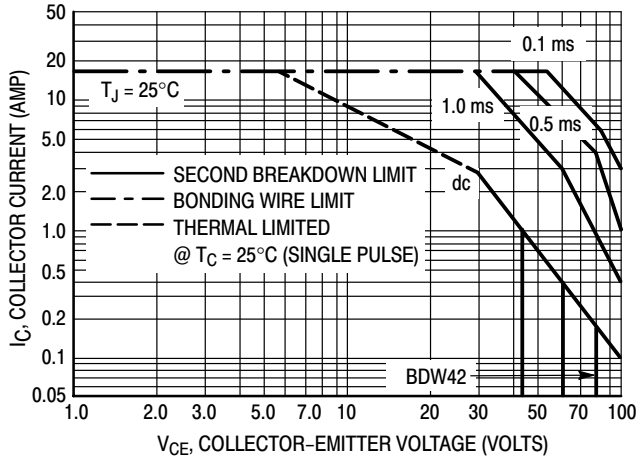


Figure 5. BDW42

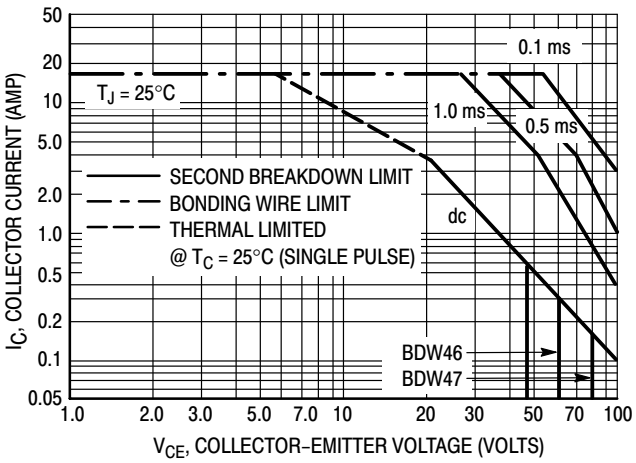


Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 and 6 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

*Linear extrapolation

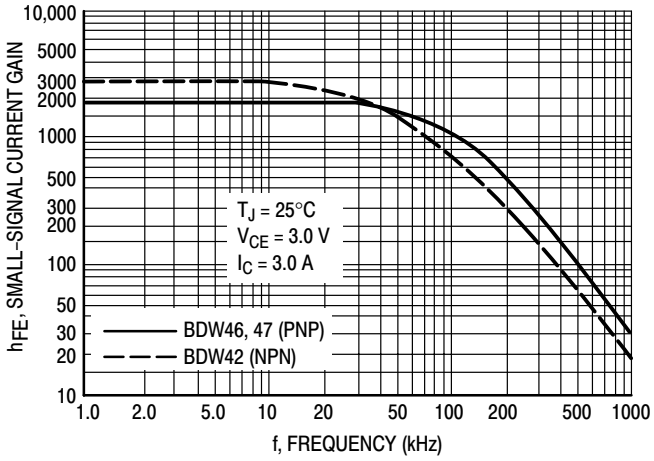


Figure 7. Small–Signal Current Gain

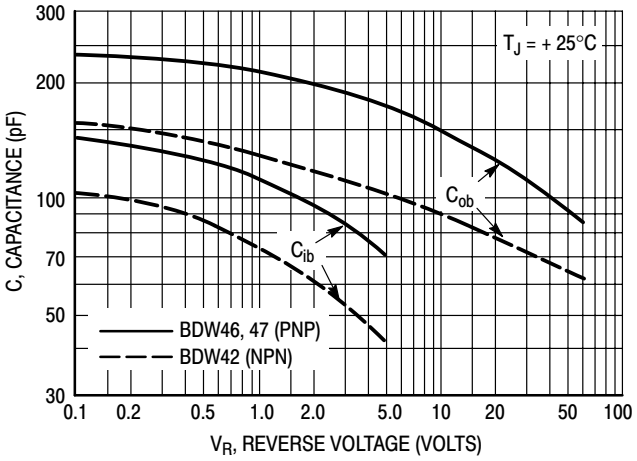


Figure 8. Capacitance

BDW40, 41, 42 (NPN)

BDW45, 46, 47 (PNP)

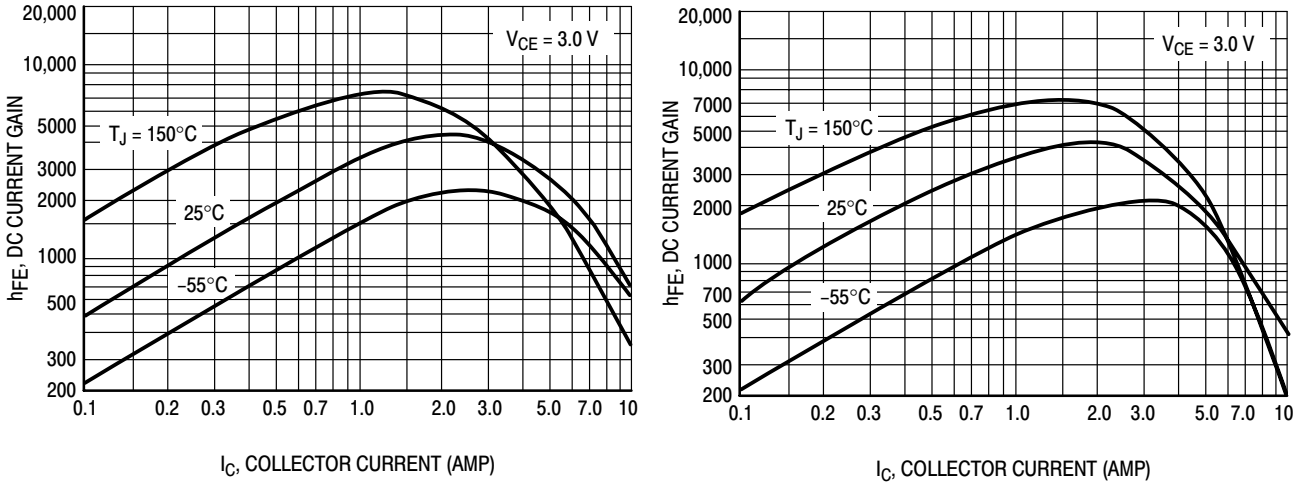


Figure 9. DC Current Gain

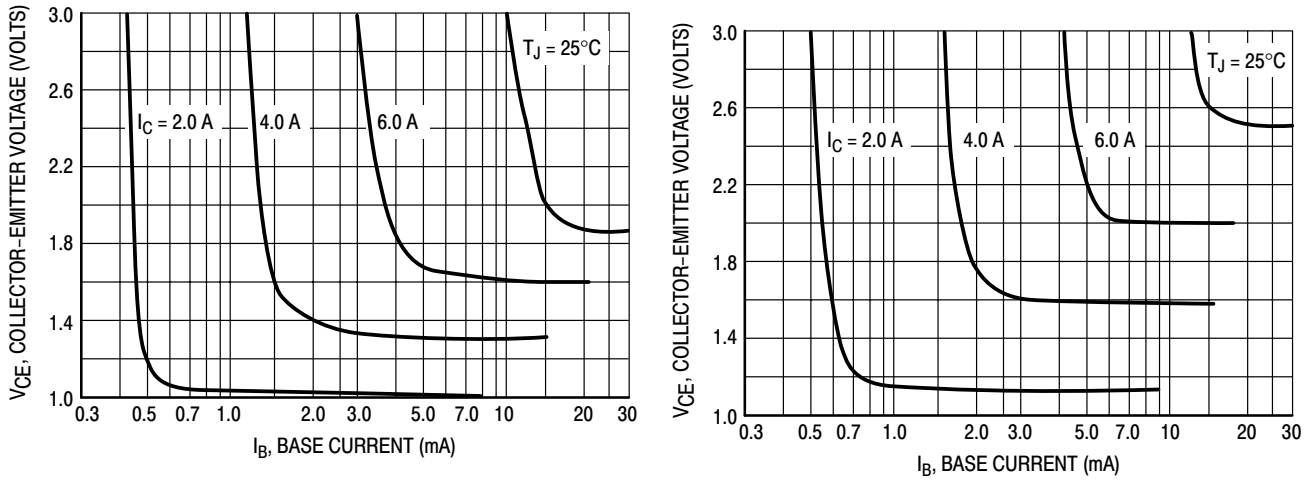


Figure 10. Collector Saturation Region

BDW40, 41, 42 (NPN) **BDW45, 46, 47 (PNP)**

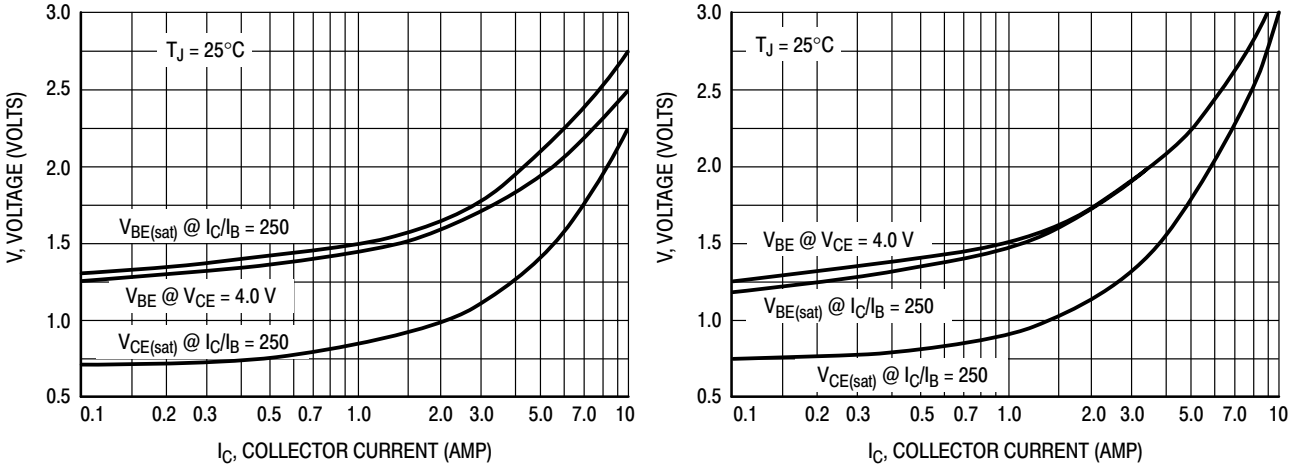


Figure 11. “On” Voltages

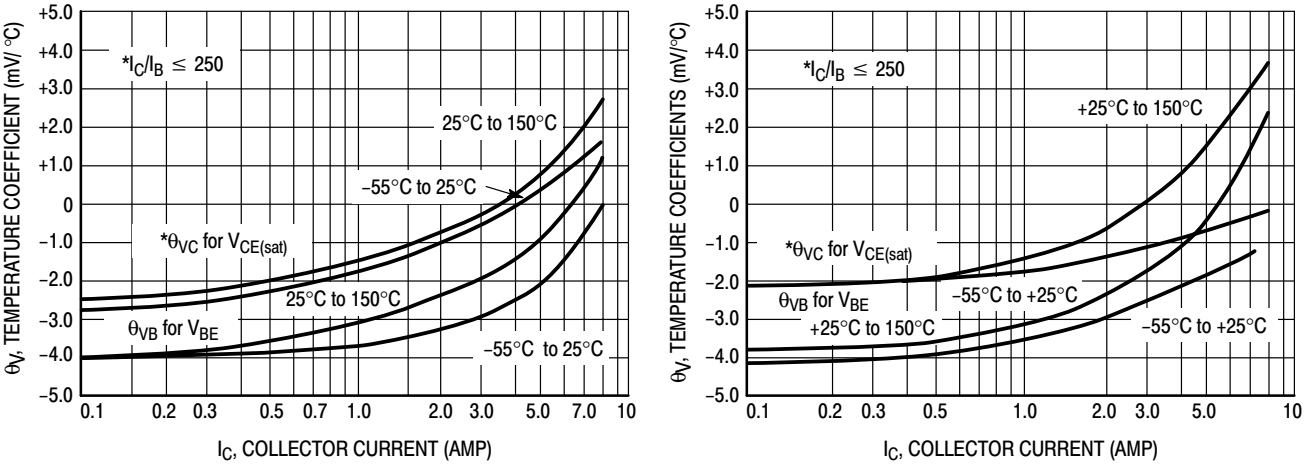


Figure 12. Temperature Coefficients

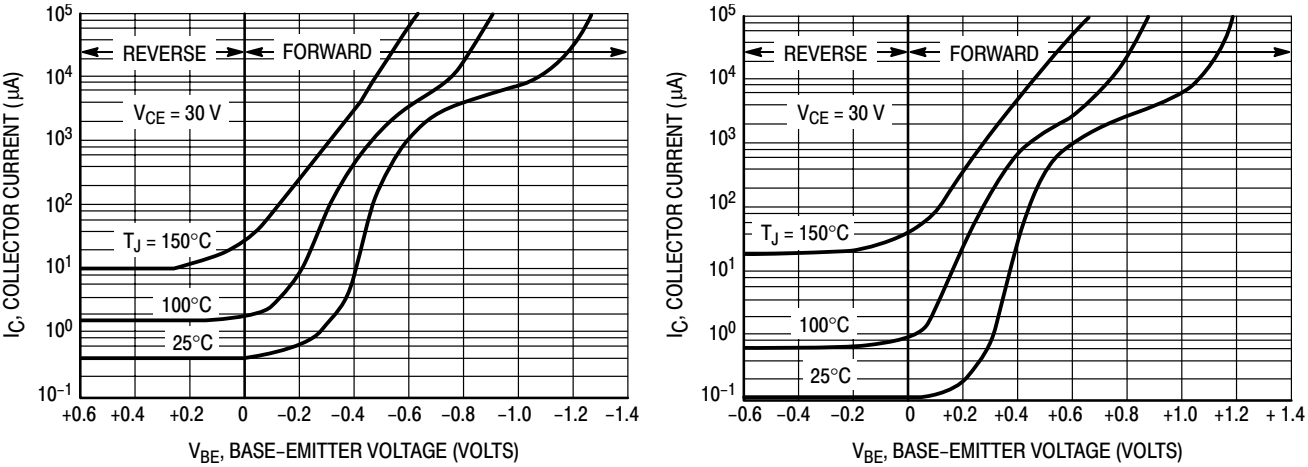


Figure 13. Collector Cut−Off Region

Figure 14. Darlington Schematic

Darlington Complementary Silicon Power Transistors

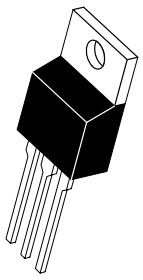
. . . designed for general purpose and low speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (typ.) at I_C = 4.0
- Collector–Emitter Sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDX33B, 34B
  100 Vdc (min.) — BDX33C, 34C
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max.) at I_C = 3.0 Adc — BDX33B, 33C/34B, 34C
- Monolithic Construction with Build–In Base–Emitter Shunt resistors
- TO–220AB Compact Package

NPN
BDX33B
BDX33C*
PNP
BDX34B
BDX34C*

*ON Semiconductor Preferred Device

DARLINGTON
10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
70 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15		Adc
Base Current	I_B	0.25		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 70 0.56		 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
BDX33B/D

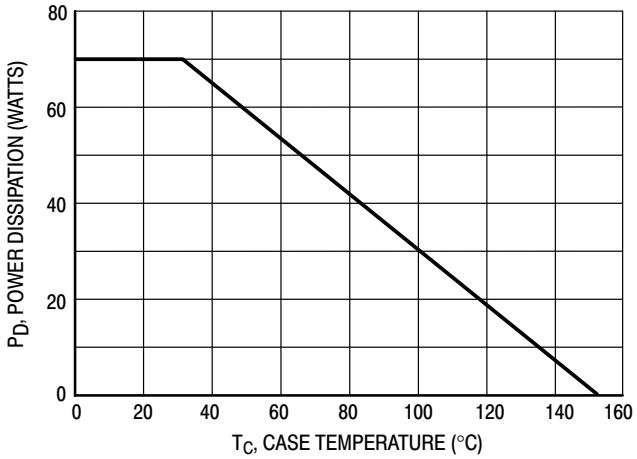


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)	BDX33B/BDX34B BDX33C/BDX33C	$V_{CER(sus)}$	 80 100	 — —	Vdc
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEX(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 1/2 rated V_{CEO}, I_B = 0)	T_C = 25°C T_C = 100°C	I_{CEO}	 — —	 0.5 10	mAdc
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)	T_C = 25°C T_C = 100°C	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	h_{FE}	750	—	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc)	BDX33B, 33C/34B, 34C	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	$V_{BE(on)}$	—	2.5	Vdc
Diode Forward Voltage (I_C = 8.0 Adc)		V_F	—	4.0	Vdc

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
[2] Pulse Test non repetitive: Pulse Width = 0.25 s.

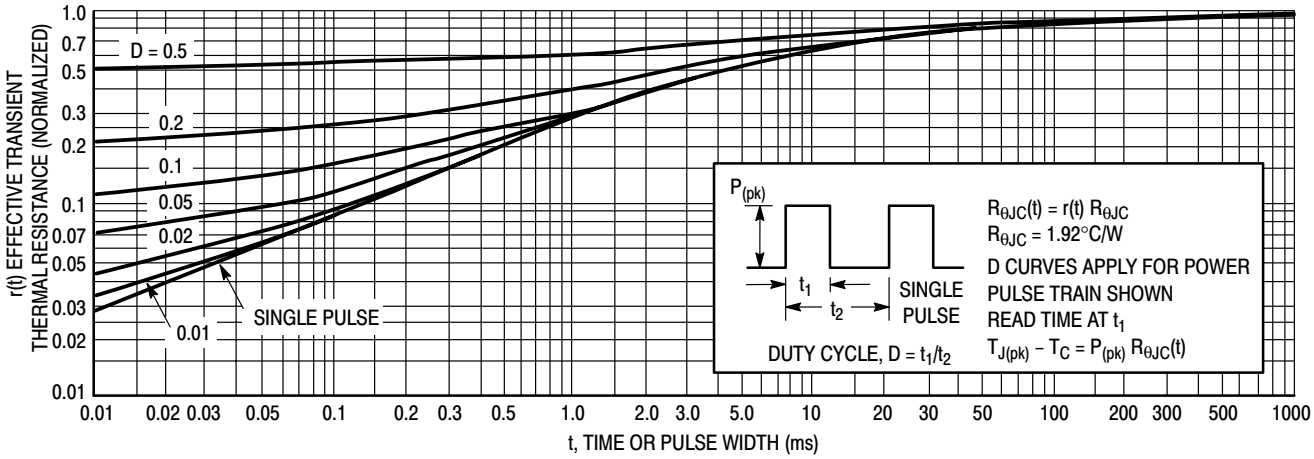


Figure 1. Thermal Response

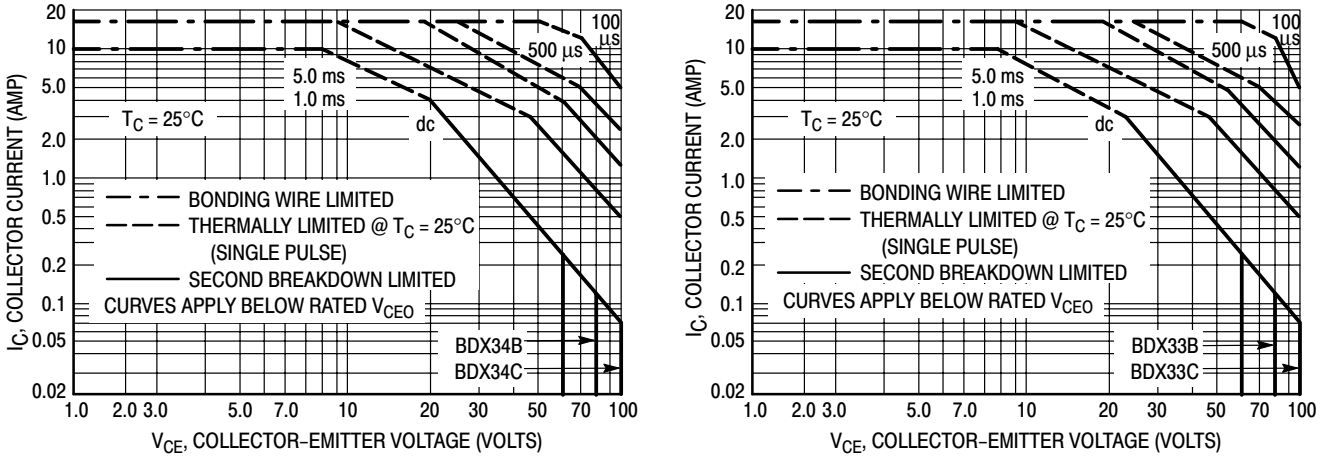


Figure 2. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ = 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

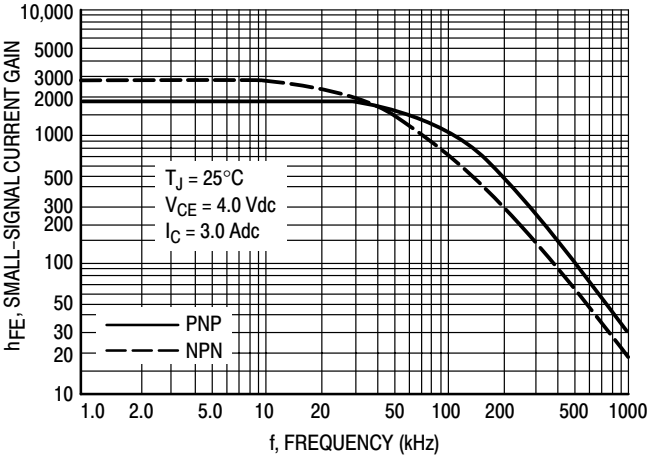


Figure 3. Small−Signal Current Gain

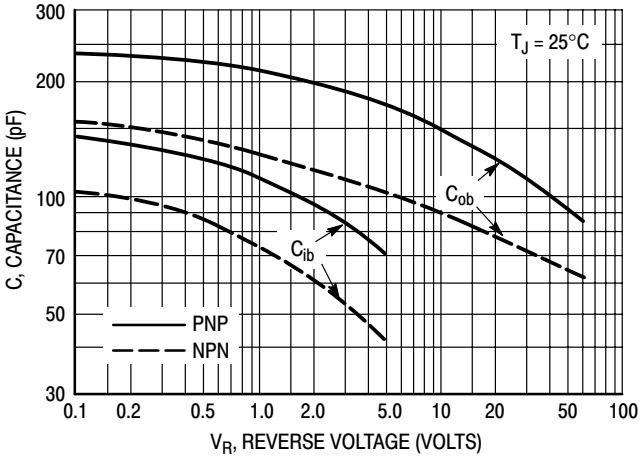


Figure 4. Capacitance

NPN
BDX33B, 33C

PNP
BDX34B, 34C

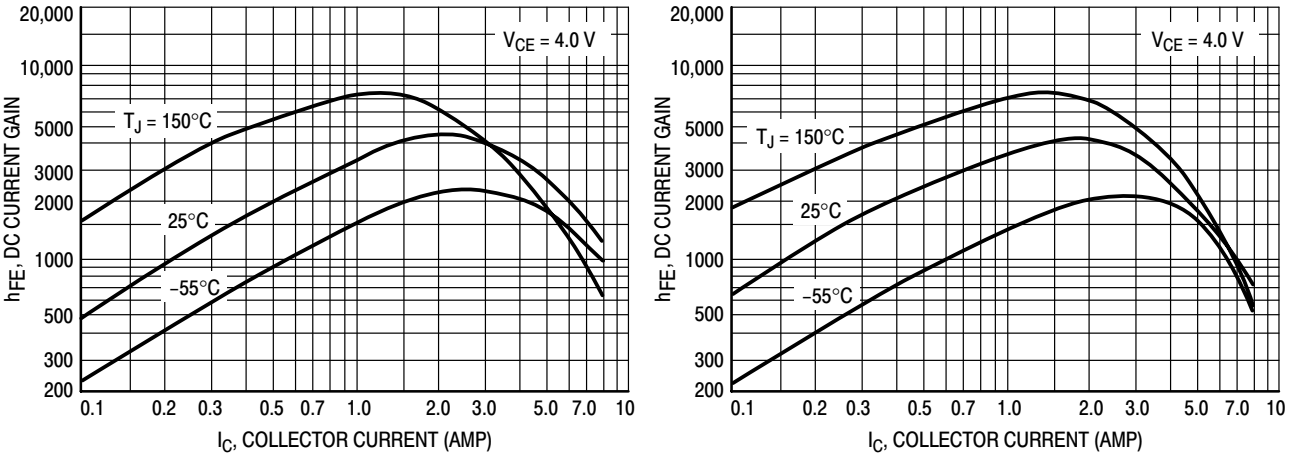


Figure 5. DC Current Gain

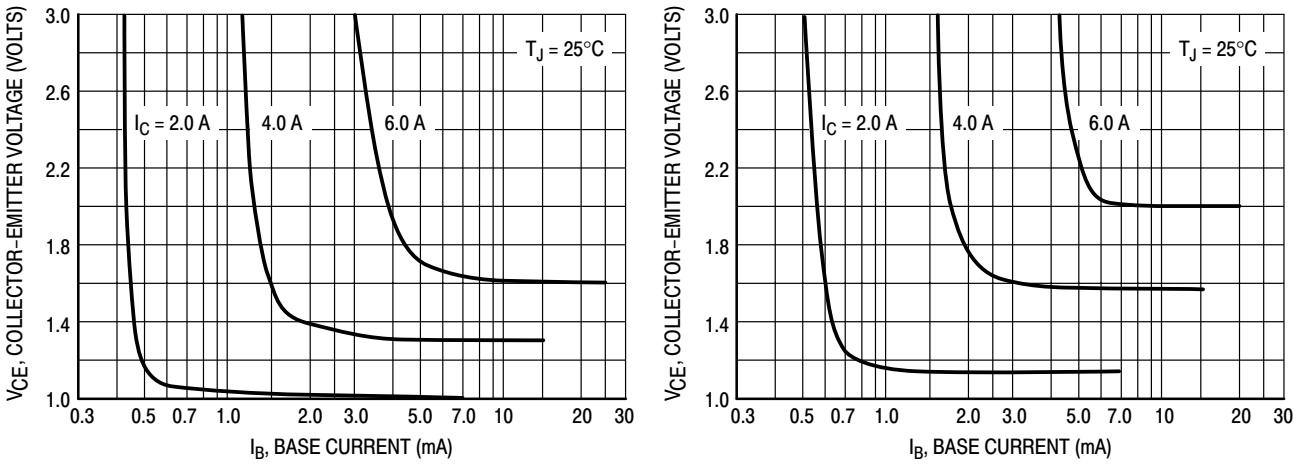


Figure 6. Collector Saturation Region

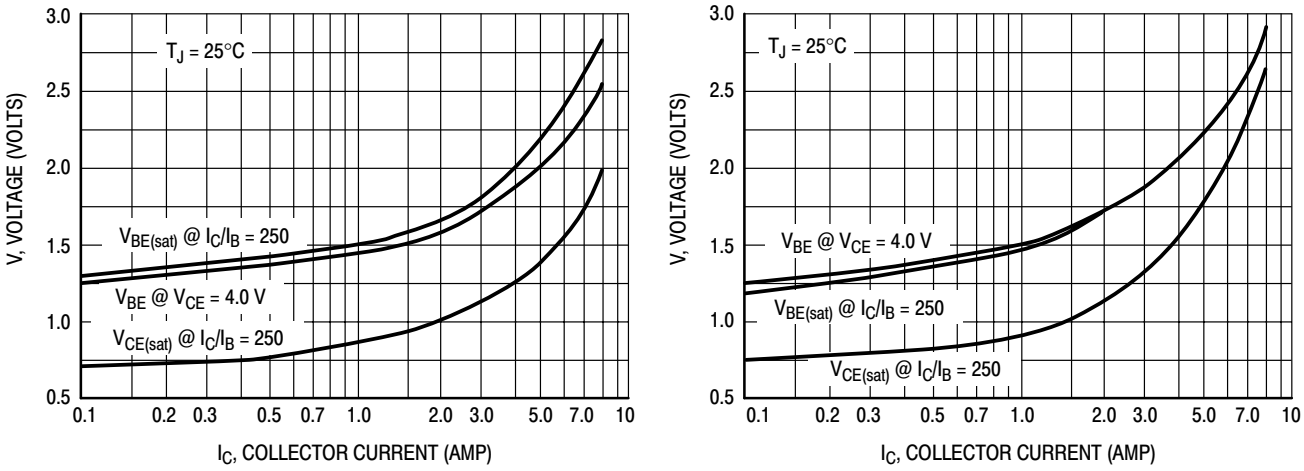


Figure 7. “On” Voltages

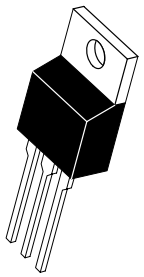
Plastic Medium-Power Complementary Silicon Transistors

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BDX53B, 54B
  = 100 Vdc (Min) — BDX53C, 54C
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
BDX53B
BDX53C
PNP
BDX54B
BDX54C

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
65 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 12		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	70	°C/W

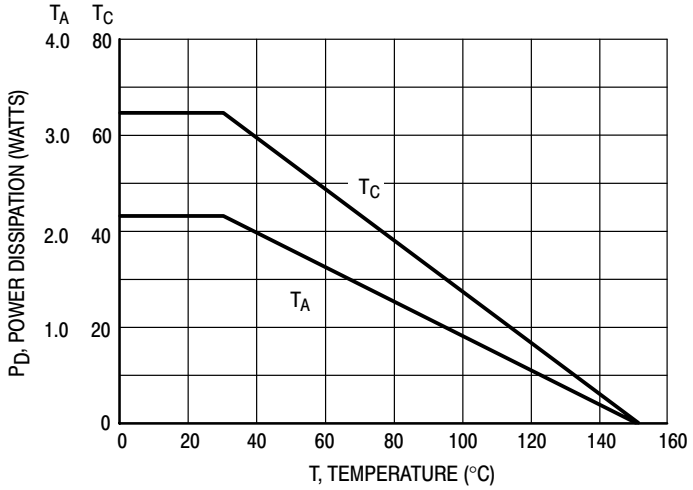


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	BDX53B, BDX54B		80	—	
	BDX53C, BDX54C		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	BDX53B, BDX54B		—	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	BDX53C, BDX54C		—	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 80 Vdc, I_E = 0)	BDX53B, BDX54B		—	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	BDX53C, BDX54C		—	0.2	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}	750	—	—
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			—	2.0	
			—	4.0	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$	—	2.5	Vdc
(I_C = 3.0 Adc, I_C = 12 mA)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	4.0	—	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53B, 53C		—	300	
	BDX54B, 54C		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

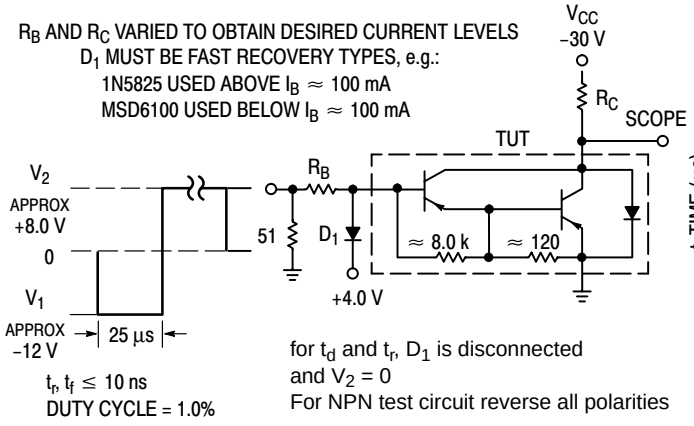


Figure 2. Switching Time Test Circuit

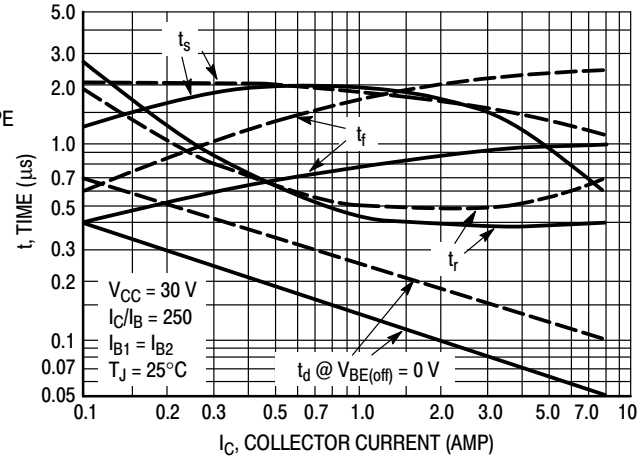


Figure 3. Switching Times

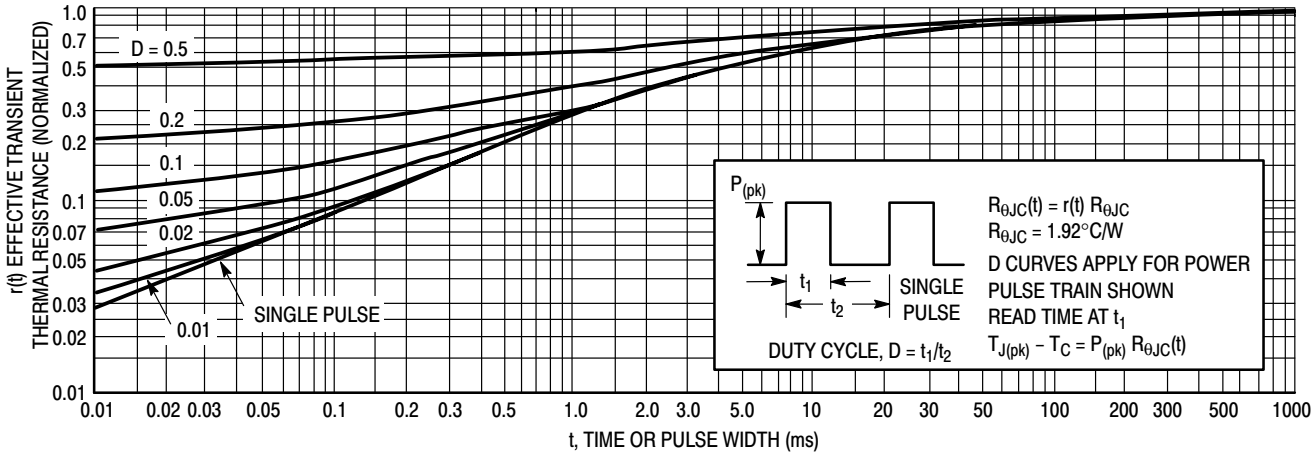


Figure 4. Thermal Response

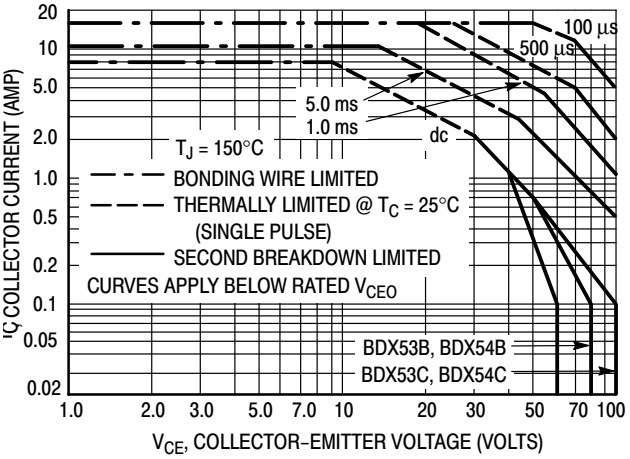


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

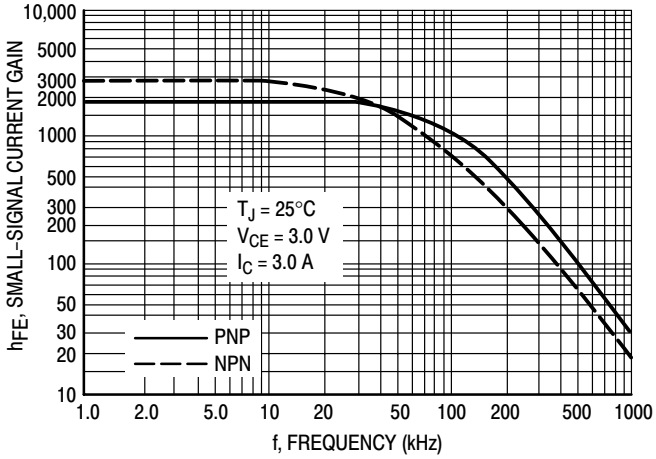


Figure 6. Small-Signal Current Gain

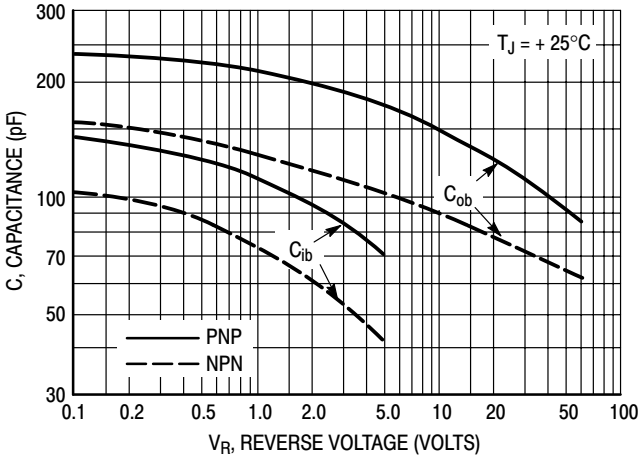


Figure 7. Capacitance

NPN
BDX53B, 53C

PNP
BDX54B, 54C

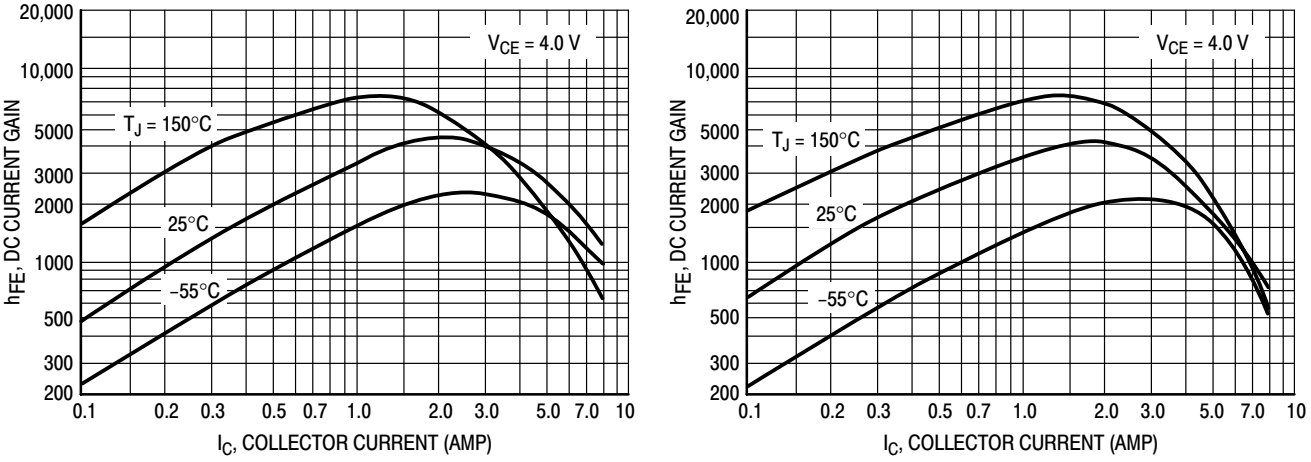


Figure 8. DC Current Gain

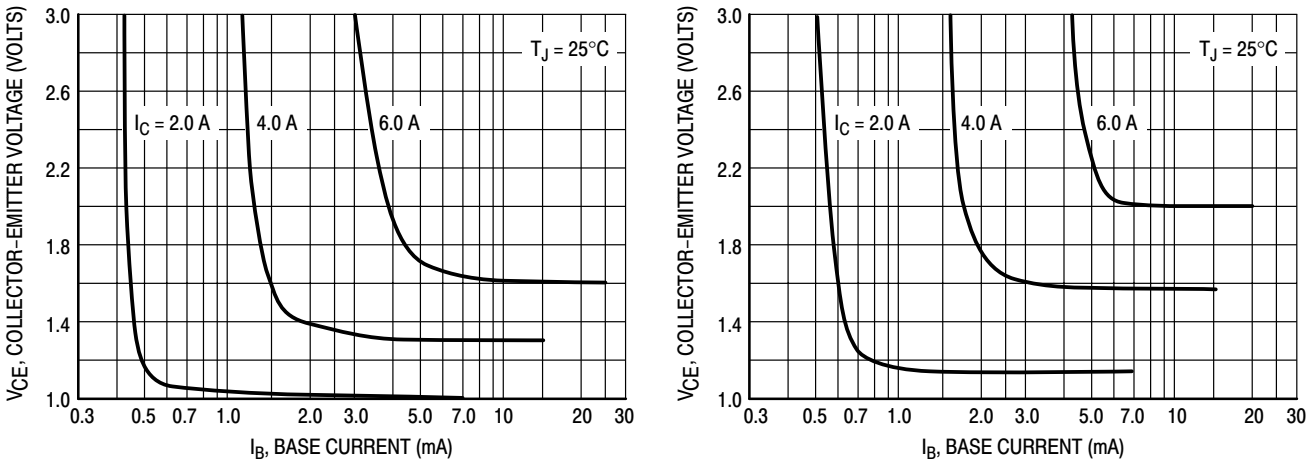


Figure 9. Collector Saturation Region

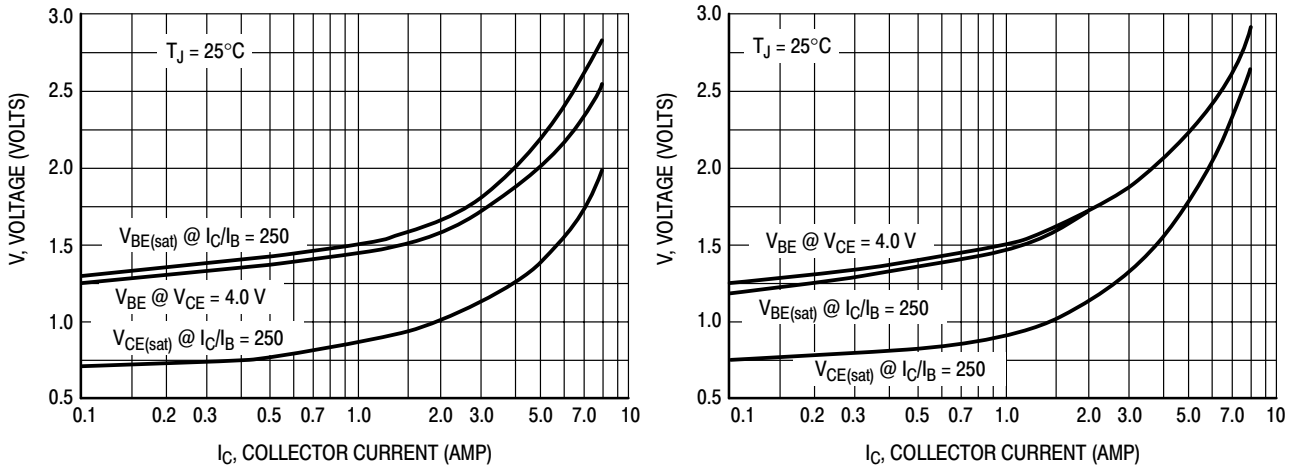


Figure 10. “On” Voltages

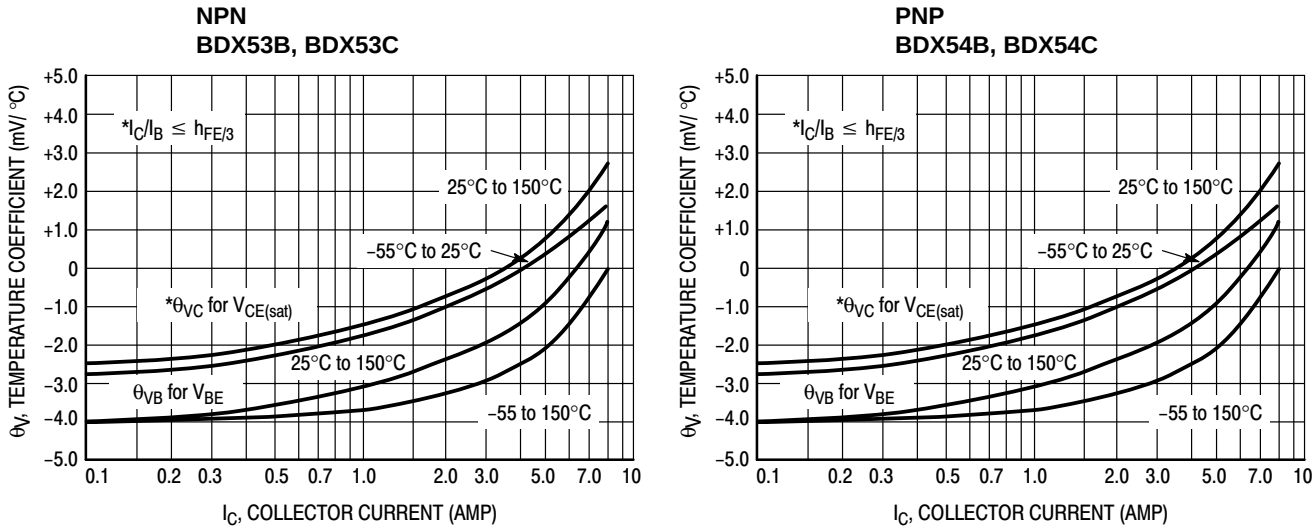


Figure 11. Temperature Coefficients

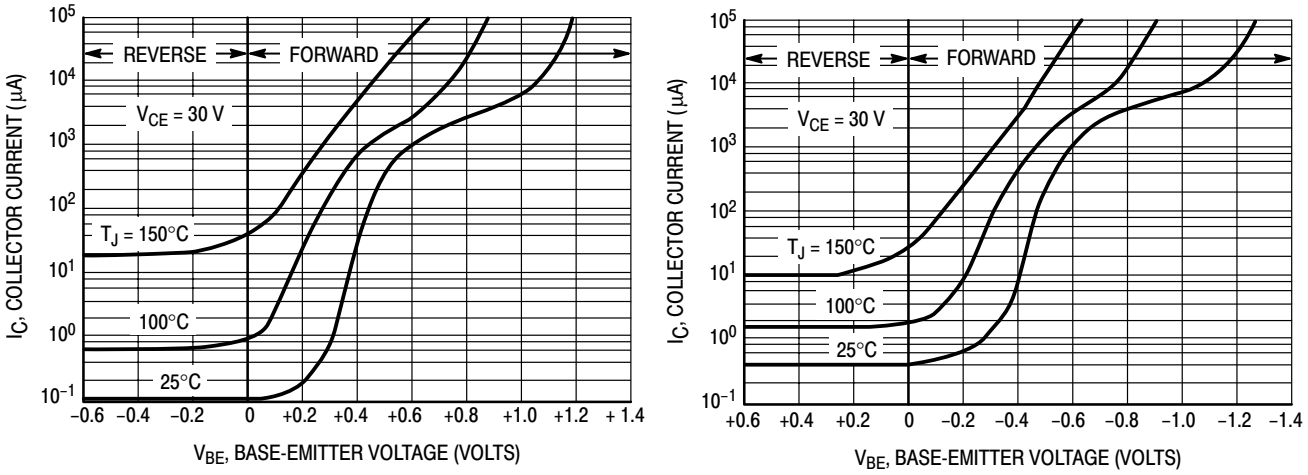


Figure 12. Collector Cut–Off Region

Figure 13. Darlington Schematic

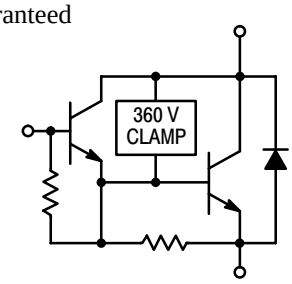
BU323Z

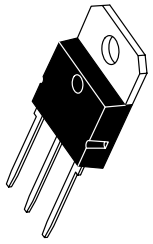
NPN Silicon Power Darlington
High Voltage Autoprotected

AUTOPROTECTED DARLINGTON 10 AMPERES 360–450 VOLTS CLAMP 150 WATTS

The BU323Z is a planar, monolithic, high–voltage power Darlington with a built–in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control, and exhibit the following main features:

- Integrated High–Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the –40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times
- Offered in Plastic SOT–93/TO–218 Type or TO–220 Packages





CASE 340D–02
SOT–93/TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector–Emitter Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak	I_B I_{BM}	3.0 6.0	Adc
Total Power Dissipation (T_C = 25°C) Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

March, 2001 – Rev. 10
Publication Order Number:
BU323Z/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Clamping Voltage (I_C = 7.0 A) (T_C = –40°C to +125°C)	V_{CLAMP}	350	—	450	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 200 V, I_B = 0)	I_{CEO}	—	—	100	μAdc
Emitter–Base Leakage Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	50	mAdc
ON CHARACTERISTICS (1)					
Base–Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 100 mAdc)		—	—	2.2	
(I_C = 10 Adc, I_B = 0.25 Adc)		—	—	2.5	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 7.0 Adc, I_B = 70 mAdc)		—	—	1.6	
(T_C = 125°C)		—	—	1.8	
(I_C = 8.0 Adc, I_B = 0.1 Adc)		—	—	1.8	
(T_C = 125°C)		—	—	2.1	
(I_C = 10 Adc, I_B = 0.25 Adc)		—	—	1.7	
Base–Emitter On Voltage	$V_{BE(on)}$				Vdc
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (T_C = –40°C to +125°C)		1.1	—	2.1	
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		1.3	—	2.3	
Diode Forward Voltage Drop (I_F = 10 Adc)	V_F	—	—	2.5	Vdc
DC Current Gain	h_{FE}				—
(I_C = 6.5 Adc, V_{CE} = 1.5 Vdc) (T_C = –40°C to +125°C)		150	—	—	
(I_C = 5.0 Adc, V_{CE} = 4.6 Vdc)		500	—	3400	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	—	2.0	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	200	pF
Input Capacitance (V_{EB} = 6.0 V)	C_{ib}	—	—	550	pF
CLAMPING ENERGY (see notes)					
Repetitive Non–Destructive Energy Dissipated at turn–off: (I_C = 7.0 A, L = 8.0 mH, R_{BE} = 100 Ω) (see Figures 2 and 4)	W_{CLAMP}	200	—	—	mJ

SWITCHING CHARACTERISTICS: Inductive Load (L = 10 mH)

Fall Time	(I_C = 6.5 A, I_{B1} = 45 mA, $V_{BE(off)}$ = 0, $R_{BE(off)}$ = 0, V_{CC} = 14 V, V_Z = 300 V)	t_{fi}	—	625	—	ns
Storage Time		t_{si}	—	10	30	μs
Cross–over Time		t_c	—	1.7	—	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

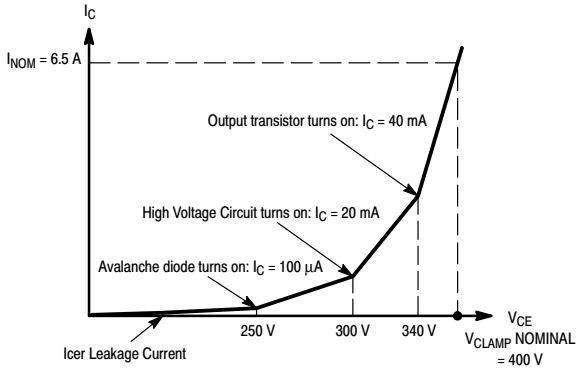


Figure 1. $I_C = f(V_{CE})$ Curve Shape

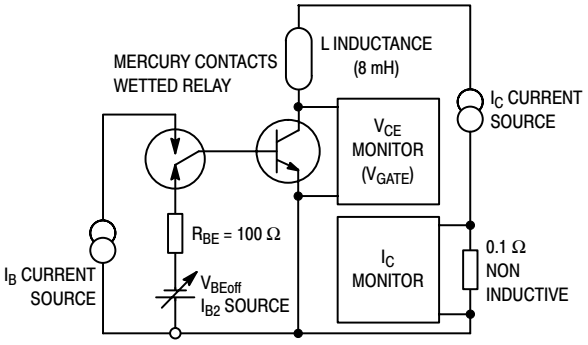


Figure 2. Basic Energy Test Circuit

By design, the BU323Z has a built–in avalanche diode and a special high voltage driving circuit. During an auto–protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in "FBSOA." Because of the built–in zener and associated network, the $I_C = f(V_{CE})$ curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1.

The bias parameters, V_{CLAMP}, I_{B1}, $V_{BE(off)}$, I_{B2}, I_C, and the inductance, are applied according to the Device Under Test (DUT) specifications. V_{CE} and I_C are monitored by the test system while making sure the load line remains within the limits as described in Figure 4.

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2 and 4, to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:
$I_{C(peak)}$ = 7.0 A, I_CH = 5.0 A, I_CL = 100 mA, I_B = 100 mA, R_{BE} = 100 Ω, V_{gate} = 280 V, L = 8.0 mH

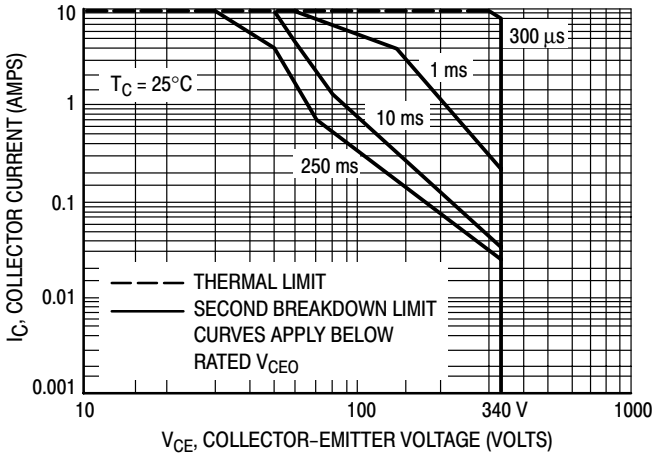
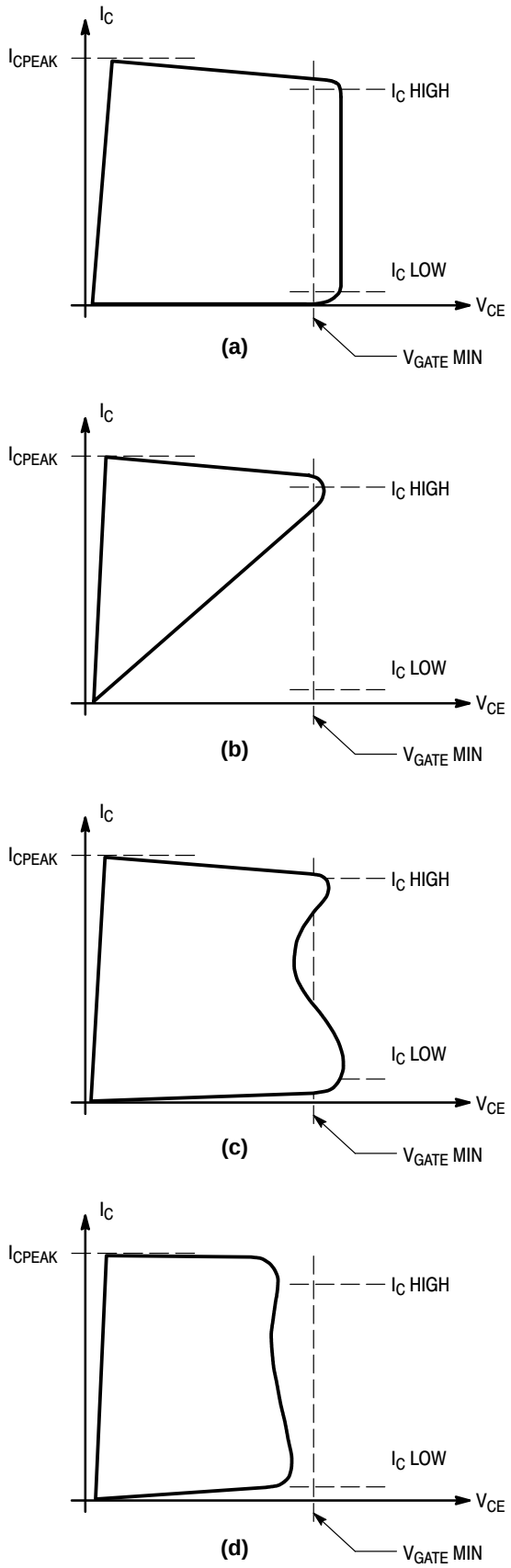


Figure 3. Forward Bias Safe Operating Area



The shaded area represents the amount of energy the device can sustain, under given DC biases ($I_C/I_B/V_{BE(off)}/R_{BE}$), without an external clamp; see the test schematic diagram, Figure 2.

The transistor PASSES the Energy test if, for the inductive load and $I_{CPEAK}/I_B/V_{BE(off)}$ biases, the V_{CE} remains outside the shaded area and greater than the V_{GATE} minimum limit, Figure 4a.

The transistor FAILS if the V_{CE} is less than the V_{GATE} (minimum limit) at any point along the V_{CE}/I_C curve as shown on Figures 4b, and 4c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.

The transistor FAILS if its Collector/Emitter breakdown voltage is less than the V_{GATE} value, Figure 4d.

Figure 4. Energy Test Criteria for BU323Z

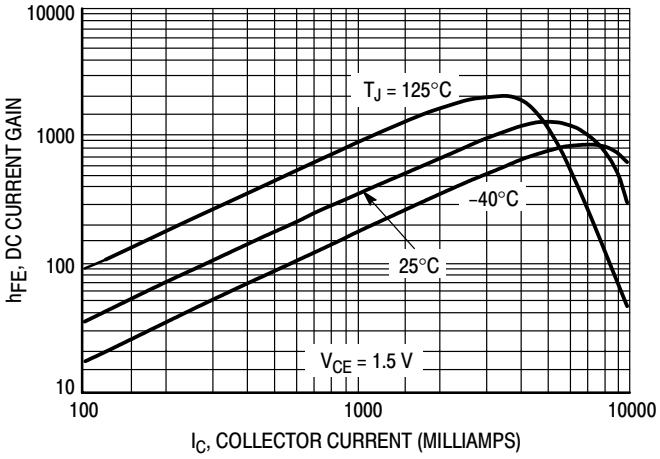


Figure 5. DC Current Gain

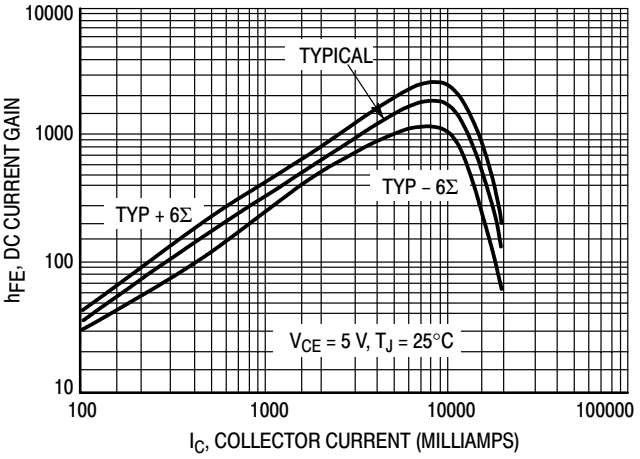


Figure 6. DC Current Gain

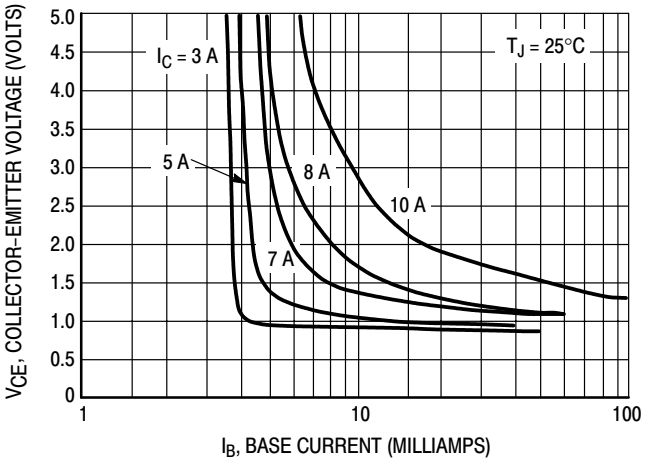


Figure 7. Collector Saturation Region

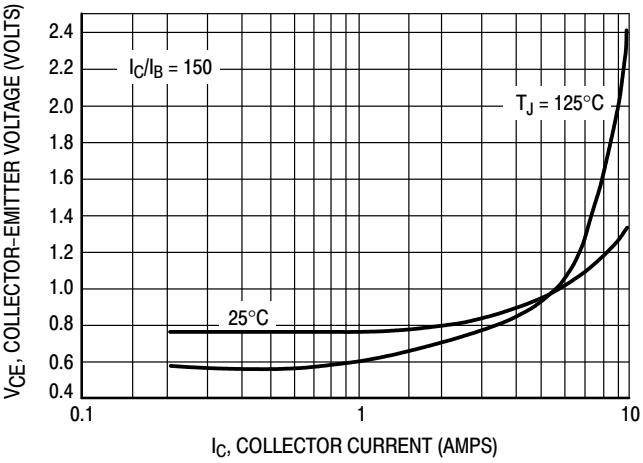


Figure 8. Collector−Emitter Saturation Voltage

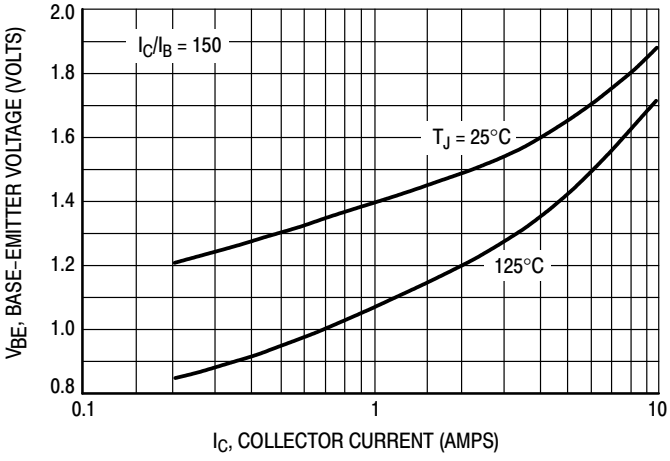


Figure 9. Base−Emitter Saturation Voltage

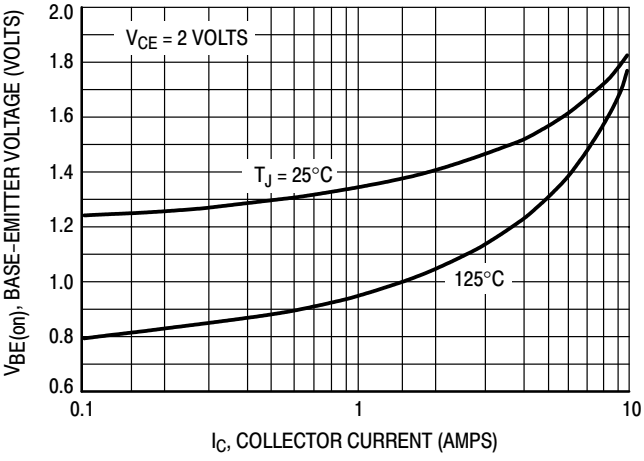


Figure 10. Base−Emitter “ON” Voltages

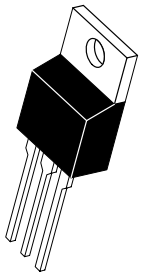
BU406
BU407

NPN Power Transistors

These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed: t_f = 750 ns (max)
- Low Saturation Voltage: $V_{CE(sat)}$ = 1 V (max) @ 5 A
- Packaged in Compact JEDEC TO–220AB

7 AMPERES
NPN SILICON
POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BU406	BU407	Unit
Collector–Emitter Voltage	V_{CEO}	200	150	Vdc
Collector–Emitter Voltage	V_{CEV}	400	330	Vdc
Collector–Base Voltage	V_{CBO}	400	330	Vdc
Emitter Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous Peak Repetitive Peak (10 ms)	I_C	7 10 15		Adc
Base Current	I_B	4		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

March, 2001 – Rev. 4
Publication Order Number:
BU406/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage(1) (I_C = 100 mAdc, I_B = 0)	BU406 BU407	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0, T_C = 150°C)		I_{CES}	 — — —	 — — —	 5 0.1 1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	BU406, BU407	I_{EBO}	—	—	1	mAdc
ON CHARACTERISTICS (1)						
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	—	—	1.2	Vdc
Forward Diode Voltage (I_{EC} = 5 Adc) “D” only		V_{EC}	—	—	2	Volts
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 20 MHz)		f_T	10	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS						
Inductive Load Crossover Time (V_{CC} = 40 Vdc, I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc, L = 150 μH)		t_c	—	—	0.75	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

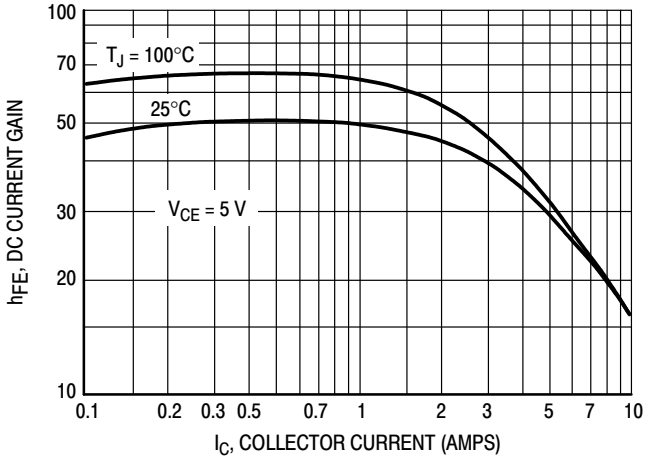


Figure 11. DC Current Gain

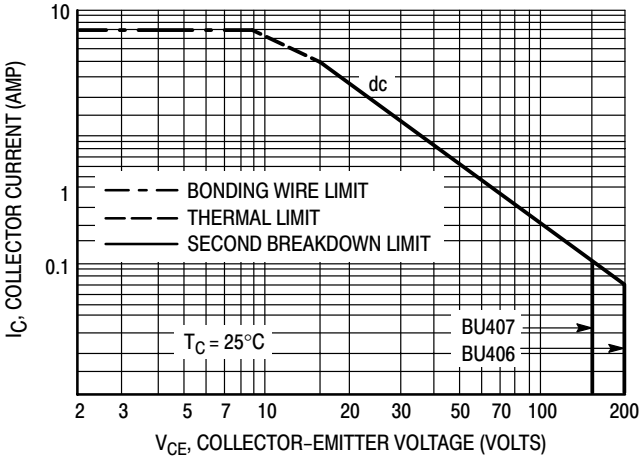
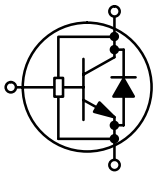


Figure 12. Maximum Rated Forward Bias Safe Operating Area

BUD44D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

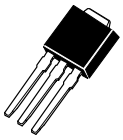
POWER TRANSISTORS
2 AMPERES
700 VOLTS
25 WATTS



The BUD44D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

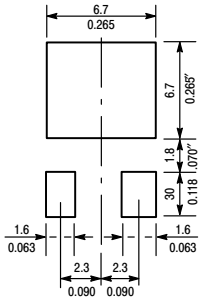
- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- Six Sigma Process Providing Tight and Reproductible Parameter Spreads
- It's characteristics make it also suitable for PFC application.



CASE 369–07

CASE 369A–13

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2 5	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	1 2	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	25 0.2	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 5 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	470		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	920		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}			50 500	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C	I_{CES}			50 500 100	μAdc
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.78 0.65	0.9 0.8	Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.87 0.76	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 20 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.45 0.67	0.65 1	Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.25 0.27	0.4 0.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.28 0.35	0.5 0.6	
DC Current Gain (I_C = 0.4 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	20 18	32 26		—
(I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 7	14 9.5		
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		8	11		
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 0.2 Adc)	@ T_C = 25°C	V_{EC}		0.8	1	V
(I_{EC} = 0.2 Adc)	@ T_C = 125°C			0.6		
(I_{EC} = 0.4 Adc)	@ T_C = 25°C			0.9	1.2	
(I_{EC} = 1 Adc)	@ T_C = 25°C			1.1	1.5	
Forward Recovery Time (see Figure 22 bis) (I_F = 0.2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C	T_{fr}		415		ns
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			390		
(I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			340		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C	$V_{CE(dsat)}$		3.3		V
			@ T_C = 125°C			6.8		
		@ 3 µs	@ T_C = 25°C			0.5		
			@ T_C = 125°C			1.3		
	I_C = 1 A, I_{B1} = 0.2 A, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C			4.4		
			@ T_C = 125°C			12.8		
		@ 3 µs	@ T_C = 25°C			0.5		
			@ T_C = 125°C			1.8		
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)				f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)				C_{ob}		50	75	pF
Input Capacitance (V_{EB} = 8 Vdc)				C_{ib}		240	500	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 µs)								
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc, V_{CC} = 300 Vdc		@ T_C = 25°C	t_{on}		90	150	ns
			@ T_C = 125°C			105		
Turn–off Time			@ T_C = 25°C	t_{off}		1.1	1.25	µs
			@ T_C = 125°C			1.5		
Turn–on Time	I_C = 0.5 Adc, I_{B1} = 50 mAdc, I_{B2} = 250 mAdc, V_{CC} = 300 Vdc		@ T_C = 25°C	t_{on}	400		600	ns
			@ T_C = 125°C			600		
Turn–off Time			@ T_C = 25°C	t_{off}	750		1000	ns
			@ T_C = 125°C			1300		

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		110 105	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.55 0.7	0.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		85 80	150	ns
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		100 90	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.05 1.45	1.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		100 100	175	ns
Fall Time	I_C = 0.8 Adc I_{B1} = 160 mAdc I_{B2} = 160 mAdc	@ T_C = 25°C @ T_C = 125°C	t_f		110 180	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.05	 2.8	2.35	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		180 400	300	ns
Fall Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 40 mAdc	@ T_C = 25°C @ T_C = 125°C	t_f		150 175	225	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	1.65	 2.2	1.95	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 330	250	ns

TYPICAL STATIC CHARACTERISTICS

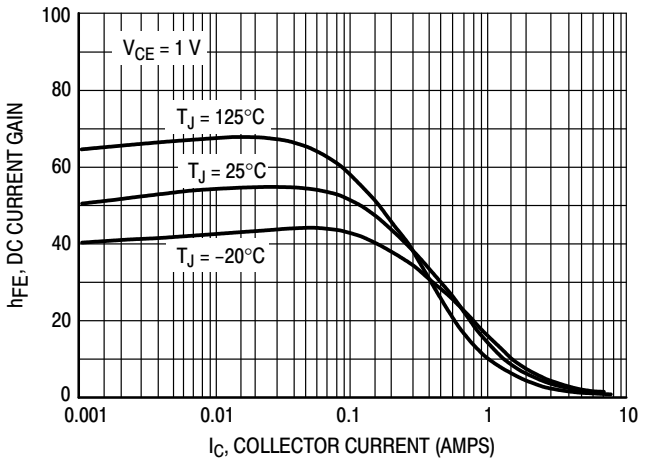


Figure 13. DC Current Gain @ 1 Volt

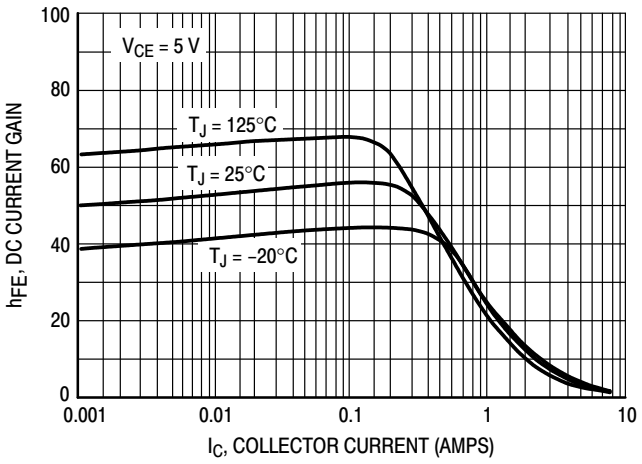


Figure 14. DC Current Gain @ 5 Volt

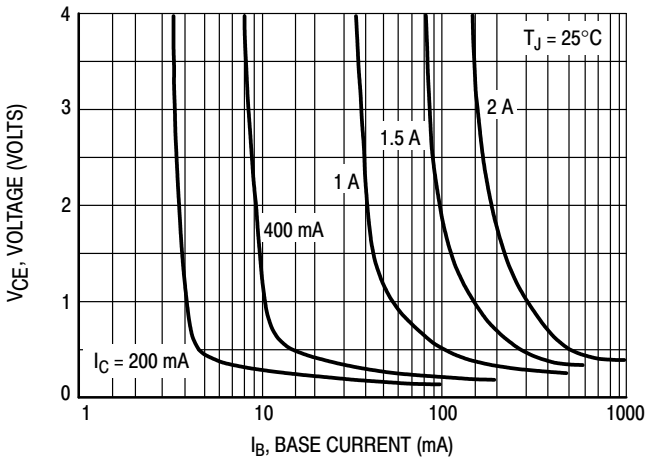


Figure 15. Collector Saturation Region

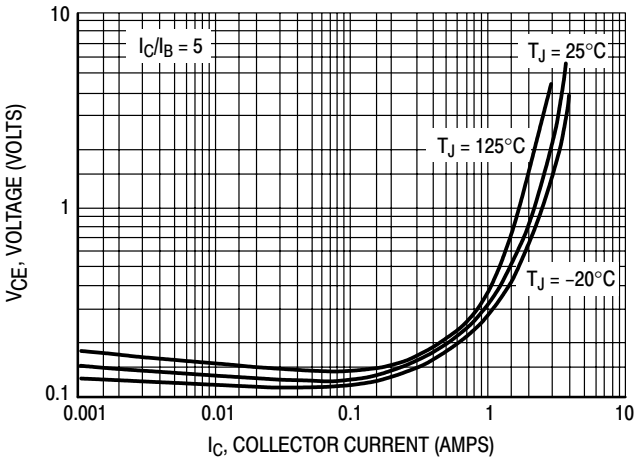


Figure 16. Collector–Emitter Saturation Voltage

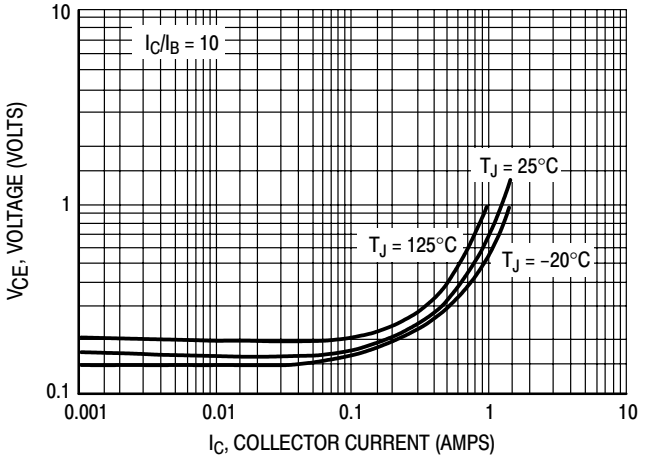


Figure 17. Collector–Emitter Saturation Voltage

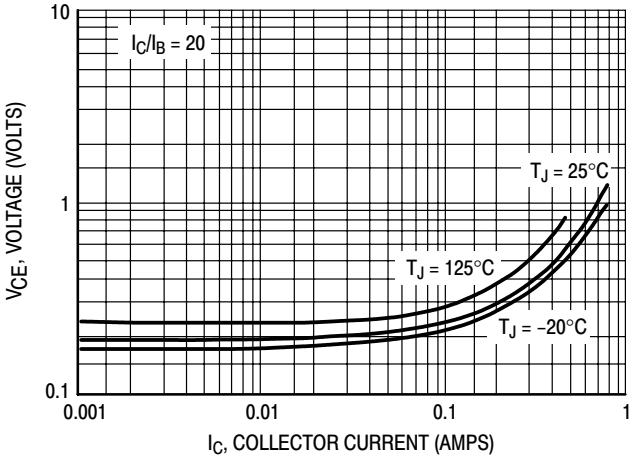


Figure 18. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

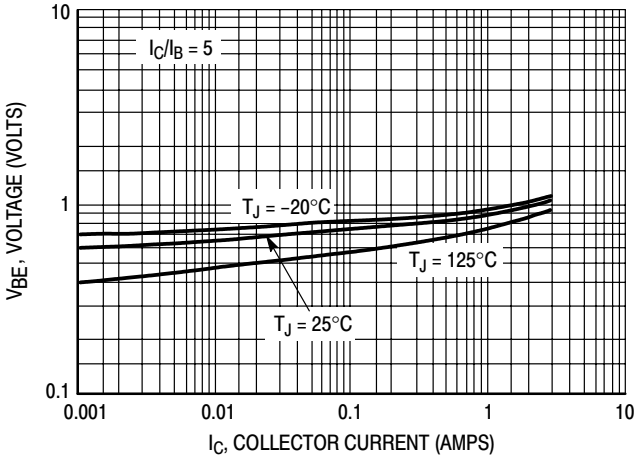


Figure 7A. Base–Emitter Saturation Region

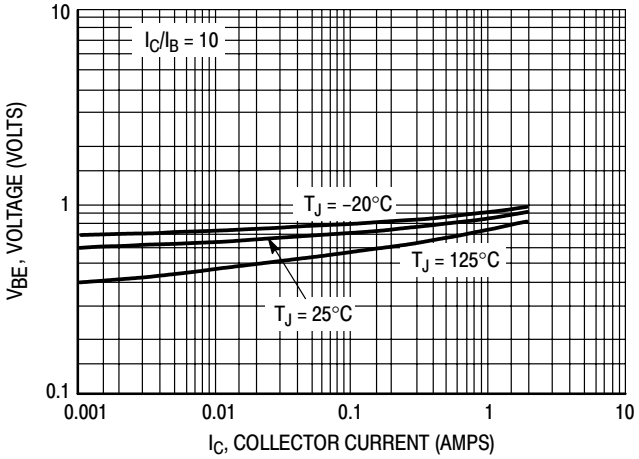


Figure 7B. Base–Emitter Saturation Region

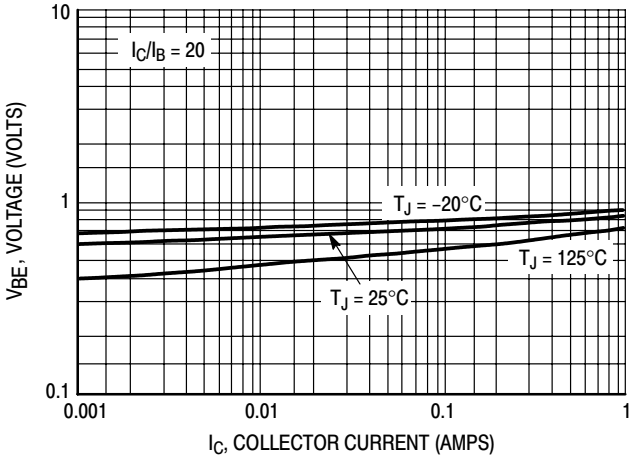


Figure 7C. Base–Emitter Saturation Region

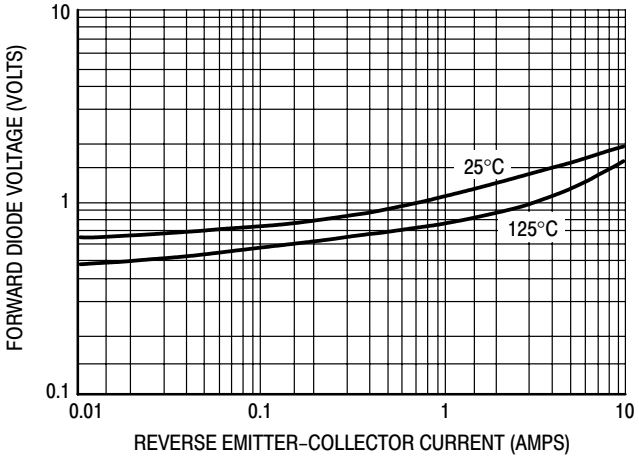


Figure 8. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

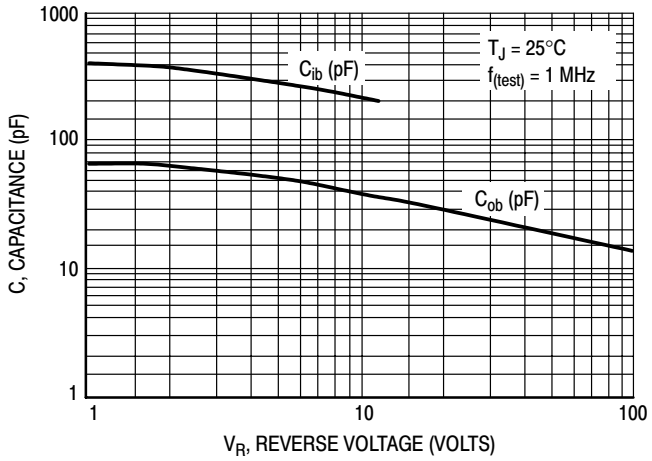


Figure 9. Capacitance

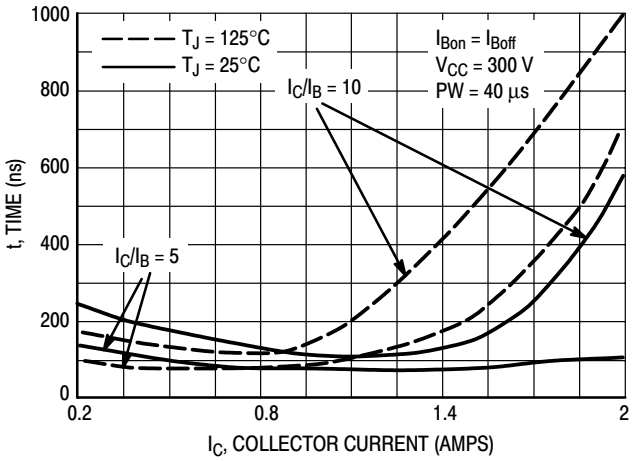


Figure 10. Resistive Switch Time, t_{on}

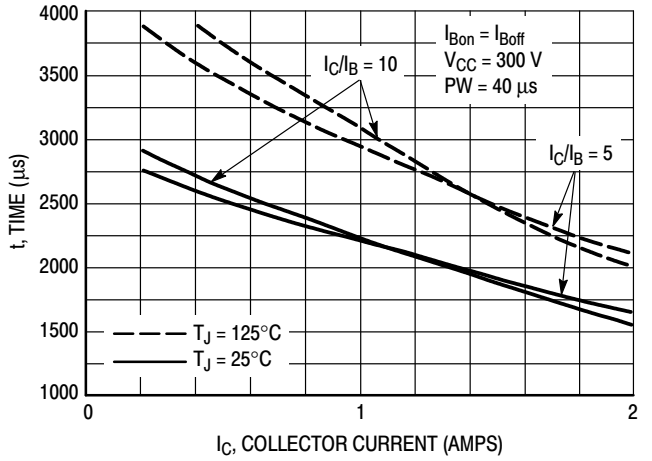


Figure 11. Resistive Switch Time, t_{off}

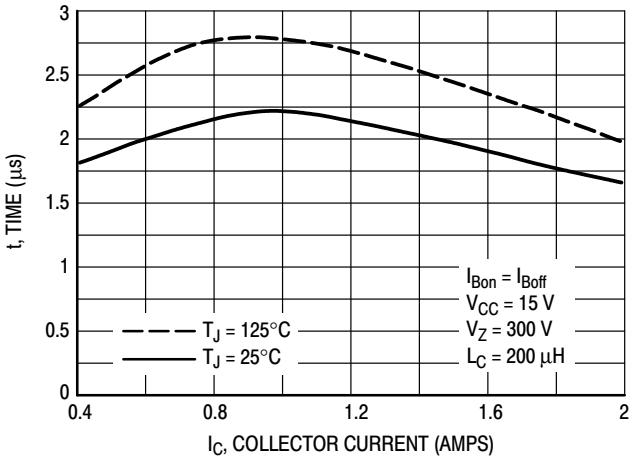


Figure 12. Inductive Storage Time, t_{si} @ I_C/I_B = 5

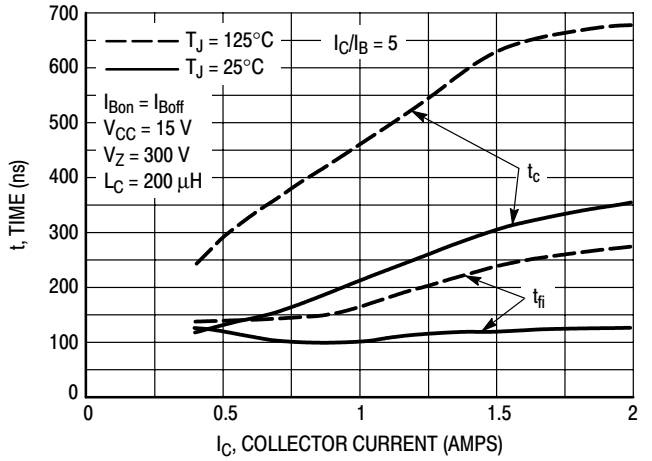


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

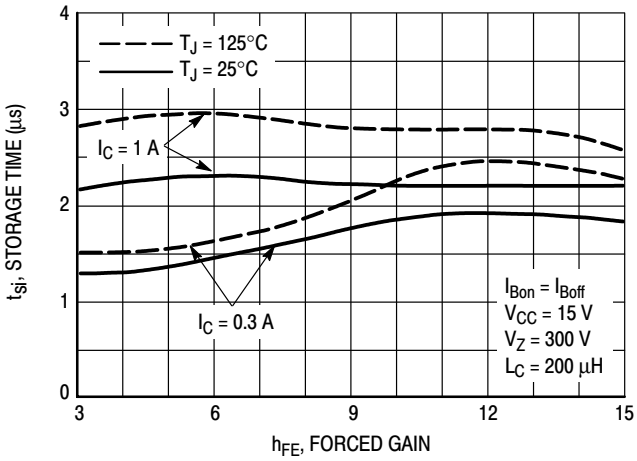


Figure 14. Inductive Storage Time

TYPICAL SWITCHING CHARACTERISTICS

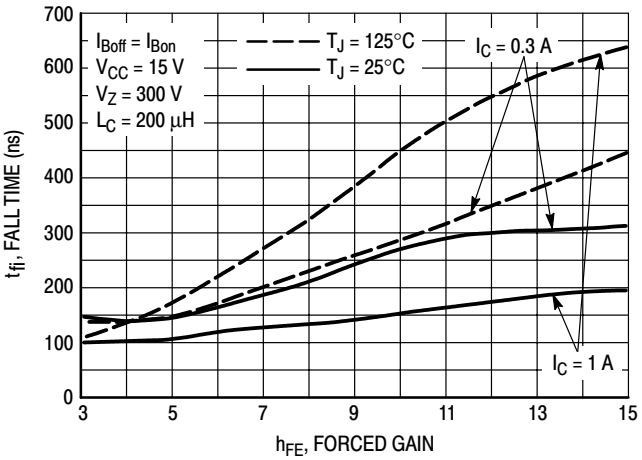


Figure 15. Inductive Fall Time

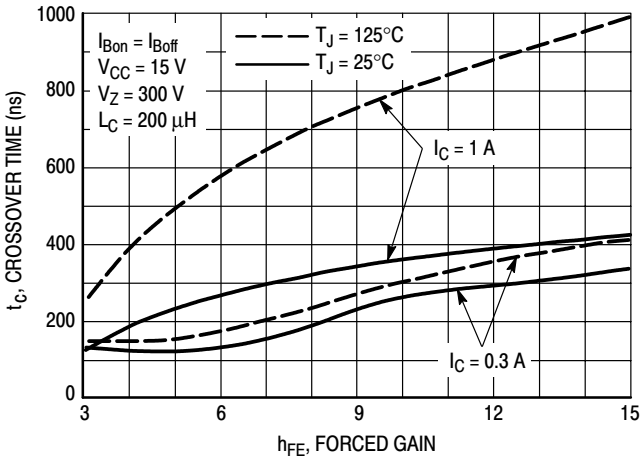


Figure 16. Inductive Crossover Time

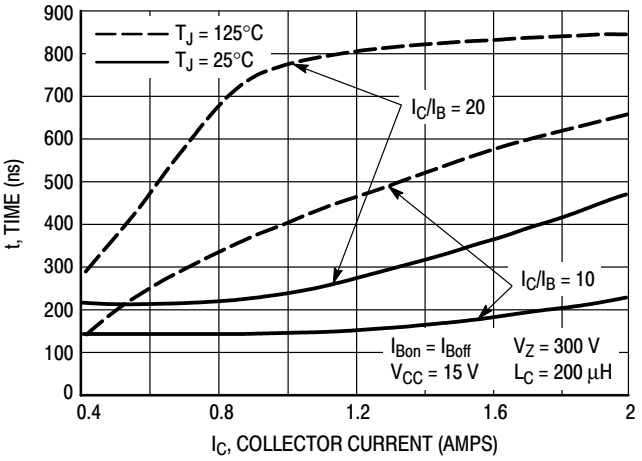


Figure 17. Inductive Switching, t_{fi}

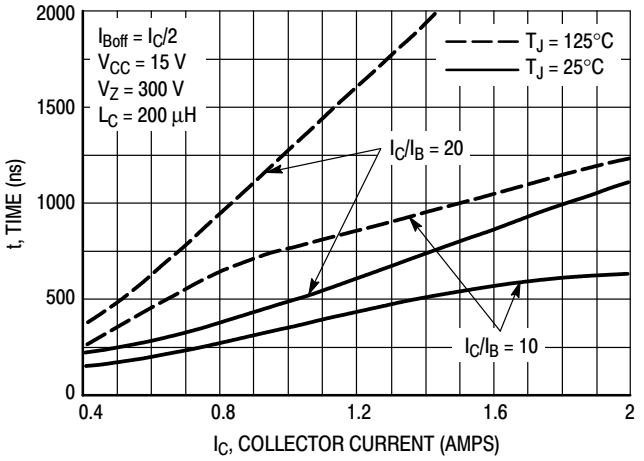


Figure 18. Inductive Switching, t_c

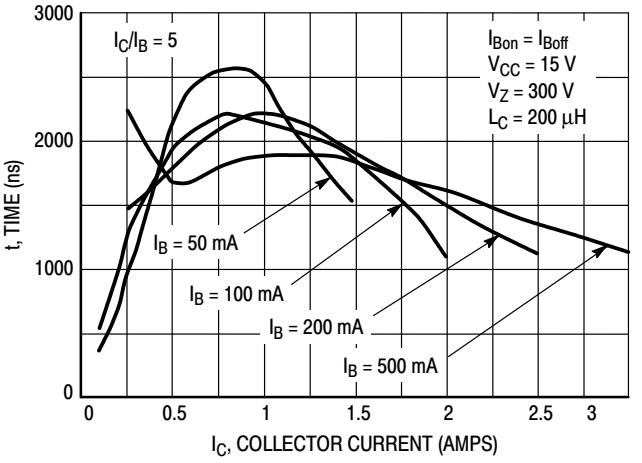


Figure 19. Inductive Storage Time, t_{si}

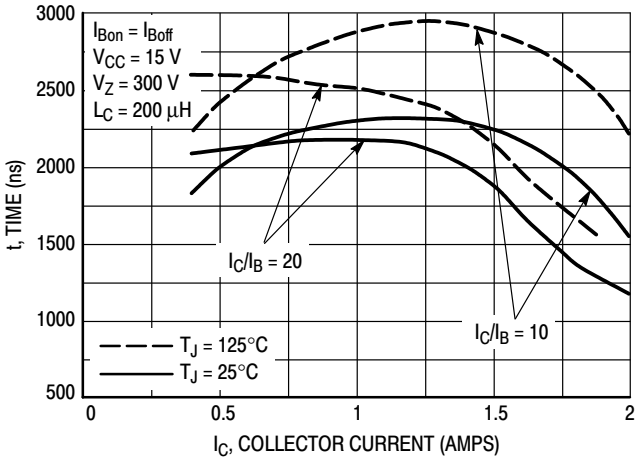


Figure 20. Inductive Storage Time, t_{si}

TYPICAL SWITCHING CHARACTERISTICS

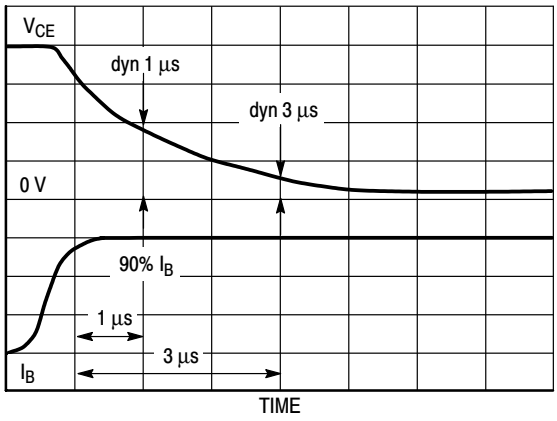


Figure 21. Dynamic Saturation Voltage Measurements

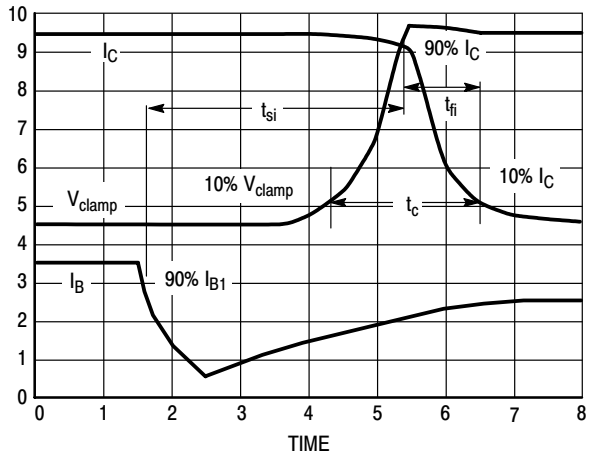


Figure 22. Inductive Switching Measurements

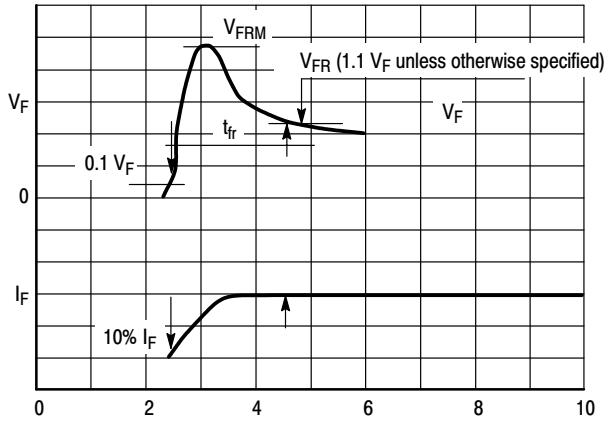
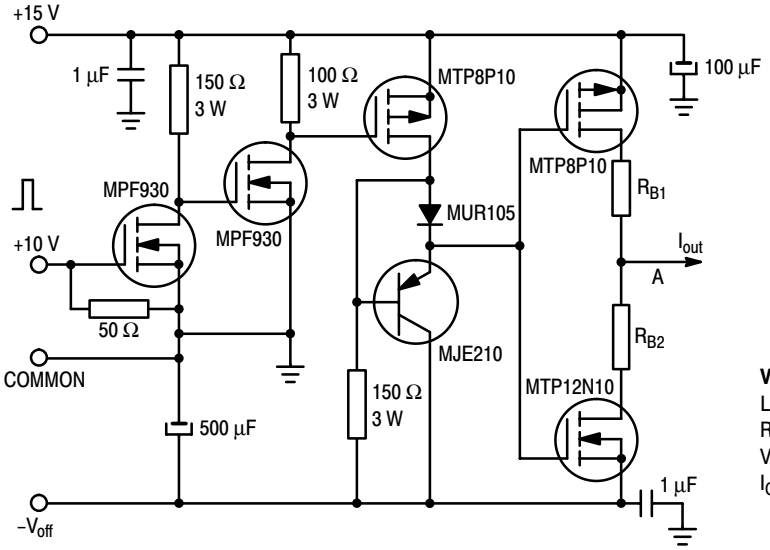
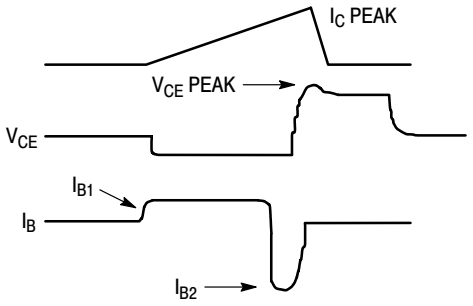


Figure 22 bis. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL STATIC CHARACTERISTICS

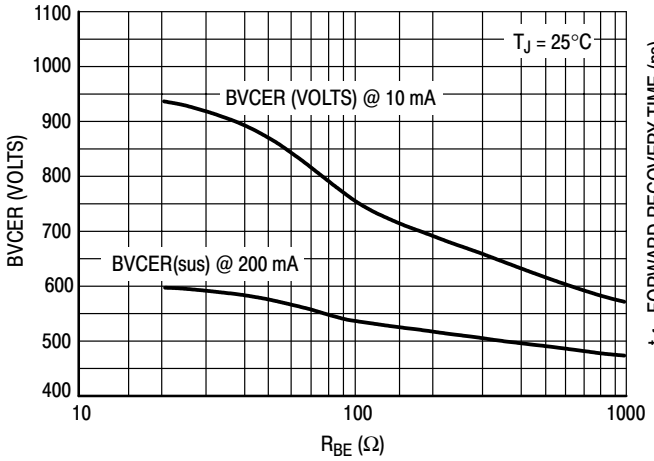


Figure 23. BVCER

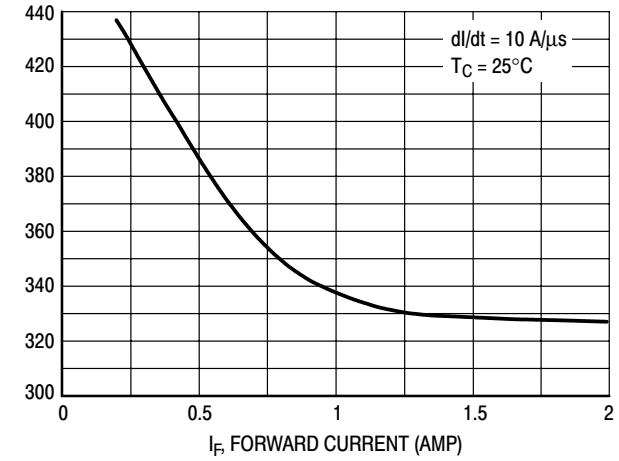


Figure 24. Forward Recovery Time t_{fr}

BUH100

SWITCHMODE™ NPN Silicon Planar Power Transistor

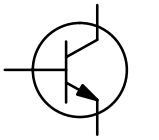
POWER TRANSISTOR
10 AMPERES
700 VOLTS
100 WATTS

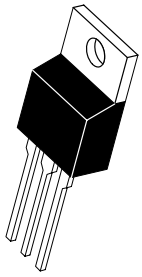
The BUH100 has an application specific state–of–art die designed for use in 100 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start–up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions





CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 10	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	100 0.8	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

March, 2001 – Rev. 2
Publication Order Number:
BUH100/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	460		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	860		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C	$V_{BE(sat)}$		1	1.1	Vdc
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.37 0.37	0.6 0.6	Vdc
(I_C = 7 Adc, I_B = 1.5 Adc)	@ T_C = 25°C @ T_C = 125°C			0.5 0.6	0.75 1.5	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 16	24 28		—
(I_C = 5 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 10	15 14.5		—
(I_C = 7 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		8 7	12 10.5		—
(I_C = 10 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	9.5 8		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1} (See Figure 19)	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V; @ T_C = 25°C	$V_{CE(dsat)}$		1.1		V
	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V; @ T_C = 125°C			2.1		V
	I_C = 7.5 Adc, I_{B1} = 1.5 Adc, V_{CC} = 300 V; @ T_C = 25°C			1.7		V
	I_C = 7.5 Adc, I_{B1} = 1.5 Adc, V_{CC} = 300 V; @ T_C = 125°C			5		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		100	150	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		1300	1750	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		130 140	200	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		6.8 8.5	8	μs
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		140 150	200	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.4 4.3	4	μs
Turn–on Time	I_C = 5 Adc, I_{B1} = 1 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		250 800	500	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.9 3.6	3.5	μs
Turn–on Time	I_C = 7.5 Adc, I_{B1} = 1.5 Adc I_{B2} = 1.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		500 900	700	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.1 2.5	2.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		150 180	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		5.1 5.8	6	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		230 300	325	ns
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		150 170	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.5 2.8	3	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		260 300	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 1 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		100 140	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.9 4.6	3.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		220 450	300	ns
Fall Time	I_C = 7.5 Adc I_{B1} = 1.5 Adc I_{B2} = 1.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		100 150	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2 2.5	2.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

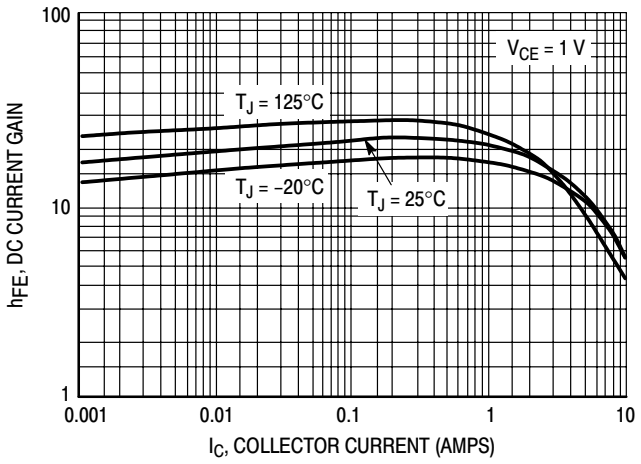


Figure 19. DC Current Gain @ 1 Volt

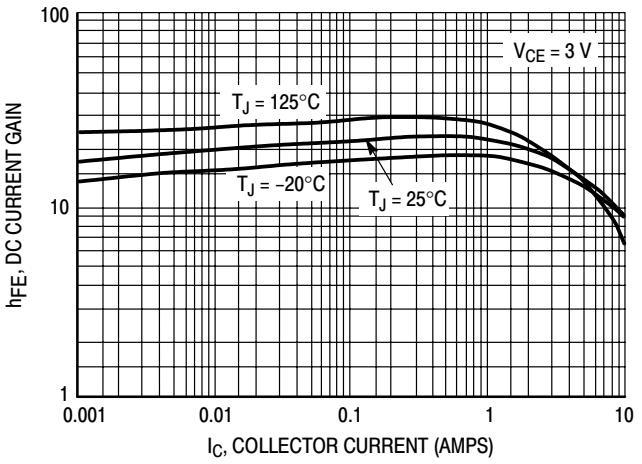


Figure 20. DC Current Gain @ 3 Volt

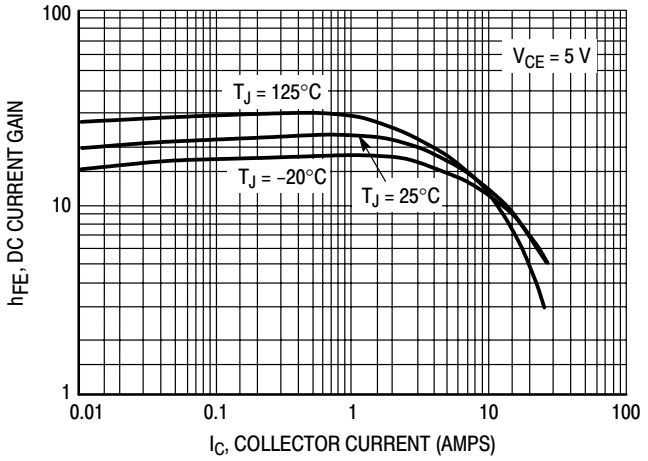


Figure 21. DC Current Gain @ 5 Volt

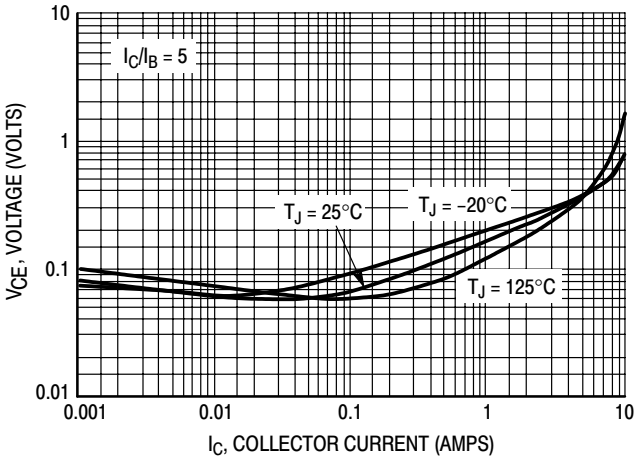


Figure 22. Collector–Emitter Saturation Voltage

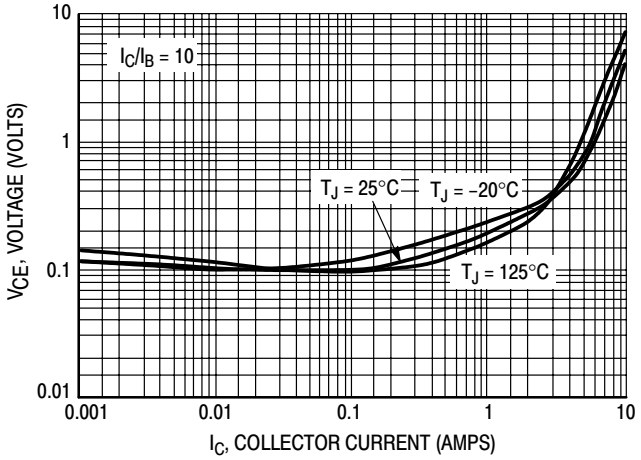


Figure 23. Collector–Emitter Saturation Voltage

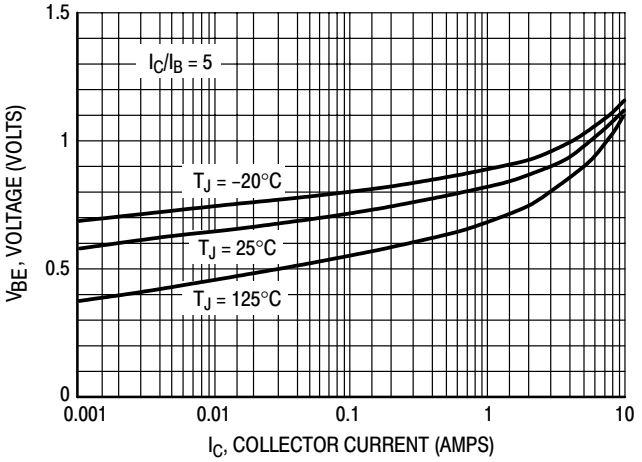


Figure 24. Base–Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

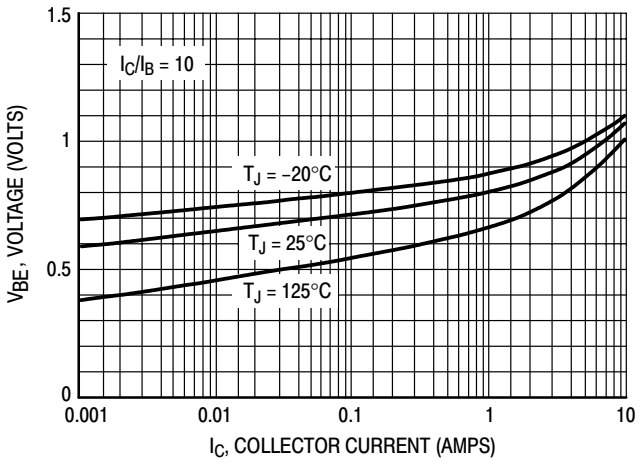


Figure 25. Base−Emitter Saturation Region

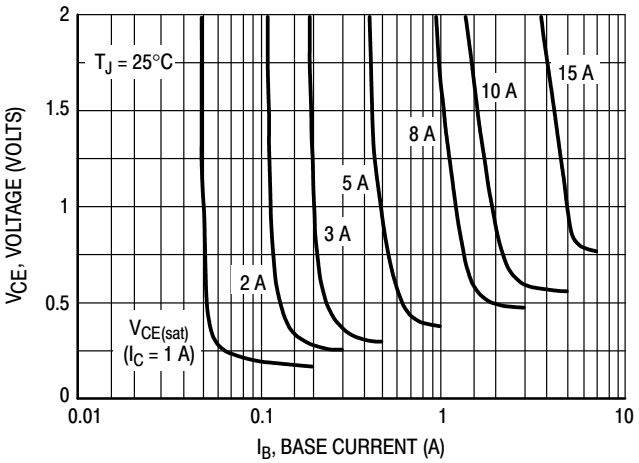


Figure 26. Collector Saturation Region

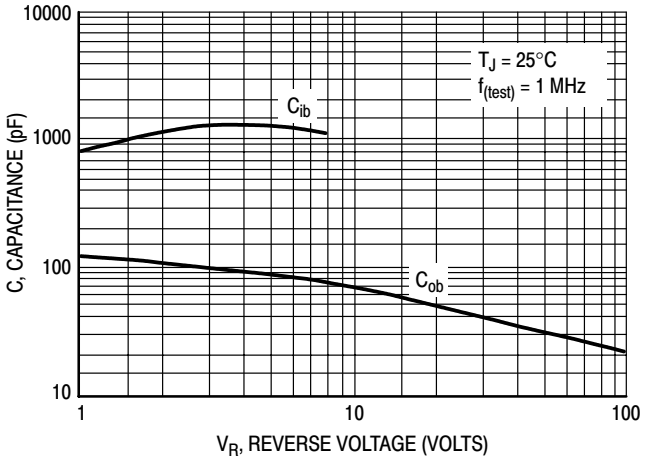


Figure 27. Capacitance

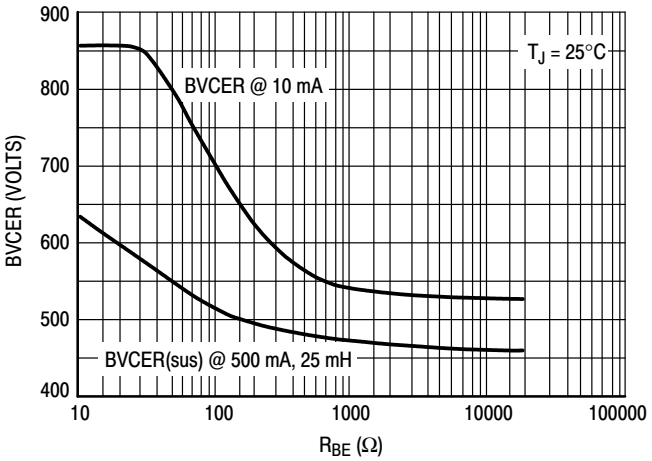


Figure 28. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

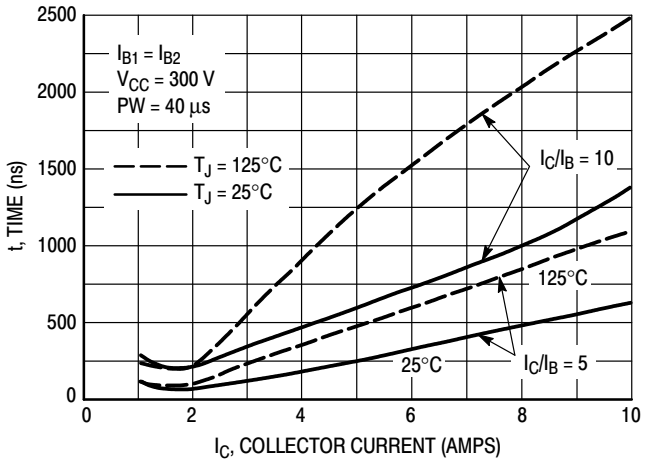


Figure 29. Resistive Switching Time, t_{on}

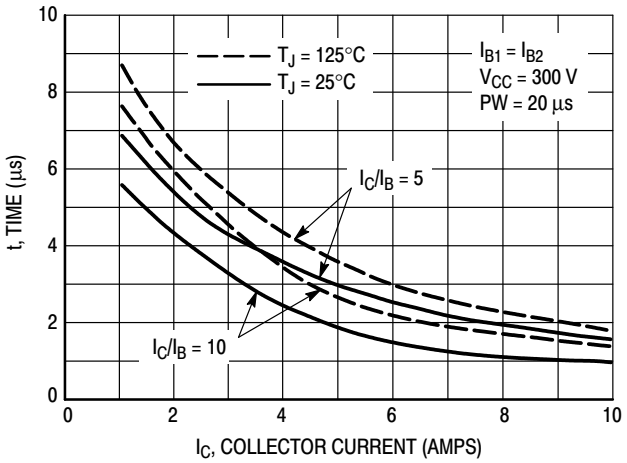


Figure 30. Resistive Switch Time, t_{off}

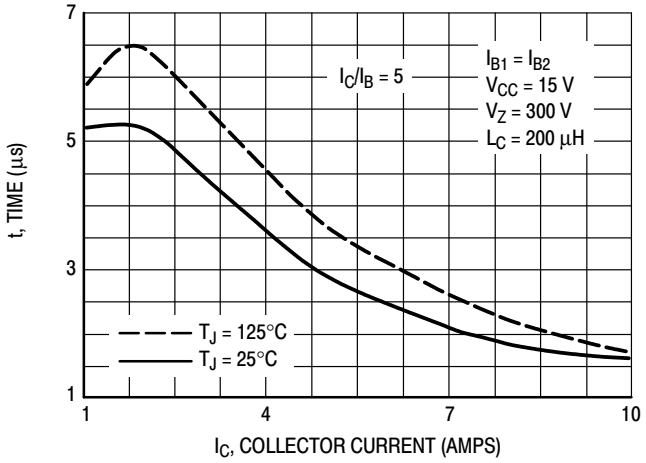


Figure 31. Inductive Storage Time, t_{si}

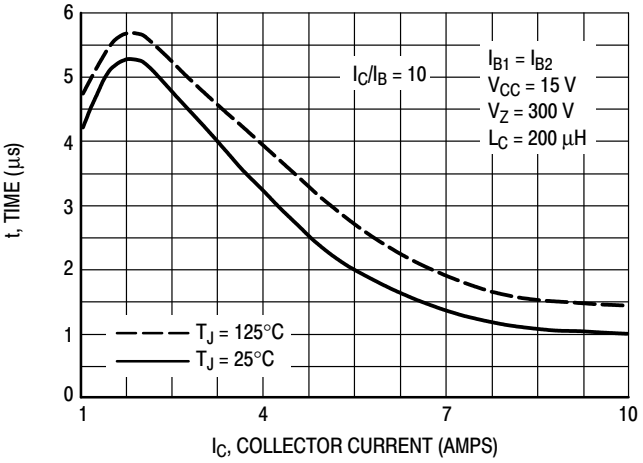


Figure 13 Bis. Inductive Storage Time, t_{si}

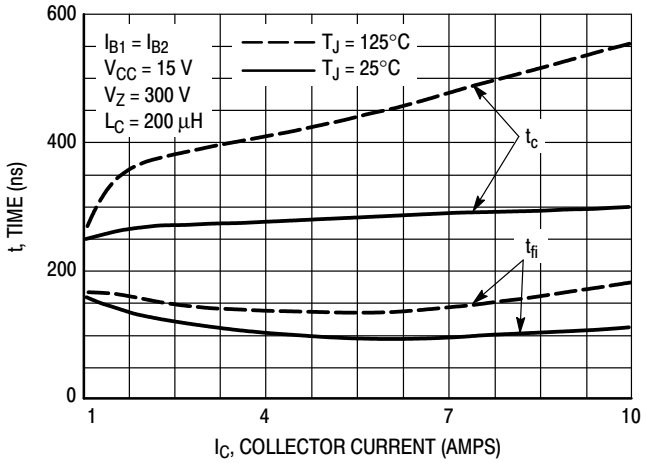


Figure 32. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

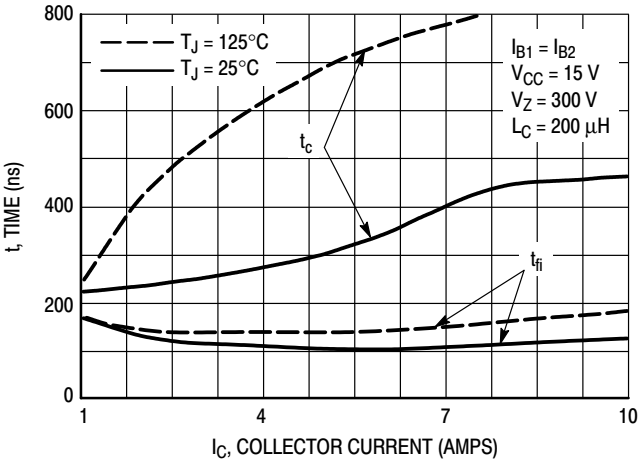


Figure 33. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

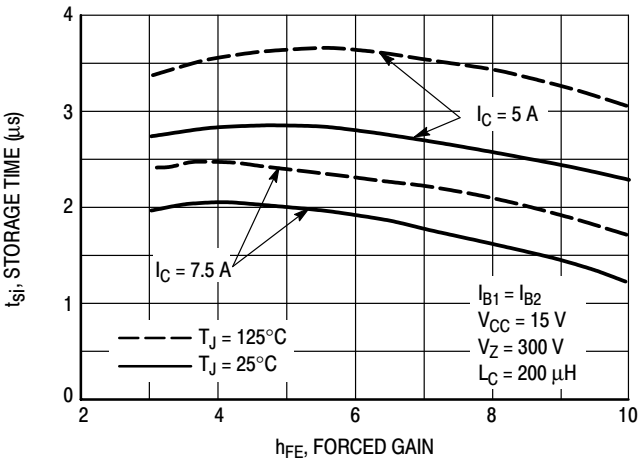


Figure 34. Inductive Storage Time

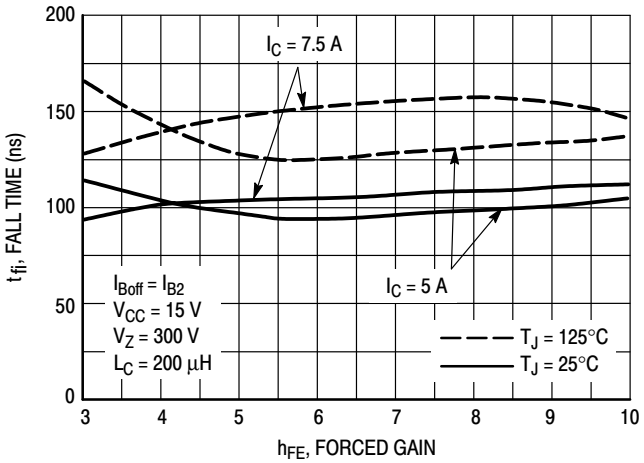


Figure 35. Inductive Fall Time

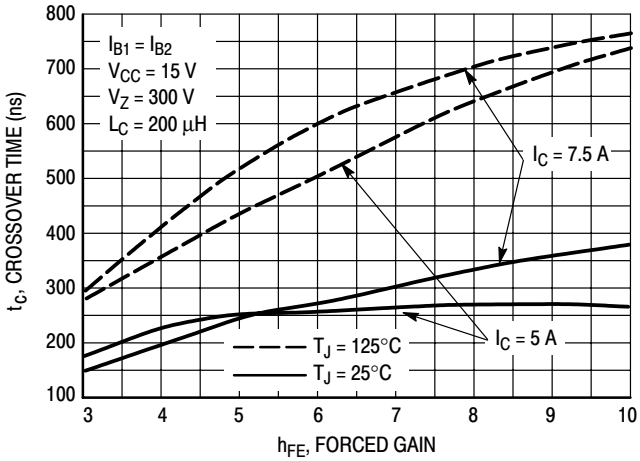


Figure 36. Inductive Crossover Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

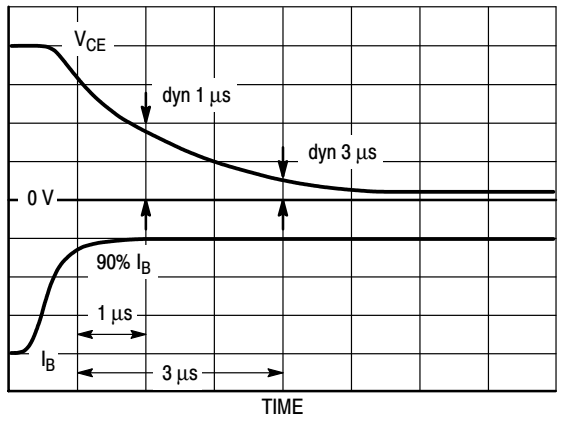


Figure 37. Dynamic Saturation Voltage Measurements

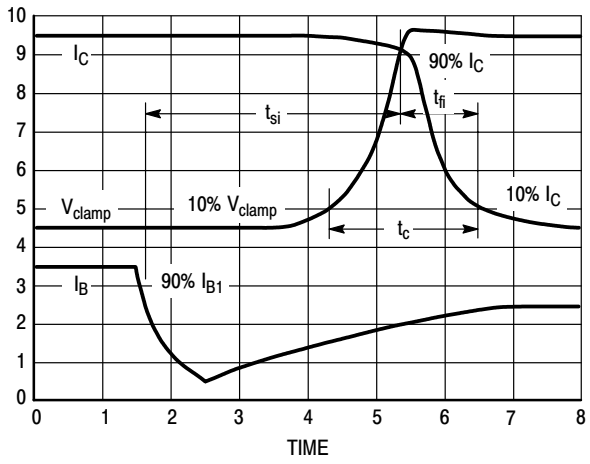
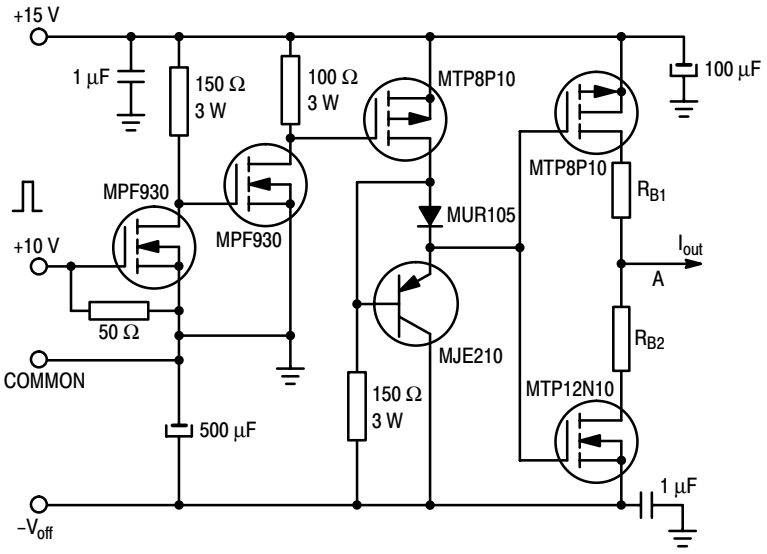
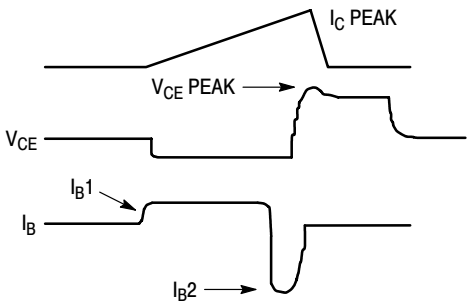


Figure 38. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

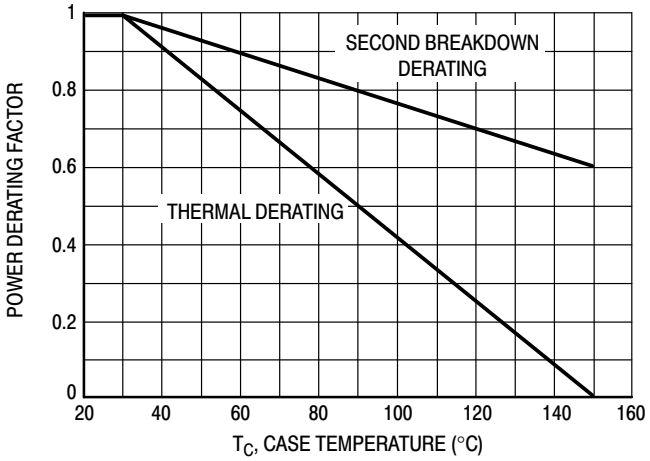


Figure 39. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

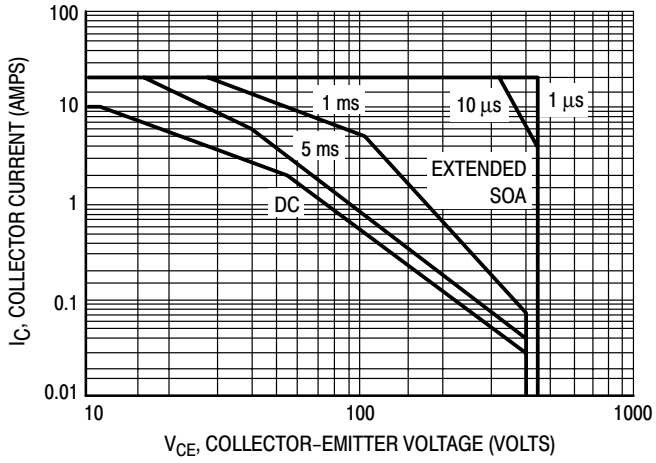


Figure 40. Forward Bias Safe Operating Area

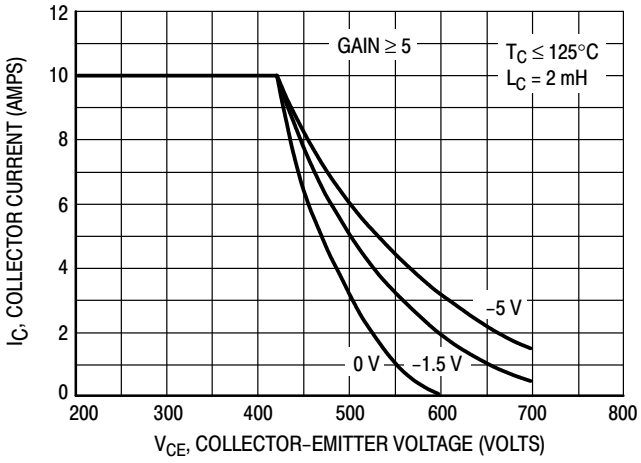


Figure 41. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

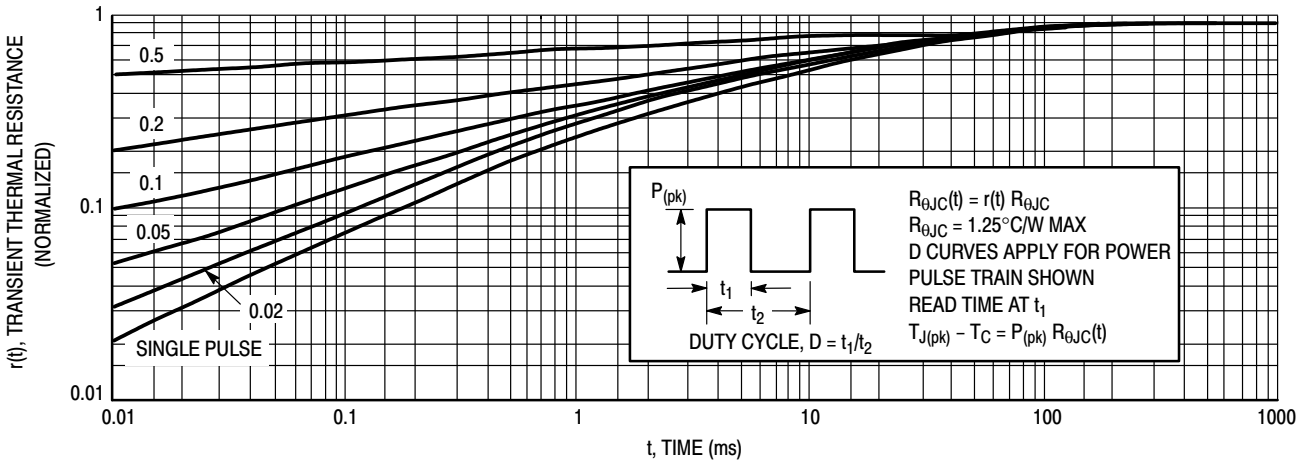
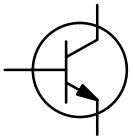
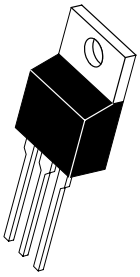


Figure 42. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH100

BUH150

POWER TRANSISTOR
15 AMPERES
700 VOLTS
150 WATTS





CASE 221A–09
TO–220AB

SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH150 has an application specific state–of–art die designed for use in 150 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start–up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 25	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	150 1.2	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.85 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	460		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	860		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.3		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc)		$V_{BE(sat)}$		1	1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.16 0.15	0.4 0.4	Vdc
(I_C = 10 Adc, I_B = 2 Adc)	@ T_C = 25°C			0.45	1	Vdc
(I_C = 20 Adc, I_B = 4 Adc)	@ T_C = 25°C			2	5	Vdc
DC Current Gain (I_C = 20 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	4 2.5	7 4.5		—
(I_C = 10 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		8 6	12 10		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		12 14	20 22		—
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C		10	20		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1} (see Figure 19)	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$		1.5		V
		@ T_C = 125°C			2.8		V
	I_C = 10 Adc, I_{B1} = 2 Adc, V_{CC} = 300 V	@ T_C = 25°C			2.4		V
		@ T_C = 125°C			5		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		100	150	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		1300	1750	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		200	300	ns
Storage Time		@ T_C = 25°C	t_s		5.3	6.5	μs
Fall Time		@ T_C = 25°C	t_f		240	350	ns
Turn–off Time		@ T_C = 25°C	t_{off}		5.6	7	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		100	200	ns
Storage Time		@ T_C = 25°C	t_s		6.1	7.5	μs
Fall Time		@ T_C = 25°C	t_f		320	500	ns
Turn–off Time		@ T_C = 25°C	t_{off}		6.5	8	μs
Turn–on Time	I_C = 5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		450 800	650	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.5 3.9	3	μs
Turn–on Time	I_C = 10 Adc, I_{B1} = 2 Adc I_{B2} = 2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		500 900	700	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.25 2.75	2.75	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 2 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 160	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		6.5 8	8	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		235 240	350	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 170	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		6 7.8	7.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 270	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 140	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		3.25 4.6	3.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		275 450	350	ns
Fall Time	I_C = 10 Adc I_{B1} = 2 Adc I_{B2} = 2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 160	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.3 2.8	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

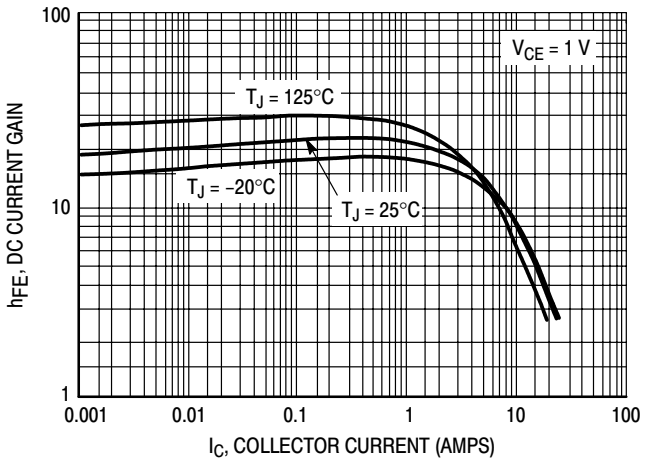


Figure 43. DC Current Gain @ 1 Volt

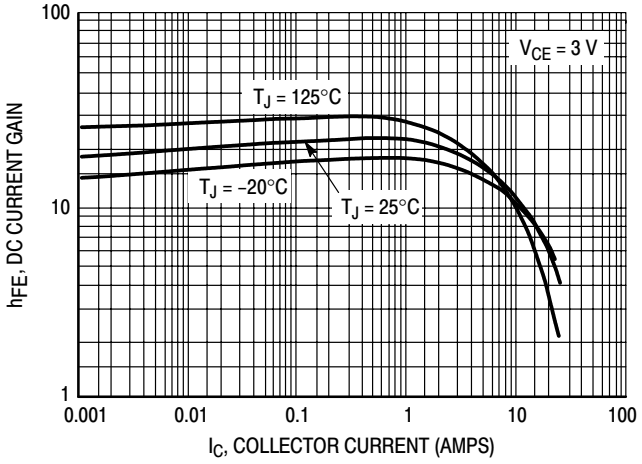


Figure 44. DC Current Gain @ 3 Volt

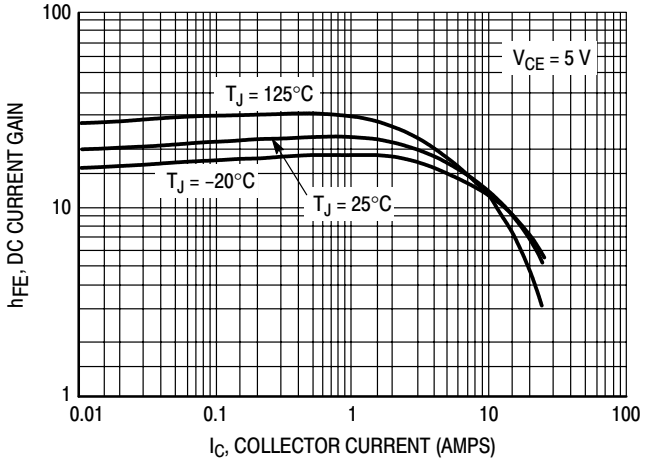


Figure 45. DC Current Gain @ 5 Volt

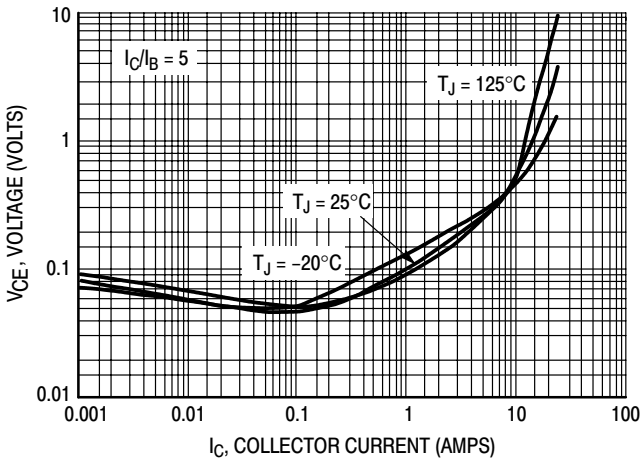


Figure 46. Collector–Emitter Saturation Voltage

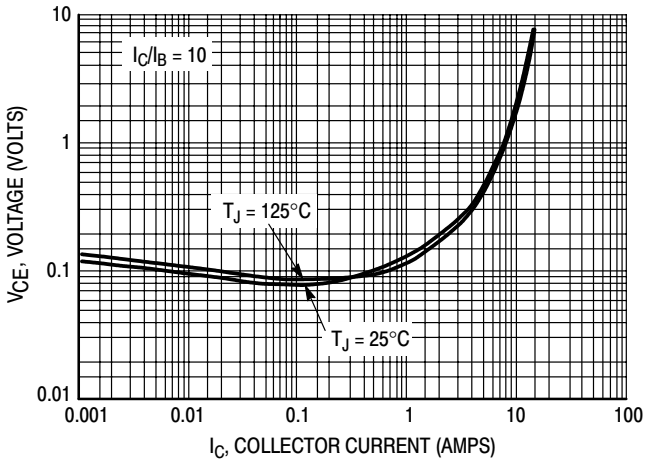


Figure 47. Collector–Emitter Saturation Voltage

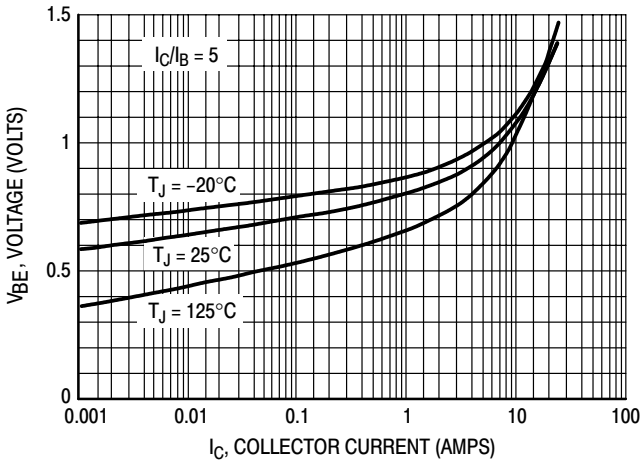


Figure 48. Base–Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

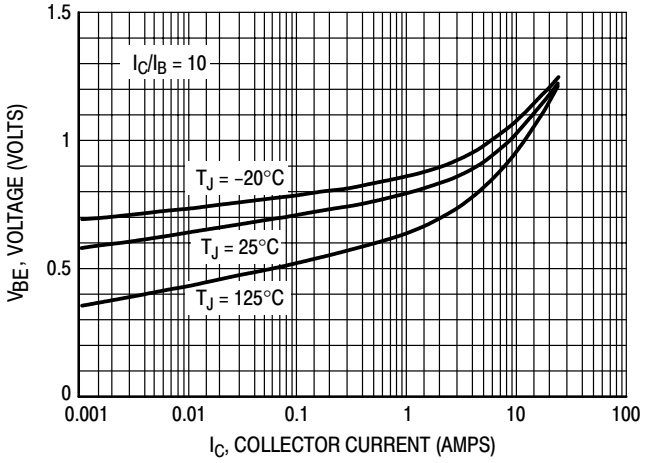


Figure 49. Base−Emitter Saturation Region

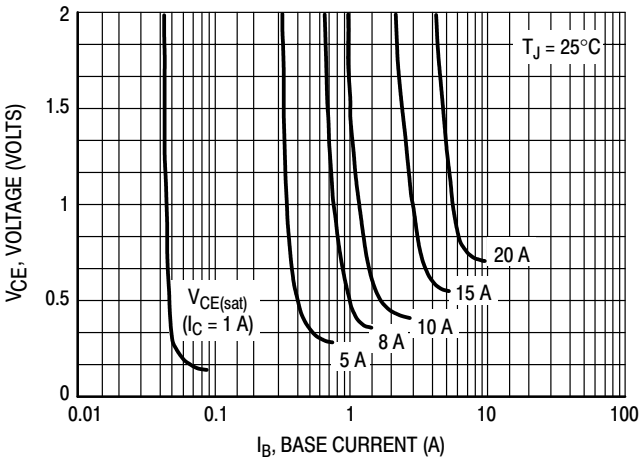


Figure 50. Collector Saturation Region

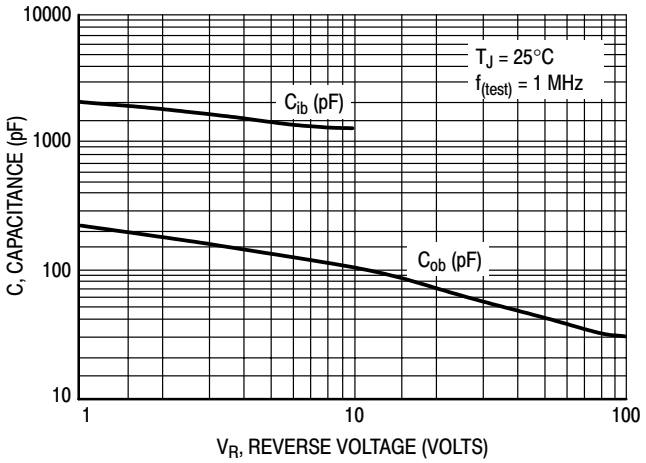


Figure 51. Capacitance

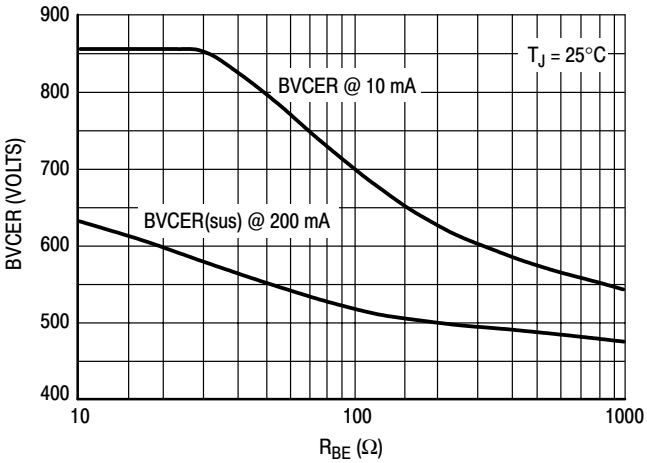


Figure 52. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

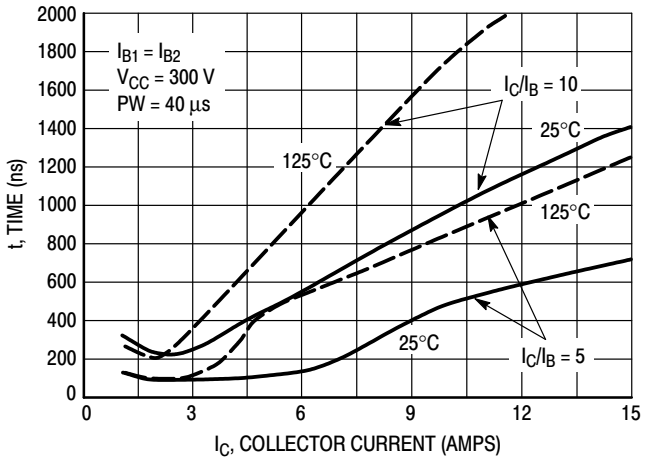


Figure 53. Resistive Switching, t_{on}

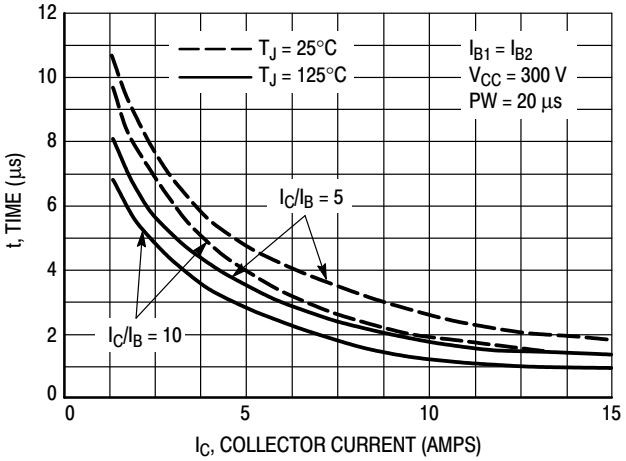


Figure 54. Resistive Switch Time, t_{off}

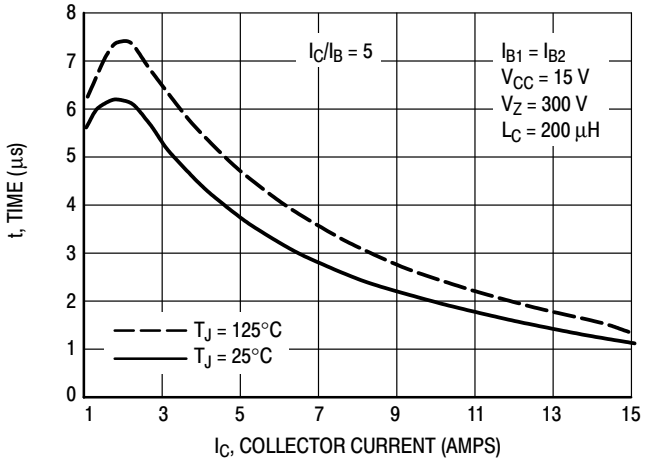


Figure 55. Inductive Storage Time, t_{si}

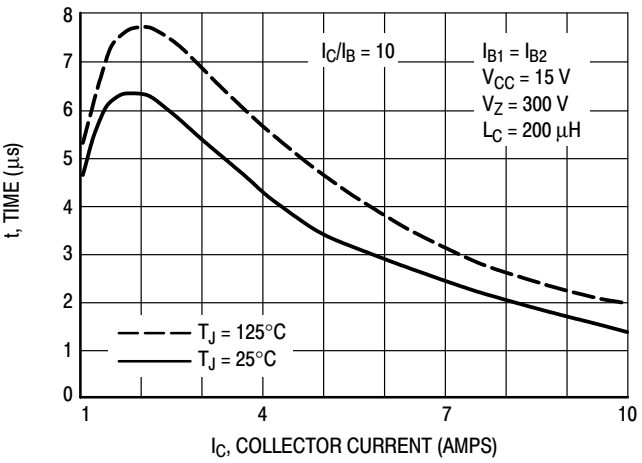


Figure 13 Bis. Inductive Storage Time, t_{si}

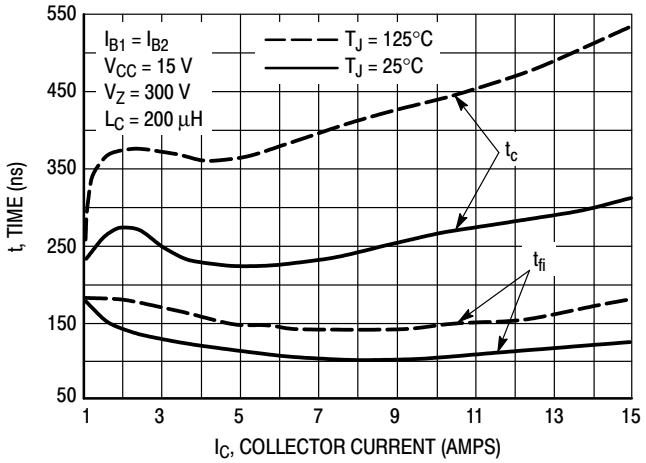


Figure 56. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

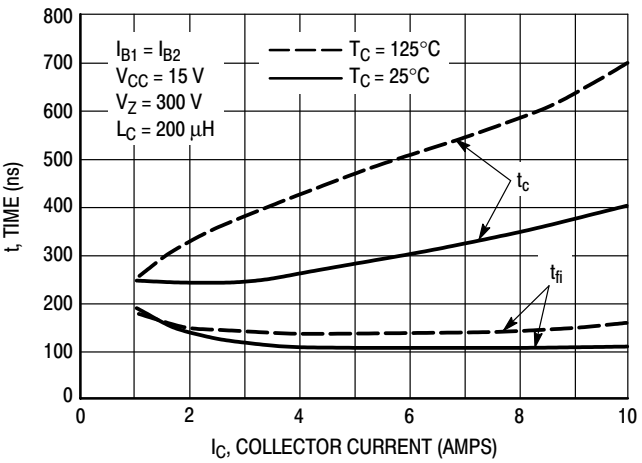


Figure 57. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

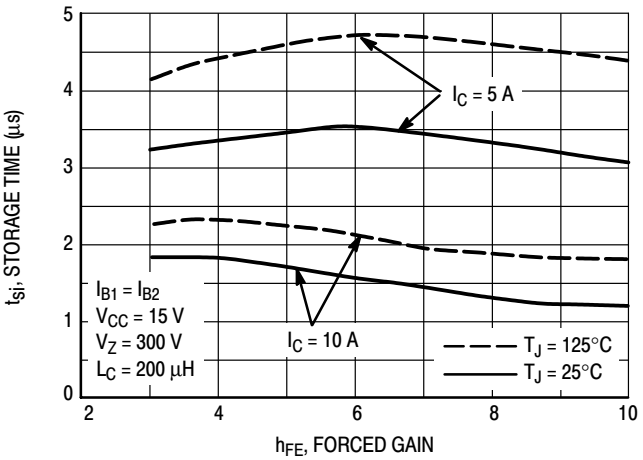


Figure 58. Inductive Storage Time

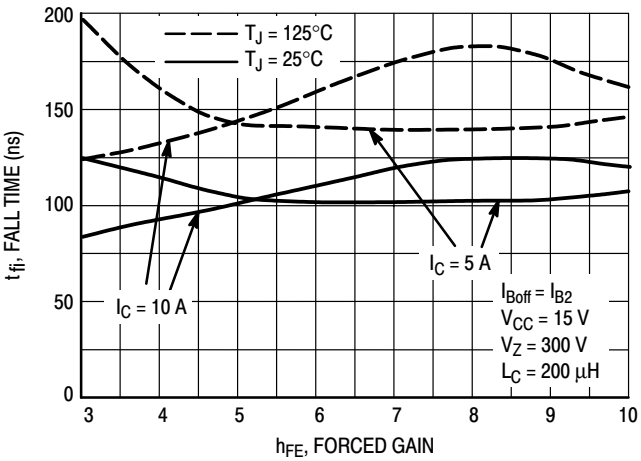


Figure 59. Inductive Fall Time

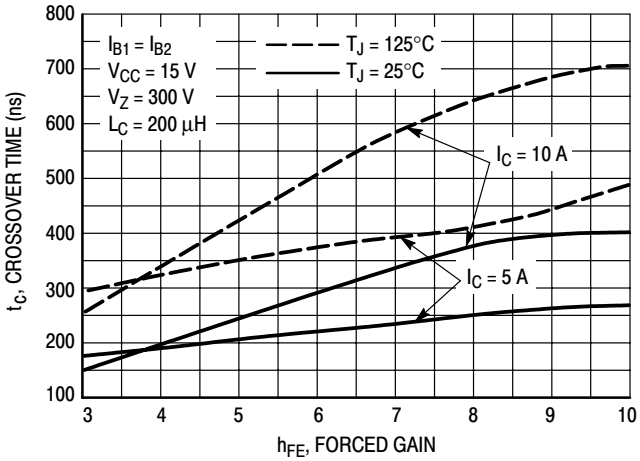


Figure 60. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

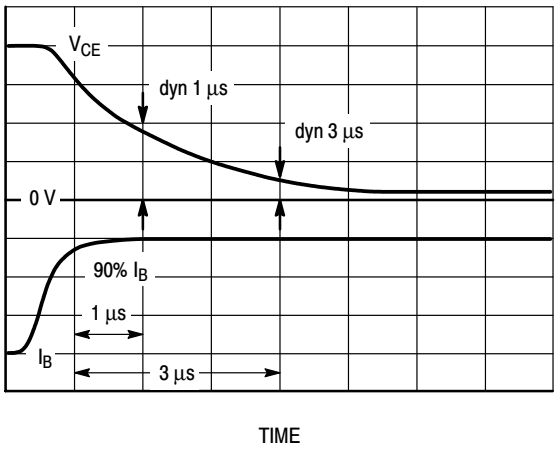


Figure 61. Dynamic Saturation Voltage Measurements

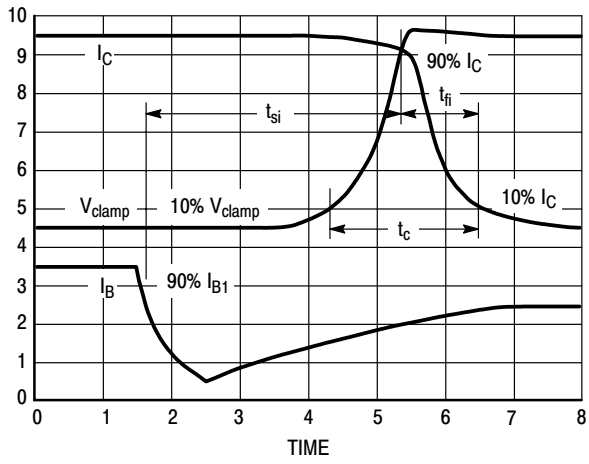
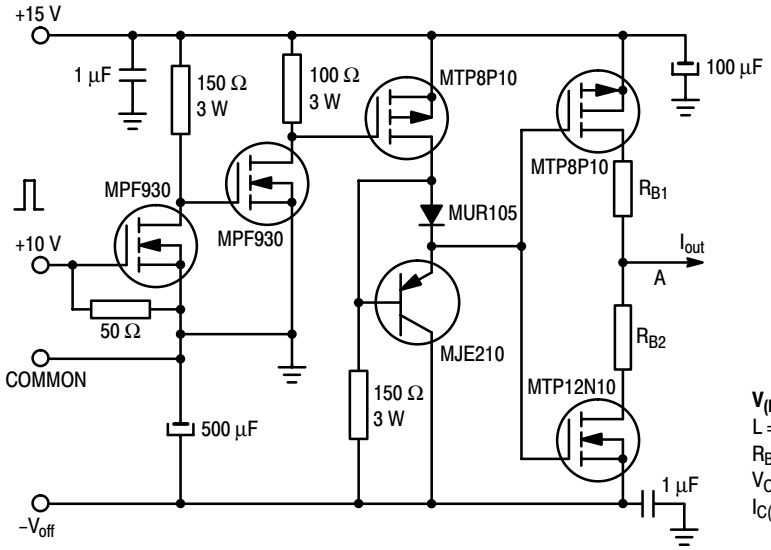
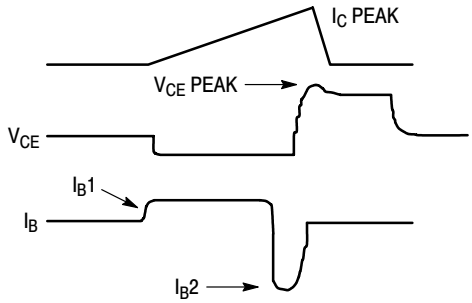


Figure 62. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

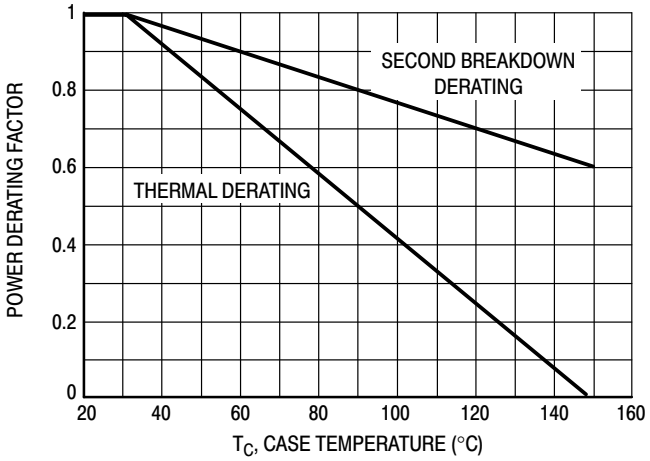


Figure 63. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 64 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 64 may be found at any case temperature by using the appropriate curve on Figure 63.

$T_{J(pk)}$ may be calculated from the data in Figure 66. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 65). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

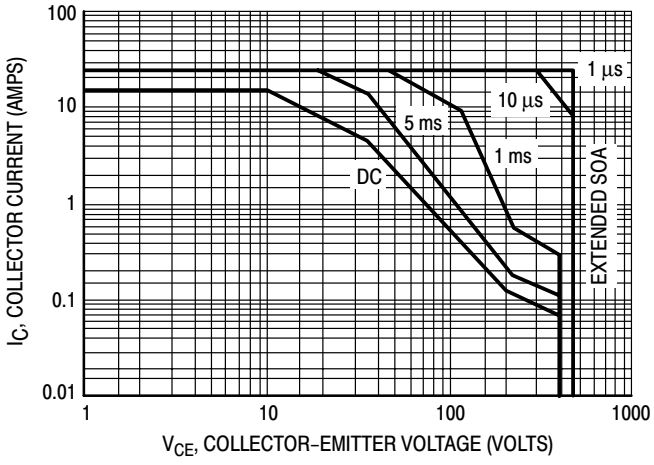


Figure 64. Forward Bias Safe Operating Area

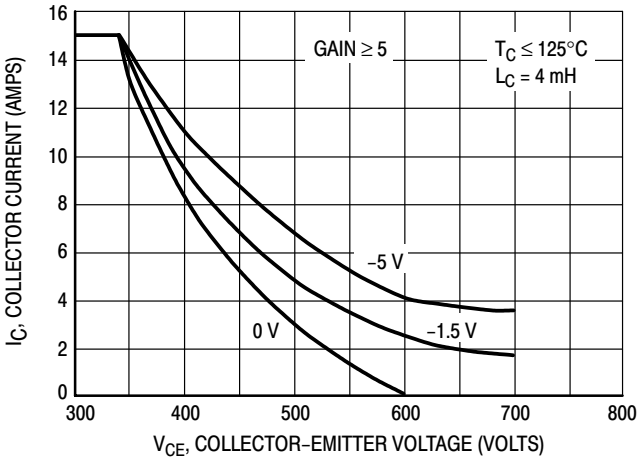


Figure 65. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

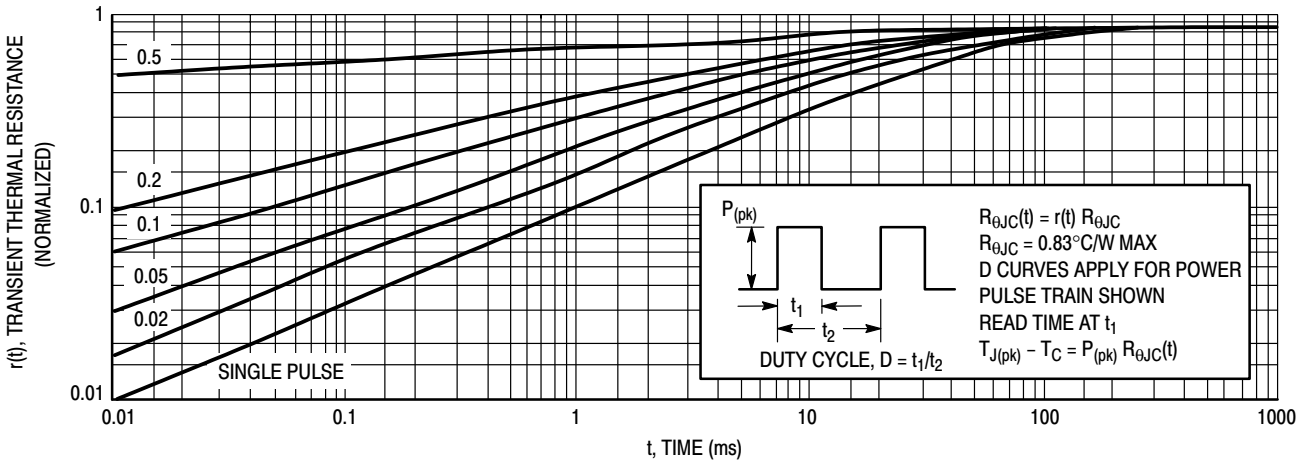


Figure 66. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH150

BUH50

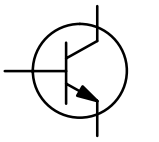
POWER TRANSISTOR
4 AMPERES
800 VOLTS
50 WATTS

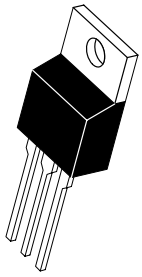
SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH50 has an application specific state–of–art die designed for use in 50 Watts HALOGEN electronic transformers and SWITCHMODE applications.

This high voltage/high speed transistor exhibits the following main feature:

- Improved Efficiency Due to Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproductible Parametric Distributions
- Specified Dynamic Saturation Data
- Full Characterization at 125°C





CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter–Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	500			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc) (I_C = 2 Adc, I_B = 0.66 Adc) 25°C (I_C = 2 Adc, I_B = 0.66 Adc) 100°C		$V_{BE(sat)}$		 0.86 0.94 0.85	 1.2 1.6 1.5	Vdc
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc)	@ T_C = 25°C	$V_{CE(sat)}$		0.2	0.5	Vdc
(I_C = 2 Adc, I_B = 0.66 Adc)	@ T_C = 25°C @ T_C = 125°C			0.32 0.29	0.6 0.7	
(I_C = 3 Adc, I_B = 1 Adc)	@ T_C = 25°C			0.5	1	
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C	h_{FE}	7	13		—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		5	10		—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4			MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		50	100	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}		850	1200	pF

DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 A I_{B1} = 0.33 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		1.75 5	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C			0.3 0.5	V
	I_C = 2 A I_{B1} = 0.66 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C			6 14	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C			0.75 4	V

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		95	250	ns
Turn–off Time		@ T_C = 25°C	t_{off}		2.5	3.5	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		110	250	ns
Turn–off Time		@ T_C = 25°C	t_{off}		0.95	2	μs
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.3 Adc I_{B2} = 0.3 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		100	200	ns
Turn–off Time		@ T_C = 25°C	t_{off}		2.9	3.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		80 95	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.2 1.7	2.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 180	300	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.66 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		90 100	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.7 2.5	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		190 220	350	ns

TYPICAL STATIC CHARACTERISTICS

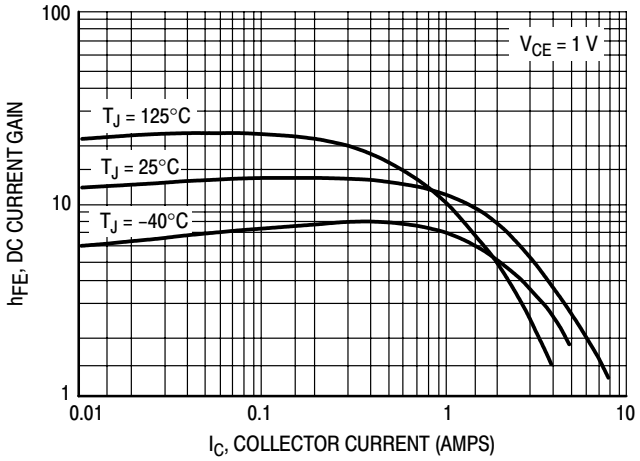


Figure 67. DC Current Gain @ 1 Volt

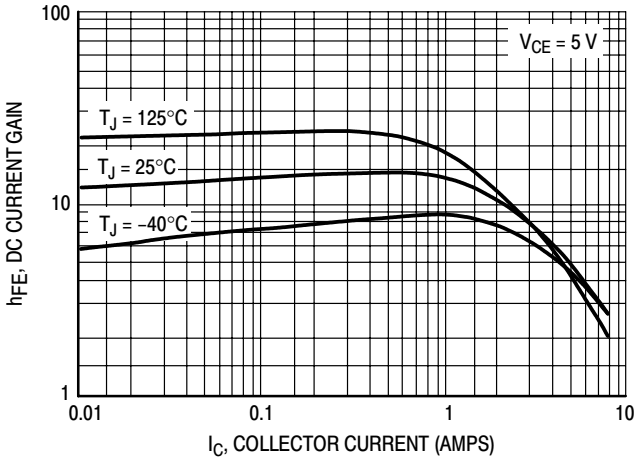


Figure 68. DC Current Gain @ 5 Volt

TYPICAL STATIC CHARACTERISTICS

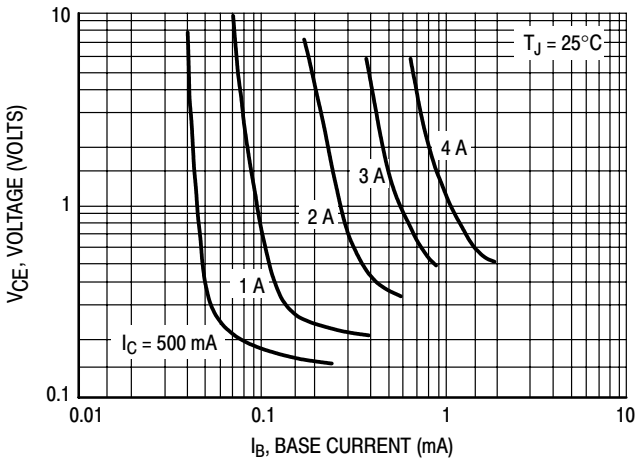


Figure 69. Collector Saturation Region

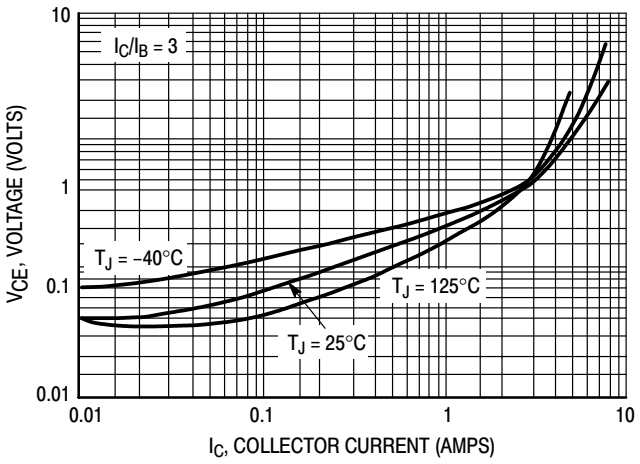


Figure 70. Collector–Emitter Saturation Voltage

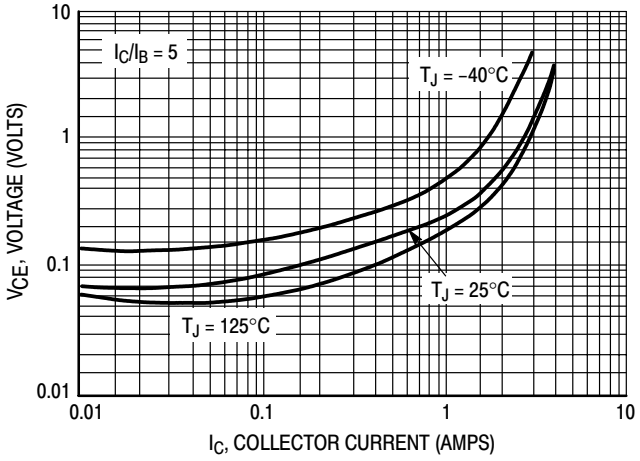


Figure 71. Collector–Emitter Saturation Voltage

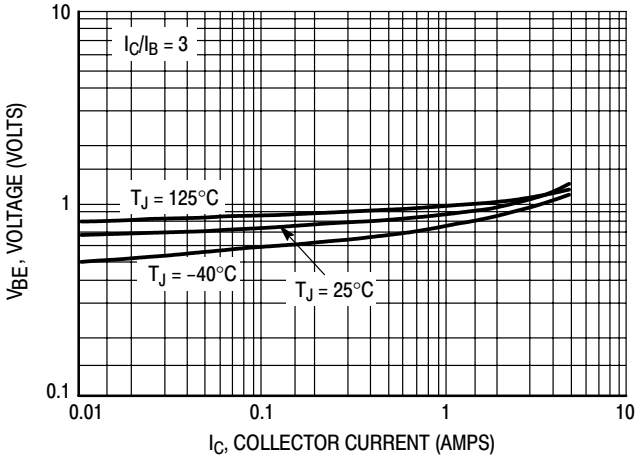


Figure 72. Base–Emitter Saturation Region

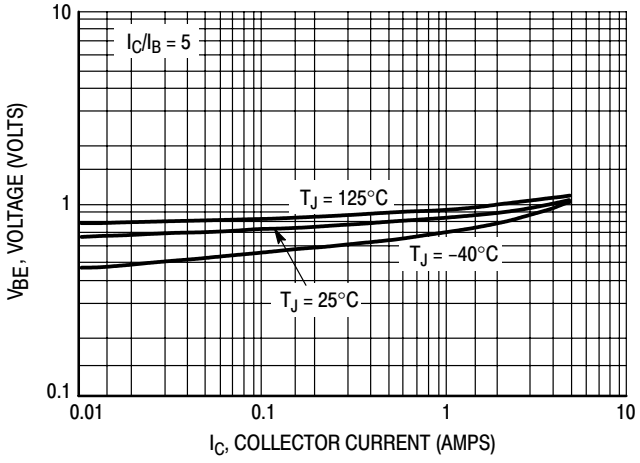


Figure 73. Base–Emitter Saturation Region

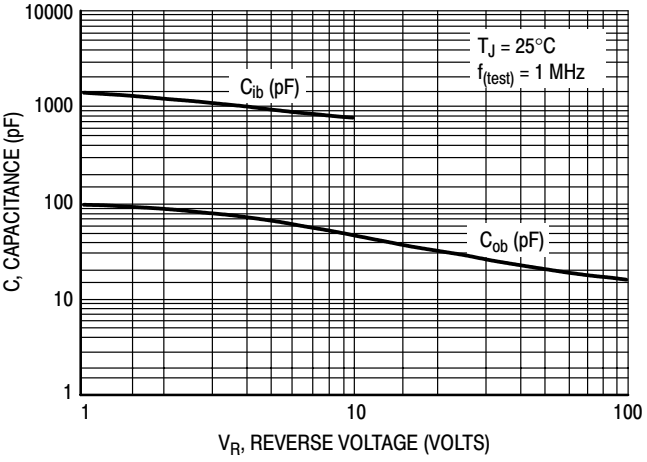


Figure 74. Capacitance

TYPICAL SWITCHING CHARACTERISTICS

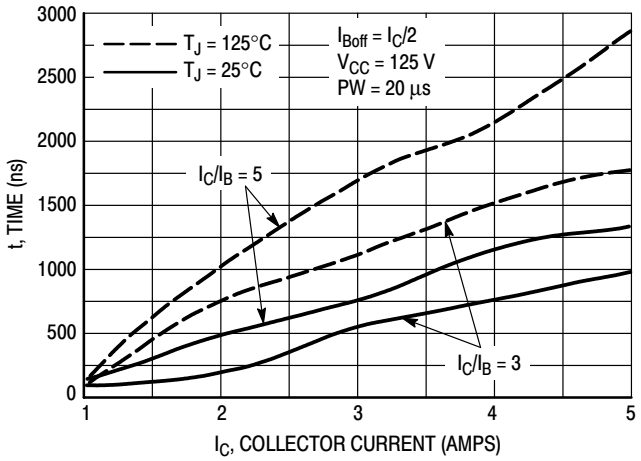


Figure 75. Resistive Switching, t_{on}

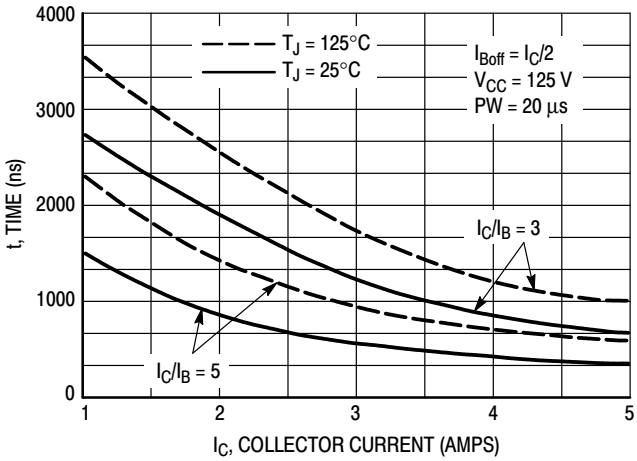


Figure 76. Resistive Switch Time, t_{off}

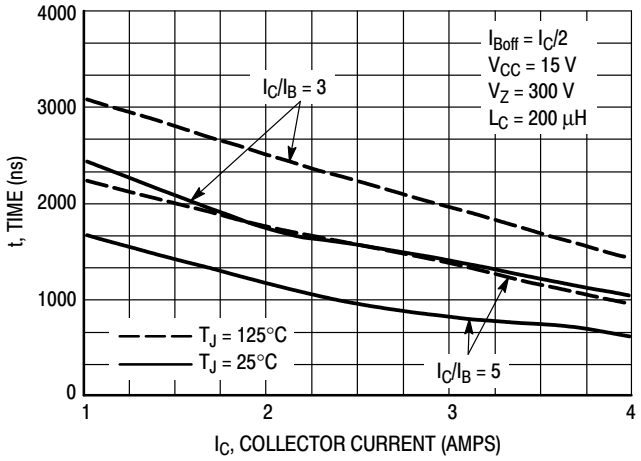


Figure 77. Inductive Storage Time, t_{si}

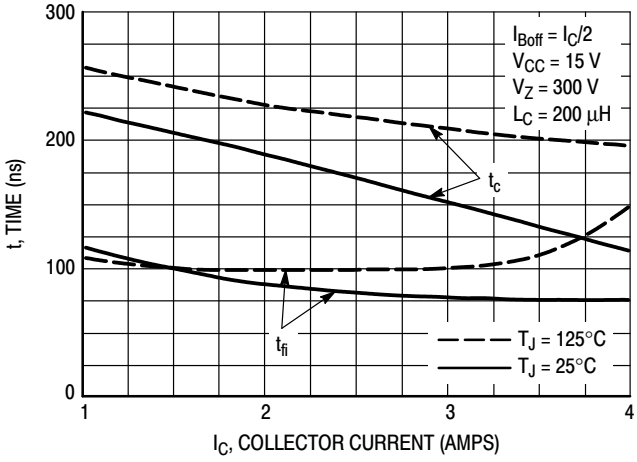


Figure 78. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 3

TYPICAL CHARACTERISTICS

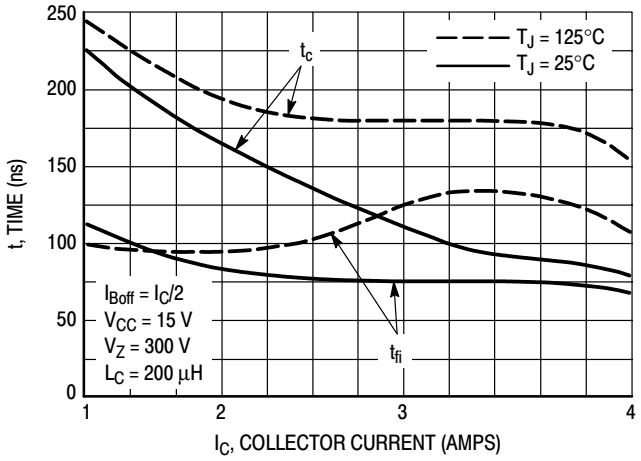


Figure 79. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

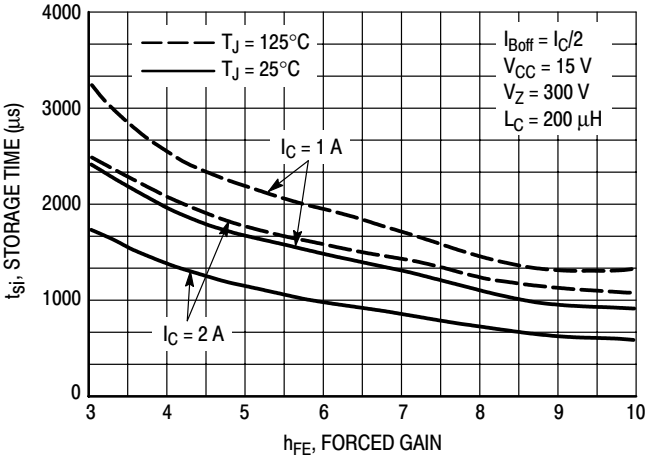


Figure 80. Inductive Storage Time

TYPICAL CHARACTERISTICS

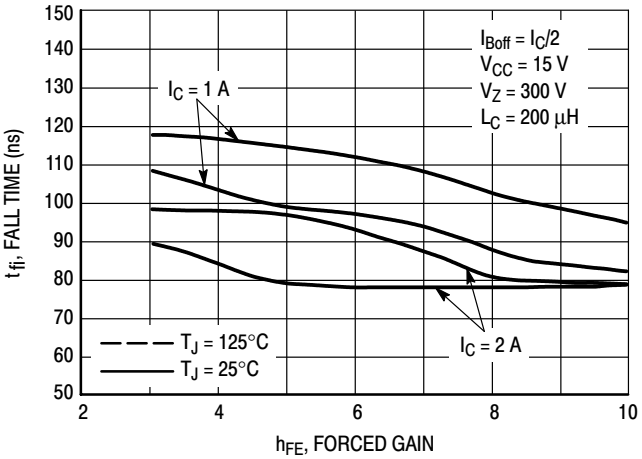


Figure 81. Inductive Fall Time

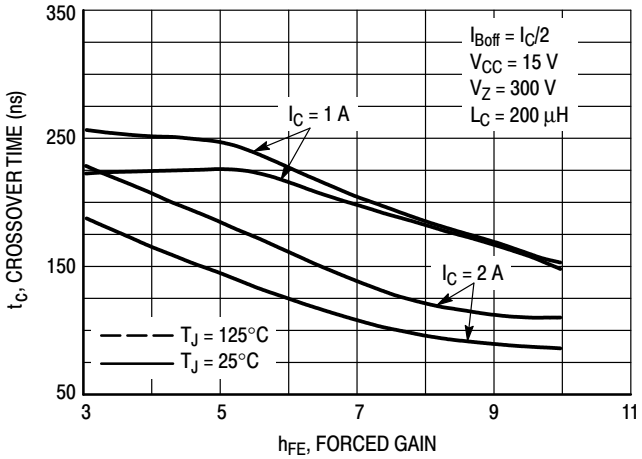


Figure 82. Inductive Crossover Time

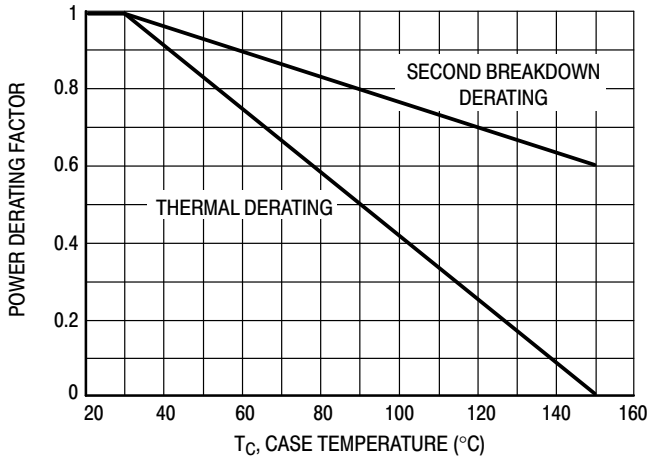


Figure 83. Forward Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 86 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 86 may be found at any case temperature by using the appropriate curve on Figure 83.

$T_{J(pk)}$ may be calculated from the data in Figure 88. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 87). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL CHARACTERISTICS

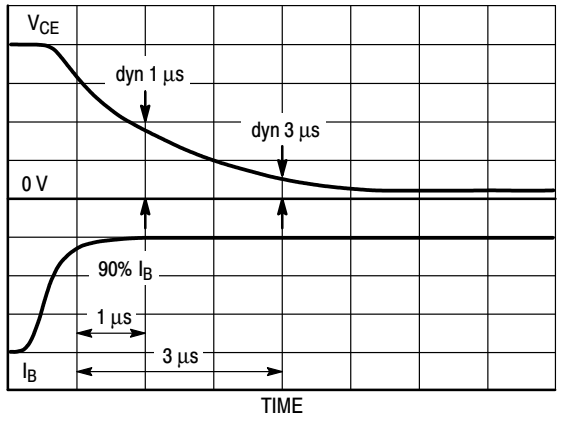


Figure 84. Dynamic Saturation Voltage

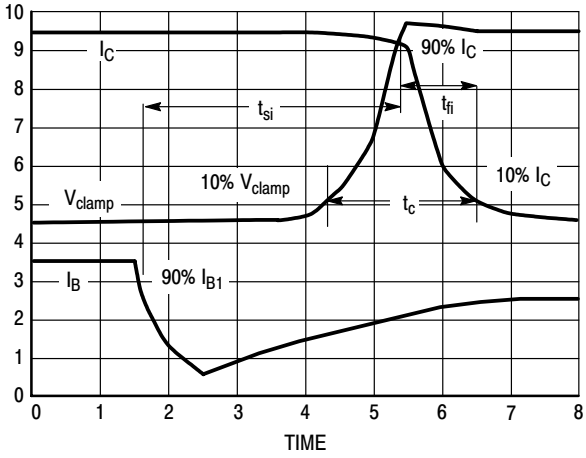


Figure 85. Inductive Switching Measurements

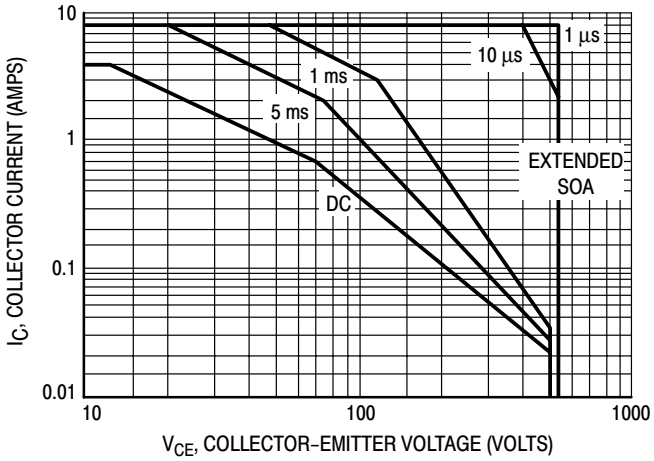


Figure 86. Forward Bias Safe Operating Area

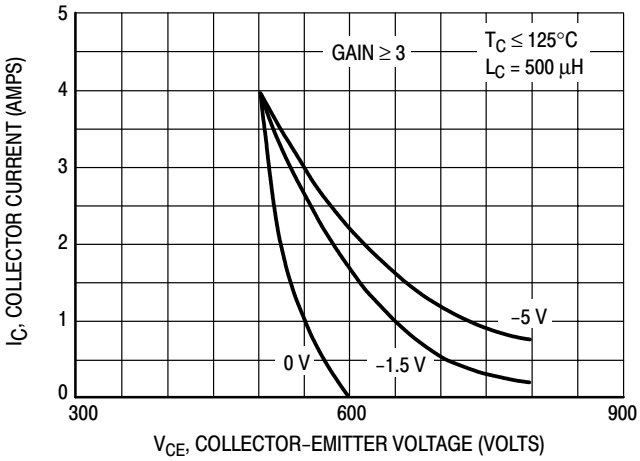
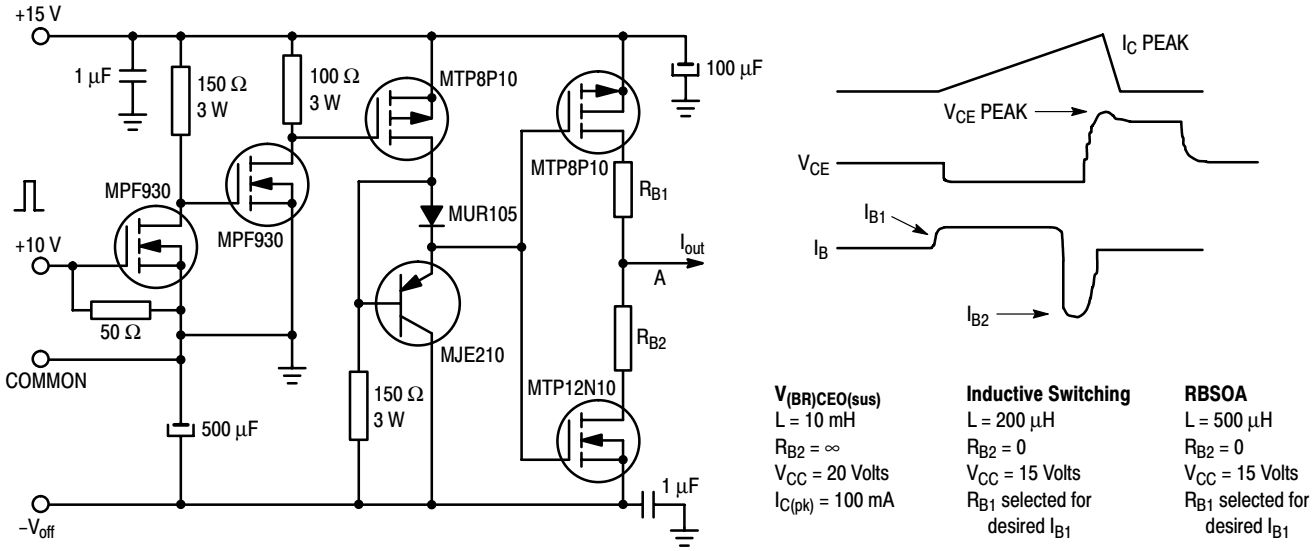


Figure 87. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



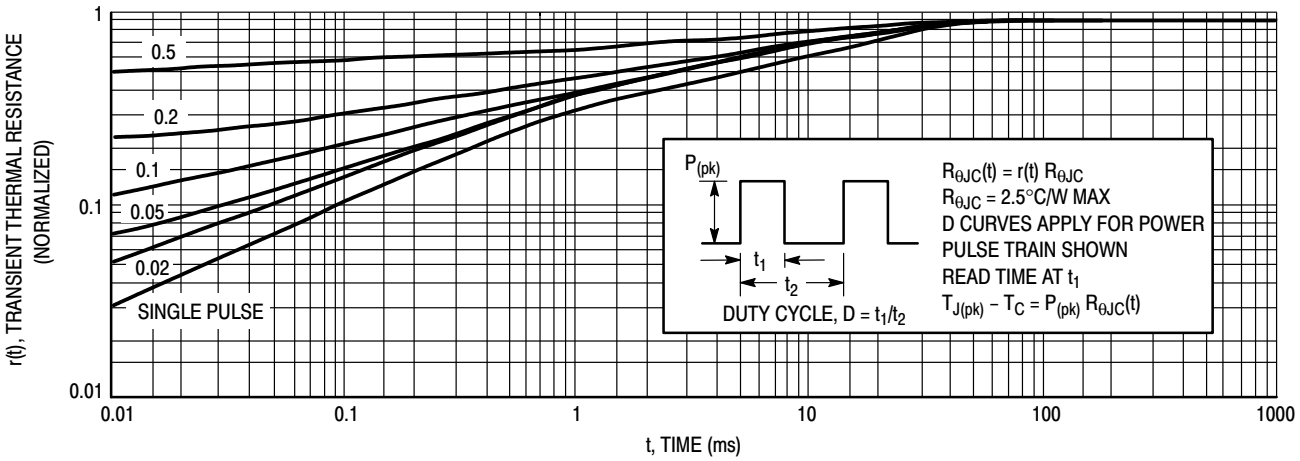
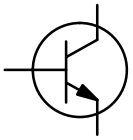
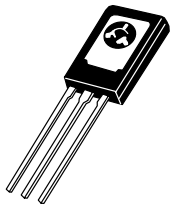


Figure 88. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH50

BUH51

POWER TRANSISTOR
3 AMPERES
800 VOLTS
50 WATTS





CASE 77–09
TO–225AA TYPE

SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH51 has an application specific state–of–art die designed for use in 50 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start–up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Providing Tight and Reproducible
  Parametric Distributions

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter–Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	3 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 100	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	500	550		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	800	950		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.92 0.8	1.1	Vdc
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.3 0.32	0.5 0.6	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	8 6	10 8		—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		5 4	7.5 6.2		—
(I_C = 0.8 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 8	14 13		—
(I_C = 10 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		14 18	20 25		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc, I_{B1} = 0.2 Adc, V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$		1.7		V
		@ T_C = 125°C			6		V
	I_C = 2 Adc, I_{B1} = 0.4 Adc, V_{CC} = 300 V	@ T_C = 25°C			5.1		V
		@ T_C = 125°C			15		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		34	100	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		200	500	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		110 125	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.5 4.1	4	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		700 1250	1000	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.75 2.1	2	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		200 320	300	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		3.4 4	3.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		350 640	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		140 300	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.3 2.8	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		400 725	600	ns

TYPICAL STATIC CHARACTERISTICS

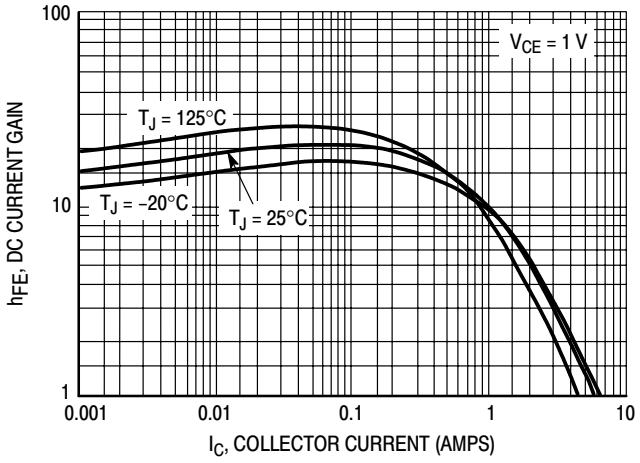


Figure 89. DC Current Gain @ 1 Volt

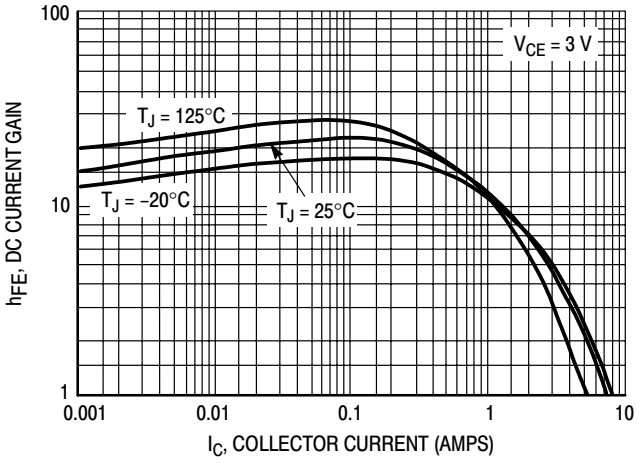


Figure 90. DC Current Gain @ 3 Volt

TYPICAL STATIC CHARACTERISTICS

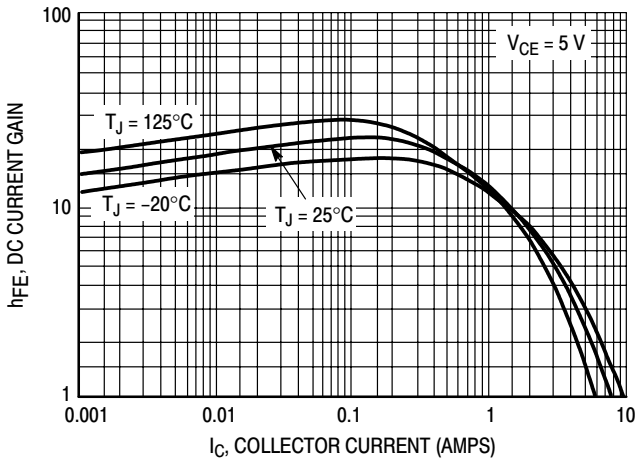


Figure 91. DC Current Gain @ 5 Volt

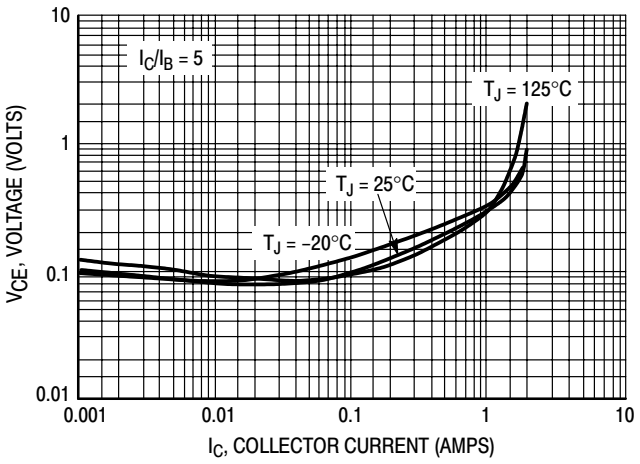


Figure 92. Collector–Emitter Saturation Voltage

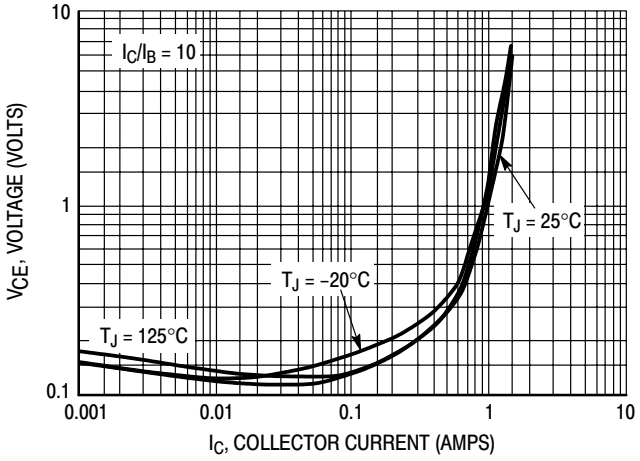


Figure 93. Collector–Emitter Saturation Voltage

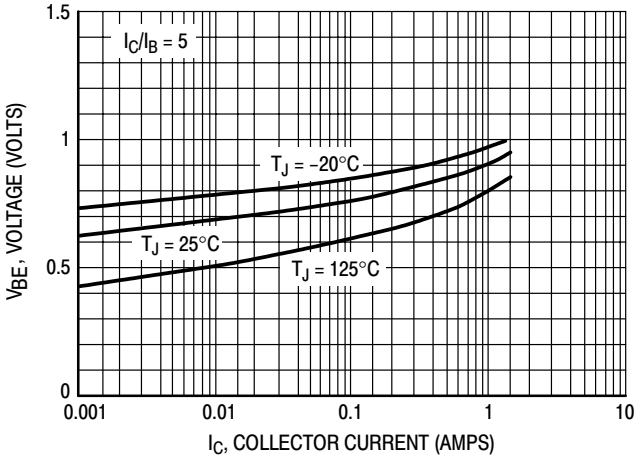


Figure 94. Base–Emitter Saturation Region

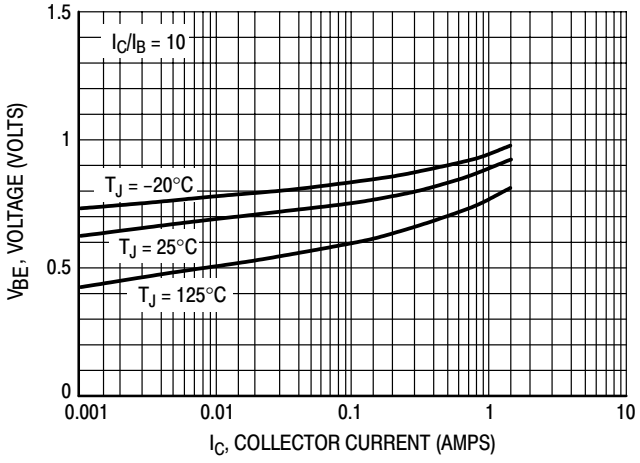


Figure 95. Base–Emitter Saturation Region

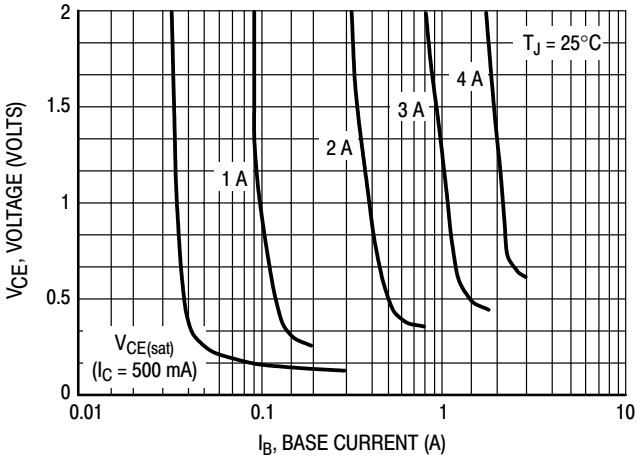


Figure 96. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

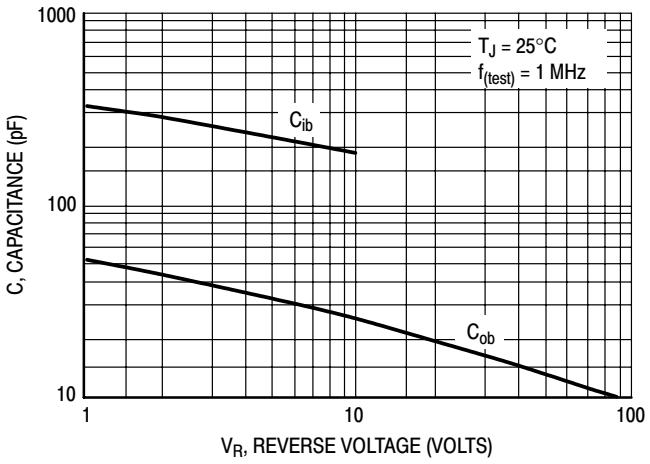


Figure 97. Capacitance

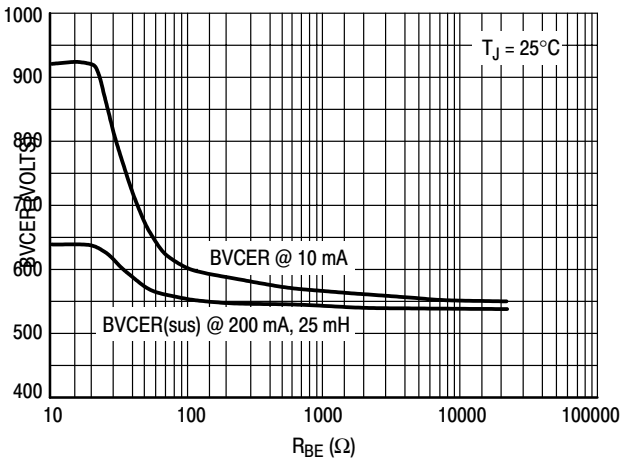


Figure 98. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

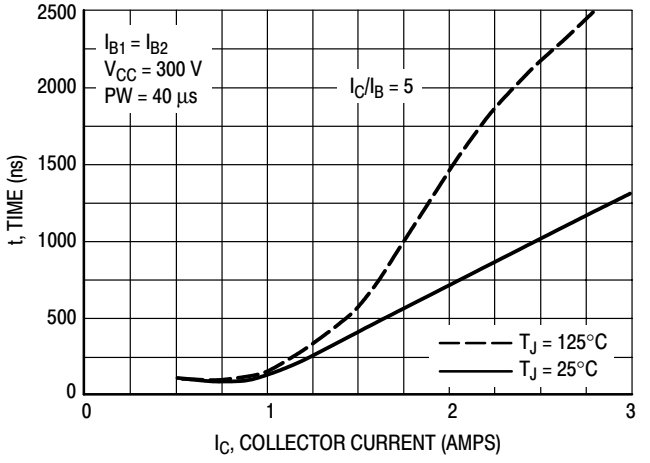


Figure 99. Resistive Switching, t_{on}

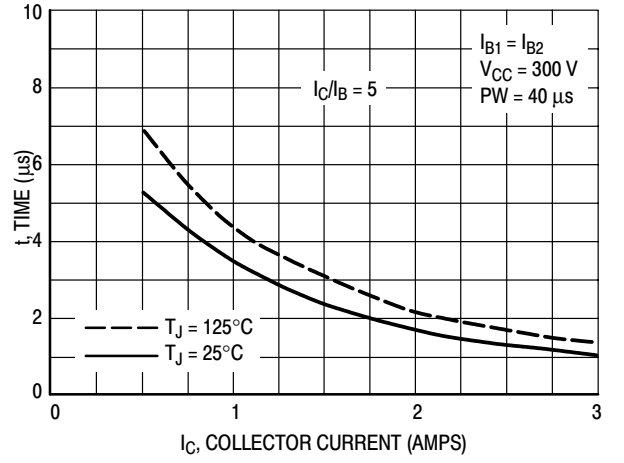


Figure 100. Resistive Switch Time, t_{off}

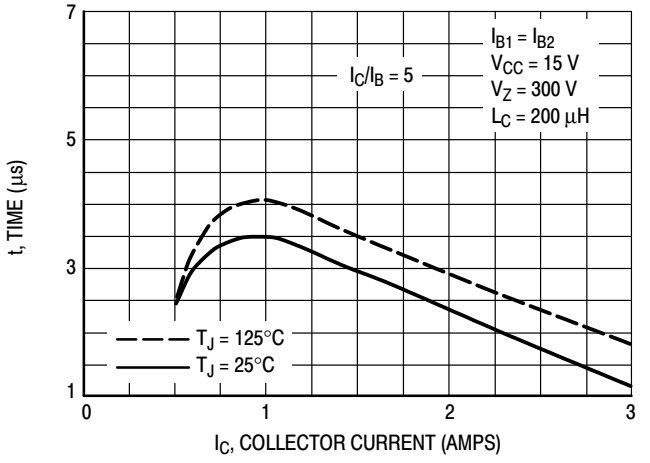


Figure 101. Inductive Storage Time, t_{si}

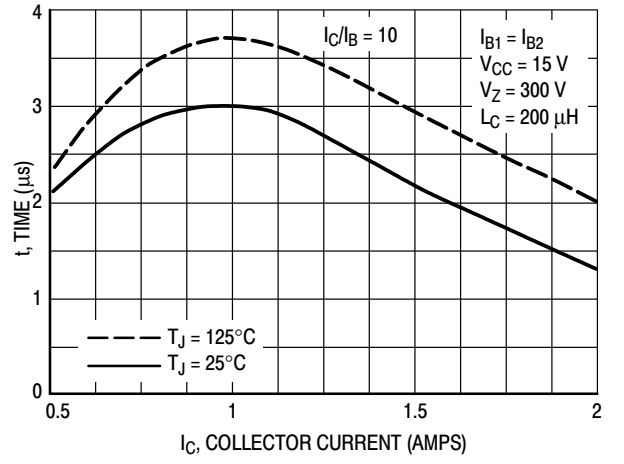


Figure 13 Bis. Inductive Storage Time, t_{si}

TYPICAL SWITCHING CHARACTERISTICS

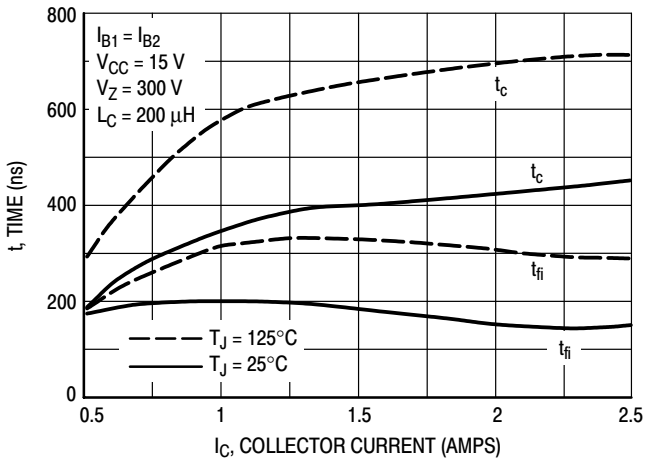


Figure 102. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

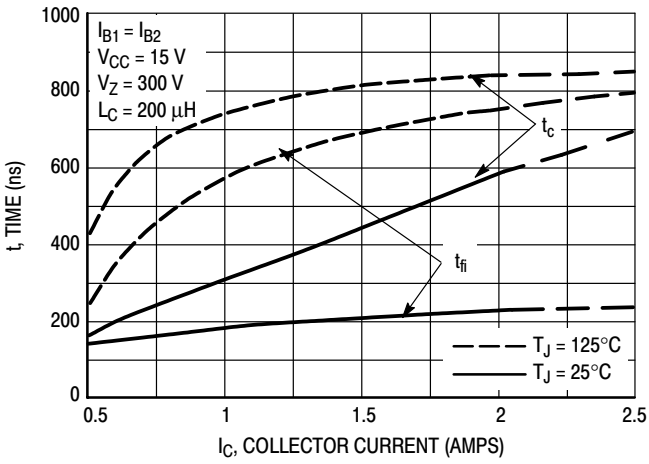


Figure 103. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

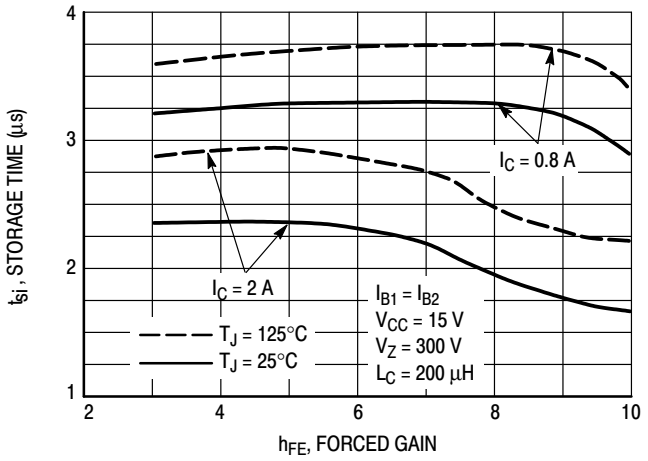


Figure 104. Inductive Storage Time

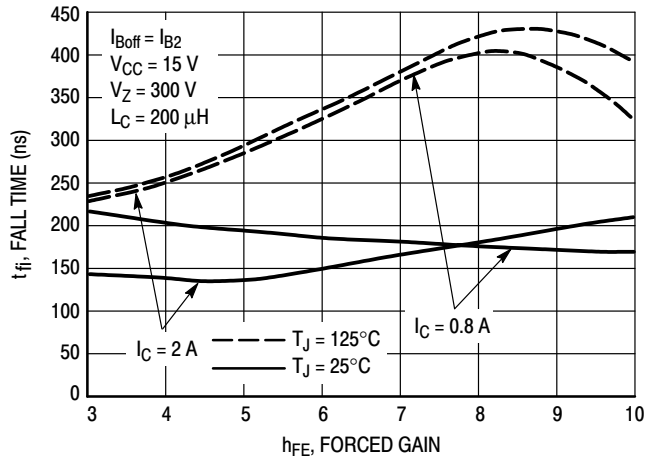


Figure 105. Inductive Fall Time

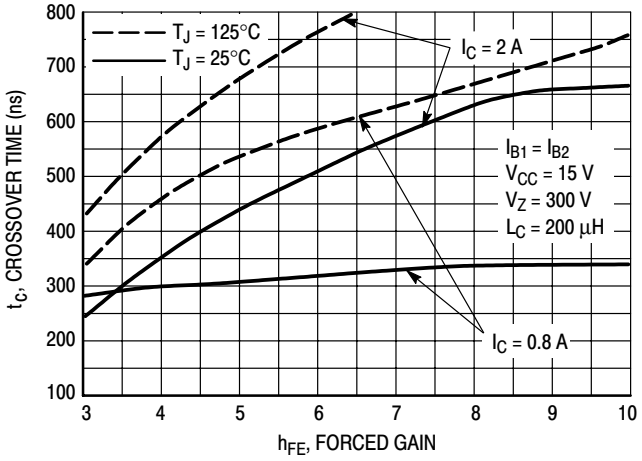


Figure 106. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

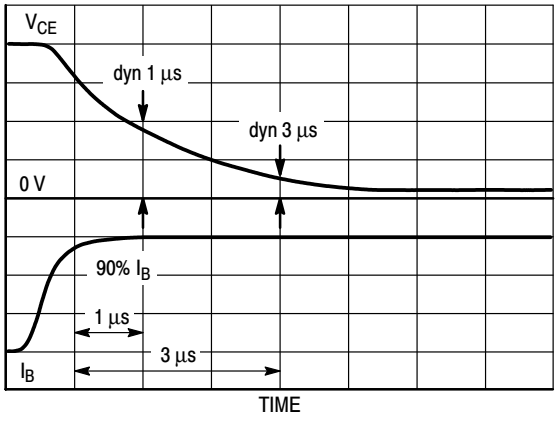


Figure 107. Dynamic Saturation Voltage Measurements

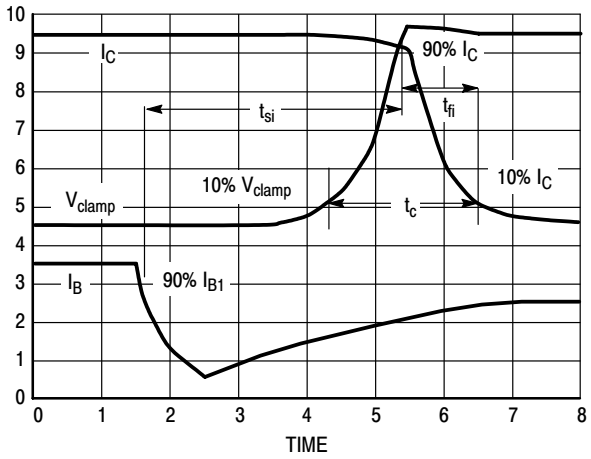
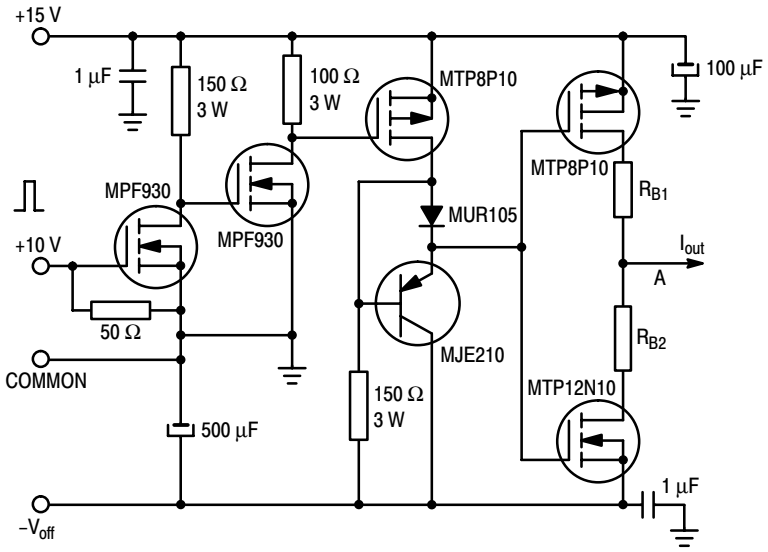
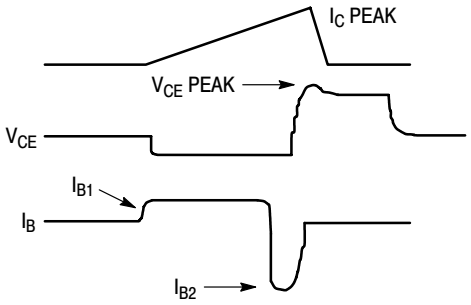


Figure 108. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

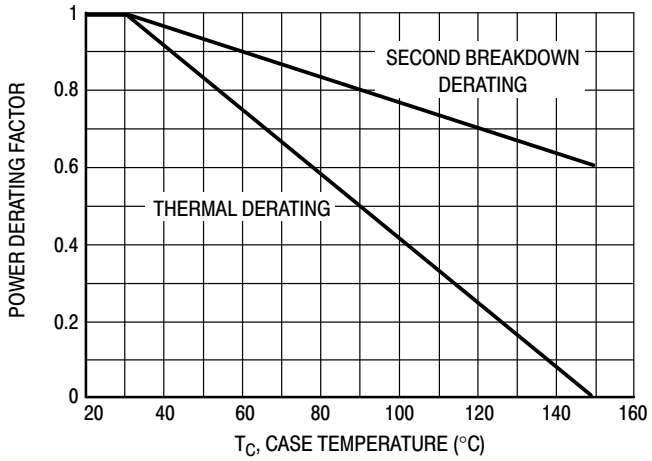


Figure 109. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 110 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 110 may be found at any case temperature by using the appropriate curve on Figure 109.

$T_{J(pk)}$ may be calculated from the data in Figure 112. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 111). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

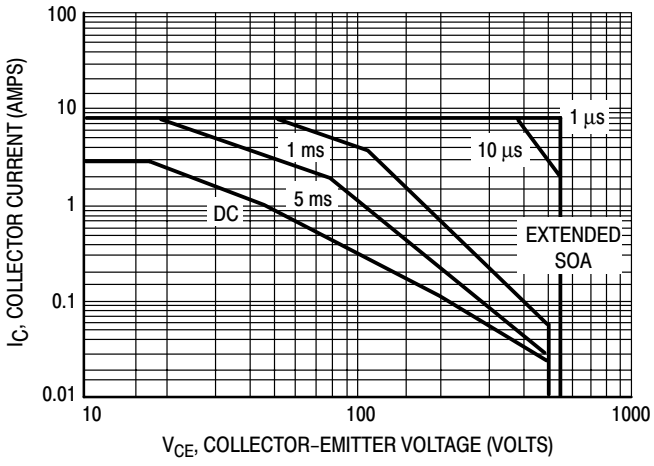


Figure 110. Forward Bias Safe Operating Area

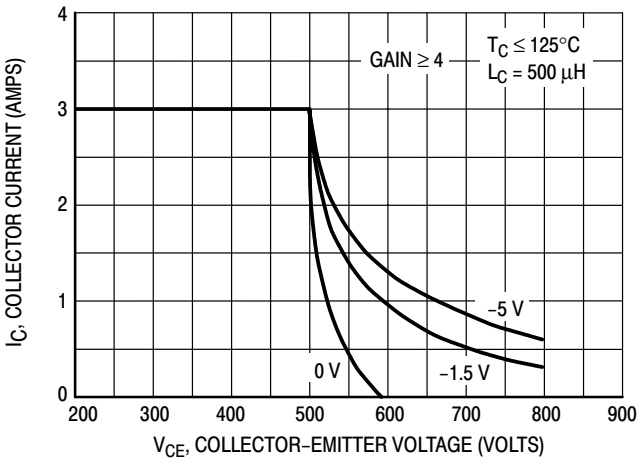


Figure 111. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

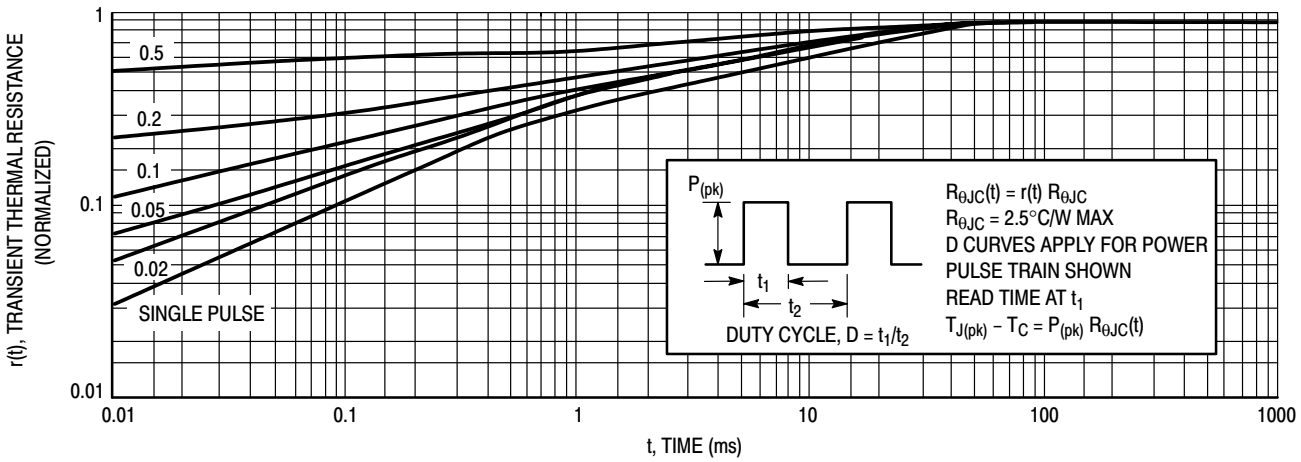


Figure 112. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH51

SWITCHMODE™

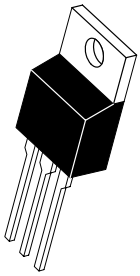
NPN Bipolar Power Transistor For Switching Power Supply Applications

BUL146
BUL146F

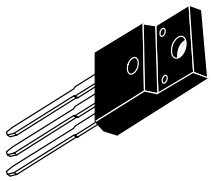
POWER TRANSISTOR
6.0 AMPERES
700 VOLTS
40 and 100 WATTS

The BUL146/BUL146F have an applications specific state–of–the–art die designed for use in fluorescent electric lamp ballasts to 130 Watts and in Switchmode Power supplies for all types of electronic equipment. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Two Packages Choices: Standard TO220 or Isolated TO220
- Parametric Distributions are Tight and Consistent Lot–to–Lot
- BUL146F, Case 221D, is UL Recognized to 3500 V_{RMS}: File # E69369



BUL146
CASE 221A–09
TO–220AB



CASE 221D–02
ISOLATED TO–220 TYPE
BUL146F

MAXIMUM RATINGS

Rating	Symbol	BUL146	BUL146F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current – Continuous – Peak(1)	I_C I_{CM}	6.0 15		Adc
Base Current – Continuous – Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolation Voltage: (2) (for 1 sec, R.H. $\leq$ 30%, T_C = 25° C)	V_{ISOL1} V_{ISOL2} V_{ISOL3}	– – –	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	40 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL146	BUL146F	Unit
Thermal Resistance – Junction to Case – Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	–	–	100	μAdc
(T_C = 125°C)		–	–	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		–	–	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS – (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc)	$V_{BE(sat)}$	–	0.82	1.1	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)		–	0.93	1.25	
Collector–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc)	$V_{CE(sat)}$	–	0.22	0.5	Vdc
(T_C = 125°C)		–	0.20	0.5	
(I_C = 3.0 Adc, I_B = 0.6 Adc)		–	0.30	0.7	
(T_C = 125°C)		–	0.30	0.7	
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	–	34	–
(T_C = 125°C)		–	30	–	
(I_C = 1.3 Adc, V_{CE} = 1.0 Vdc)		12	20	–	
(T_C = 125°C)		12	20	–	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		8.0	13	–	
(T_C = 125°C)		7.0	12	–	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	–	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	–	14	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{OB}	–	95	150	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{IB}	–	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18) — (I_C = 1.3 Adc, I_{B1} = 300 mAdc, V_{CC} = 300 V)	$V_{CE(dsat)}$	–	2.5	–	V
1.0 μs (T_C = 125°C)		–	6.5	–	
3.0 μs		–	0.6	–	
3.0 μs (T_C = 125°C)		–	2.5	–	
(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, V_{CC} = 300 V) 1.0 μs		–	3.0	–	
1.0 μs (T_C = 125°C)		–	7.0	–	
3.0 μs		–	0.75	–	
3.0 μs (T_C = 125°C)		–	1.4	–	

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn–On Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	– –	100 90	200 –	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	– –	1.35 1.90	2.5 –	μs
Turn–On Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B1} = 1.5 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	– –	90 100	150 –	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	– –	1.7 2.1	2.5 –	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc) (T_C = 125°C)	t_{fi}	– –	115 120	200 –	ns
Storage Time	(T_C = 125°C)	t_{si}	– –	1.35 1.75	2.5 –	μs
Crossover Time	(T_C = 125°C)	t_c	– –	200 210	350 –	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B2} = 1.5 Adc) (T_C = 125°C)	t_{fi}	– –	85 100	150 –	ns
Storage Time	(T_C = 125°C)	t_{si}	– –	1.75 2.25	2.5 –	μs
Crossover Time	(T_C = 125°C)	t_c	– –	175 200	300 –	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B2} = 0.6 Adc) (T_C = 125°C)	t_{fi}	80 –	– 210	180 –	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 –	– 4.5	3.8 –	μs
Crossover Time	(T_C = 125°C)	t_c	– –	230 400	350 –	ns

TYPICAL STATIC CHARACTERISTICS

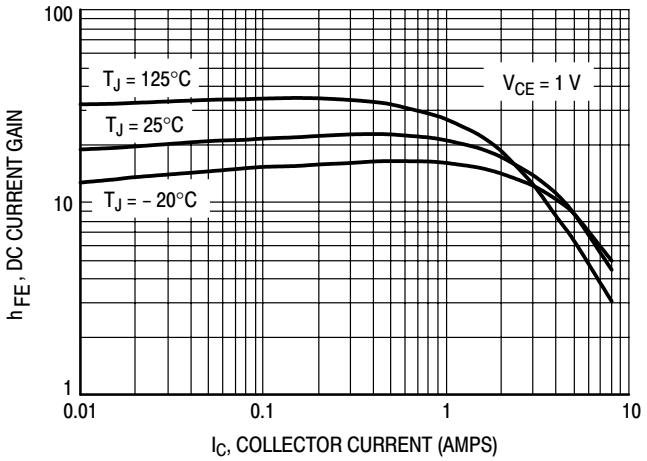


Figure 1. DC Current Gain @ 1 Volt

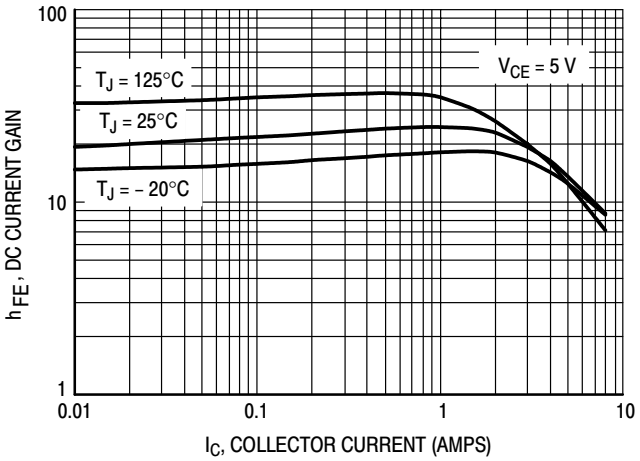


Figure 2. DC Current Gain @ 5 Volts

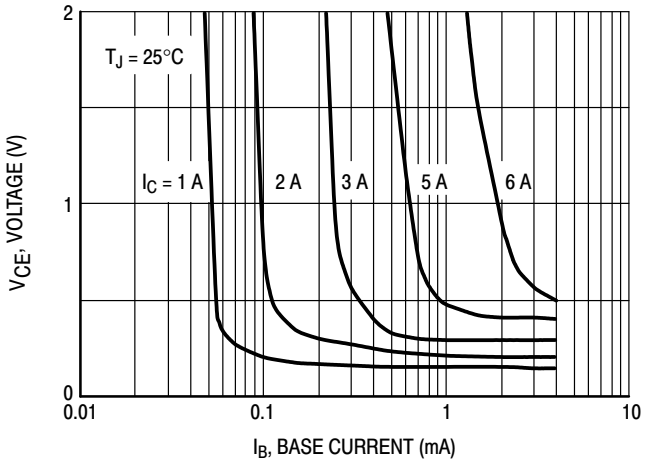


Figure 3. Collector Saturation Region

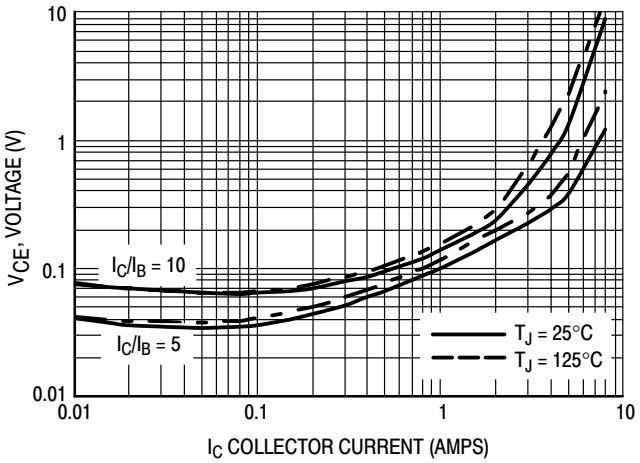


Figure 4. Collector–Emitter Saturation Voltage

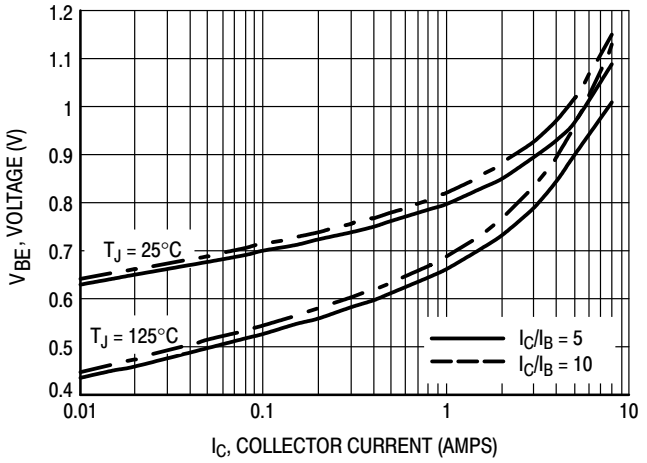


Figure 5. Base–Emitter Saturation Region

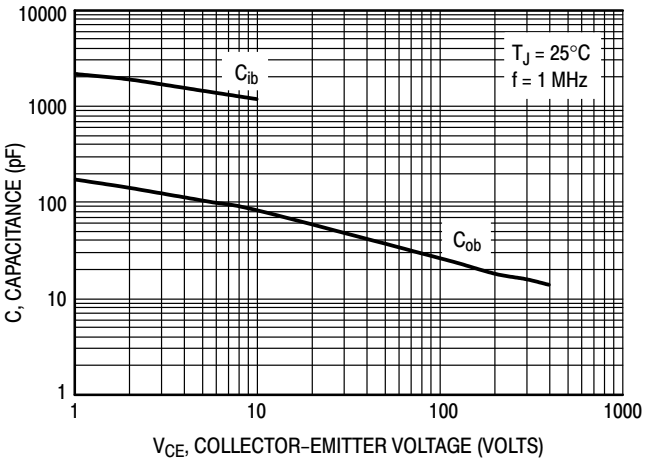


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

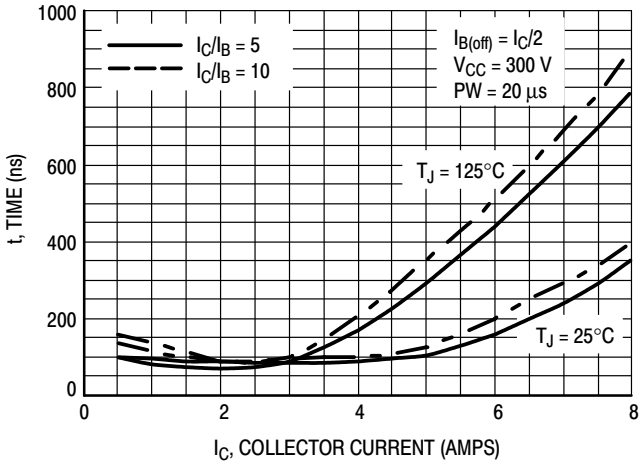


Figure 7. Resistive Switching, t_{on}

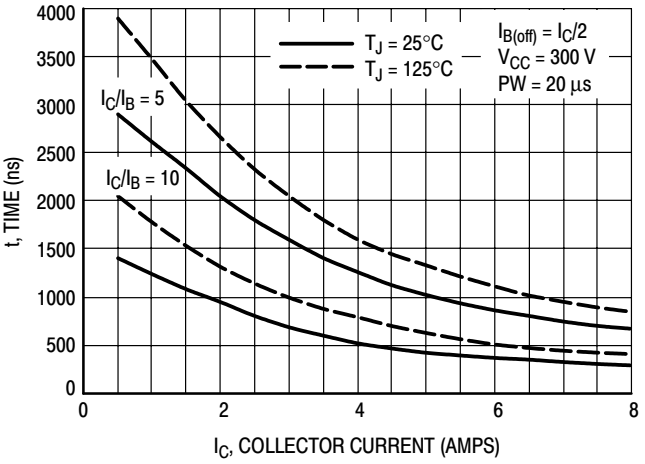


Figure 8. Resistive Switching, t_{off}

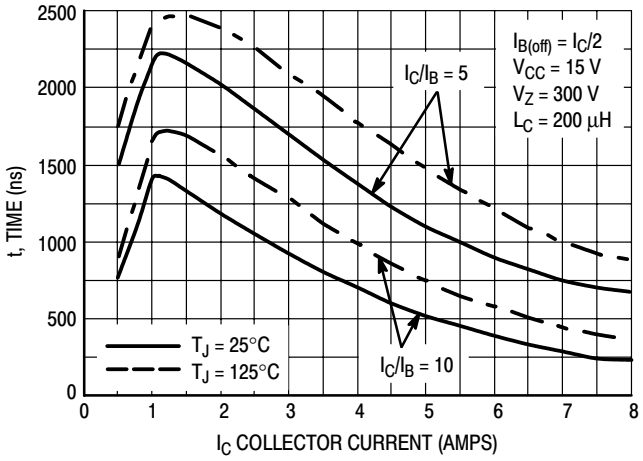


Figure 9. Inductive Storage Time, t_{si}

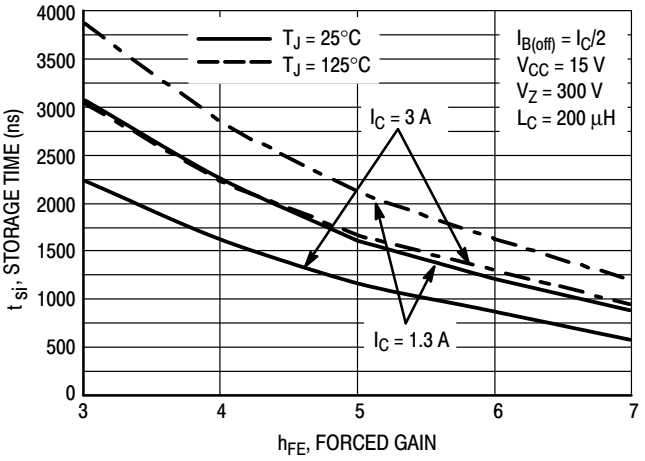


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

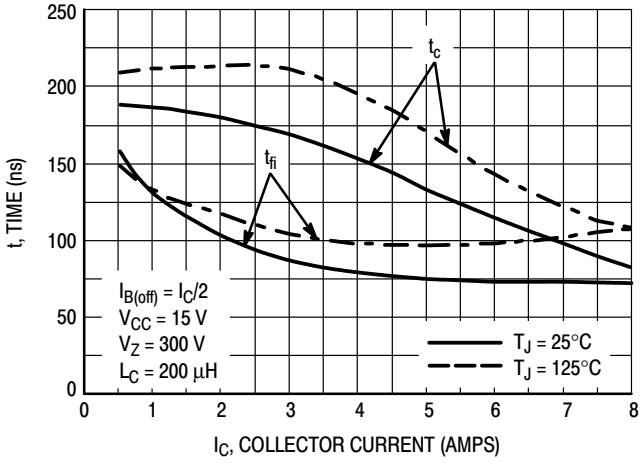


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

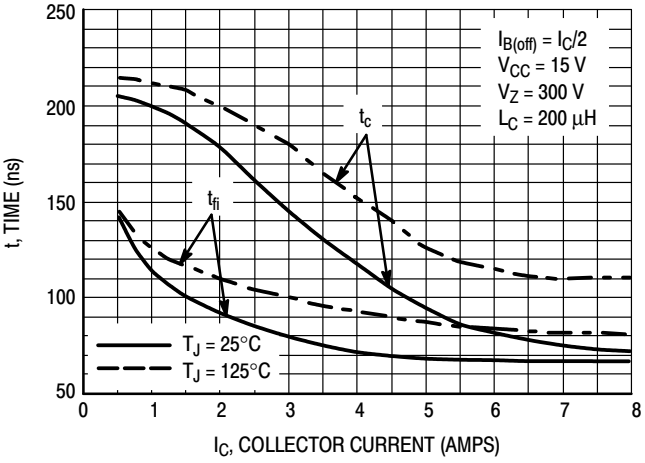


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

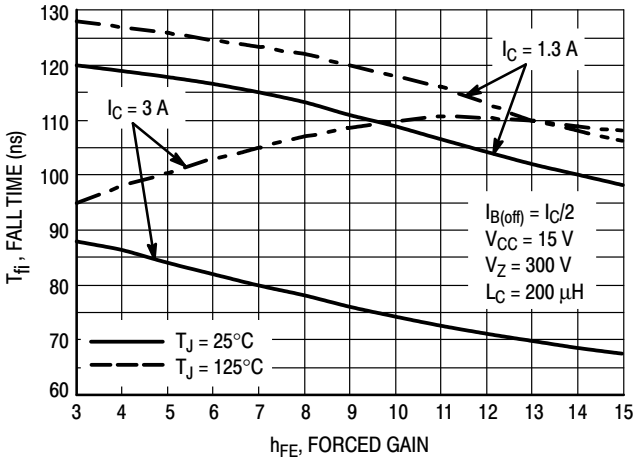


Figure 13. Inductive Fall Time

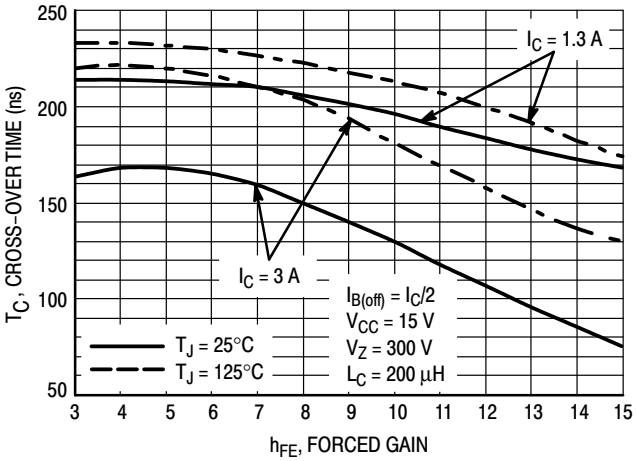


Figure 14. Inductive Cross–Over Time

GUARANTEED SAFE OPERATING AREA INFORMATION

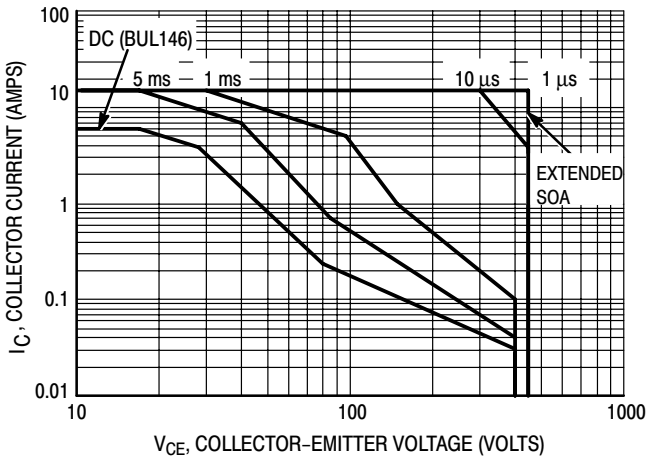


Figure 15. Forward Bias Safe Operating Area

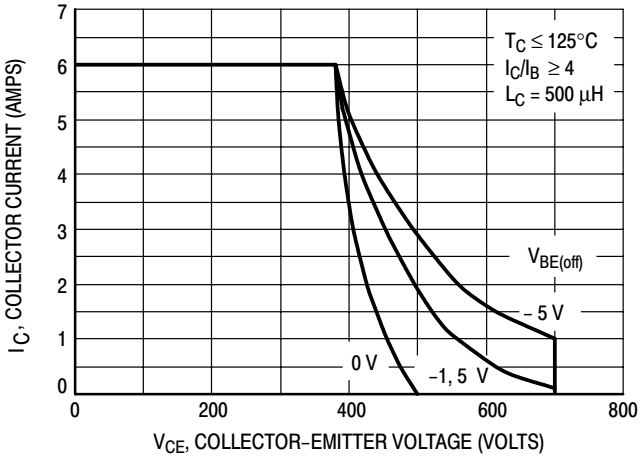


Figure 16. Reverse Bias Switching Safe Operating Area

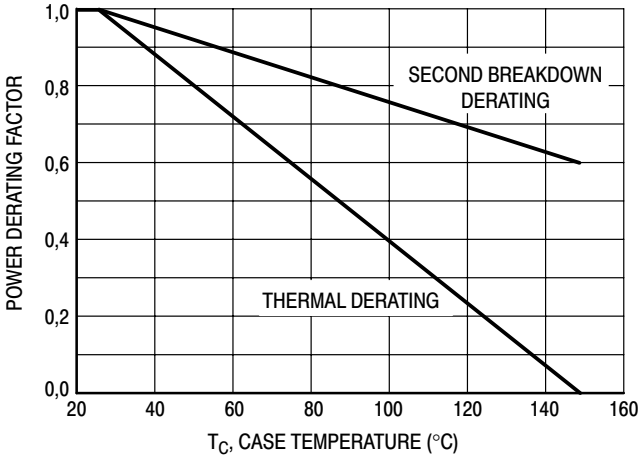


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

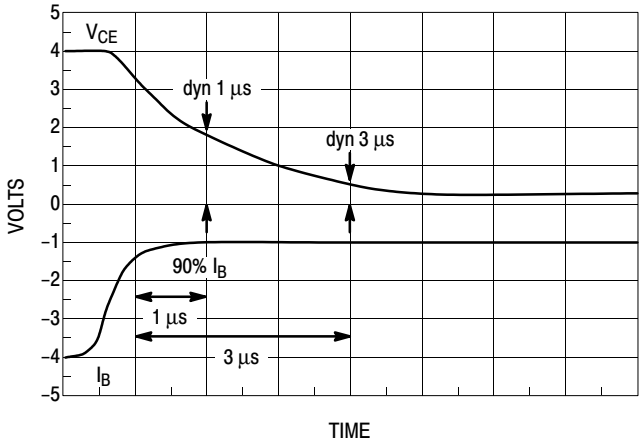


Figure 18. Dynamic Saturation Voltage Measurements

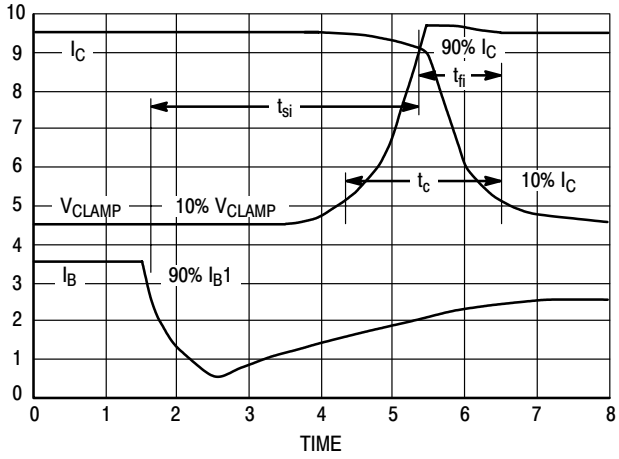
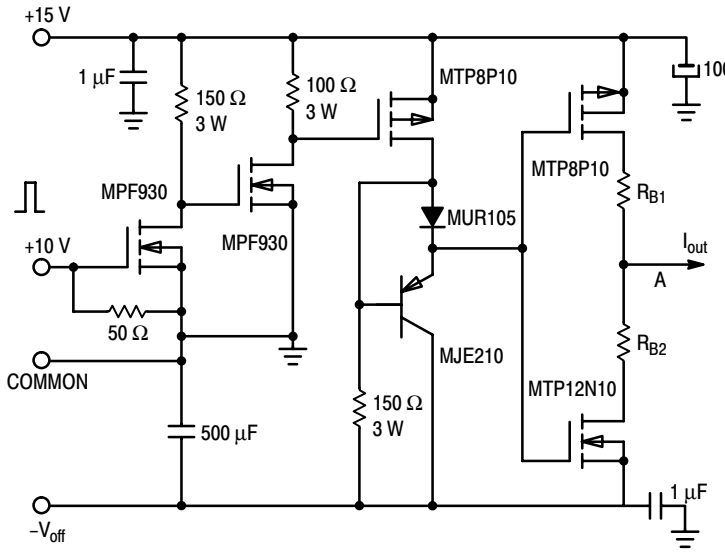
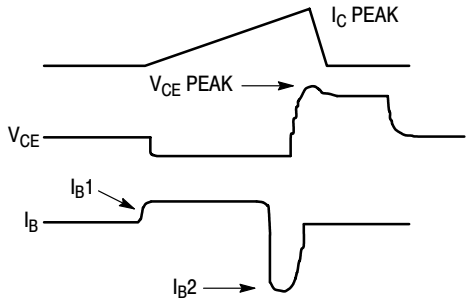


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

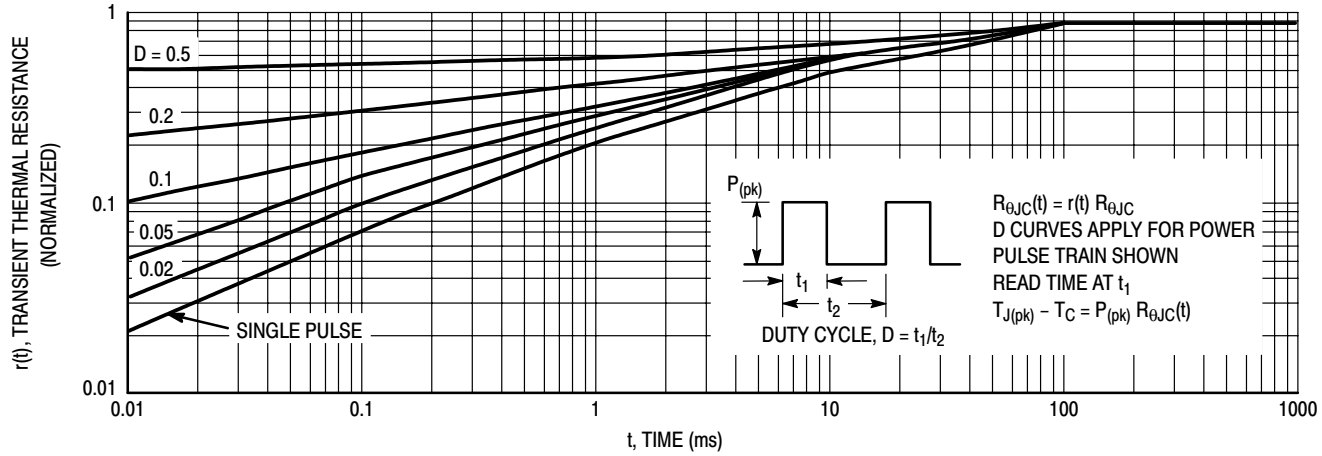


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL146

TYPICAL THERMAL RESPONSE

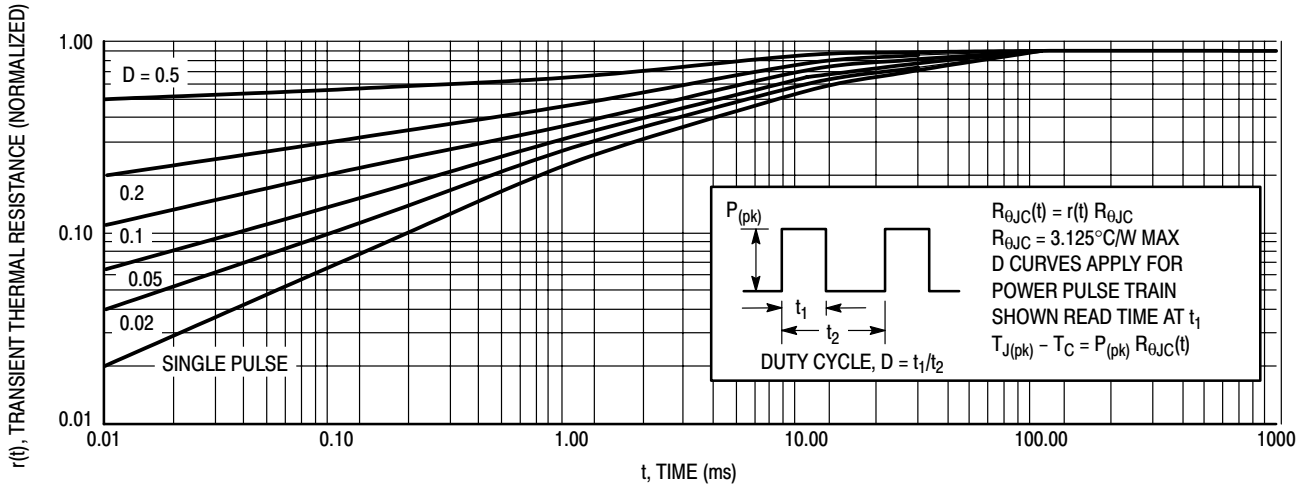


Figure 21. Typical Thermal Response for BUL146F

TEST CONDITIONS FOR ISOLATION TESTS*

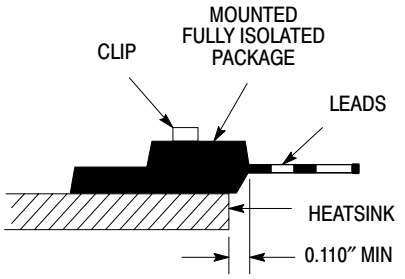


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

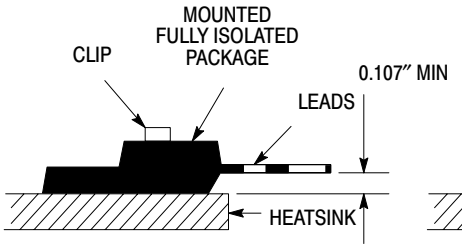


Figure 22b. Clip Mounting Position for Isolation Test Number 2

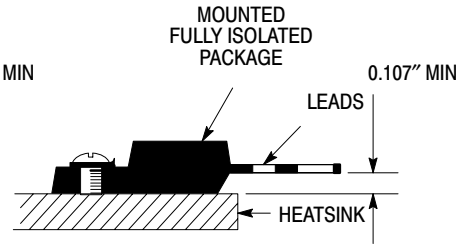


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

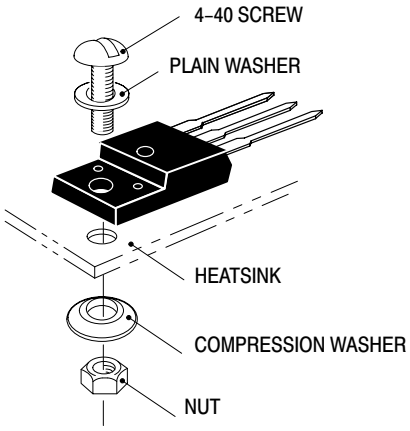


Figure 23a. Screw–Mounted

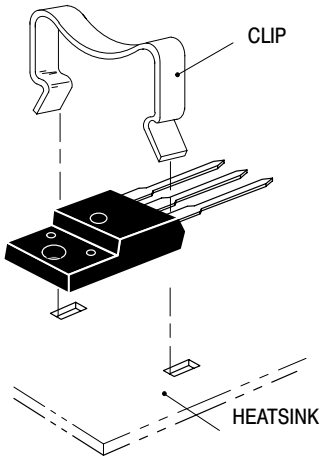


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

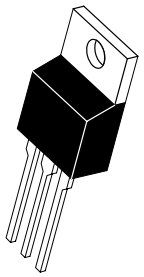
BUL147

SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
8.0 AMPERES
700 VOLTS
45 and 125 WATTS

The BUL147 have an applications specific state–of–the–art die designed for use in electric fluorescent lamp ballasts to 180 Watts and in Switchmode Power supplies for all types of electronic equipment. These high–voltage/high–speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Parametric Distributions are Tight and Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220



BUL147
CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BUL147	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.92	1.25	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		—	0.25	0.5	
(T_C = 125°C)		—	0.3	0.5	
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.35	0.7	
(T_C = 125°C)		—	0.35	0.8	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	—	34	—
(T_C = 125°C)		—	30	—	
(I_C = 4.5 Adc, V_{CE} = 1.0 Vdc)		8.0	12	—	
(T_C = 125°C)		7.0	11	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (T_C = 25°C to 125°C)		10	18	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	—	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	100	175	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{ib}	—	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18) — (I_C = 2.0 Adc, I_{B1} = 200 mAdc, V_{CC} = 300 V) — 1.0 μs	$V_{CE(dsat)}$	—	3.0	—	Volts
(T_C = 125°C)		—	5.5	—	
3.0 μs		—	0.8	—	
(T_C = 125°C)		—	1.4	—	
(I_C = 5.0 Adc, I_{B1} = 0.9 Adc, V_{CC} = 300 V) — 1.0 μs		—	3.3	—	
(T_C = 125°C)		—	8.5	—	
3.0 μs		—	0.4	—	
(T_C = 125°C)		—	1.0	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn–On Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 1.0 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	200 190	350 —	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	— —	1.0 1.6	2.5 —	μs
Turn–On Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B1} = 2.25 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	85 100	150 —	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	— —	1.5 2.0	2.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 1.0 Adc) (T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.3 1.9	2.5 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	210 230	350 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B2} = 2.25 Adc) (T_C = 125°C)	t_{fi}	— —	80 100	150 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.6 2.1	3.2 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	170 200	300 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B2} = 0.9 Adc) (T_C = 125°C)	t_{fi}	60 —	— 150	180 —	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 —	— 4.3	3.8 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	200 330	350 —	ns

TYPICAL STATIC CHARACTERISTICS

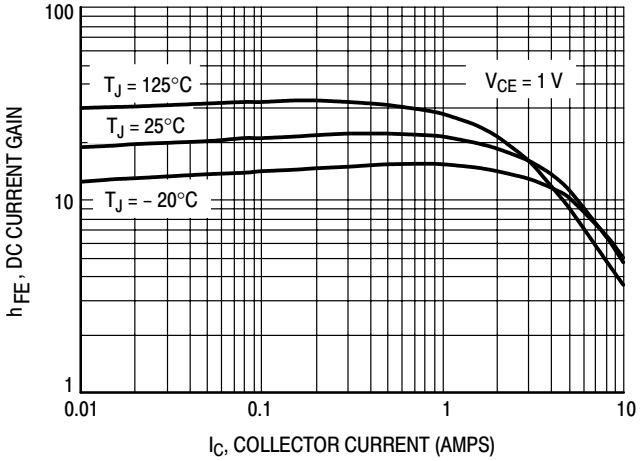


Figure 1. DC Current Gain @ 1 Volt

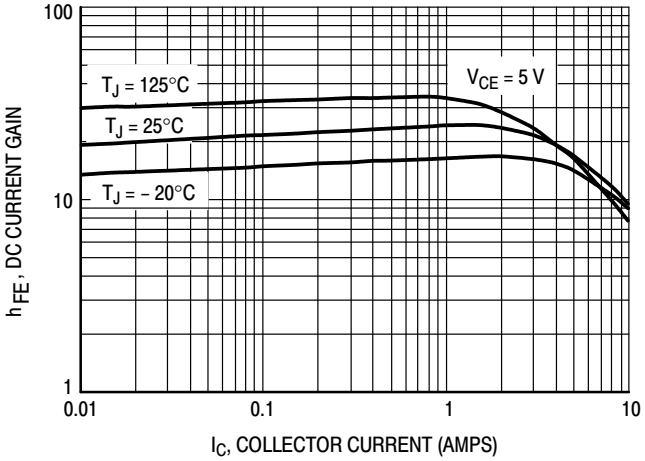


Figure 2. DC Current Gain @ 5 Volts

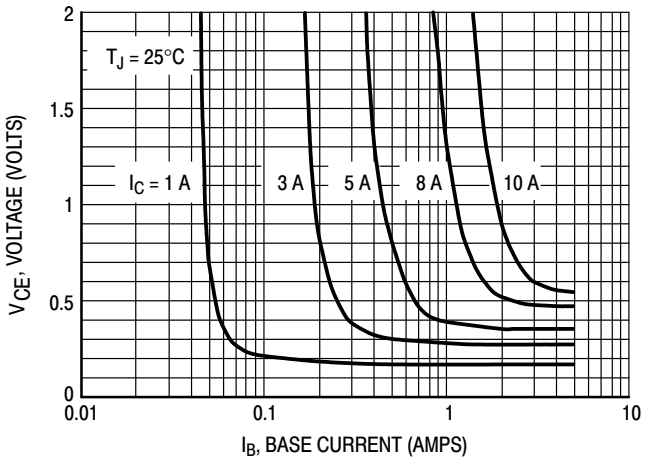


Figure 3. Collector Saturation Region

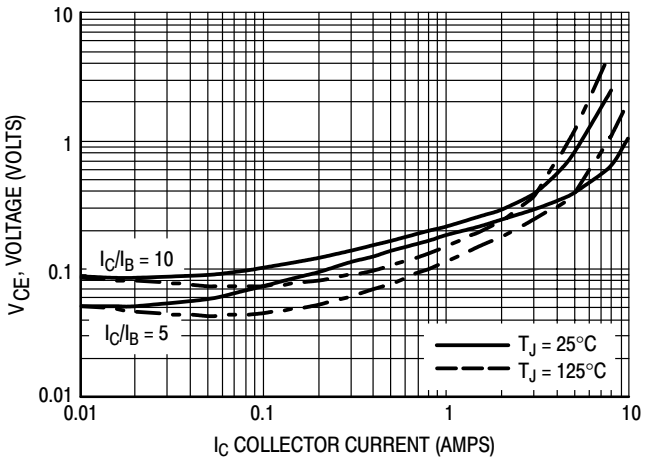


Figure 4. Collector–Emitter Saturation Voltage

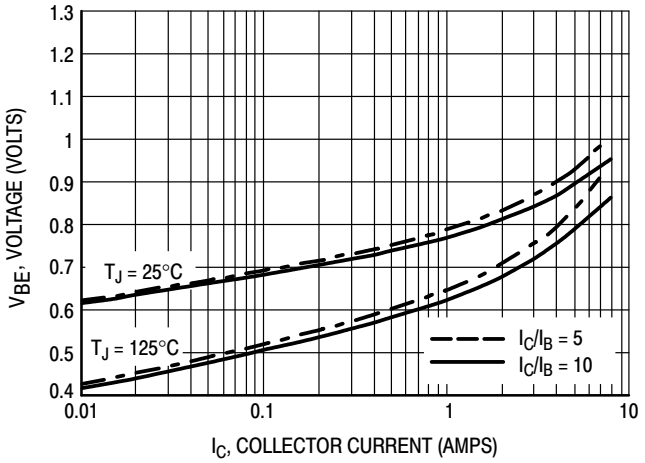


Figure 5. Base–Emitter Saturation Region

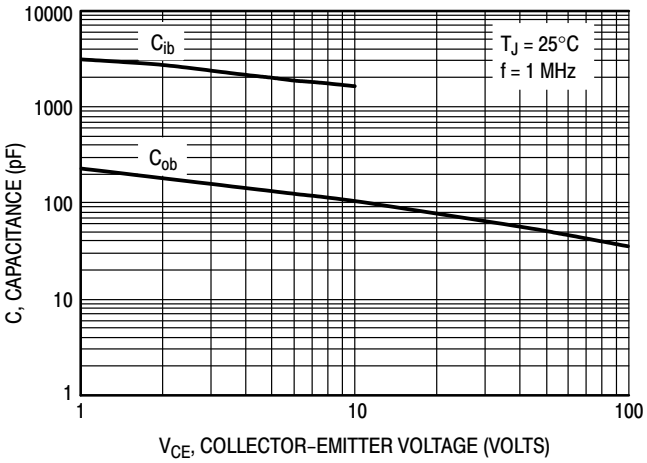


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

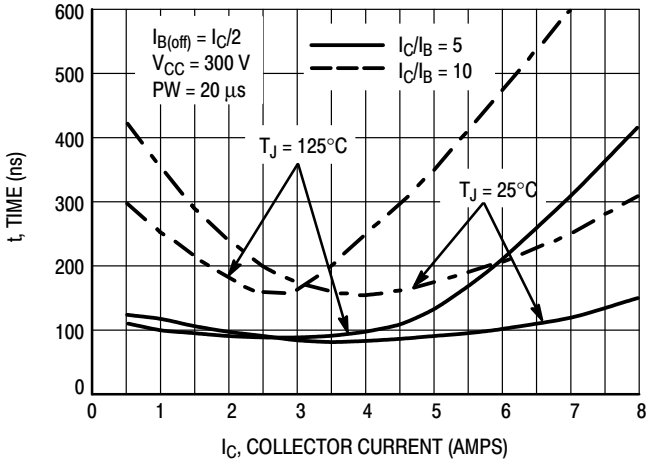


Figure 7. Resistive Switching, t_{on}

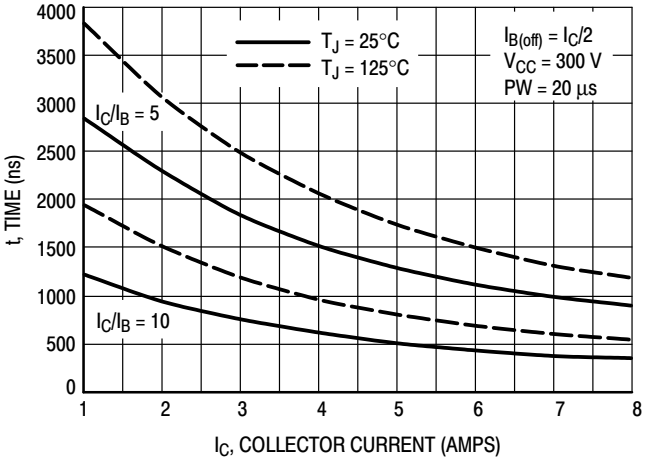


Figure 8. Resistive Switching, t_{off}

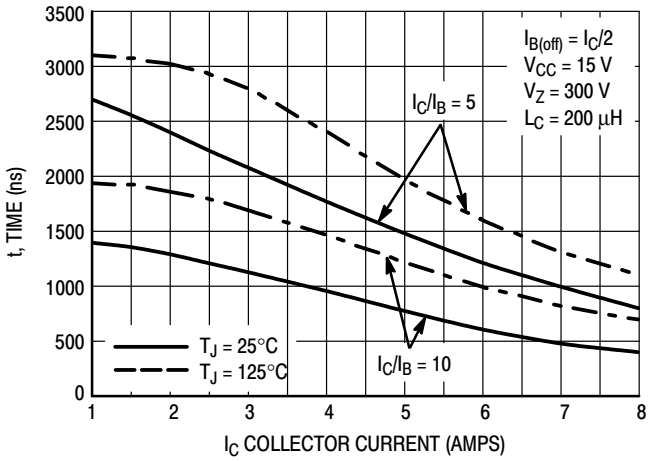


Figure 9. Inductive Storage Time, t_{si}

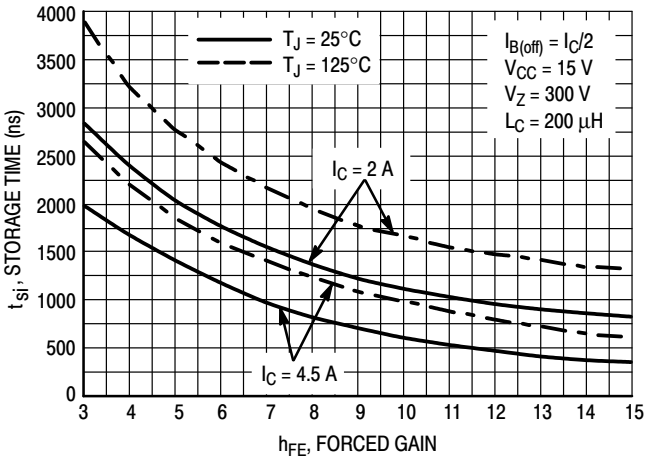


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

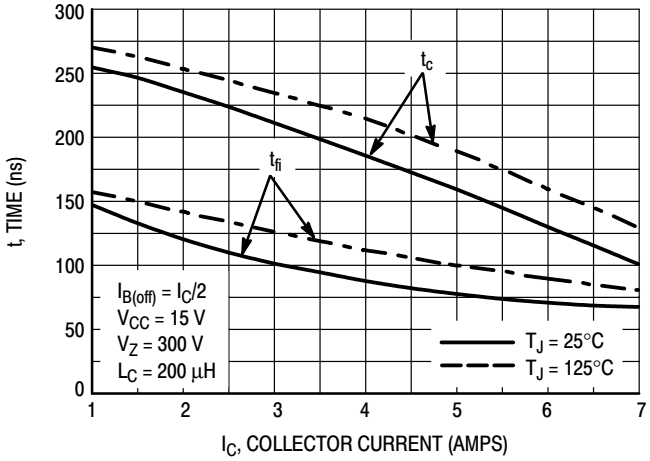


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

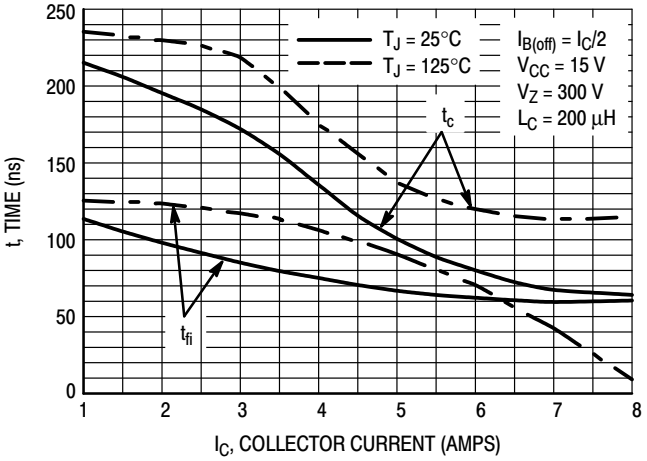


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

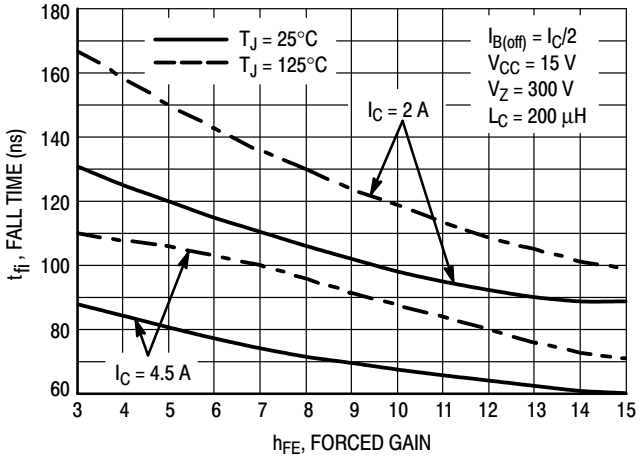


Figure 13. Inductive Fall Time

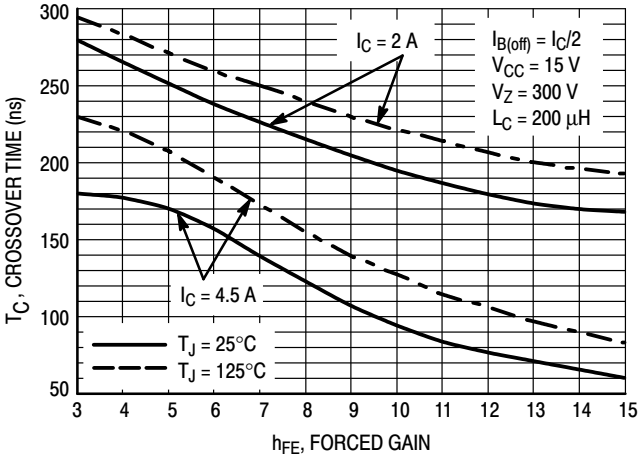


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

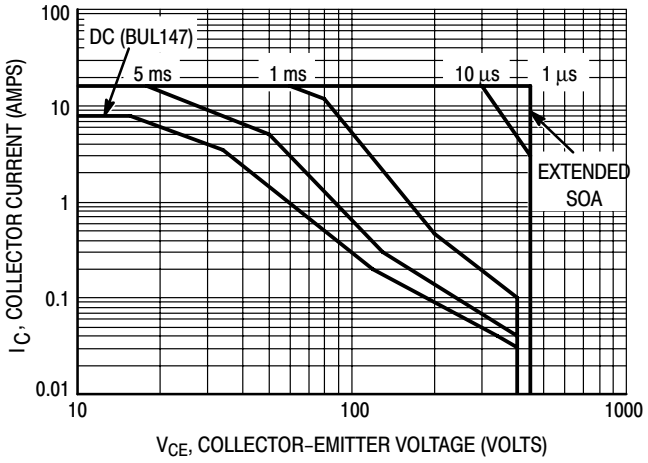


Figure 15. Forward Bias Safe Operating Area

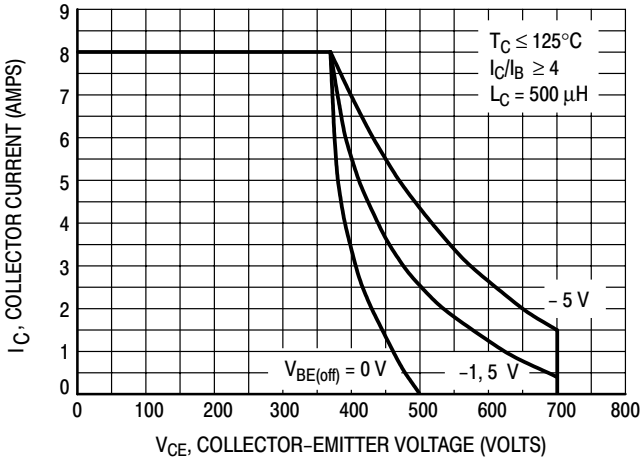


Figure 16. Reverse Bias Switching Safe Operating Area

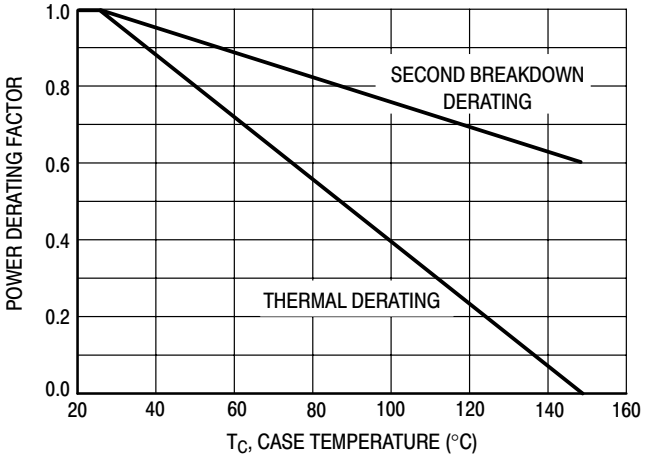


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and NO TAG. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

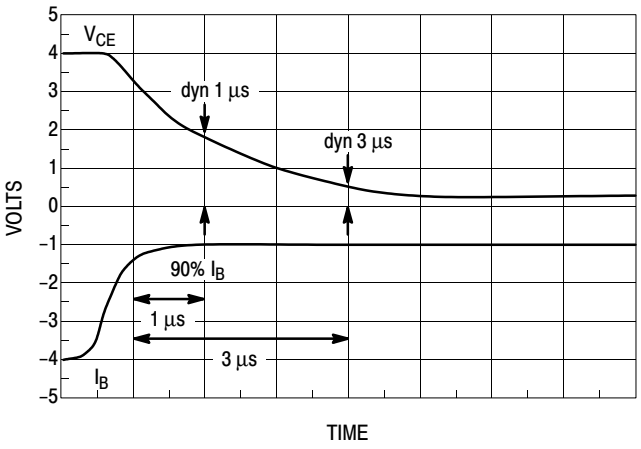


Figure 18. Dynamic Saturation Voltage Measurements

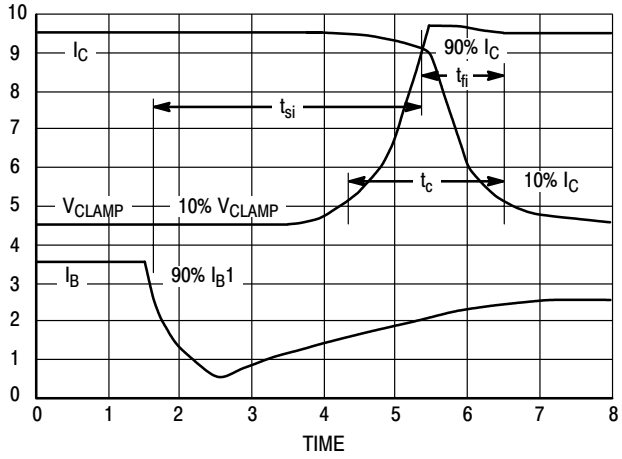
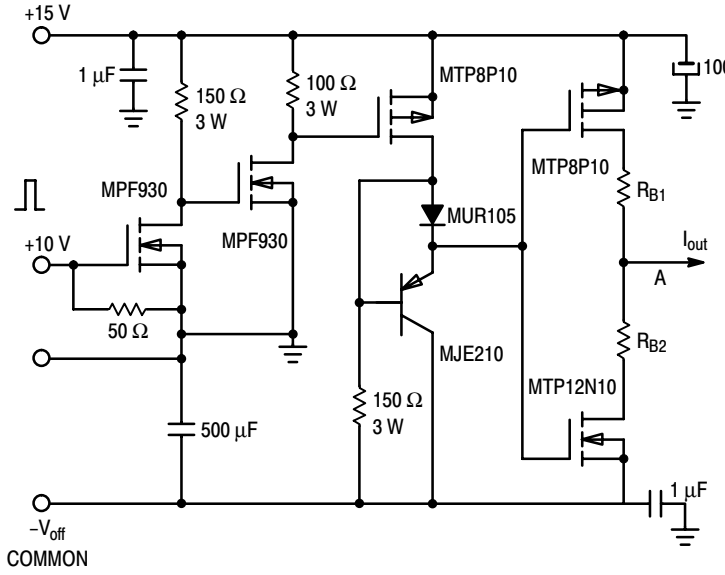
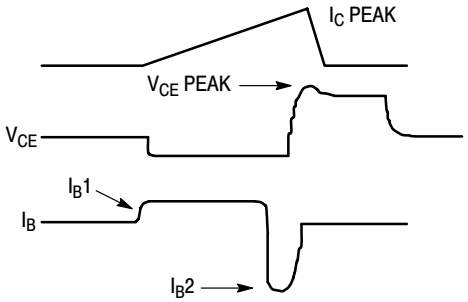


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

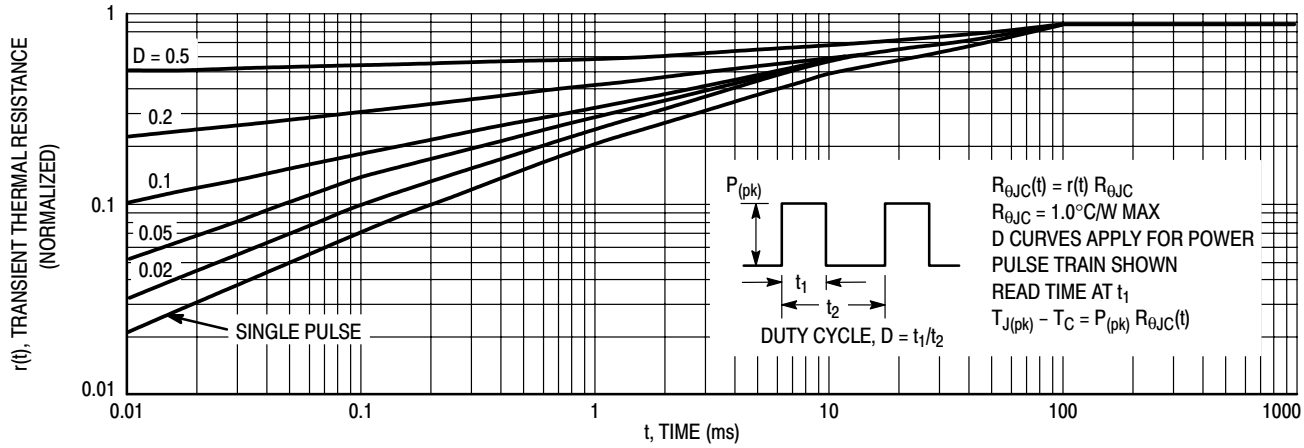


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL147

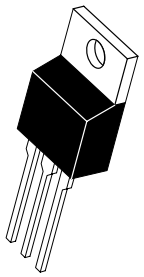
BUL44

SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
2.0 AMPERES
700 VOLTS
40 and 100 WATTS

The BUL44 have an applications specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Tight Parametric Distributions are Consistent Lot–to–Lot



BUL44
CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	2.0 5.0	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	1.0 2.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

May, 2001 – Rev. 4
Publication Order Number:
BUL44/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	—	0.85	1.1	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)		—	0.92	1.25	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)		—	0.20	0.5	
(T_C = 125°C)		—	0.20	0.5	
(I_C = 1.0 Adc, I_B = 0.2 Adc)		—	0.25	0.6	
(T_C = 125°C)		—	0.25	0.6	
DC Current Gain	h_{FE}				—
(I_C = 0.2 Adc, V_{CE} = 5.0 Vdc)		14	—	34	
(T_C = 125°C)		—	32	—	
(I_C = 0.4 Adc, V_{CE} = 1.0 Vdc)		12	20	—	
(T_C = 125°C)		12	20	—	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		8.0	14	—	
(T_C = 125°C)		7.0	13	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	22	—	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{OB}	—	38	60	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{IB}	—	380	600	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} — (I_C = 0.4 Adc, I_{B1} = 40 mAdc, V_{CC} = 300 V), 1.0 μs	$V_{CE(dsat)}$	—	2.5	—	Vdc
(T_C = 125°C)		—	2.7	—	
3.0 μs		—	1.3	—	
(T_C = 125°C)		—	1.15	—	
(I_C = 1.0 Adc, I_{B1} = 0.2 Adc, V_{CC} = 300 V), 1.0 μs		—	3.2	—	
(T_C = 125°C)		—	7.5	—	
3.0 μs		—	1.25	—	
(T_C = 125°C)		—	1.6	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(continued)

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn–On Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	40 40	100 —	ns
Turn–Off Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{off}	— —	1.5 2.0	2.5 —	μs
Turn–On Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B1} = 0.5 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	85 85	150 —	ns
Turn–Off Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{off}	— —	1.75 2.10	2.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc) (T_C = 125°C)	t_{fi}	— —	125 120	200 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	0.7 0.8	1.25 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	110 110	200 —	ns
Fall Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc) (T_C = 125°C)	t_{fi}	— —	110 120	175 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.7 2.25	2.75 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	180 210	300 —	ns
Fall Time	(I_C = 0.8 Adc, I_{B1} = 160 mAdc I_{B2} = 160 mAdc) (T_C = 125°C)	t_{fi}	70 —	— 180	170 —	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 —	— 4.2	3.8 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	190 350	300 —	ns

TYPICAL STATIC CHARACTERISTICS

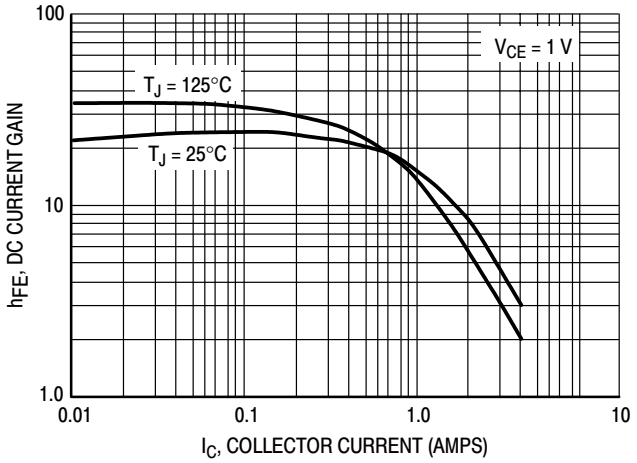


Figure 21. DC Current Gain at 1 Volt

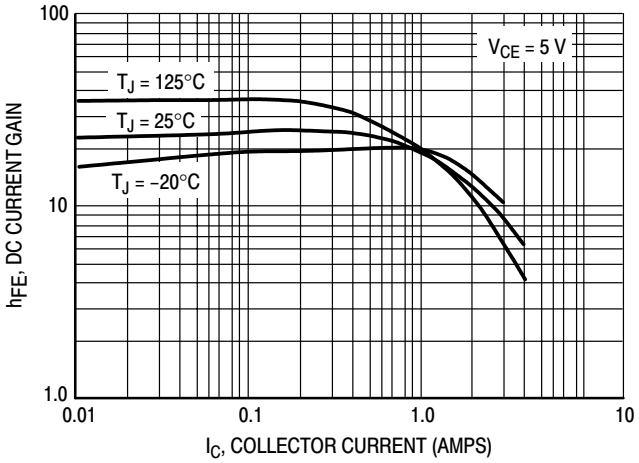


Figure 22. DC Current Gain at 5 Volts

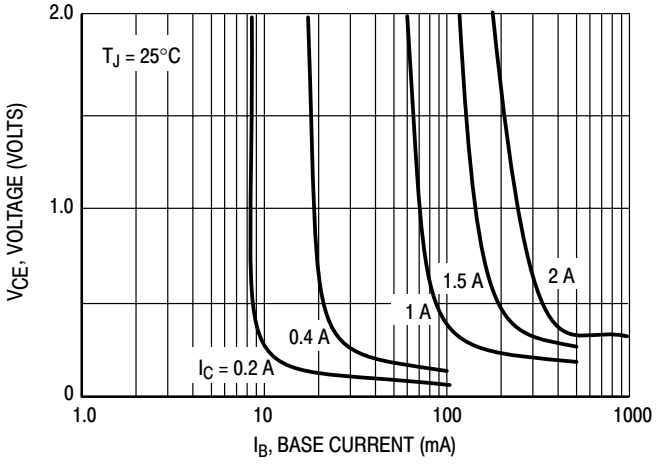


Figure 23. Collector Saturation Region

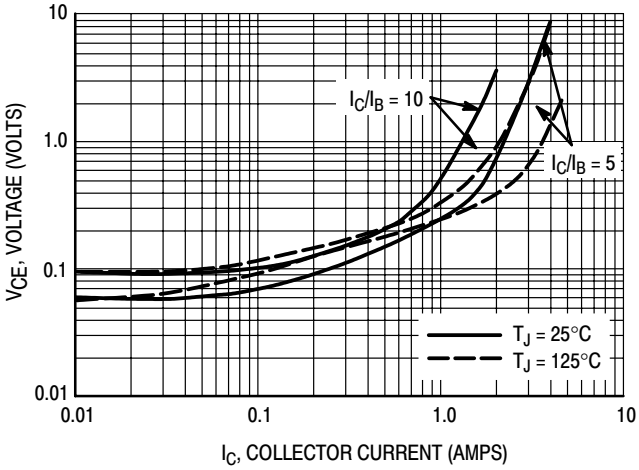


Figure 24. Collector–Emitter Saturation Voltage

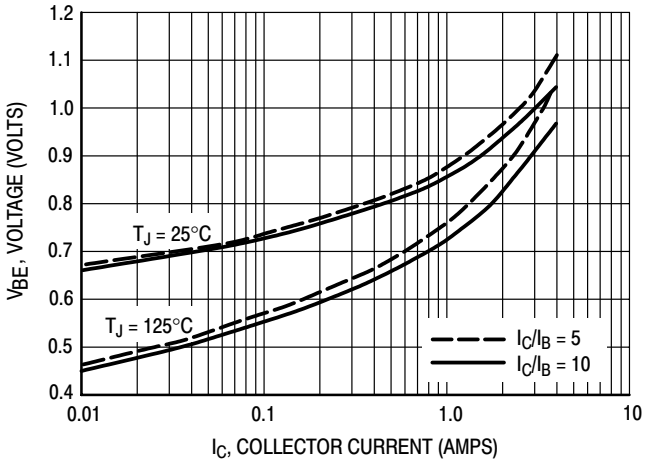


Figure 25. Base–Emitter Saturation Region

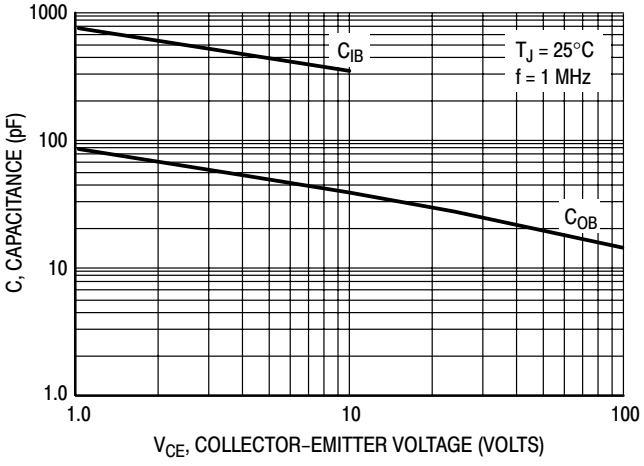


Figure 26. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

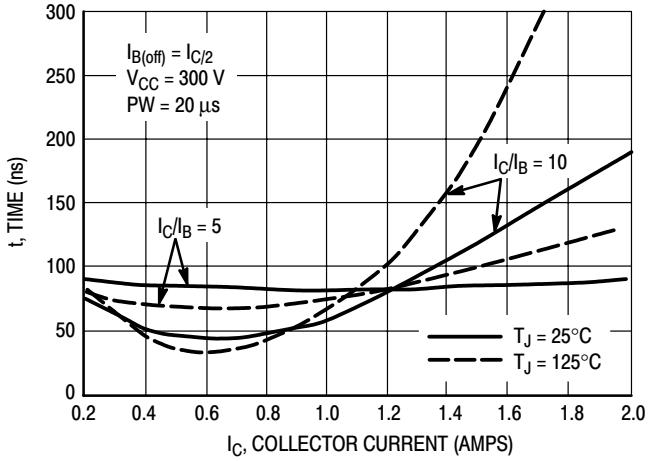


Figure 27. Resistive Switching, t_{on}

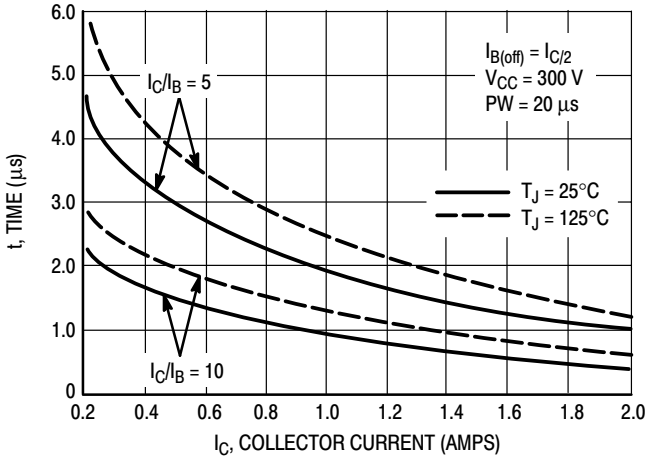


Figure 28. Resistive Switching, t_{off}

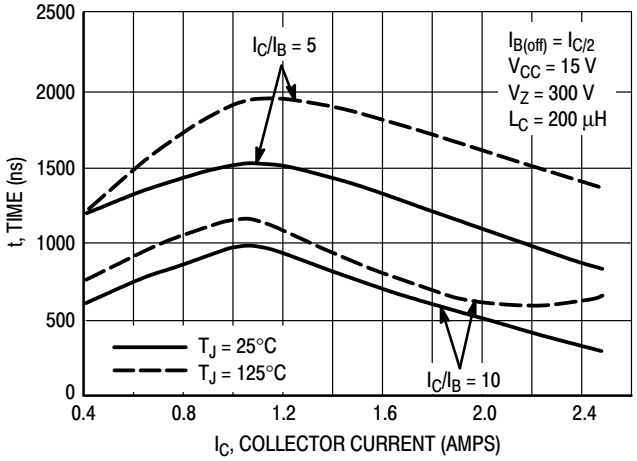


Figure 29. Inductive Storage Time, t_{si}

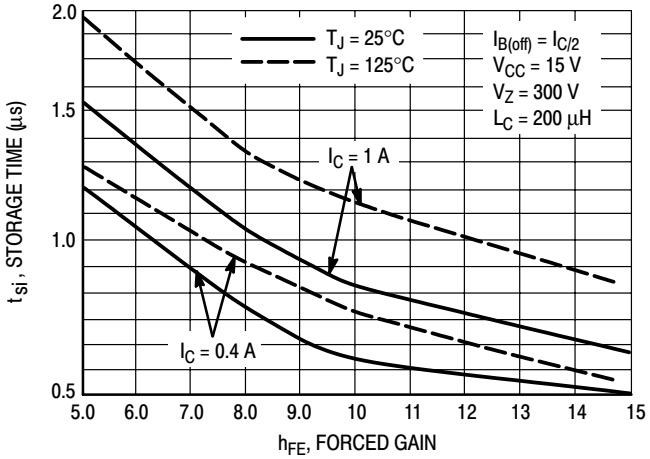


Figure 30. Inductive Storage Time

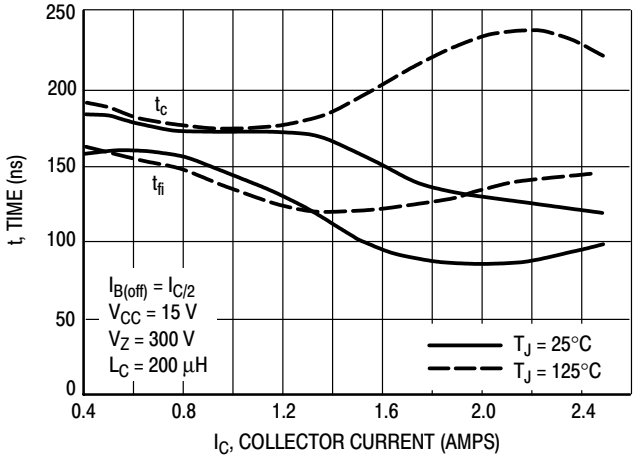


Figure 31. Inductive Switching, t_c and t_{fi} I_C/I_B = 5

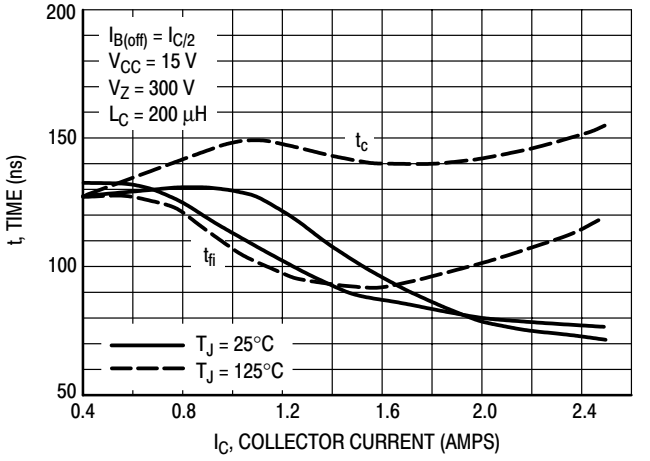


Figure 32. Inductive Switching, t_c and t_{fi} I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

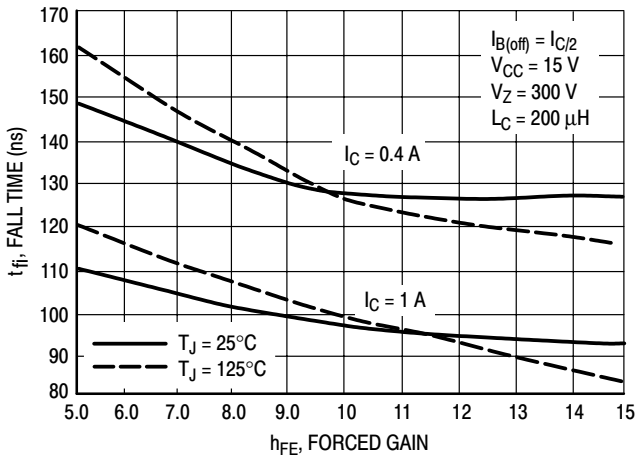


Figure 33. Inductive Fall Time

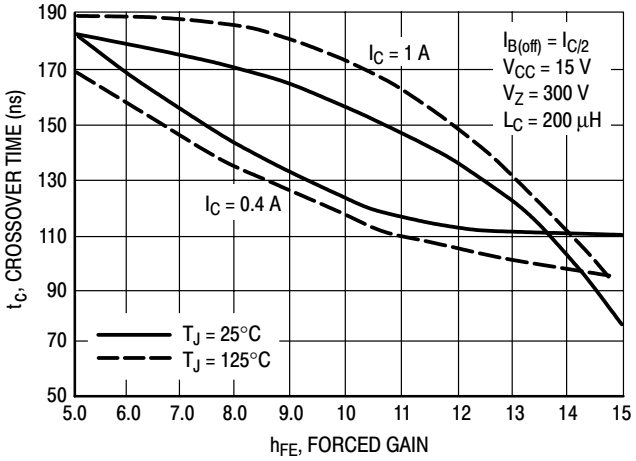


Figure 34. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

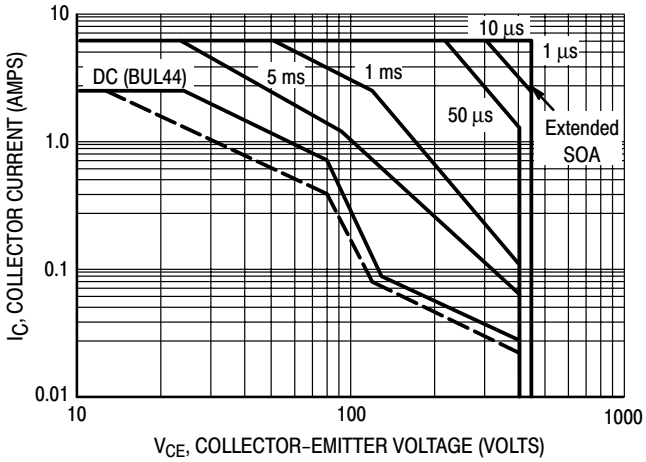


Figure 35. Forward Bias Safe Operating Area

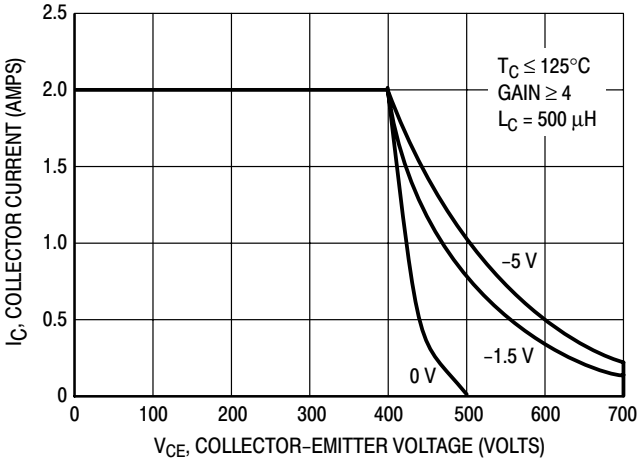


Figure 36. Reverse Bias Switching Safe Operating Area

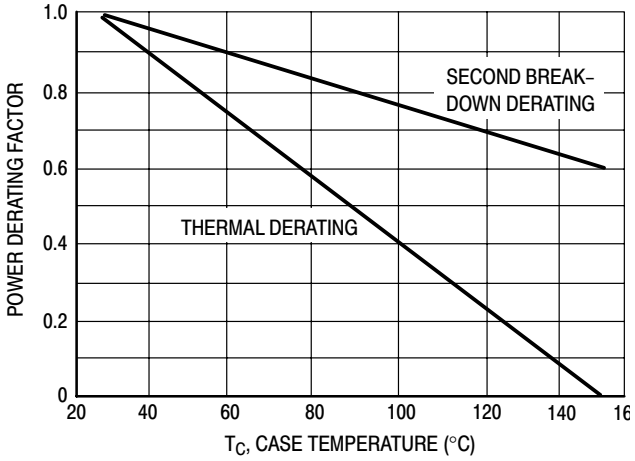


Figure 37. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 35 is based on T_C = 25°C; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on figure 35 may be found at any case temperature by using the appropriate curve on figure 37. $T_{J(PK)}$ may be calculated from the data in figure 40. At any case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 36). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

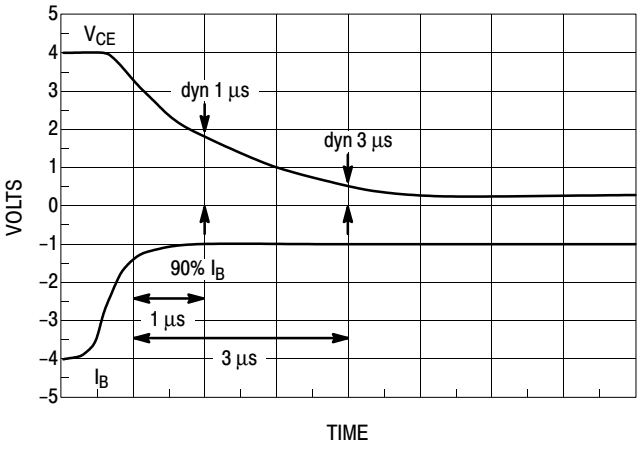


Figure 38. Dynamic Saturation Voltage Measurements

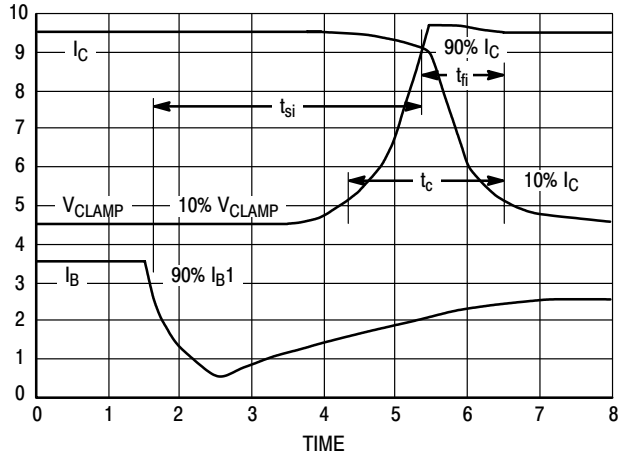
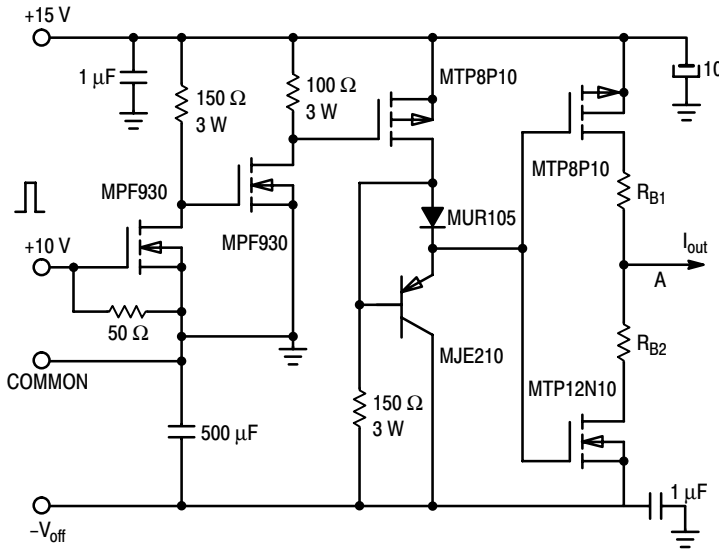
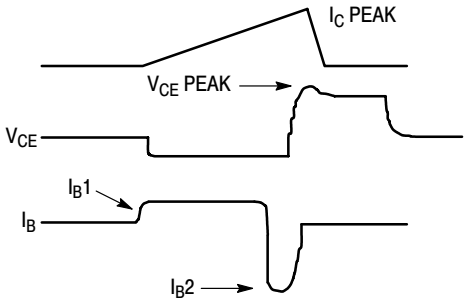


Figure 39. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

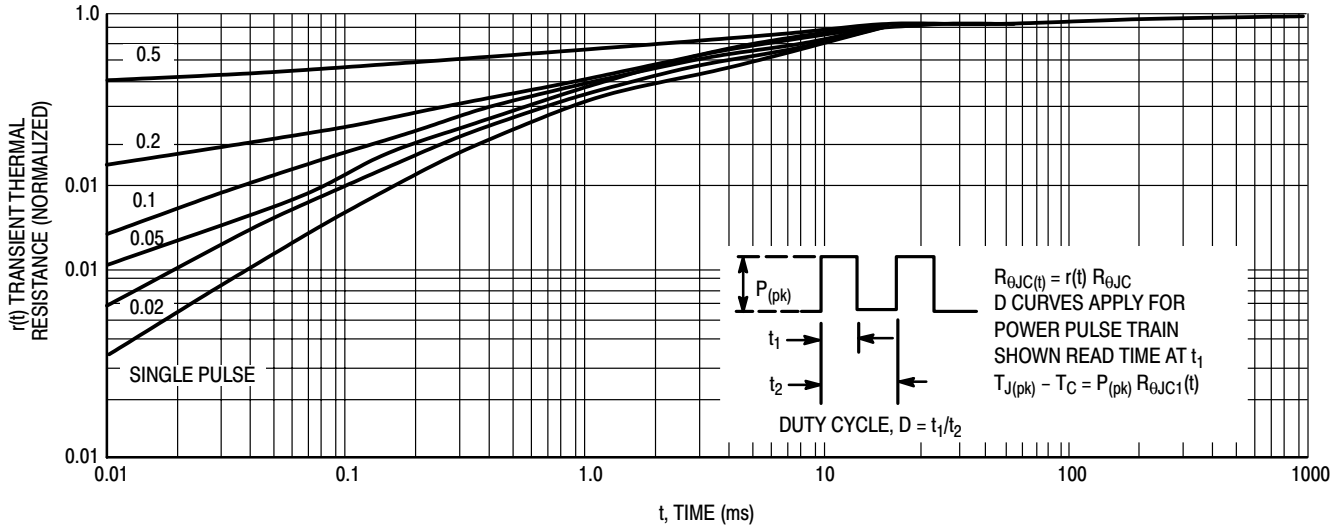
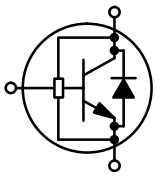


Figure 40. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL44

BUL45D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
5 AMPERES
700 VOLTS
75 WATTS

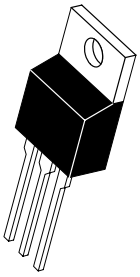


The BUL45D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.65 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

March, 2001 – Rev. 2
Publication Order Number:
BUL45D2/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	450		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	910		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14.1		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.89 0.79	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.28 0.32	0.4 0.5	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.32 0.38	0.5 0.6	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.46 0.62	0.75 1	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	22 20	34 29		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 7	14 9.5		
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1 Adc)	@ T_C = 25°C @ T_C = 125°C	V_{EC}		1.04 0.7	1.5	V
(I_{EC} = 2 Adc)	@ T_C = 25°C @ T_C = 125°C			1.2	1.6	
(I_{EC} = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.85 0.62	1.2	
Forward Recovery Time (see Figure 27) (I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C	T_{fr}		330		ns
(I_F = 2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			360		
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			320		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)				f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)				C_{ob}		50	75	pF
Input Capacitance (V_{EB} = 8 Vdc)				C_{ib}		340	500	pF
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 A I_{B1} = 100 mA V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		3.7 9.4		V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C			0.35 2.7		V
	I_C = 2 A I_{B1} = 0.8 A V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C			3.9 12		V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C			0.4 1.5		V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}		90 105	150	ns
Turn–off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.5	1.3	µs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}		90 110	150	ns
Turn–off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}	2.1	 3.1	2.4	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc		@ T_C = 25°C @ T_C = 125°C	t_f		90 93	150	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s		0.72 1.05	0.9	µs
Crossover Time			@ T_C = 25°C @ T_C = 125°C	t_c		95 95	150	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc		@ T_C = 25°C @ T_C = 125°C	t_f		80 105	150	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s	1.95	 2.9	2.25	µs
Crossover Time			@ T_C = 25°C @ T_C = 125°C	t_c		225 450	300	ns

TYPICAL STATIC CHARACTERISTICS

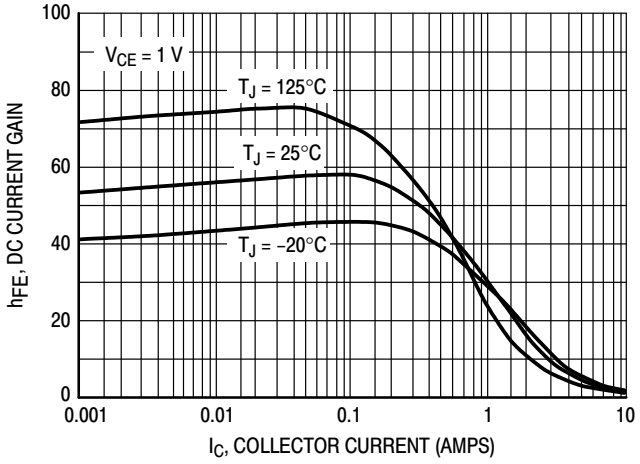


Figure 41. DC Current Gain @ 1 Volt

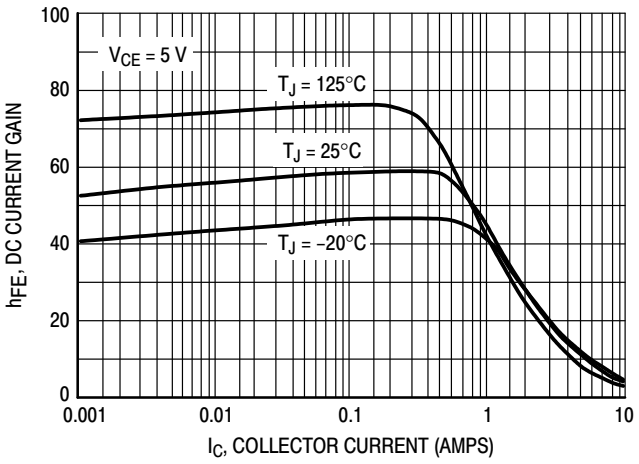


Figure 42. DC Current Gain @ 5 Volt

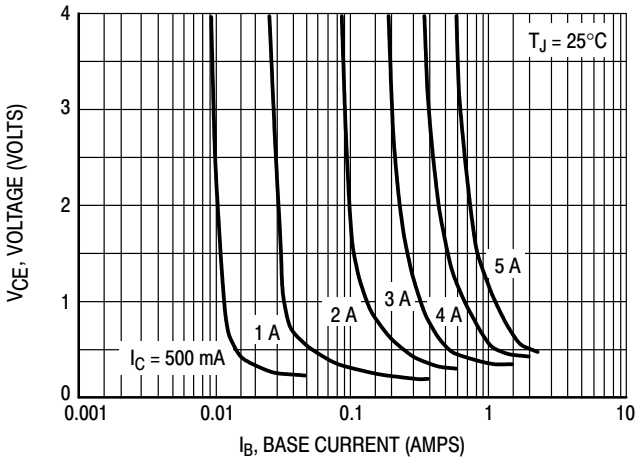


Figure 43. Collector Saturation Region

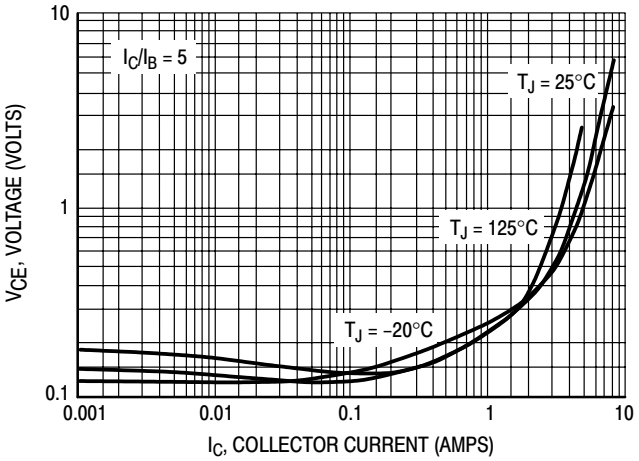


Figure 44. Collector–Emitter Saturation Voltage

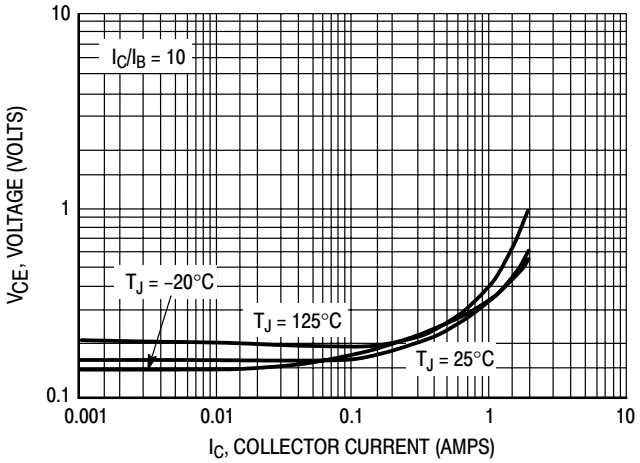


Figure 45. Collector–Emitter Saturation Voltage

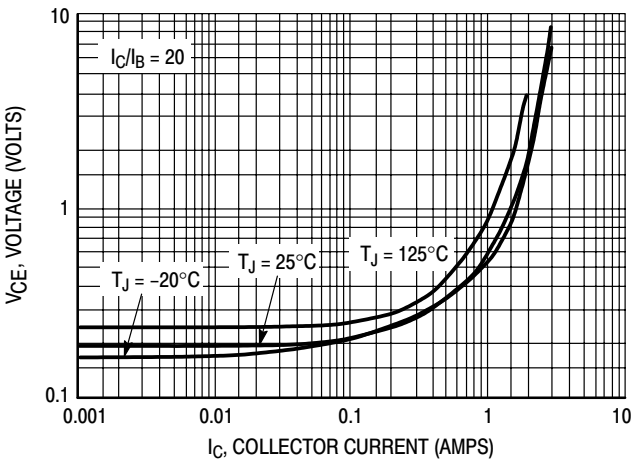


Figure 46. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

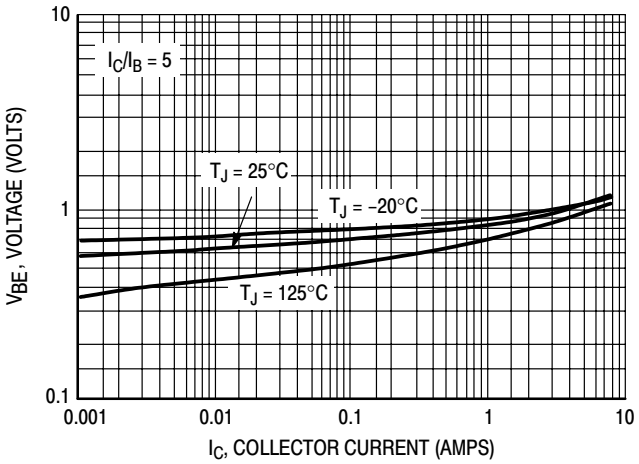


Figure 47. Base−Emitter Saturation Region

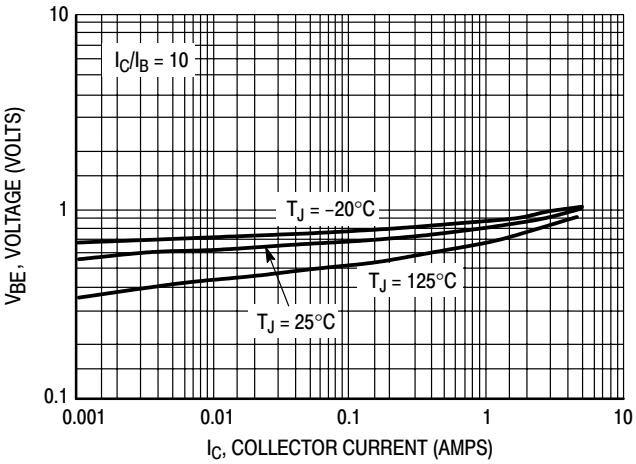


Figure 48. Base−Emitter Saturation Region

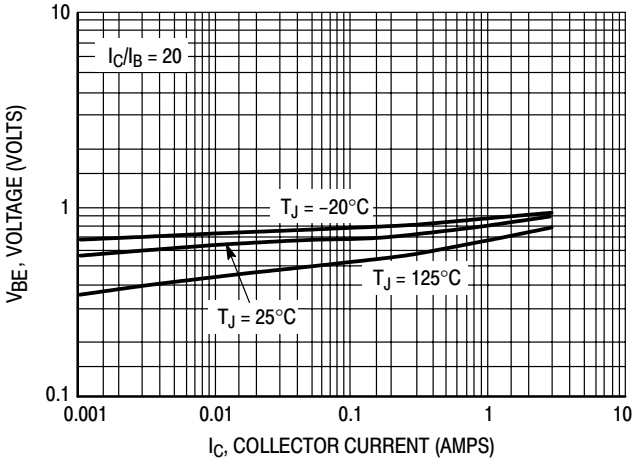


Figure 49. Base−Emitter Saturation Region

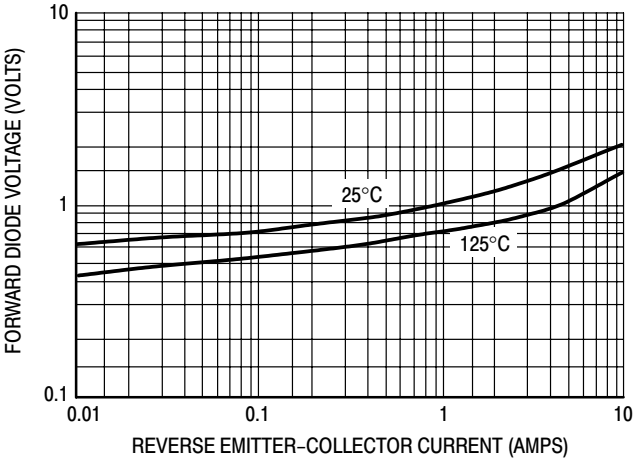


Figure 50. Forward Diode Voltage

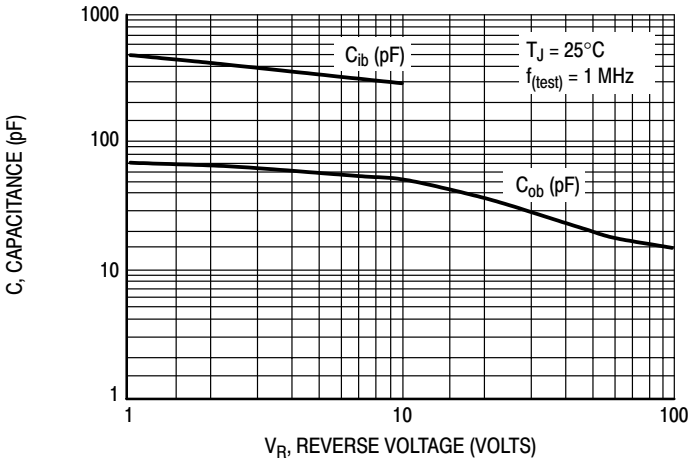


Figure 51. Capacitance

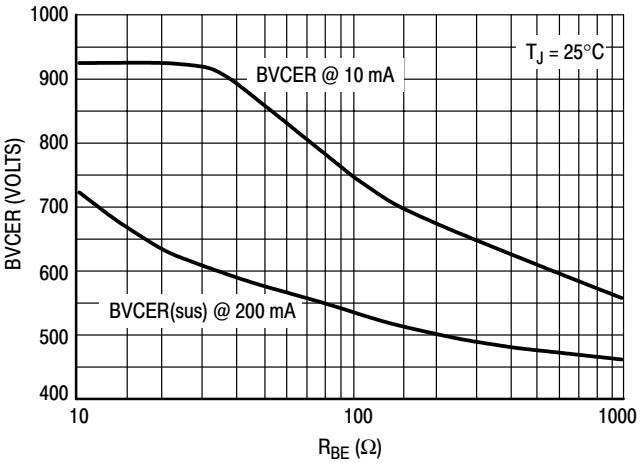


Figure 52. BVCER = f(ICER)

TYPICAL SWITCHING CHARACTERISTICS

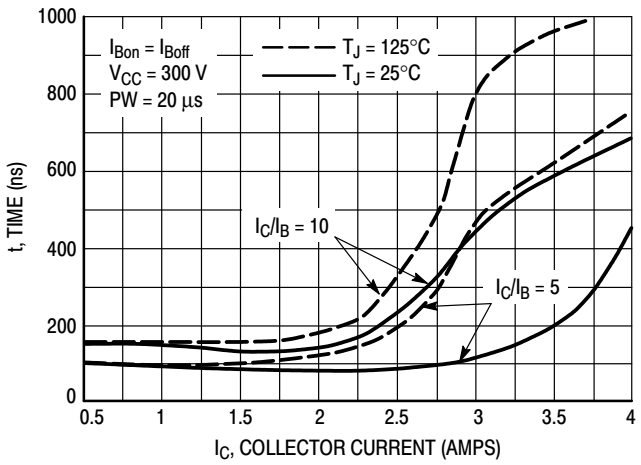


Figure 53. Resistive Switch Time, t_{on}

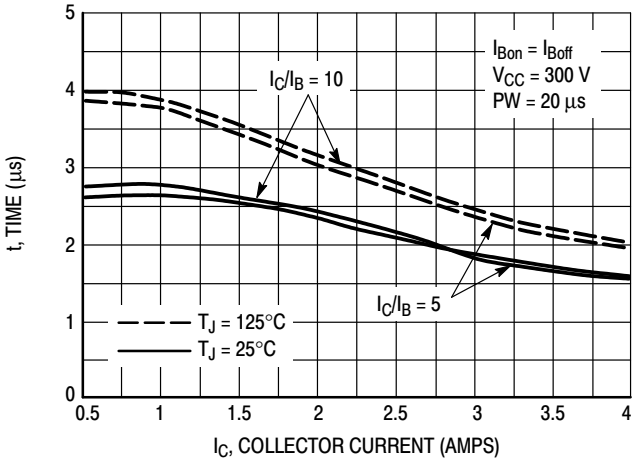


Figure 54. Resistive Switch Time, t_{off}

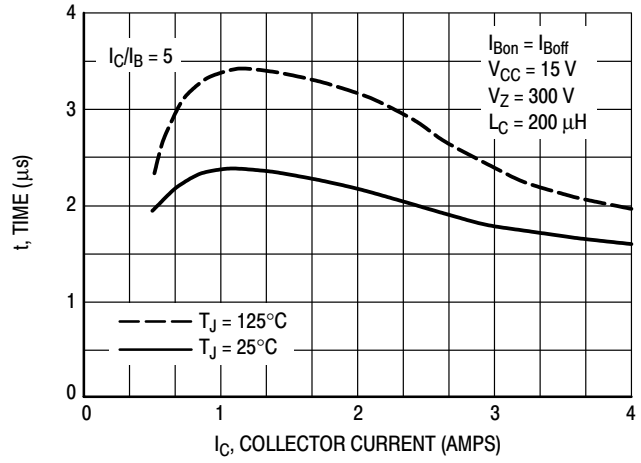


Figure 55. Inductive Storage Time, t_{si} @ I_C/I_B = 5

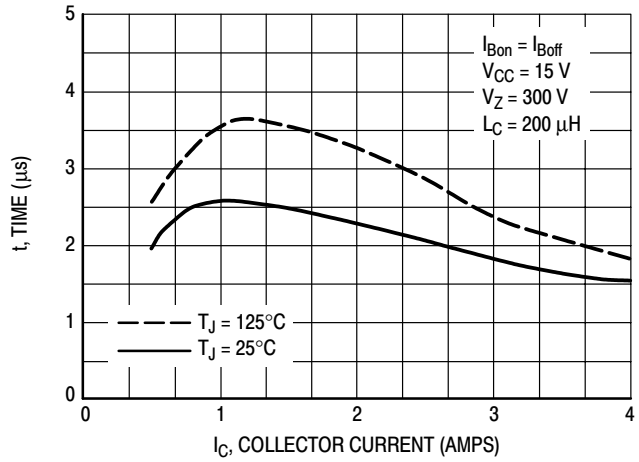


Figure 56. Inductive Storage Time, t_{si} @ I_C/I_B = 10

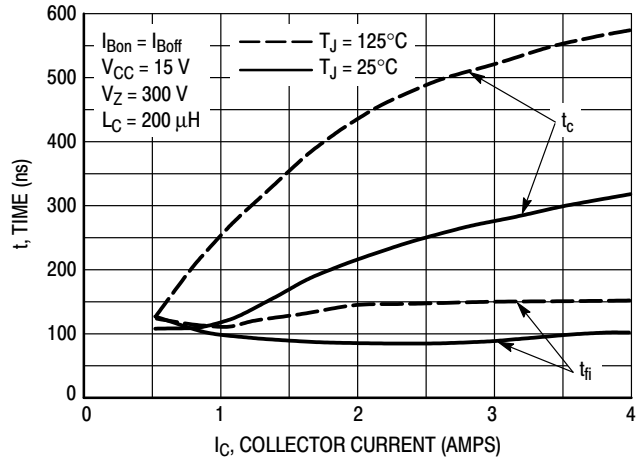


Figure 57. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

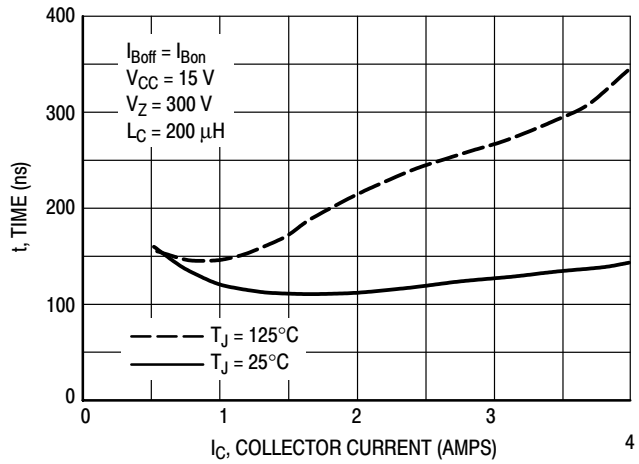


Figure 58. Inductive Switching, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

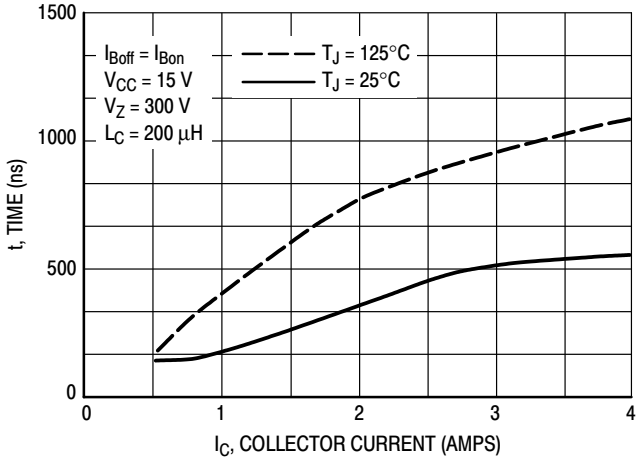


Figure 59. Inductive Switching, t_c @ I_C/I_B = 10

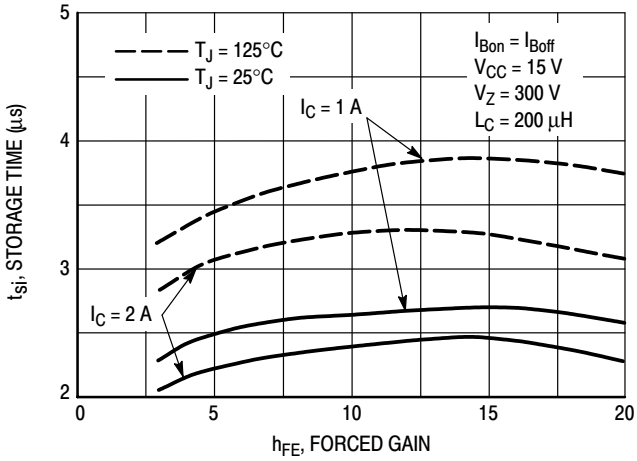


Figure 60. Inductive Storage Time

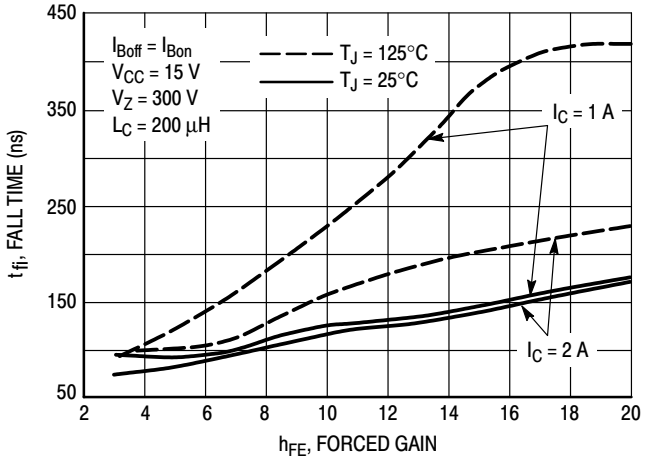


Figure 61. Inductive Fall Time

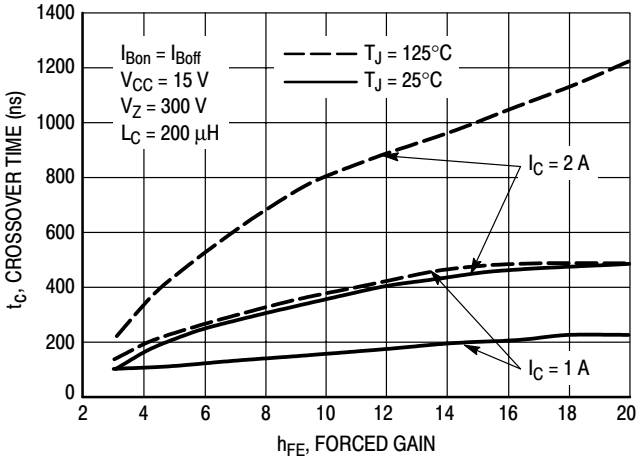


Figure 62. Inductive Crossover Time

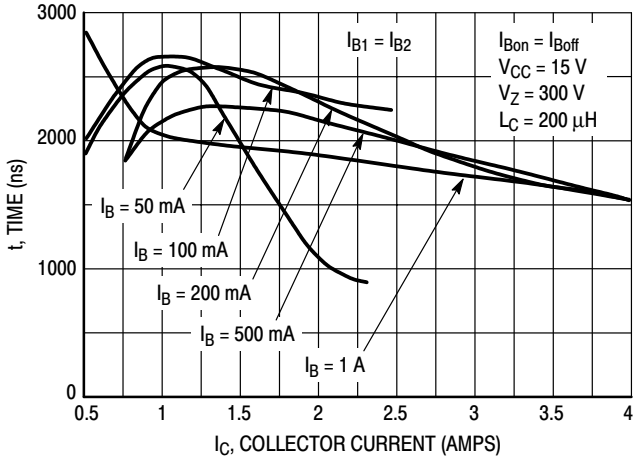


Figure 63. Inductive Storage Time, t_{si}

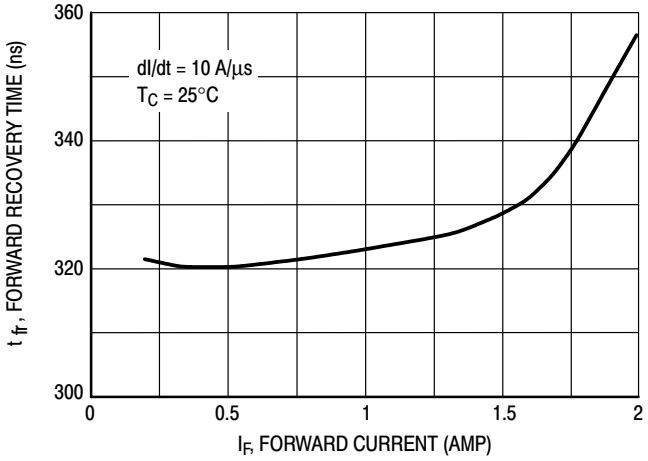


Figure 64. Forward Recovery Time t_{fr}

TYPICAL SWITCHING CHARACTERISTICS

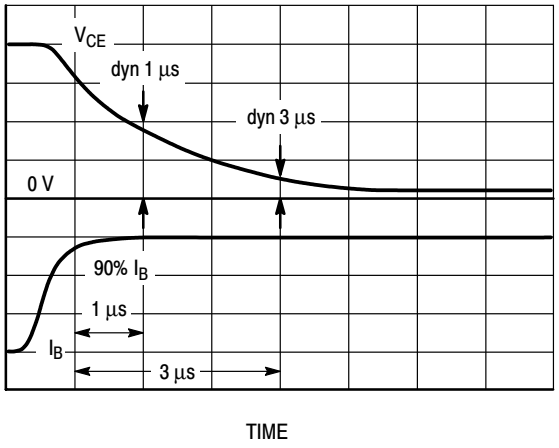


Figure 65. Dynamic Saturation Voltage Measurements

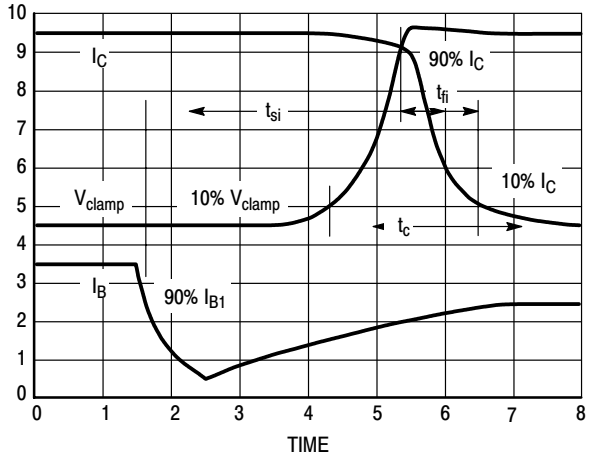


Figure 66. Inductive Switching Measurements

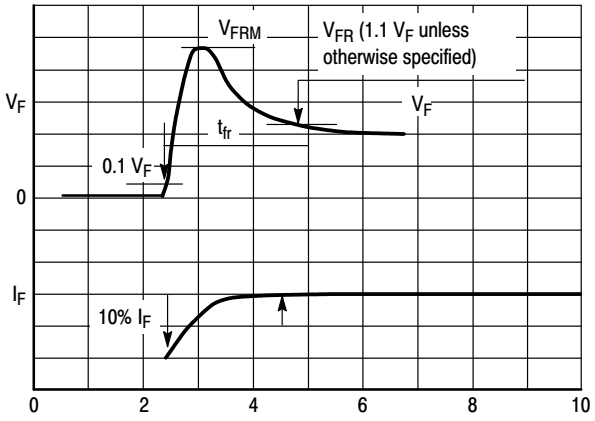
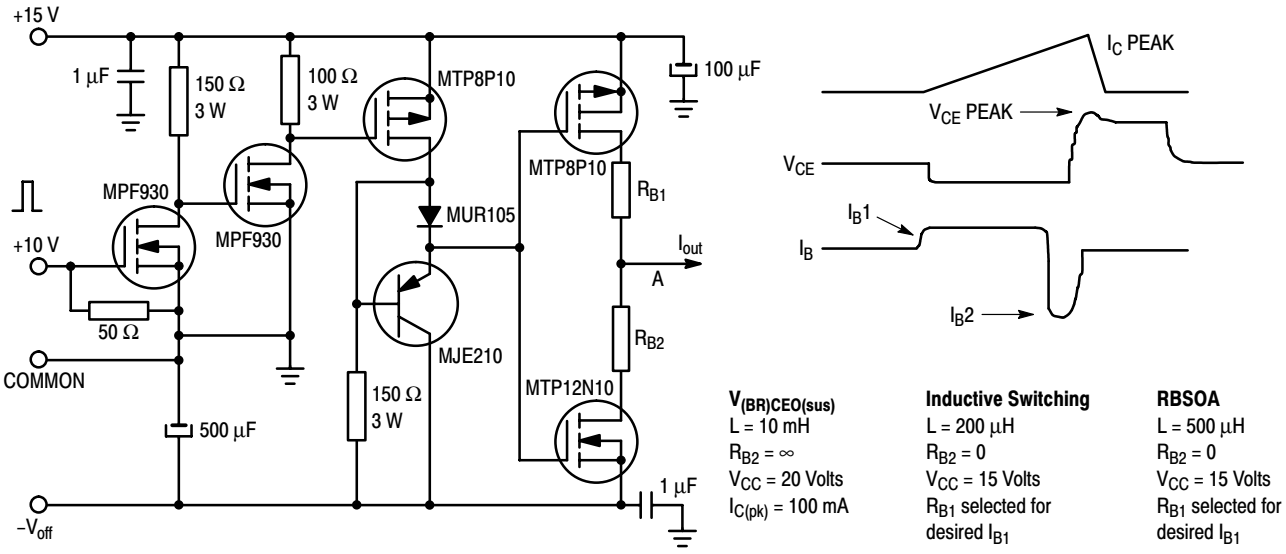


Figure 67. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



TYPICAL CHARACTERISTICS

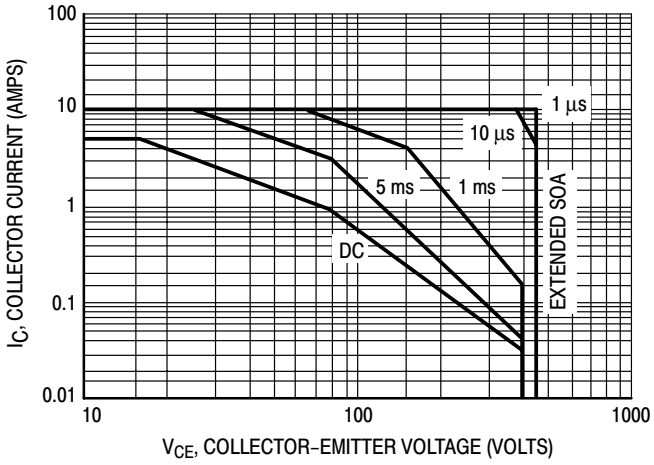


Figure 68. Forward Bias Safe Operating Area

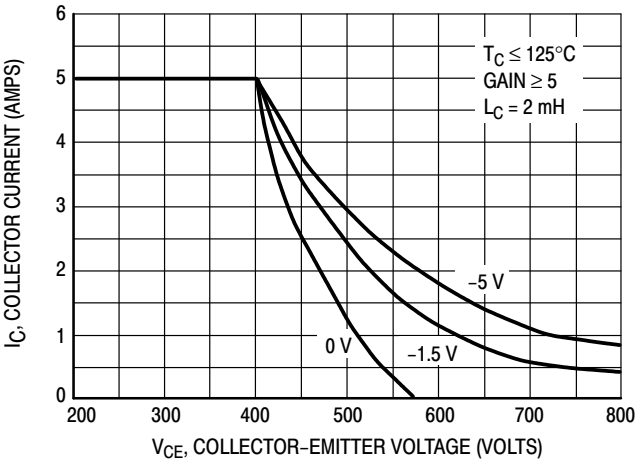


Figure 69. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

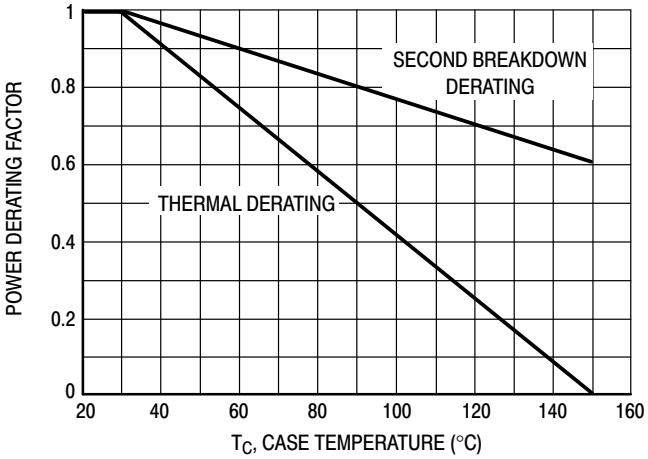


Figure 70. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 68 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 68 may be found at any case temperature by using the appropriate curve on Figure 70.

$T_{J(pk)}$ may be calculated from the data in Figure 71. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 69). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

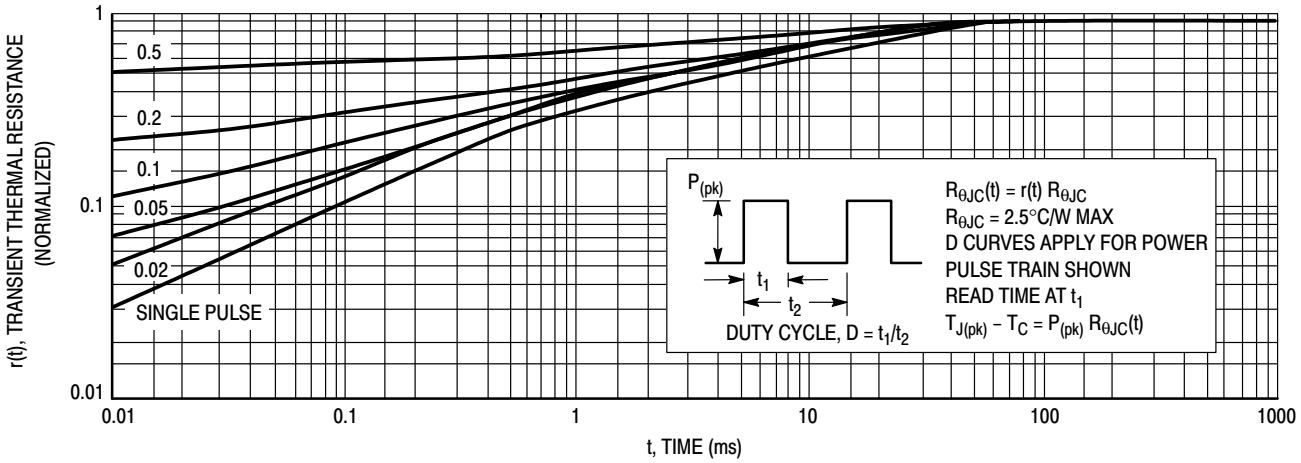


Figure 71. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45D2

BUL45

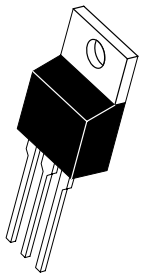
NPN Silicon Power Transistor

High Voltage SWITCHMODE™ Series

POWER TRANSISTOR
5.0 AMPERES
700 VOLTS
35 and 75 WATTS

Designed for use in electronic ballast (light ballast) and in Switchmode Power supplies up to 50 Watts. Main features include:

- Improved Efficiency Due to:
  - Low Base Drive Requirements (High and Flat DC Current Gain h_{FE})
  - Low Power Losses (On–State and Switching Operations)
  - Fast Switching: t_{fi} = 100 ns (typ) and t_{si} = 3.2 μs (typ) @ I_C = 2.0 A, I_{B1} = I_{B2} = 0.4 A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot–to–Lot



BUL45
CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (T_C = 125°C)	I_{CES}	— —	— —	10 100	μAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

May, 2001 – Rev. 5
Publication Order Number:
BUL45/D

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc) (I_C = 2.0 Adc, I_B = 0.4 Adc)				$V_{BE(sat)}$	— —	0.84 0.89	1.2 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc) (T_C = 125°C)				$V_{CE(sat)}$	 — —	 0.175 0.150	 0.25 —	Vdc
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.4 Adc) (T_C = 125°C)				$V_{CE(sat)}$	 — —	 0.25 0.275	 0.4 —	Vdc
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc) (T_C = 125°C) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (T_C = 125°C) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				h_{FE}	14 — 7.0 5.0 10	— 32 14 12 22	34 — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	12	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	50	75	pF
Input Capacitance (V_{EB} = 8.0 Vdc)				C_{ib}	—	920	1200	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.0 Adc I_{B1} = 100 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	V_{CE} (Dyn sat)	— —	1.75 4.4	— —	Vdc
		3.0 μs	(T_C = 125°C)		— —	0.5 1.0	— —	
	(I_C = 2.0 Adc I_{B1} = 400 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	1.85 6.0	— —	
		3.0 μs	(T_C = 125°C)		— —	0.5 1.0	— —	

SWITCHING CHARACTERISTICS: Resistive Load

Turn–On Time	(I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.4 Adc Pulse Width = 20 μs, (T_C = 125°C) Duty Cycle < 20% V_{CC} = 300 V)	t_{on}	— —	75 120	110 —	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	— —	2.8 3.5	3.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 Vdc, L_C = 200 μH, V_{clamp} = 300 Vdc)

Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc) (T_C = 125°C)	t_{fi}	70 —	— 200	170 —	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 —	— 4.2	3.8 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	230 400	350 —	ns
Fall Time	(I_C = 1.0 Adc, I_{B1} = 100 mAdc I_{B2} = 0.5 Adc) (T_C = 125°C)	t_{fi}	— —	110 100	150 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.1 1.5	1.7 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	170 170	250 —	ns
Fall Time	(I_C = 2.0 Adc, I_{B1} = 250 mAdc I_{B2} = 2.0 Adc) (T_C = 125°C)	t_{fi}	—	80	120	ns
Storage Time	(T_C = 125°C)	t_{si}	—	0.6	0.9	μs
Crossover Time	(T_C = 125°C)	t_c	—	175	300	ns

TYPICAL STATIC CHARACTERISTICS

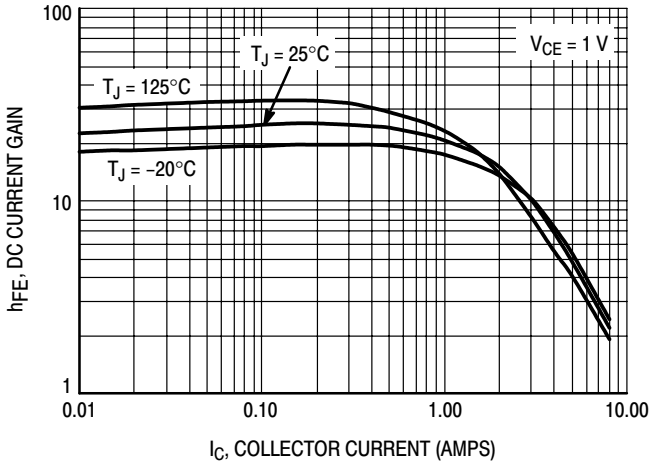


Figure 1. DC Current Gain @ 1 Volt

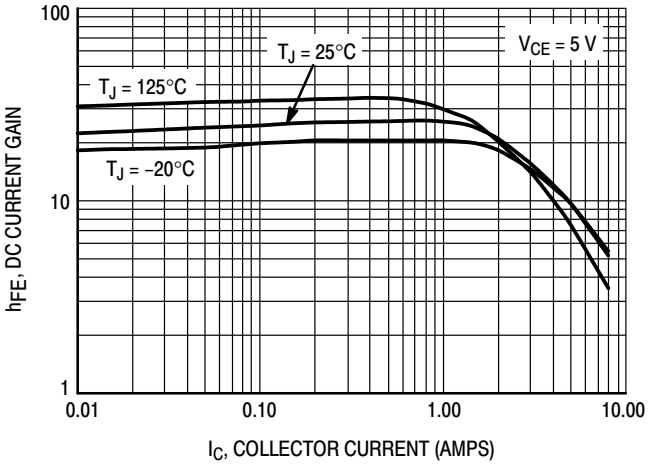


Figure 2. DC Current Gain at @ 5 Volts

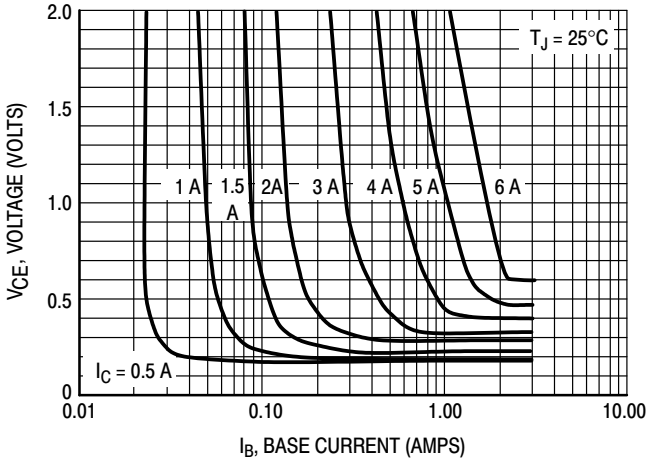


Figure 3. Collector–Emitter Saturation Region

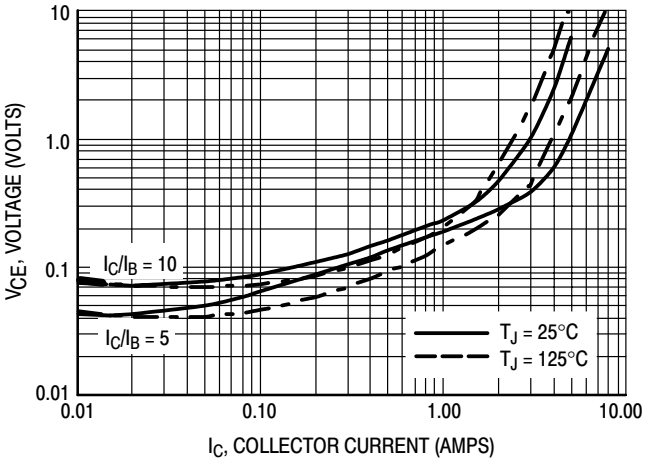


Figure 4. Collector–Emitter Saturation Voltage

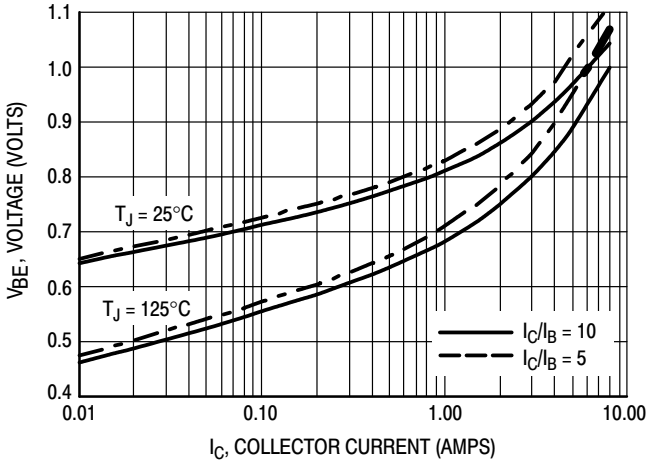


Figure 5. Base–Emitter Saturation Region

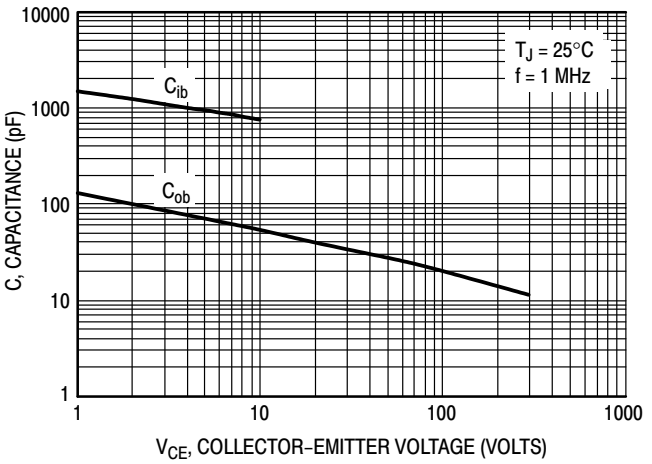


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

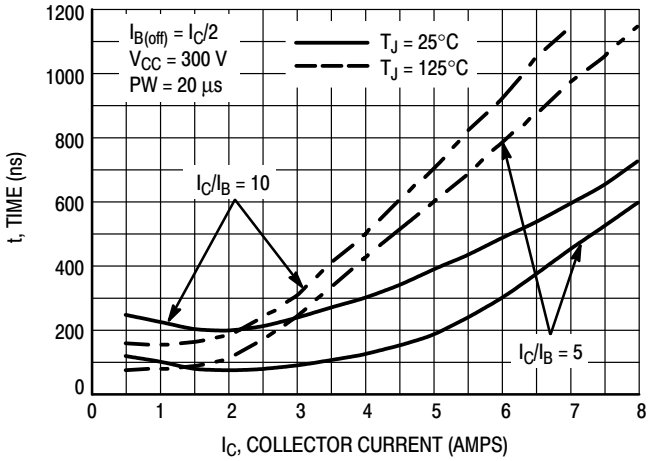


Figure 7. Resistive Switching, t_{on}

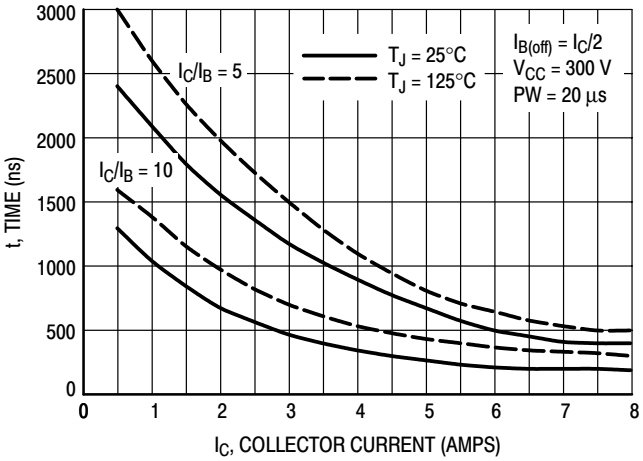


Figure 8. Resistive Switching, t_{off}

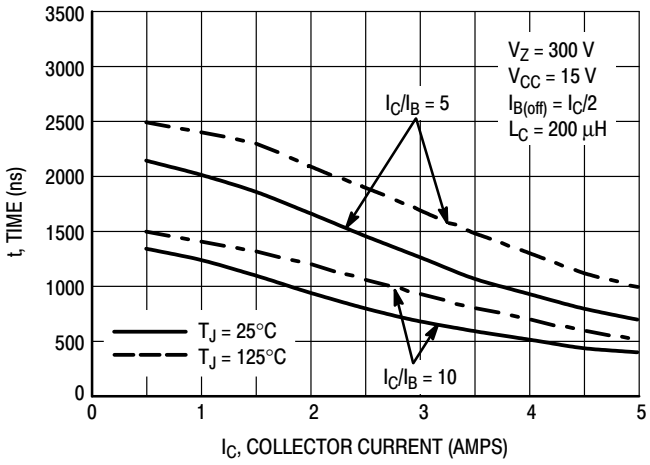


Figure 9. Inductive Storage Time, t_{si}

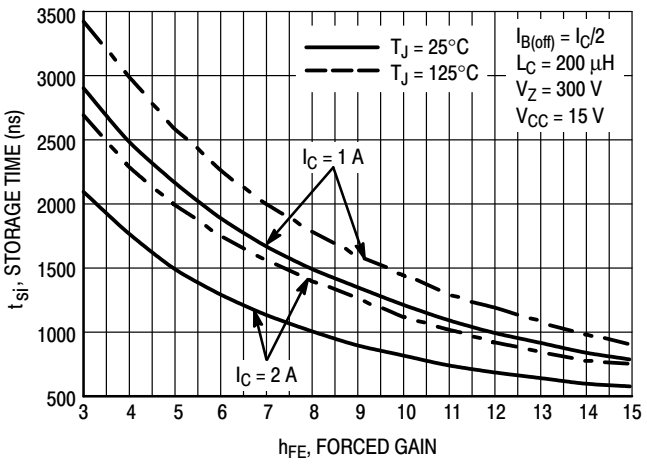


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

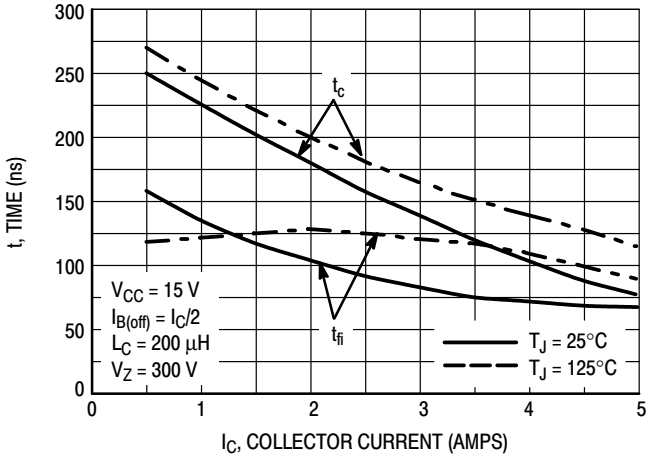


Figure 11. Inductive Switching, t_c & t_{fi}, I_C/I_B = 5

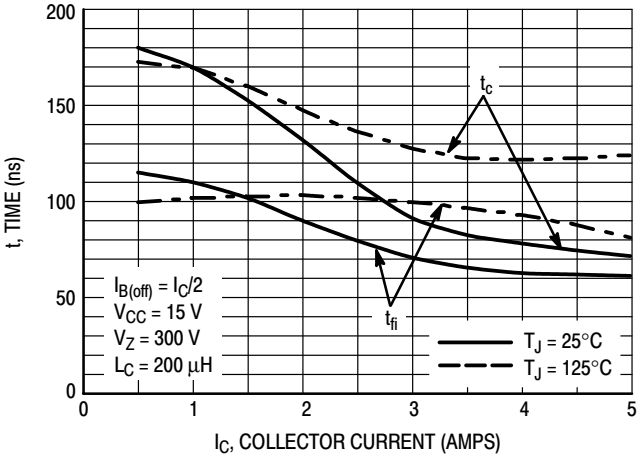


Figure 12. Inductive Switching, t_c & t_{fi}, I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

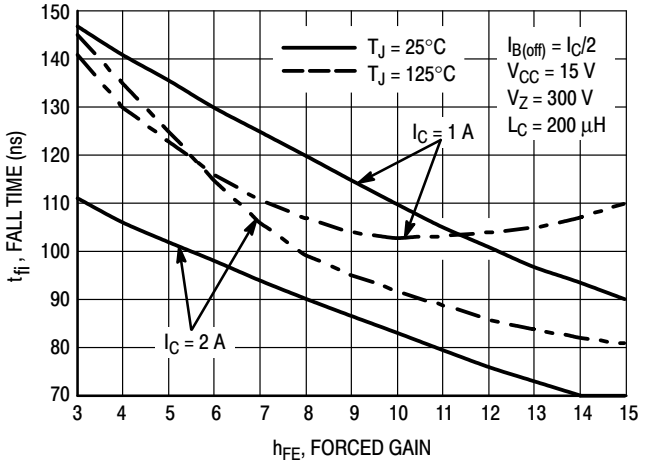


Figure 13. Inductive Fall Time, $t_{fi}(h_{FE})$

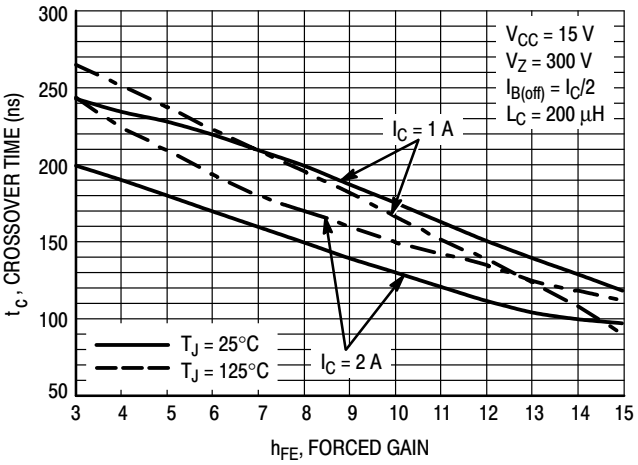


Figure 14. Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

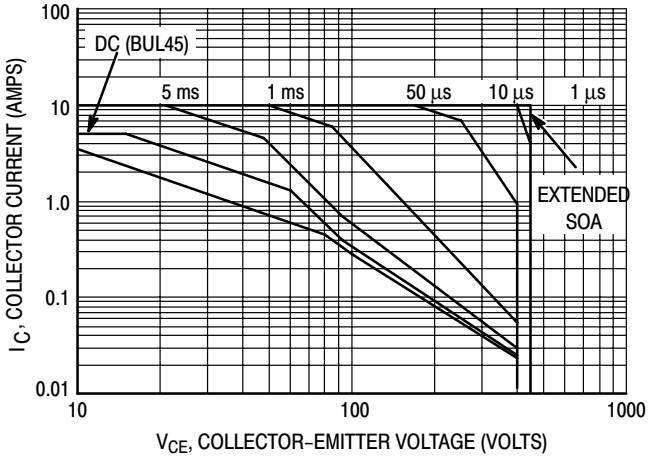


Figure 15. Forward Bias Safe Operating Area

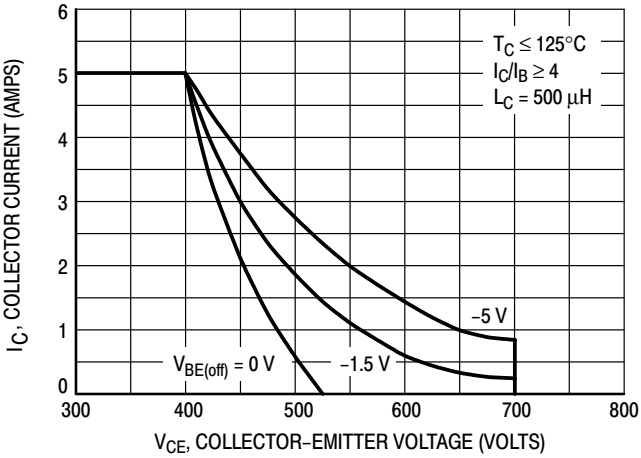


Figure 16. Reverse Bias Switching Safe Operating Area

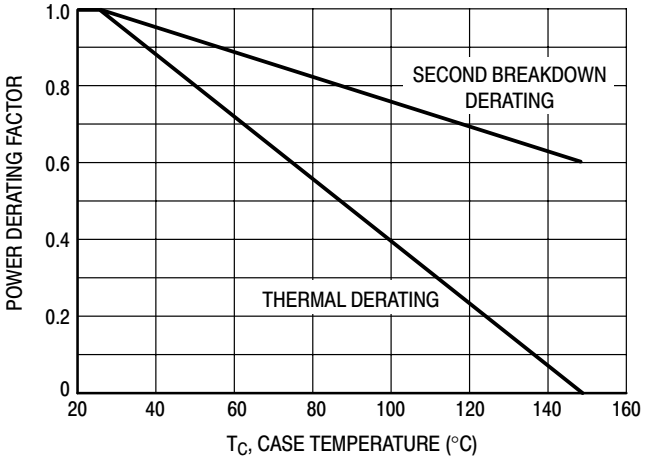


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

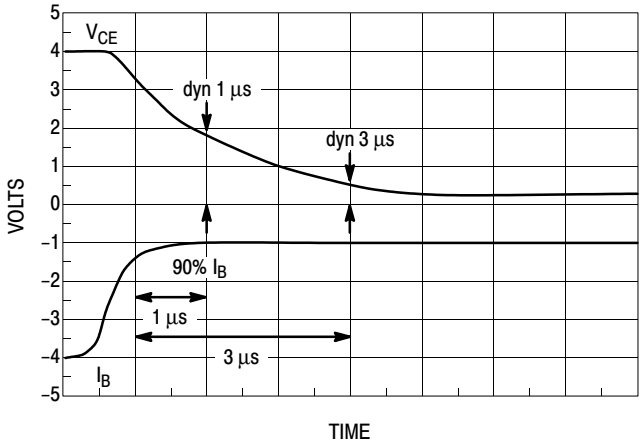


Figure 18. Dynamic Saturation Voltage Measurements

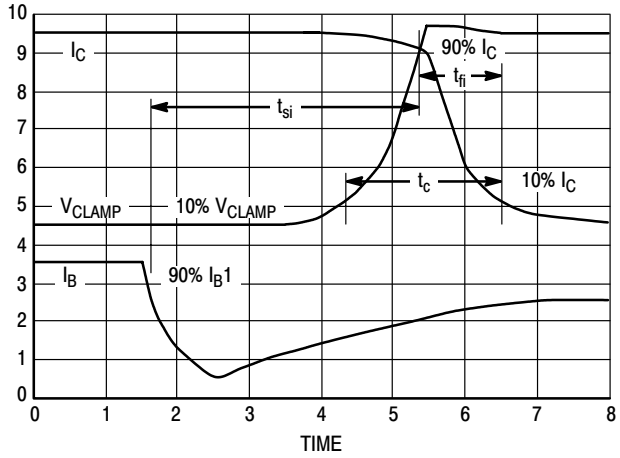
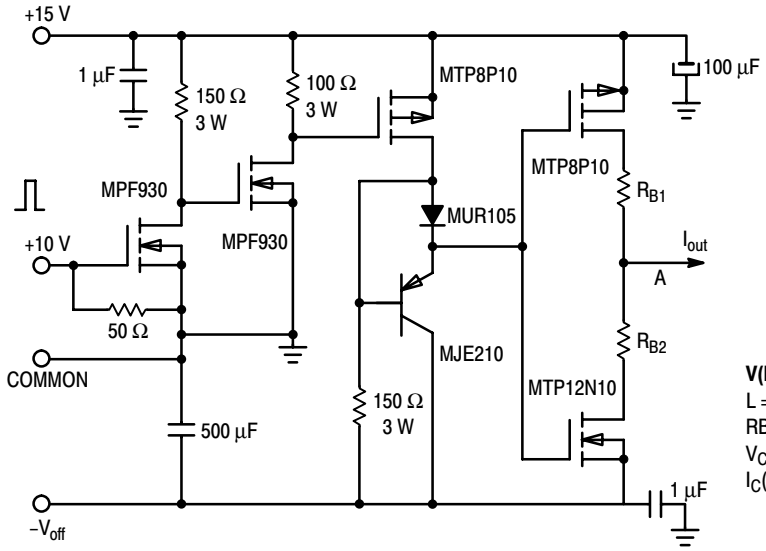
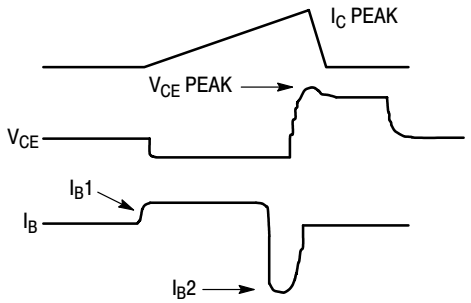


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

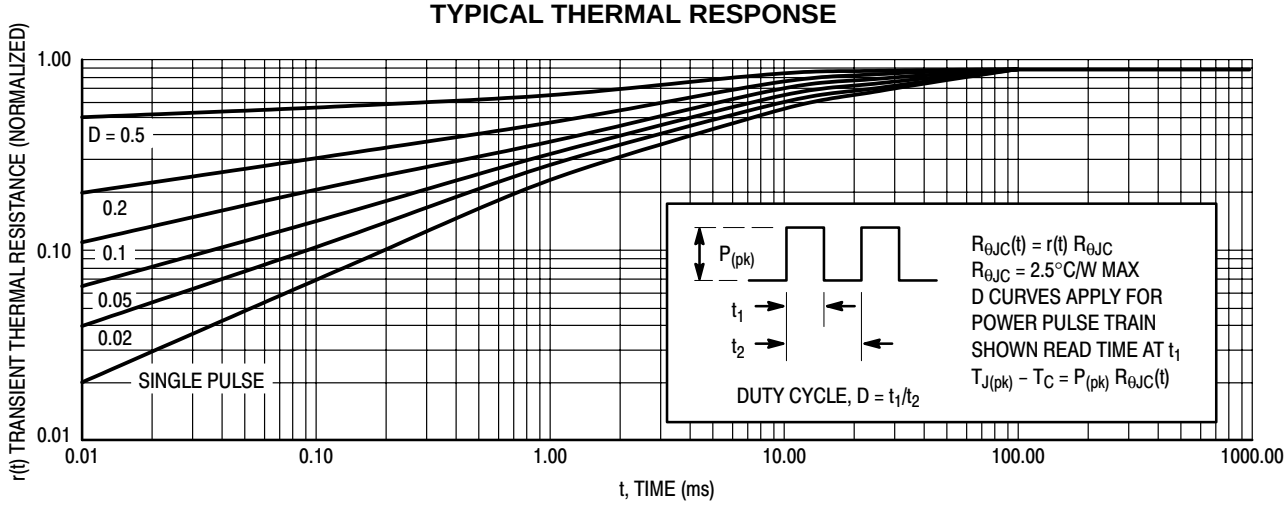
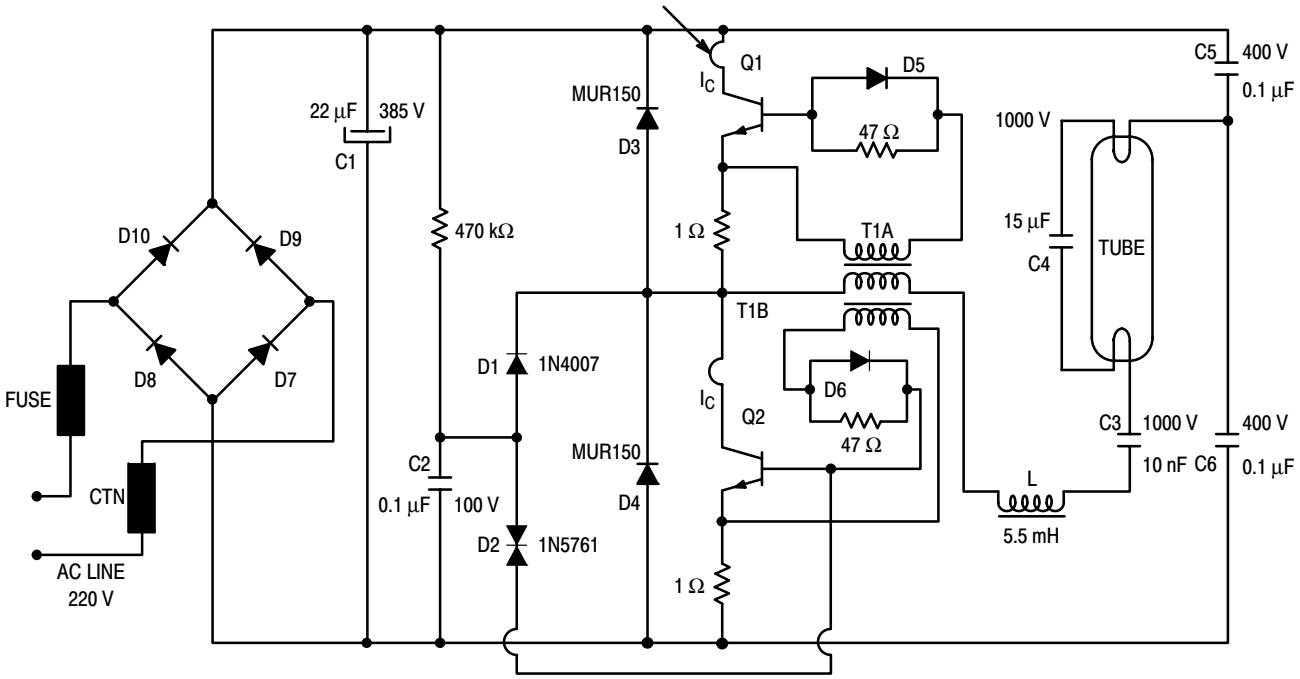


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45

The BUL45 Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by ON Semiconductor applications was built to demonstrate how well these devices operate. The circuit and detailed component list are provided below.



Components Lists

Q1 = Q2 = BUL45 Transistor
D1 = 1N4007 Rectifier
D2 = 1N5761 Rectifier
D3 = D4 = MUR150
D5 = D6 = MUR105
D7 = D8 = D9 = D10 = 1N400
CTN = 47 Ω @ 25°C
L = RM10 core, A1 = 400, B51 (LCC) 75 turns, wire ∅ = 0.6 mm
T1 = FT10 toroid, T4A (LCC)
Primary: 4 turns
Secondaries: T1A: 4 turns
T1B: 4 turns

All resistors are 1/4 Watt, ±5%
R1 = 470 kΩ
R2 = R3 = 47 Ω
R4 = R5 = 1 Ω (these resistors are optional, and might be replaced by a short circuit)
C1 = 22 μF/385 V
C2 = 0.1 μF
C3 = 10 nF/1000 V
C4 = 15 nF/1000 V
C5 = C6 = 0.1 μF/400 V

NOTES:
1. Since this design does not include the line input filter, it cannot be used “as–is” in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re–calculated with any other loads.

Figure 21. Application Example

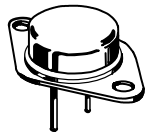
BUV20
BUV60

SWITCHMODE™ Series
NPN Silicon Power Transistor

. . . designed for high speed, high current, high power applications.

- High DC current gain:
  h_{FE} min = 20 at I_C = 25 A
  = 10 at I_C = 50 A
- Low $V_{CE(sat)}$:
  $V_{CE(sat)}$ max. = 0.6 V at I_C = 25 A
  = 0.9 V at I_C = 50 A
- Very fast switching times:
  T_F = 0.25 μs at I_C = 50 A

50 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
125 VOLTS
250 WATTS



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	BUV20	BUV60	Unit
Collector–Emititer Voltage	$V_{CEO(sus)}$	125		Vdc
Collector–Base Voltage	V_{CBO}	160	260	Vdc
Emitter–Base Voltage	V_{EBO}	7		Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	160	260	Vdc
Collector–Emitter voltage (R_{BE} = 100 Ω)	V_{CER}	150	260	Vdc
Collector–Current — Continuous — Peak (PW ≤ 10 ms)	I_C I_{CM}	50 60		Adc Apk
Base–Current continuous	I_B	10		Adc
Total Power Dissipation @ T_C = 25°C	P_D	250		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	BUV20	BUV60	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7		°C/W

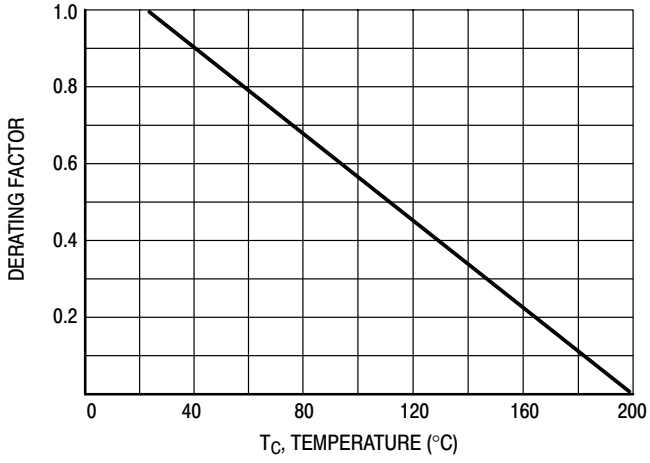


Figure 1. Power Derating

May, 2001 – Rev. 10
Publication Order Number:
BUV20/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]					
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	BUV20, BUV60	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias		I_{CEX}			mAdc
(V_{CE} = 140 V, V_{BE} = – 1.5 V)	BUV20			3.0	
(V_{CE} = 140 V, V_{BE} = – 1.5 V, T_C = 125°C)	BUV20			12	
(V_{CE} = 260 V, V_{BE} = – 1.5 V)	BUV60				
Collector–Emitter Cutoff Current (V_{CE} = 100 V)	BUV20	I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	BUV20, BUV60	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	BUV20, BUV60	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$			Adc
(V_{CE} = 20 V, t = 1 s)			12		
(V_{CE} = 40 V, t = 1 s)			1.5		
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			
(I_C = 25 A, V_{CE} = 2 V)	BUV20		20	60	
(I_C = 50 A, V_{CE} = 4 V)	BUV20		10	–	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 25 A, I_B = 2.5 A)	BUV20			0.6	
(I_C = 50 A, I_B = 5 A)	BUV20			1.2	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 50 A, I_B = 5 A)0	BUV20			2.0	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 25 A, I_B = 1.25 A)	BUV60			0.9	
(I_C = 50 A, I_B = 5 A)	BUV60			0.9	
(I_C = 60 A, I_B = 7.5 A)	BUV60			1.2	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 50 A, I_B = 5 A)	BUV60			1.6	
(I_C = 60 A, I_B = 7.5 A)	BUV60			1.8	
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)		f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)					
Turn–on Time	(I_C = 50 A, I_{B1} = I_{B2} = 5 A, V_{CC} = 30 V, R_C = 0.6 Ω)	t_{on}		1.5	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

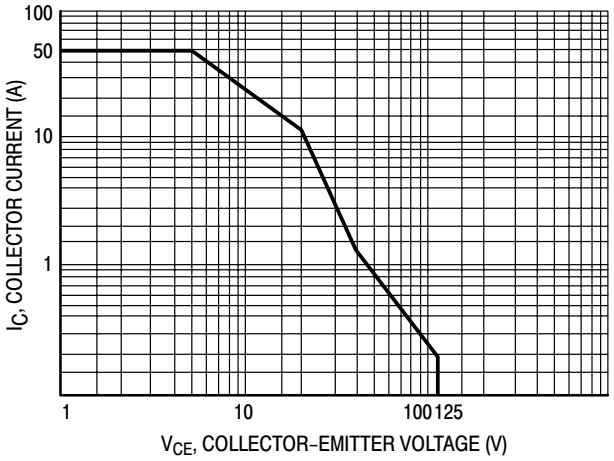


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$. $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

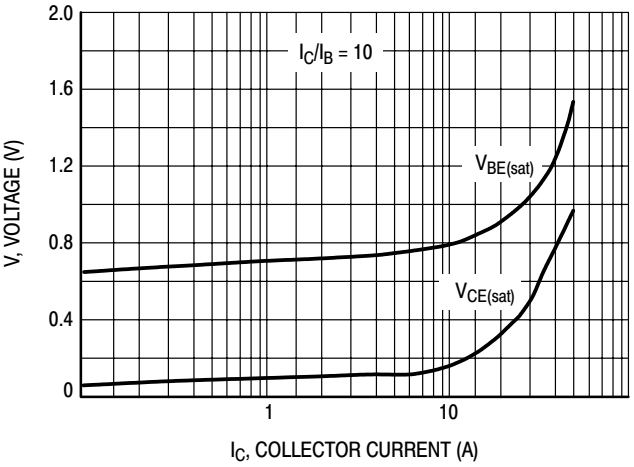


Figure 3. “On” Voltages

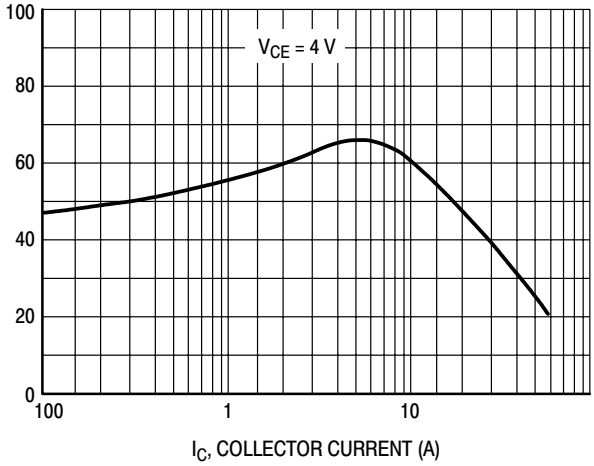


Figure 4. DC Current Gain

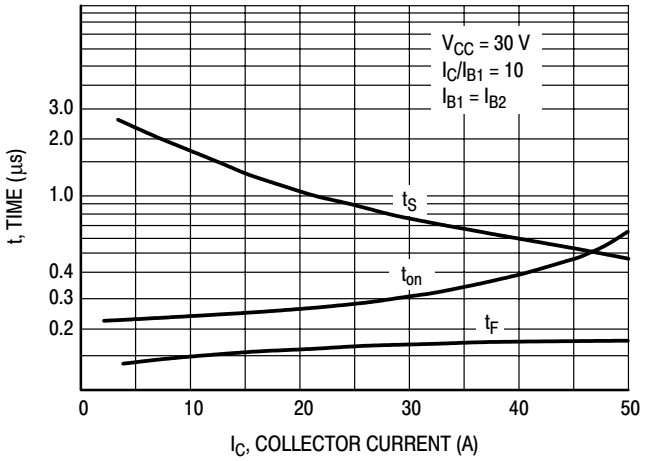
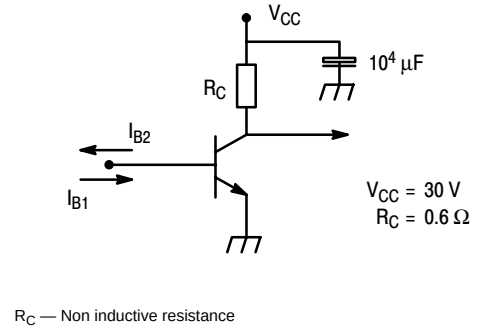


Figure 5. Resistive Switching Performance



R_C — Non inductive resistance

Figure 6. Switching Times Test Circuit

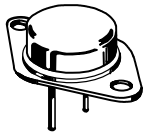
SWITCHMODE™ Series NPN Silicon Power Transistor

BUV21

40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
200 VOLTS
250 WATTS

. . . designed for high speed, high current, high power applications.

- High DC current gain:
  h_{FE} min. = 20 at I_C = 12 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$
  max. = 0.6 V at I_C = 8 A
- Very fast switching times:
  TF max. = 0.4 μs at I_C = 25 A



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector–Base Voltage	V_{CBO}	250	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	250	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector–Current — Continuous — Peak (PW ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base–Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

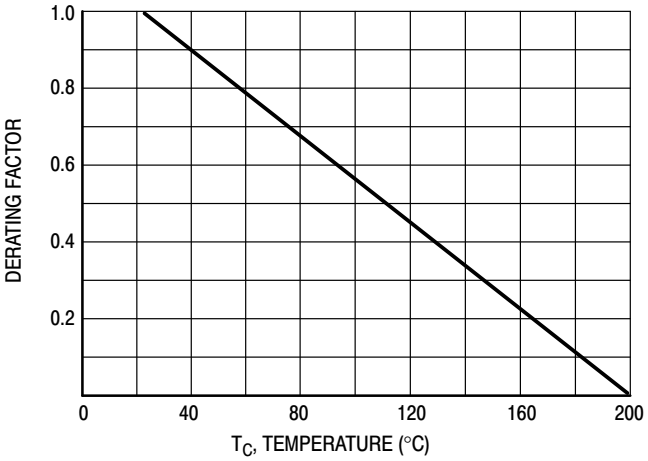


Figure 1. Power Derating

May, 2001 – Rev. 9
Publication Order Number:
BUV21/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 250 V, V_{BE} = –1.5 V) (V_{CE} = 250 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		3.0 12.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 12 A, V_{CE} = 2 V) (I_C = 25 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector–Emitter Saturation Voltage (I_C = 12 A, I_B = 1.2 A) (I_C = 25 A, I_B = 3 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 25 A, I_B = 3 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn-on Time	(I_C = 25 A, I_{B1} = I_{B2} = 3 A, V_{CC} = 100 V, R_C = 4 Ω)	t_{on}	1.0	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

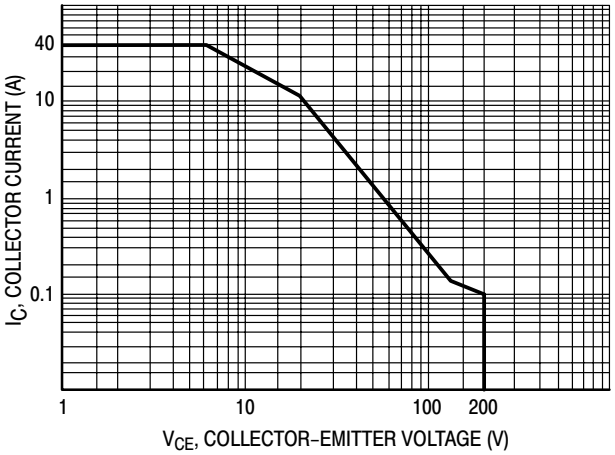


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

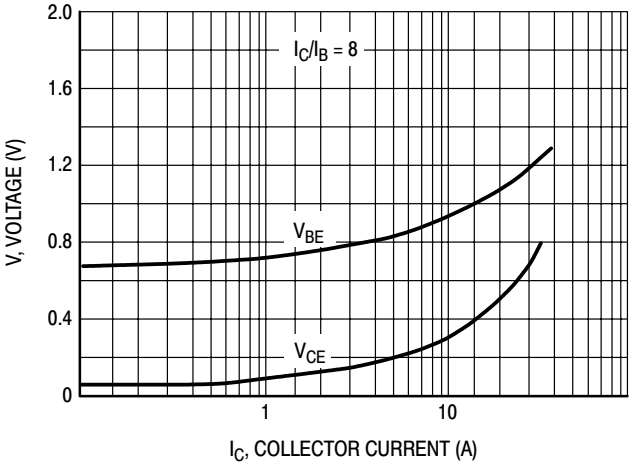


Figure 3. “On” Voltages

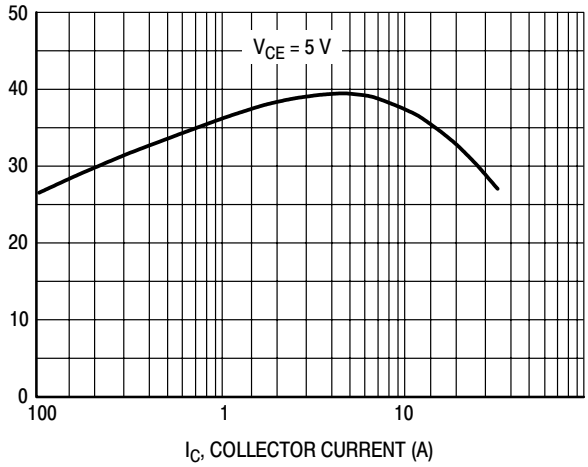


Figure 4. DC Current Gain

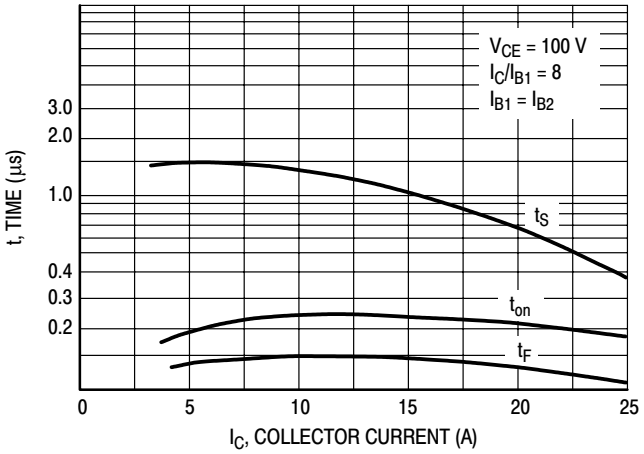
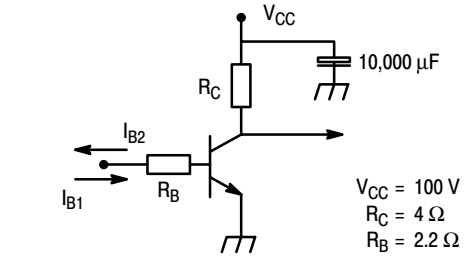


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

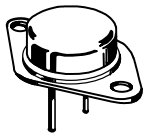
BUV22

SWITCHMODE™ Series NPN Silicon Power Transistor

40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
250 VOLTS
250 WATTS

. . . designed for high current, high speed, high power applications.

- High DC current gain:
  HFE min. = 20 at I_C = 10 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$
  max. = 1.0 V at I_C = 10 A
- Very fast switching times:
  T_F max. = 0.35 μs at I_C = 20 A



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector–Base Voltage	V_{CBO}	300	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	300	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	290	Vdc
Collector–Current — Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base–Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

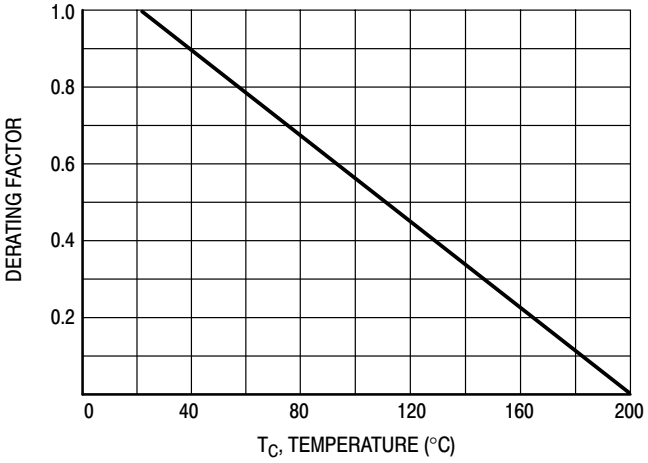


Figure 1. Power Derating

March, 2001 – Rev. 9
Publication Order Number:
BUV22/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]					
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)		$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 300 V, V_{BE} = –1.5 V) (V_{CE} = 300 V, V_{BE} = –1.5 V, T_C = 125°C)		I_{CEX}		3.0 12.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 200 V)		I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)		V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)		I_{EBO}		1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)		$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 10 A, V_{CE} = 4 V) (I_C = 20 A, V_{CE} = 4 V)		h_{FE}	20 10	60	
Collector–Emitter Saturation Voltage (I_C = 10 A, I_B = 1 A) (I_C = 20 A, I_B = 2.5 A)		$V_{CE(sat)}$		1.0 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 40 A, I_B = 4 A)		$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)		f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)					
Turn–on Time	(I_C = 20 A, I_{B1} = I_{B2} = 2.5 A, V_{CC} = 100 V, R_C = 5 Ω)	t_{on}		0.8	μs
Storage Time		t_s		2.0	
Fall Time		t_f		0.35	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

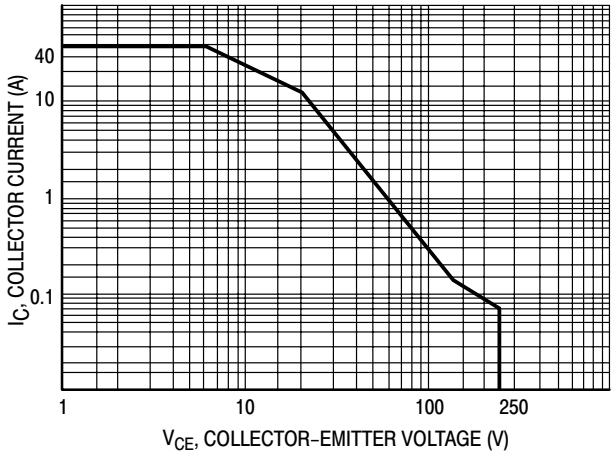


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

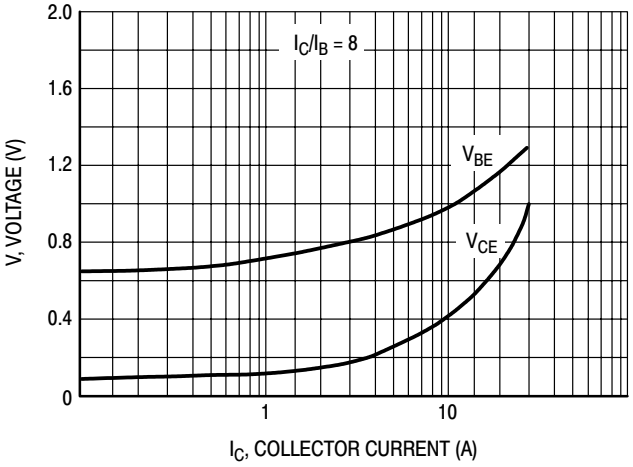


Figure 3. “On” Voltages

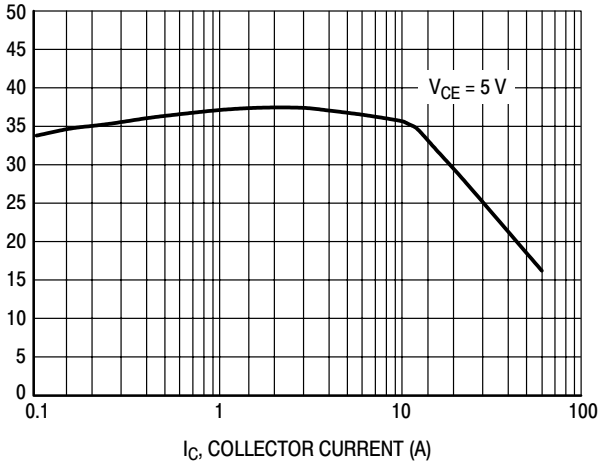


Figure 4. DC Current Gain

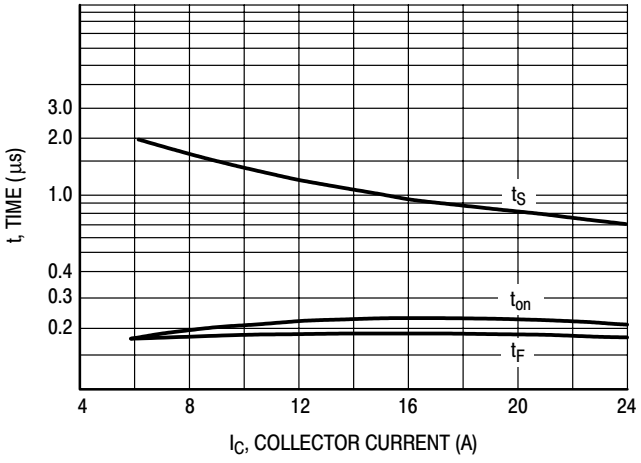
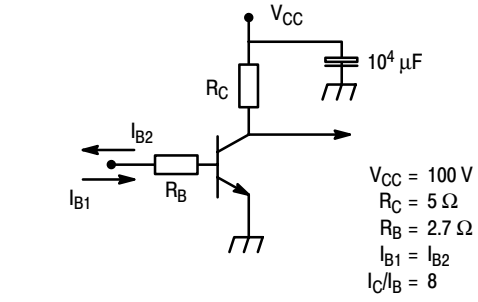


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

BUX85

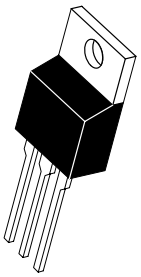
SWITCHMODE™ NPN Silicon Power Transistors

2 AMPERES
POWER TRANSISTOR
NPN SILICON
450 VOLTS
50 WATTS

The BUX85 is designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

Specifications Features:

- $V_{CEO(sus)}$ 450 V
- $V_{CES(sus)}$ 1000 V
- Fall time = 0.3 μs (typ) at I_C = 1.0 A
- $V_{CE(sat)}$ = 1.0 V (max) at I_C = 1.0 A, I_B = 0.2 A



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BUX84	BUX85	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage	V_{CES}	800	1000	Vdc
Emitter Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous — Peak (1)	 I_C I_{CM}	 2 3.0		Adc
Base Current — Continuous — Peak (1)	 I_B I_{BM}	 0.75 1.0		Adc
Reverse Base Current — Peak	I_{BM}	1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 400		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

March, 2001 – Rev. 9
Publication Order Number:
BUX85/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, (L = 25 mH) See fig. 1	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CES} = Rated Value) (V_{CES} = Rated Value, T_C = 125°C)	I_{CES}	 — —	 — —	 0.2 1.5	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5 V)	h_{FE}	30	50	—	—
Collector–Emitter Saturation Voltage (I_C = 0.3 Adc, I_B = 30 mAdc) (I_C = 1 Adc, I_B = 200 mAdc)	$V_{CE(sat)}$	 — —	 — —	 0.8 1	Vdc
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	—	—	1.1	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 1 0 Vdc, f = 1 MHz)	f_T	4	—	—	MHz
SWITCHING CHARACTERISTICS					
Turn–on Time	V_{CC} = 250 Vdc, I_C = 1 A I_{B1} = 0.2 A, I_{B2} = 0.4 A See fig. 2	t_{on}	—	0.3	0.5	μs
Storage Time		t_s	—	2	3.5	μs
Fall Time		t_f	—	0.3	—	μs
Fall Time	Same above cond. at T_C = 95°C	t_f	—	—	1.4	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦2%.

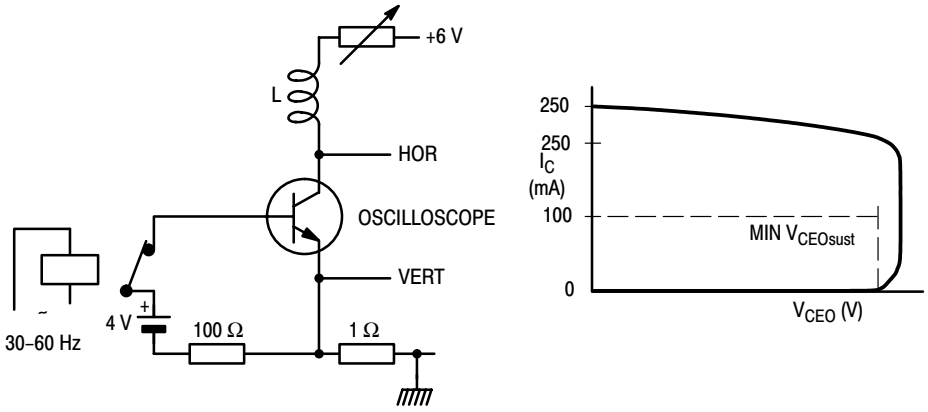


Figure 1. Test Circuit for $V_{CEOsust}$

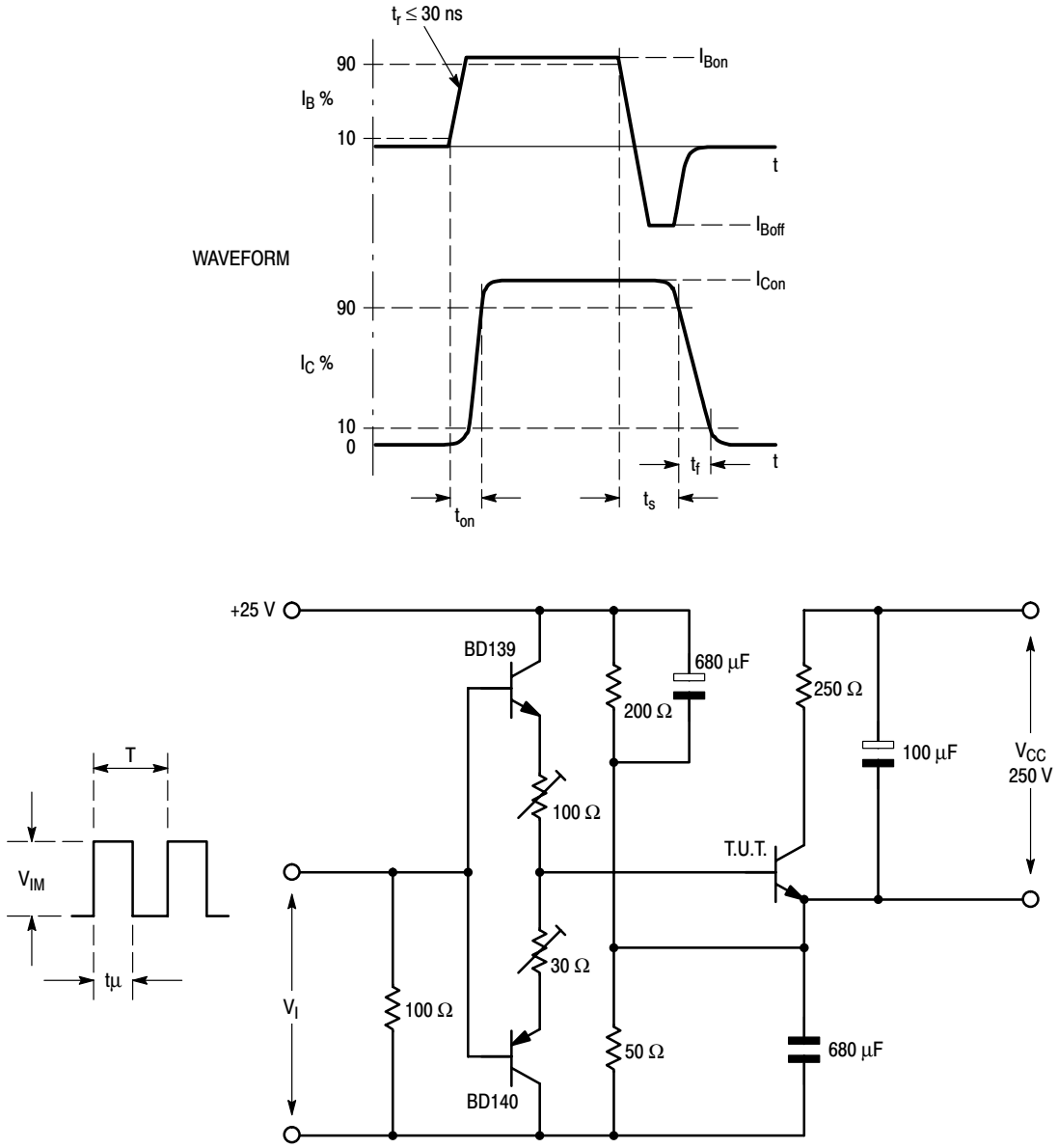


Figure 2. Switching Times/Test Circuit

Complementary Silicon Power Transistors

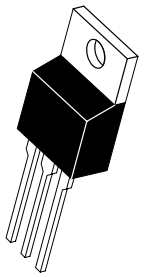
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

NPN
D44H Series*
PNP
D45H Series*

***ON Semiconductor Preferred Device**

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 80 VOLTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	D44H or D45H		Unit
		8	10, 11	
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak (1)	I_C	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	50 1.67		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	D44H10 D45H10	h_{FE}	35	—	—
	D44H8,11 D44H8,11		60	—	
(V_{CE} = 1.0 Vdc, I_C = 4.0 Adc)	D44H10 D45H10		20	—	
	D44H8,11 D45H8,11		40	—	

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 2
Publication Order Number:
D44H/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)		I_{EBO}	—	—	100	μA
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44H/D45H8,11		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D44H/D45H10		—	—	1.0	
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Collector Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, f_{test} = 1.0 MHz)	D44H Series		—	130	—	
	D45H Series		—	230	—	
Gain Bandwidth Product		f_T				MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	D44H Series		—	50	—	
	D45H Series		—	40	—	
SWITCHING TIMES						
Delay and Rise Times		$t_d + t_r$				ns
(I_C = 5.0 Adc, I_{B1} = 0.5 Adc)	D44H Series		—	300	—	
	D45H Series		—	135	—	
Storage Time		t_s				ns
(I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	D44H Series		—	500	—	
	D45H Series		—	500	—	
Fall Time		t_f				ns
(I_C = 5.0 Adc, I_{B1} = 102 = 0.5 Adc)	D44H Series		—	140	—	
	D45H Series		—	100	—	

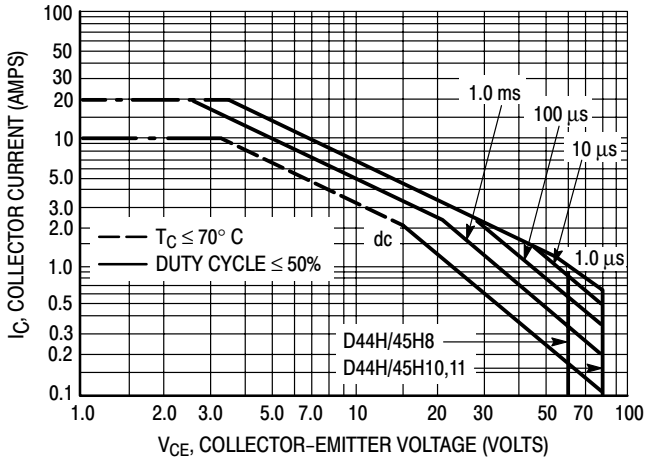


Figure 1. Maximum Rated Forward Bias Safe Operating Area

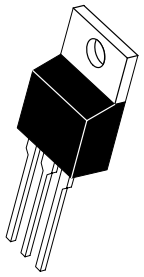
Complementary Silicon Power Transistors

NPN
D44VH
PNP
D45VH

These complementary silicon power transistors are designed for high–speed switching applications, such as switching regulators and high frequency inverters. The devices are also well–suited for drivers for high power switching circuits.

- Fast Switching —
  t_f = 90 ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 VOLTS
83 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Emitter Voltage	V_{CEV}	100	Vdc
Emitter Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(2) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

NOTE: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.

March, 2001 – Rev. 2
Publication Order Number:
D44VH/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (2) (I_C = 25 mAdc, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector–Emitter Cutoff Current		I_{CEV}				μAdc
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc)			—	—	10	
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)			—	—	100	
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)			35	—	—	
(I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)			20	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44VH10		—	—	0.4	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D45VH10		—	—	1.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)	D44VH10		—	—	0.8	
	D45VH10		—	—	1.5	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44VH10		—	—	1.2	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D45VH10		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	D44VH10		—	—	1.1	
(I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C)	D45VH10		—	—	1.5	
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	—	50	—	MHz
Output Capacitance		C_{ob}				pF
(V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz)	D44VH10		—	120	—	
	D45VH10		—	275	—	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	—	—	50	ns
Rise Time		t_r	—	—	250	
Storage Time		t_s	—	—	700	
Fall Time		t_f	—	—	90	

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

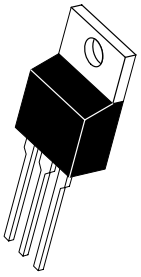
PNP
D45C
NPN
D44C

Complementary Silicon Power Transistor

. . . for general purpose driver or medium power output stages in CW or switching applications.

- Low Collector–Emitter Saturation Voltage — 0.5 V (Max)
- High f_t for Good Frequency Response
- Low Leakage Current

4.0 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 80 VOLTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Emitter Voltage	VCES	90	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C	4.0 6.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	30 1.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 0.2 Adc) (V_{CE} = 1.0 Vdc, I_C = 1.0 Adc) (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	h_{FE}	 40 20 20	 120 — —	—

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	0.1	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	10	μA
ON CHARACTERISTICS					
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	0.135	0.5	Vdc
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	—	0.85	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{cb}	—	125	—	pF
Gain Bandwidth Product (I_C = 20 mA, V_{CE} = 4.0 Vdc, f = 20 MHz)	f_T	—	40	—	MHz
SWITCHING TIMES					
Delay and Rise Times (I_C = 1.0 Adc, I_{B1} = 0.1 Adc)	$t_d + t_r$	—	50	75	ns
Storage Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_s	—	350	550	ns
Fall Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_f	—	50	75	ns

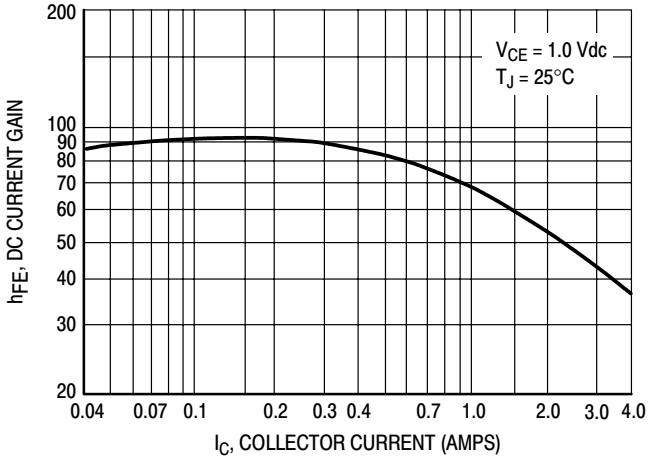


Figure 2. Typical DC Current Gain

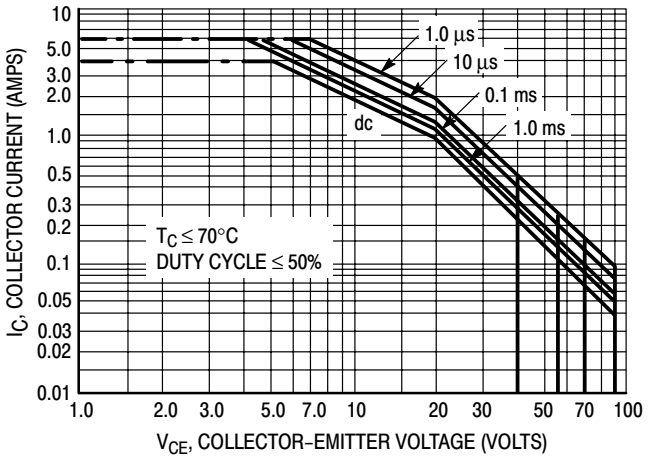


Figure 3. Maximum Rated Forward Bias Safe Operating Area

High-Current Complementary Silicon Transistors

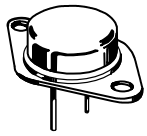
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 1000 (Min) @ I_C – 20 Adc
- Monolithic Construction with Built–in Base Emitter Shunt Resistor
- Junction Temperature to +200°C

PNP
MJ11015
NPN
MJ11012
MJ11016*

*ON Semiconductor Preferred Device

30 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–120 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11012	MJ11015 MJ11016	Unit
Collector–Emitter Voltage	V_{CEO}	60	120	Vdc
Collector–Base Voltage	V_{CB}	60	120	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	30		Adc
Base Current	I_B	1		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 1.15		Watts W/°C
Operating Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	°C

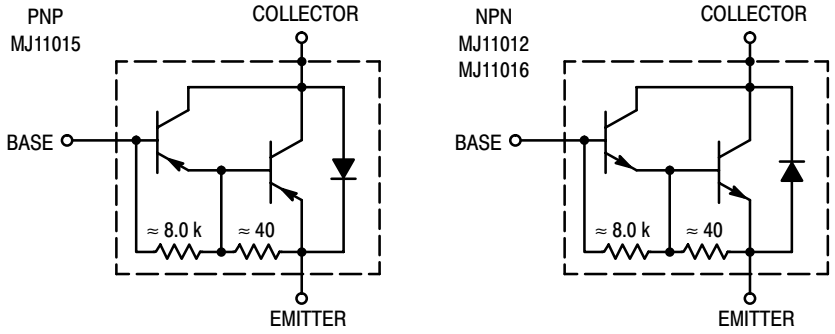


Figure 1. Darlington Circuit Schematic

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1)		$V_{(BR)CEO}$			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ11012		60	—	
	MJ11015, MJ11016		120	—	
Collector–Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm)	MJ11012		—	1	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm)	MJ11015, MJ11016		—	1	
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11012		—	5	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11015, MJ11016		—	5	
Emitter Cutoff Current		I_{EBO}	—	5	mAdc
(V_{BE} = 5 Vdc, I_C = 0)					
Collector–Emitter Leakage Current		I_{CEO}	—	1	mAdc
(V_{CE} = 50 Vdc, I_B = 0)					
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			—
(I_C = 20 Adc,V_{CE} = 5 Vdc)			1000	—	
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 200 mAdc)			—	3	
(I_C = 30 Adc, I_B = 300 mAdc)			—	4	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 A, I_B = 200 mAdc)			—	3.5	
(I_C = 30 A, I_B = 300 mAdc)			—	5	
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product		h_{fe}	4	—	MHz
(I_C = 10 A, V_{CE} = 3 Vdc, f = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

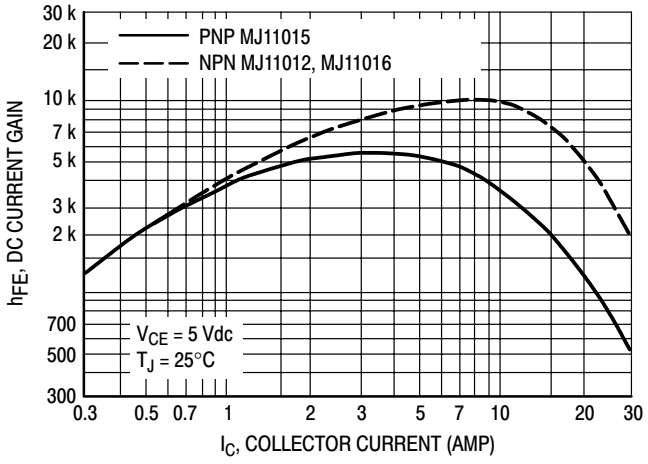


Figure 2. DC Current Gain (1)

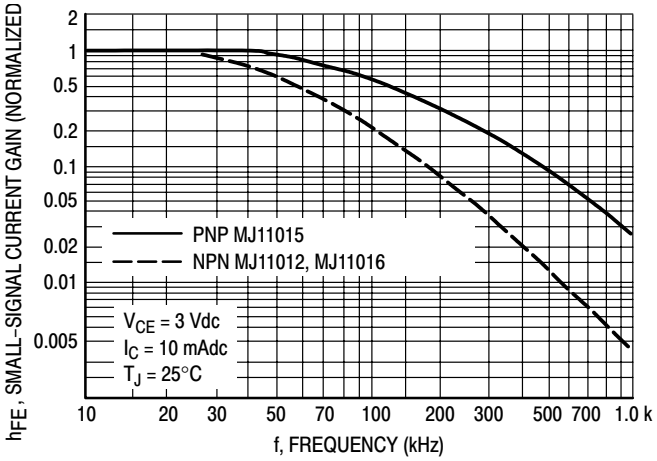


Figure 3. Small−Signal Current Gain

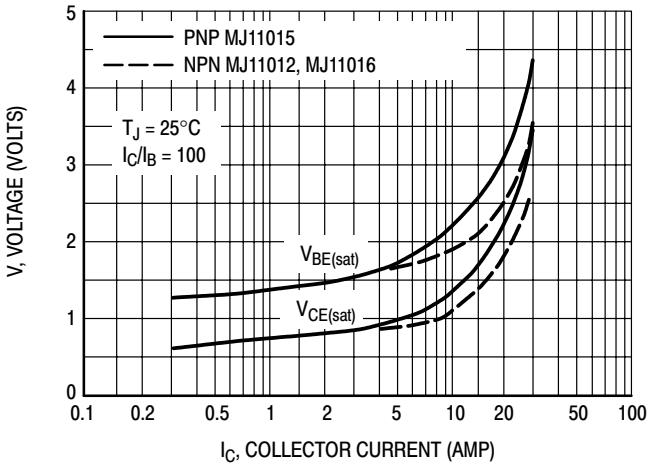


Figure 4. “On” Voltages (1)

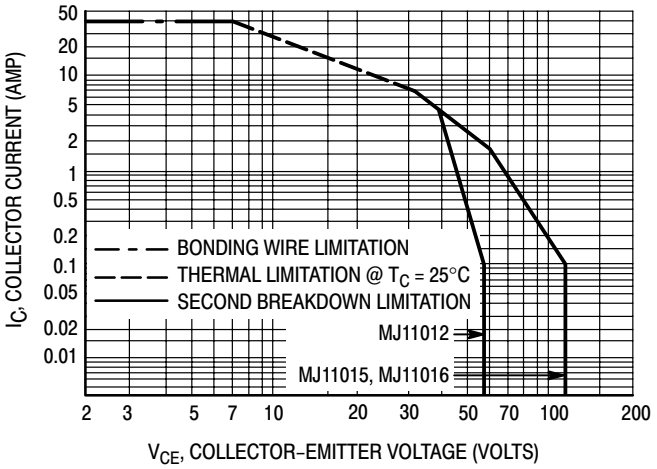


Figure 5. Active Region DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

Complementary Darlington Silicon Power Transistors

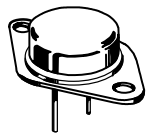
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc —
  h_{FE} = 400 Min (All Types)
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 250 Vdc (Min) – MJ11022, 21
- Low Collector–Emitter Saturation
  $V_{CE(sat)}$ = 1.0 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction
- 100% SOA Tested @
  V_{CE} = 44 V,
  I_C = 4.0 A,
  t = 250 ms.

PNP
MJ11021*
NPN
MJ11022

*ON Semiconductor Preferred Device

30 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–120 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11022 MJ11021	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CB}	250	Vdc
Emitter–Base Voltage	V_{EB}	50	Vdc
Collector Current — Continuous Peak	I_C	15 30	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	175 1.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175 –65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	°C/W

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 0
Publication Order Number:
MJ11021/D

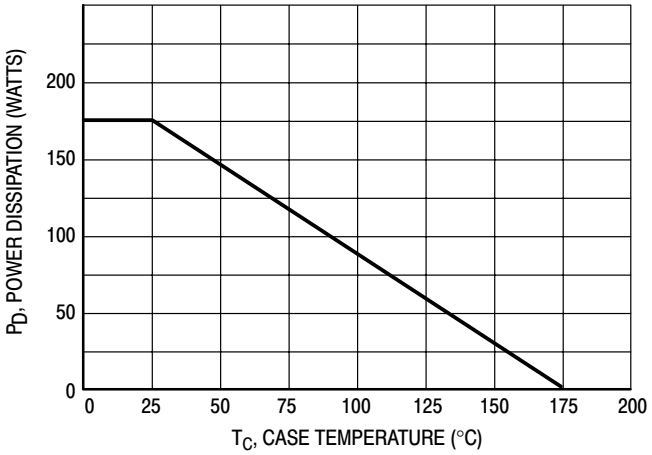


Figure 1. Power Derating

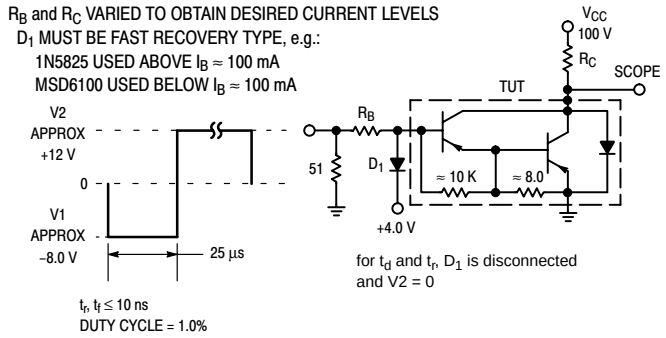
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 0. 1 Adc, I_B = 0) MJ11021, MJ11022	$V_{CEO(sus)}$	 250	 —	Vdc
Collector Cutoff Current (V_{CE} = 125, I_B = 0) MJ11021, MJ11022	I_{CEO}	 —	 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)	I_{CEV}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 400 100	 15,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)	$V_{CE(sat)}$	 — —	 2.0 3.4	Vdc
Base–Emitter On Voltage I_C = 10 A, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)	$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$[h_{fe}]$	3.0	—	Mhz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJ11022 MJ11021	C_{ob}	 — —	 400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 50 V) (See Figure 2.)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	10.0	2.5	μs

(1) Pulsed Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

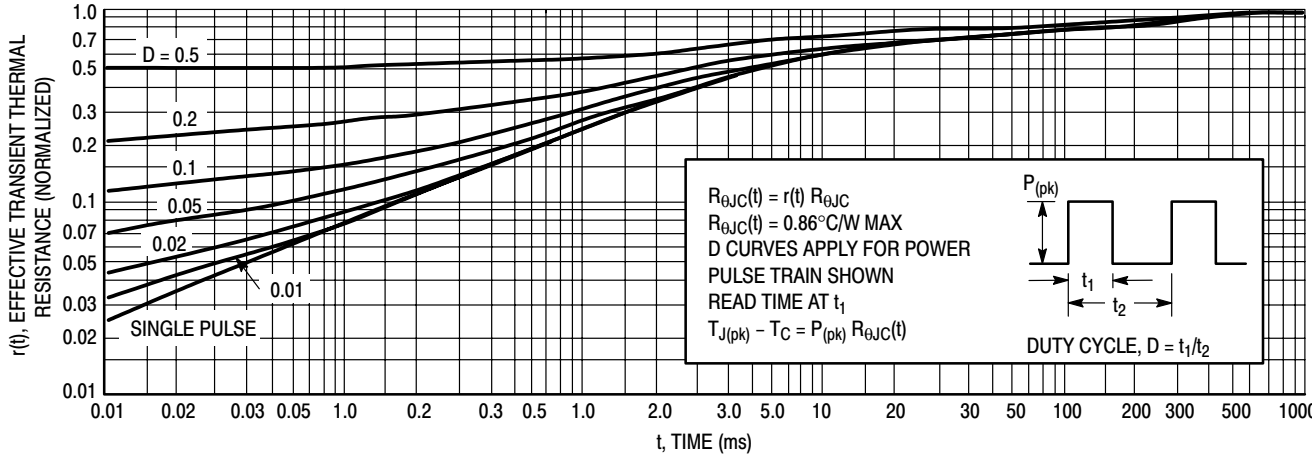


Figure 3. Thermal Response

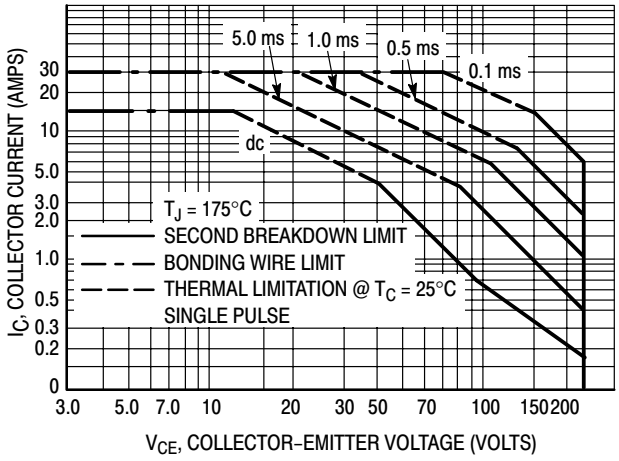


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

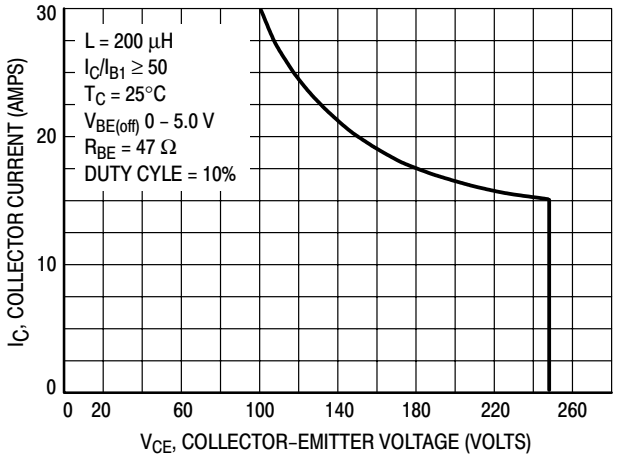


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 175°C, T_C is variable dependIng on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 175°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be hold to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

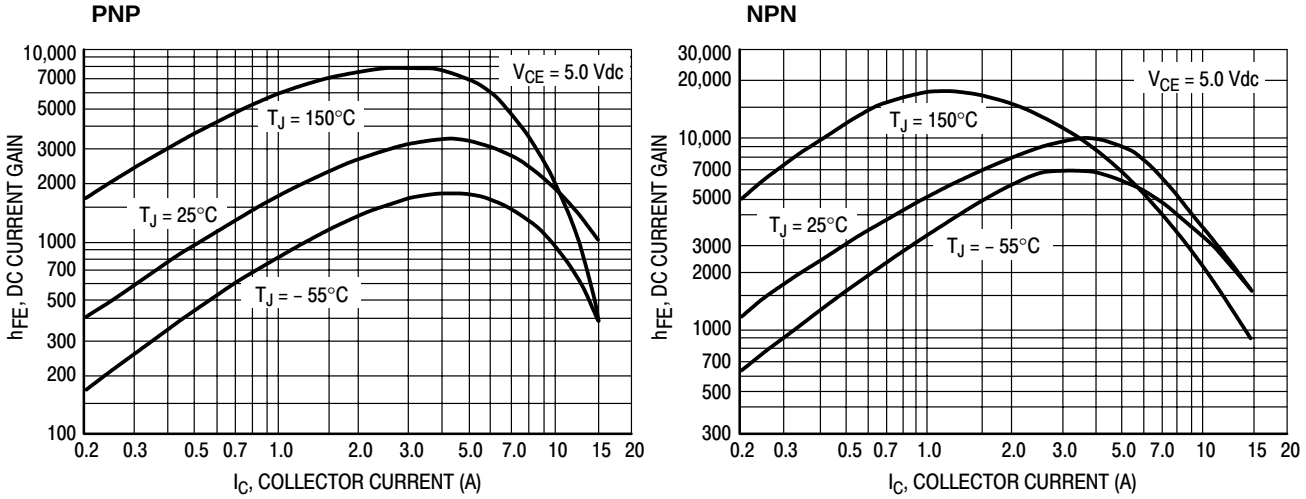


Figure 6. DC Current Gain

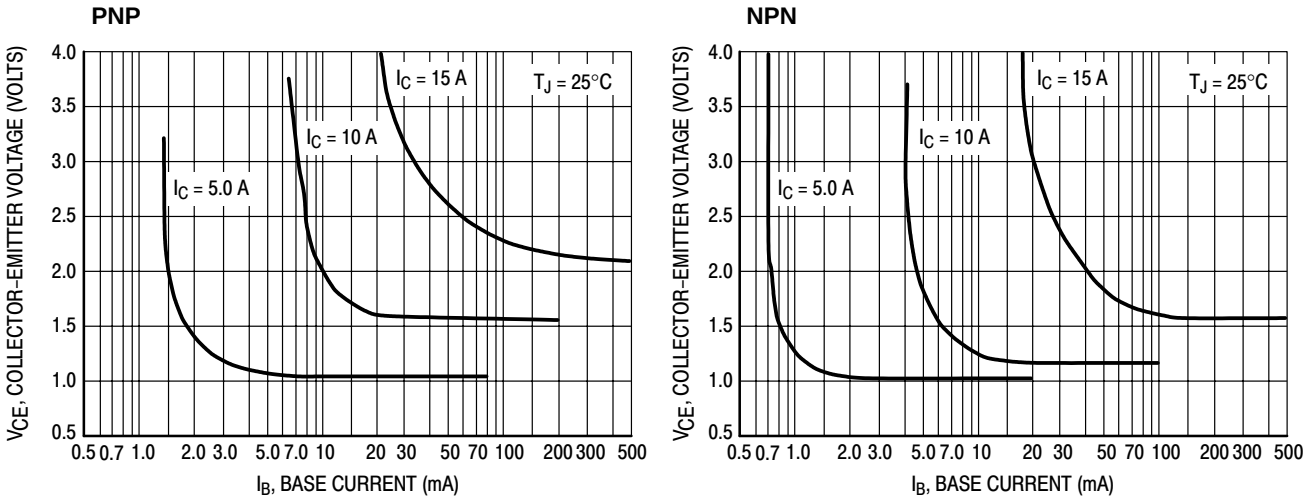


Figure 7. Collector Saturation Region

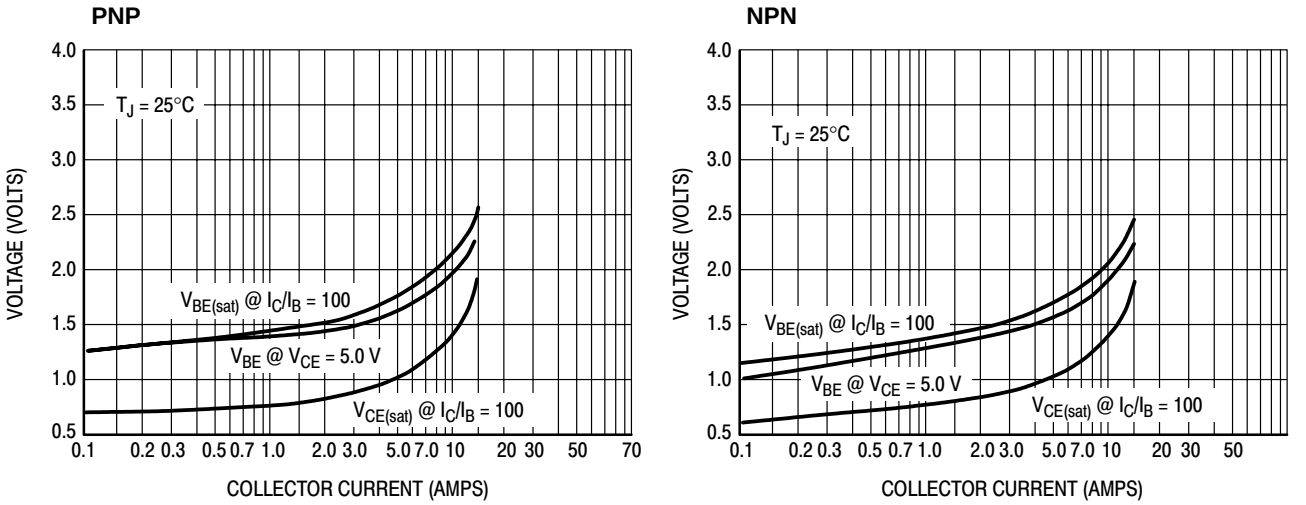


Figure 8. “On” Voltages

High-Current Complementary Silicon Transistors

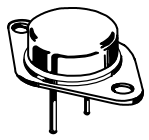
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 1000 (Min) @ I_C = 25 Adc
  h_{FE} = 400 (Min) @ I_C = 50 Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor
- Junction Temperature to +200°C

NPN
MJ11028
MJ11032*
PNP
MJ11029
MJ11033*

*ON Semiconductor Preferred Device

50 AMPERE COMPLEMENTARY SILICON DARLINGTON POWER TRANSISTORS 60–120 VOLTS 300 WATTS



CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11028 MJ11029	MJ11032 MJ11033	Unit
Collector–Emitter Voltage	V_{CEO}	60	120	Vdc
Collector–Base Voltage	V_{CB}	60	120	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C I_{CM}	50 100		Adc
Base Current — Continuous	I_B	2		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	300 1.71		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	°C

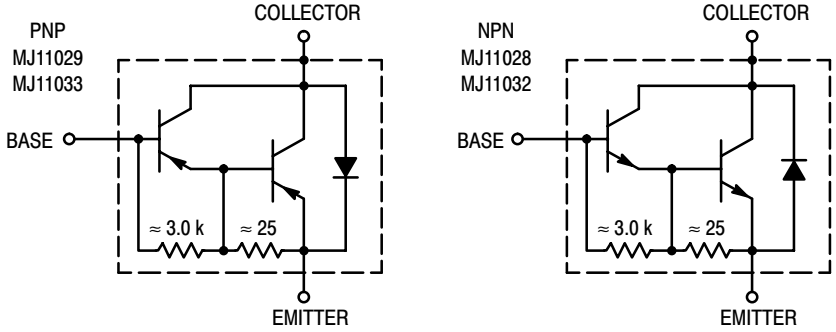


Figure 1. Darlington Circuit Schematic

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 3
Publication Order Number:
MJ11028/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (1)	MJ11028, MJ11029	$V_{(BR)CEO}$	60	—	Vdc
(I_C = 1 00 mAdc, I_B = 0)	MJ11032, MJ11033		120	—	
Collector–Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11028, MJ11029		—	2	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11032, MJ11033		—	2	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11028, MJ11029		—	10	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11032, MJ11033		—	10	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
Collector–Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 25 Adc, V_{CE} = 5 Vdc)			1 k	18 k	
(I_C = 50 Adc, V_{CE} = 5 Vdc)			400	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 250 mAdc)			—	2.5	
(I_C = 50 Adc, I_B = 500 mAdc)			—	3.5	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 200 mAdc)			—	3.0	
(I_C = 50 Adc, I_B = 300 mAdc)			—	4.5	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

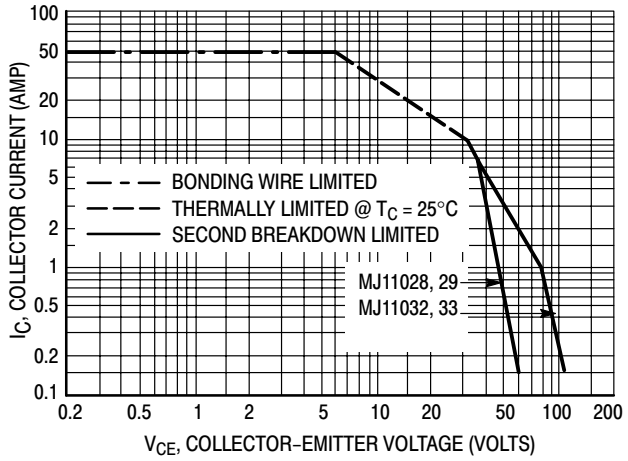


Figure 2. DC Safe Operating Area

There are two limitations on the power–handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

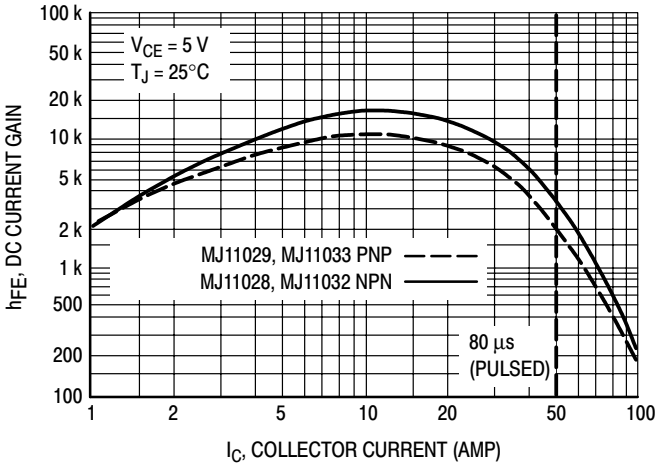


Figure 3. DC Current Gain

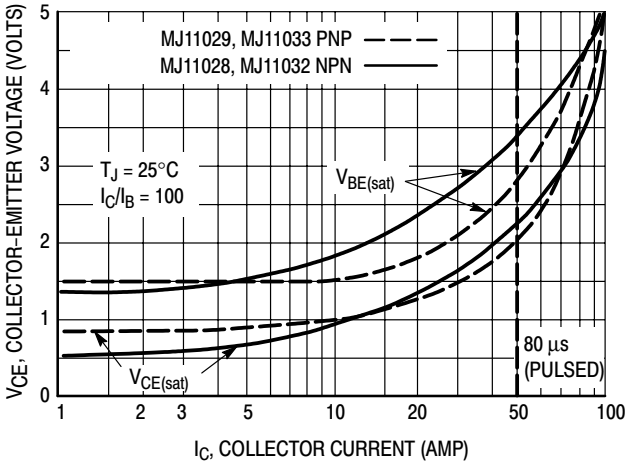


Figure 4. “On” Voltage

High-Current Complementary Silicon Power Transistors

. . . designed for use in high–power amplifier and switching circuit applications,

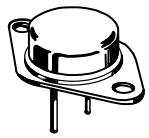
- High Current Capability —
  I_C Continuous = 60 Amperes
- DC Current Gain —
  h_{FE} = 15–100 @ I_C = 50 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

NPN
MJ14002*
PNP
MJ14001

MJ14003*

***ON Semiconductor Preferred Device**

60 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSITORS
60–80 VOLTS
300 WATTS



CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ14001	MJ14002 MJ14003	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector Base Voltage	V_{CBO}	60	80	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous	I_C	60		Adc
Base Current — Continuous	I_B	15		Adc
Emitter Current — Continuous	I_E	75		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 17		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

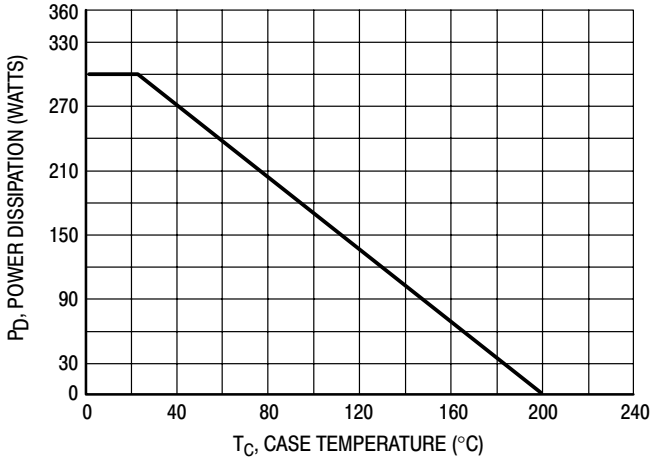


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	MJ14001 MJ14002, MJ14003	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	MJ14001 MJ14402, MJ14003	I_{CEO}	 — —	 1.0 1.0	mA
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14001 MJ14002, MJ14003	I_{CEX}	 — —	 1.0 1.0	mA
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	MJ14001 MJ14002, MJ14003	I_{CBO}	 — —	 1.0 1.0	mA
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 25 Adc, V_{CE} = 3.0 V) (I_C = 50 Adc, V_{CE} = 3.0 V) (I_C = 60 Adc, V_{CE} = 3.0 V)		h_{FE}	 30 15 5	 — 100 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 5.0 Adc) (I_C = 60 Adc, I_B = 12 Adc)		$V_{CE(sat)}$	 — — —	 1 2.5 3	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 5.0 Adc) (I_C = 60 Adc, I_B = 12 Adc)		$V_{BE(sat)}$	 — — —	 2 3 4	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	2000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

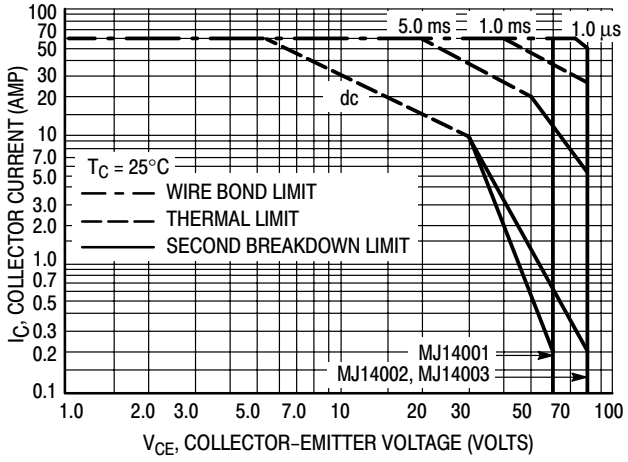


Figure 2. Maximum Rated Forward Biased Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL ELECTRICAL CHARACTERISTICS

NPN
MJ14002

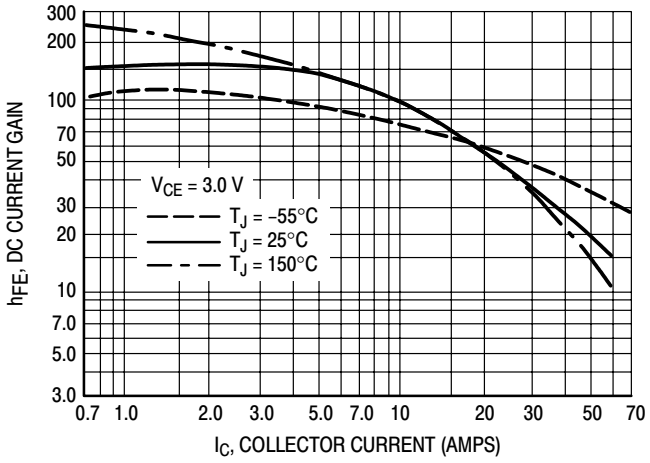


Figure 3. DC Current Gain

PNP
MJ14001, MJ14003

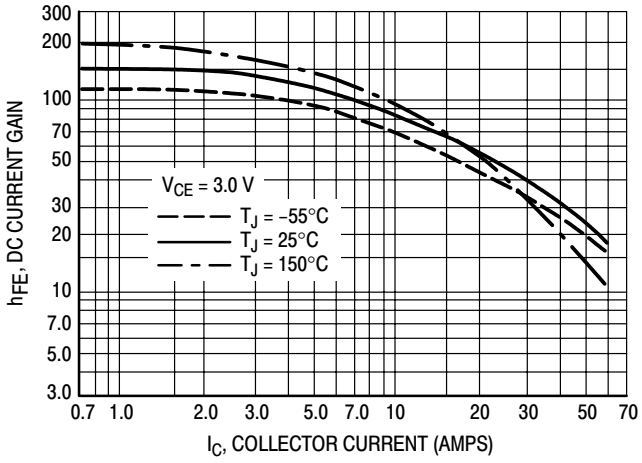


Figure 4. DC Current Gain

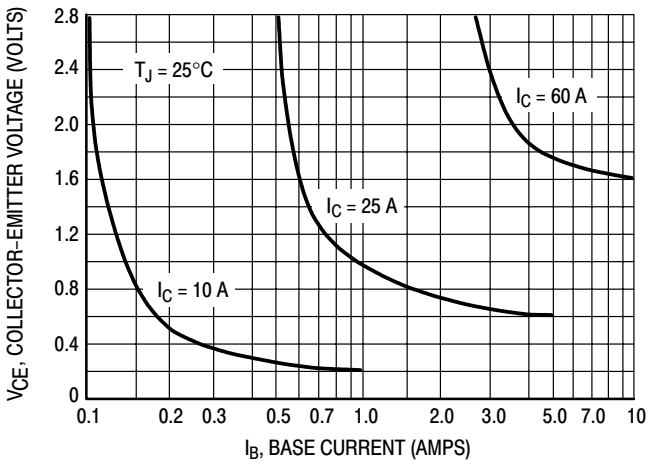


Figure 5. Collector Saturation Region

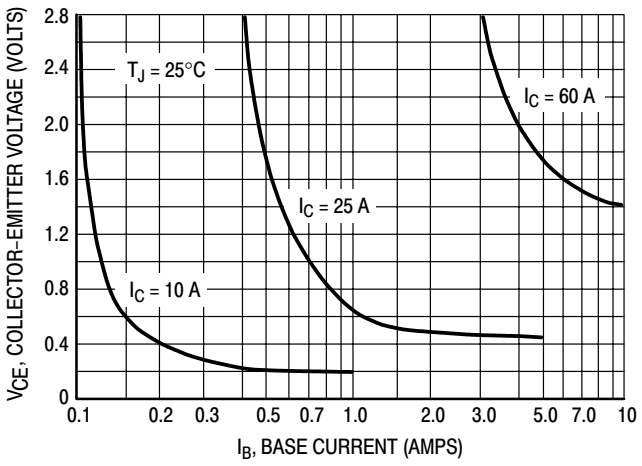


Figure 6. Collector Saturation Region

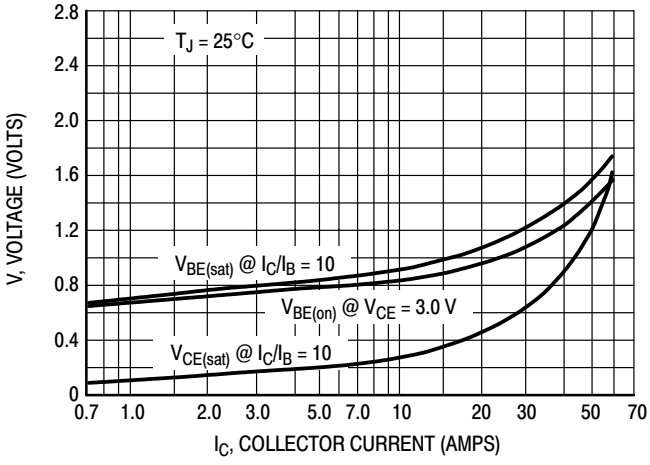


Figure 7. “On” Voltages

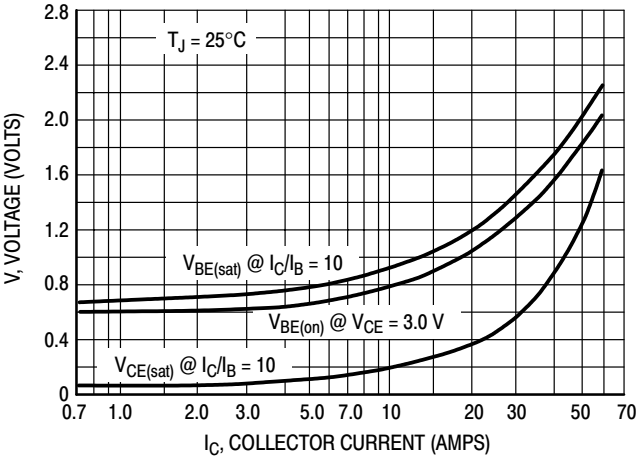


Figure 8. “On” Voltages

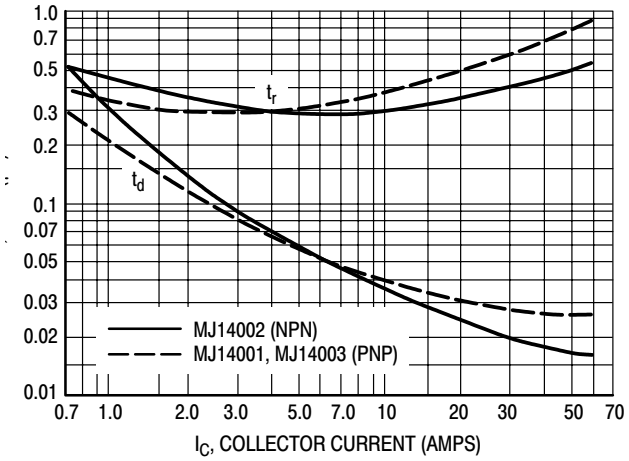


Figure 9. Turn–On Switching Times

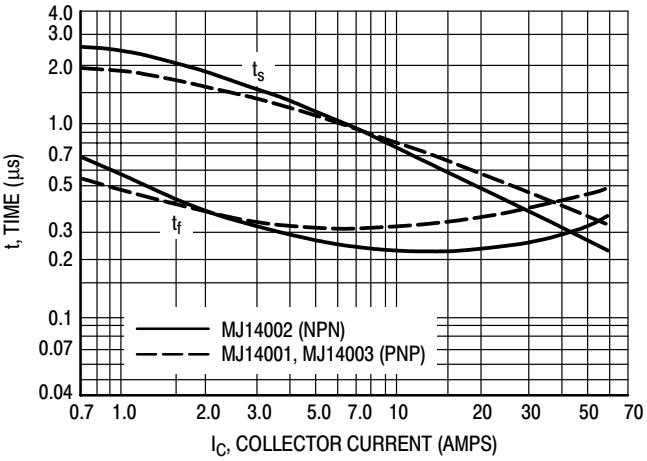


Figure 10. Turn–Off Switching Times

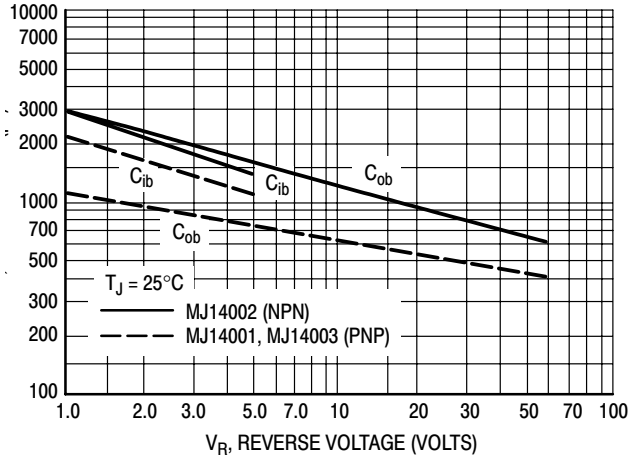
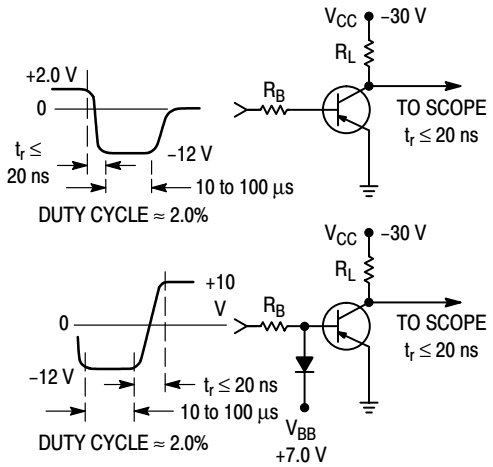


Figure 11. Capacitance Variation



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 12. Switching Test Circuit

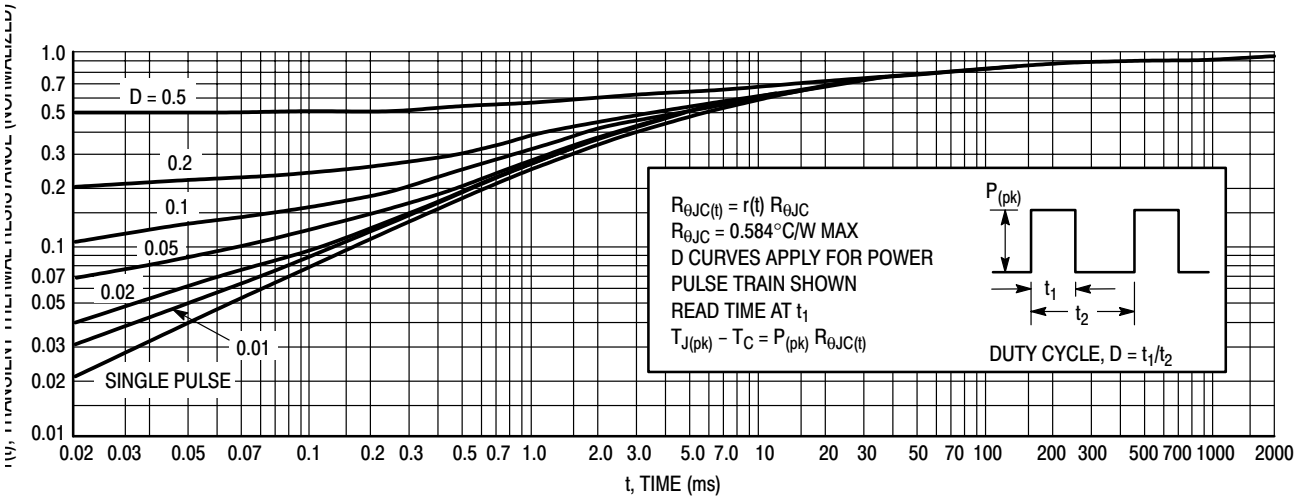


Figure 13. Thermal Response

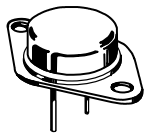
Complementary Silicon Power Transistors

NPN
MJ15001
PNP
MJ15002

The MJ15001 and MJ15002 are EpiBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  200 W @ 40 V
  50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain —
  h_{FE} = 25 (Min) @ I_C = 4 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CBO}	140	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤ 10 seconds	T_L	265	°C

March, 2001 – Rev. 2
Publication Order Number:
MJ15001/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C, = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 100 2	 μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non–repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non–repetitive))	$I_{S/b}$	 5 0.5	 — —	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

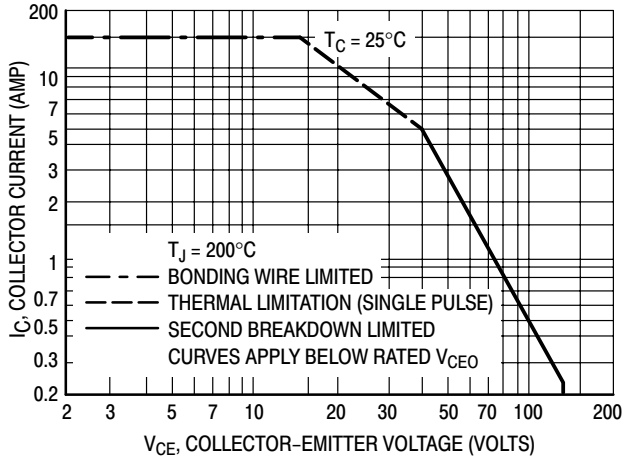


Figure 1. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J\,(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

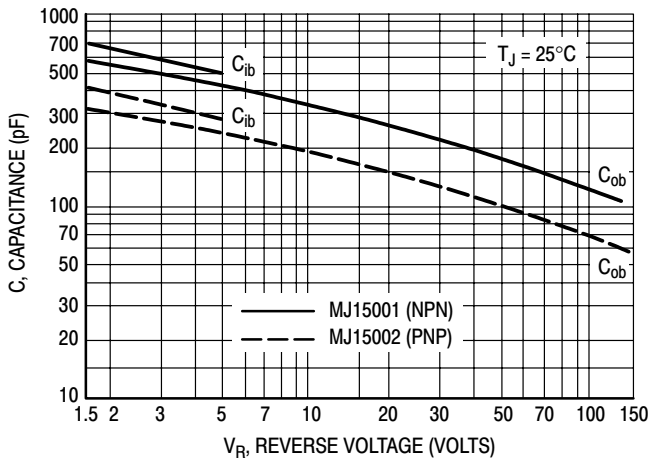


Figure 2. Capacitances

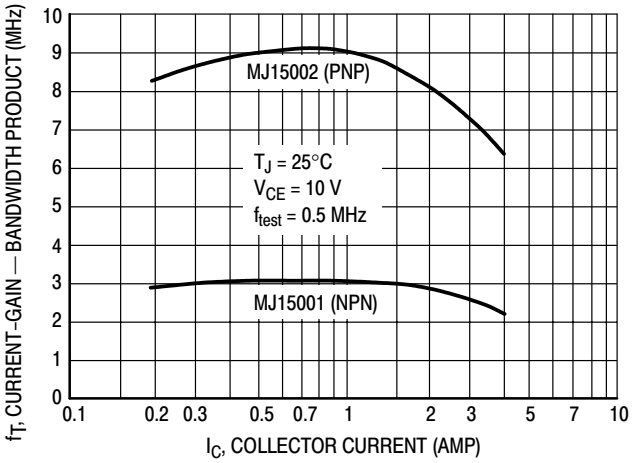


Figure 3. Current–Gain — Bandwidth Product

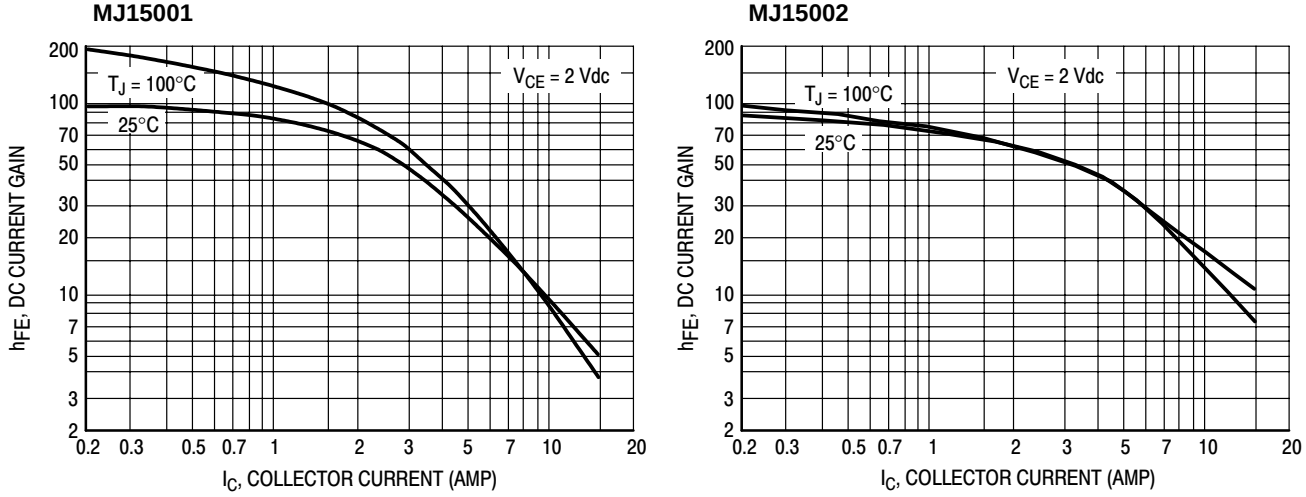


Figure 4. DC Current Gain

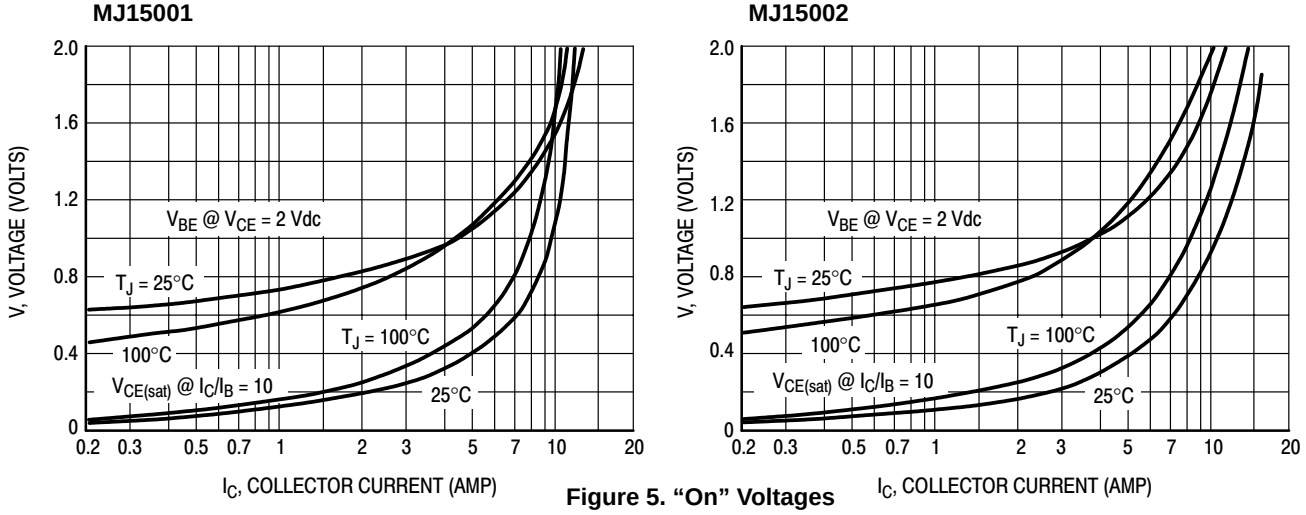


Figure 5. “On” Voltages

Complementary Silicon Power Transistors

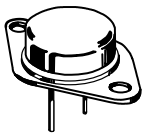
The MJ15003 and MJ15004 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) — 250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain — h_{FE} = 25 (Min) @ I_C = 5 Adc

NPN
MJ15003*
PNP
MJ15004*

*ON Semiconductor Preferred Device

20 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CBO}	140	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	20	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤ 10 seconds	T_L	265	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
MJ15003/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 100 2	 μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Baised (V_{CE} = 50 Vdc, t = 1 s (non repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non repetitive))	$I_{S/b}$	 5 1	 — —	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	
Collector Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base Emitter On Voltage (I_C = 5 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	c_{ob}	—	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

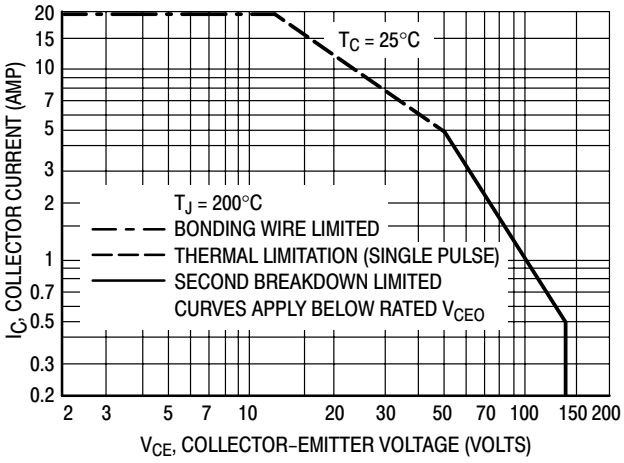


Figure 1. Active−Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Silicon Power Transistors

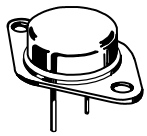
NPN
MJ15011*
PNP
MJ15012*

*ON Semiconductor Preferred Device

The MJ15011 and MJ15012 are PowerBase power transistors designed for high–power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc–to–dc converters or inverters.

- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE COMPLEMENTARY POWER TRANSISTORS 250 VOLTS 200 WATTS



CASE 1–07 TO–204AA (TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Emitter Voltage	V_{CEX}	250	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 2
Publication Order Number:
MJ15011/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{(BR)CEO}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	—	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 15 Vdc)	I_{CEX}	—	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	—	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	 20 5	 100 —	—
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.2 Adc) (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	 — —	 0.8 2 5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	—	750	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 0.5 s) (V_{CE} = 100 Vdc, t = 0.5 s)	$I_{S/b}$	 5 1.4	 — —	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

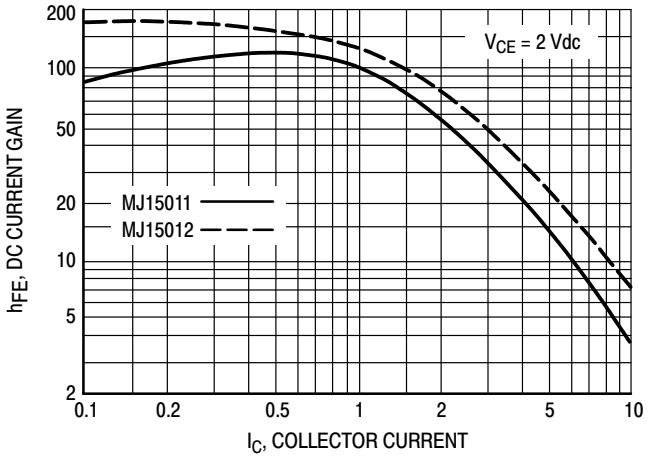


Figure 2. DC Current Gain

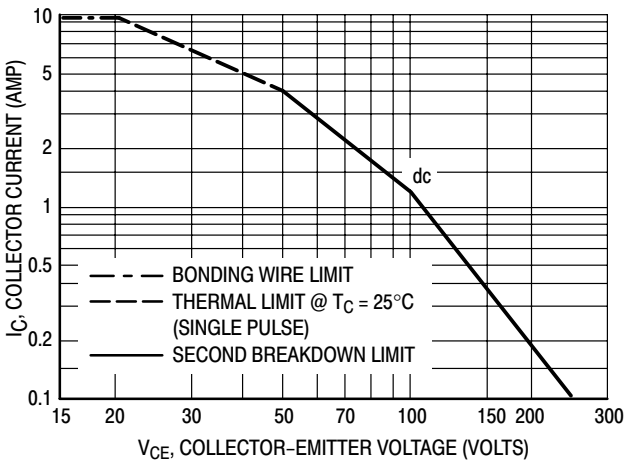


Figure 3. Active Region Safe Operating Area

Complementary Silicon Power Transistors

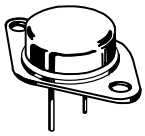
. . . designed for use as high frequency drivers in Audio Amplifiers.

- High Gain Complementary Silicon Power Transistors
- Safe Operating Area 100% Tested 50 V, 3.0 A, 1.0 Sec.
- Excellent Frequency Response — f_T = 20 MHz min.

NPN
MJ15020*
PNP
MJ15021*

*ON Semiconductor Preferred Device

4.0 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ15020 MJ15021	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	250	Vdc
Emitter–Base Voltage	V_{EBO}	7.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	6.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

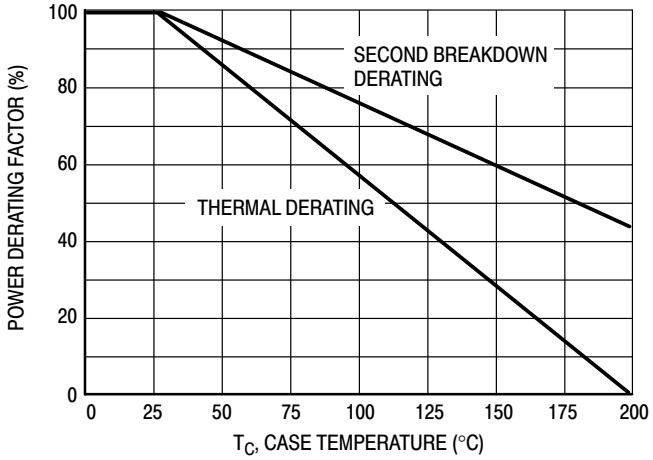


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0) MJ15020, MJ15021	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) MJ15020, MJ15021	I_{CEO}	—	500	μAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	500	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward–Biased (V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive)	$I_{S/b}$	3.0	—	Adc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 V) (I_C = 3.0 Adc, V_{CE} = 4.0 V)	h_{FE}	30 10	— —	
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter on Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	20	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, F_{test} = 1.0 MHz)	C_{ob}	—	500	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

TYPICAL DYNAMIC CHARACTERISTICS

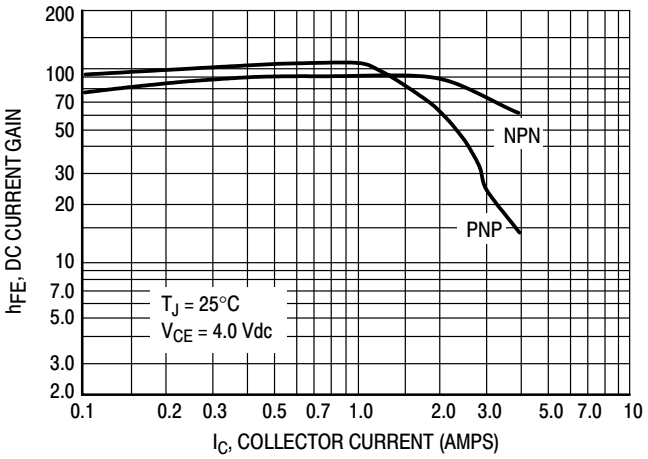


Figure 2. DC Current Gain

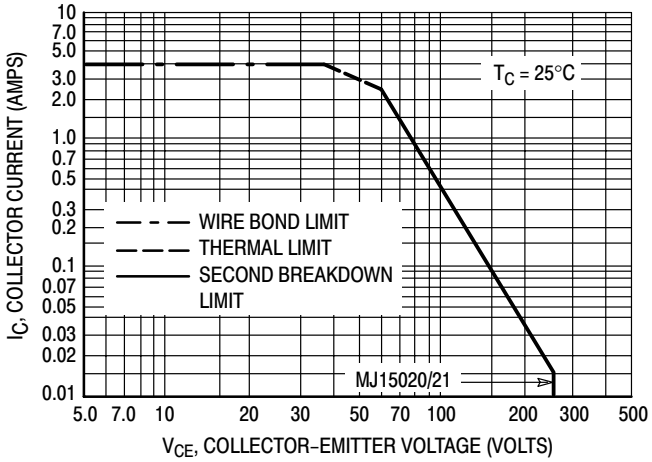


Figure 3. Maximum Rated Forward Biased Safe Operating Area

NPN
MJ15022
MJ15024 *

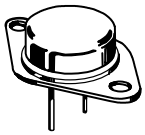
*ON Semiconductor Preferred Device

Silicon Power Transistors

The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  2 A @ 80 V
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Base Voltage	V_{CBO}	350	400	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector–Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 9
Publication Order Number:
MJ15022/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	 MJ15022 MJ15024	$V_{CEO(sus)}$	 200 250	 — —	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15022 MJ15024	I_{CEX}	 — —	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 vdc, I_B = 0)	 MJ15022 MJ15024	I_{CEO}	 — —	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)		I_{EBO}	—	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non–repetitive))		$I_{S/b}$	 5 2	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 —	—
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 — —	 1.4 4.0	Vdc
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

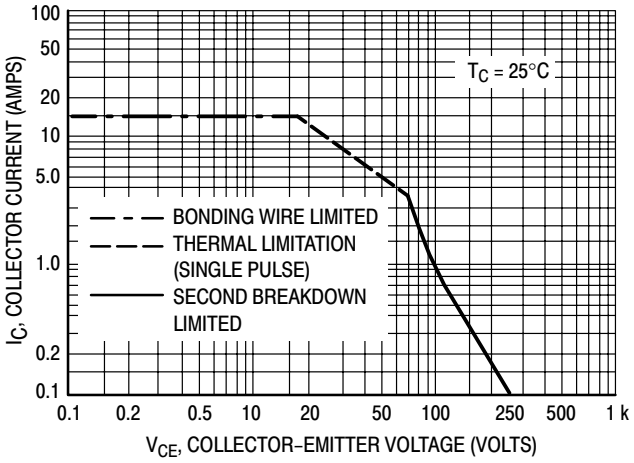


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values Ion than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

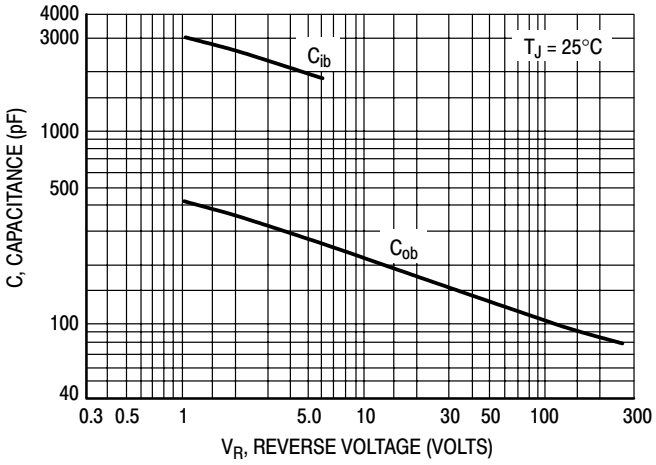


Figure 2. Capacitances

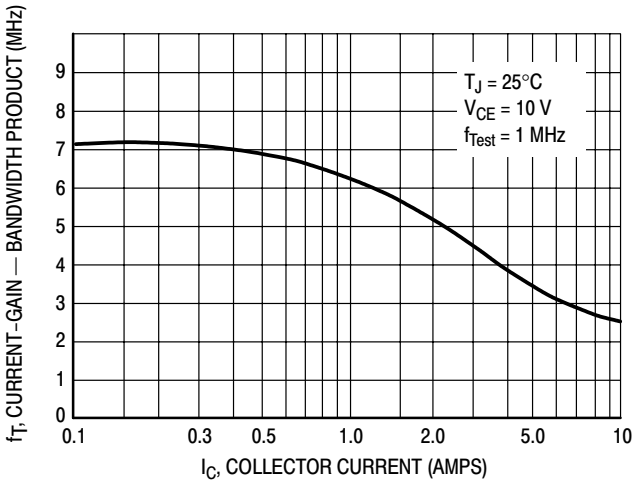


Figure 3. Current–Gain — Bandwidth Product

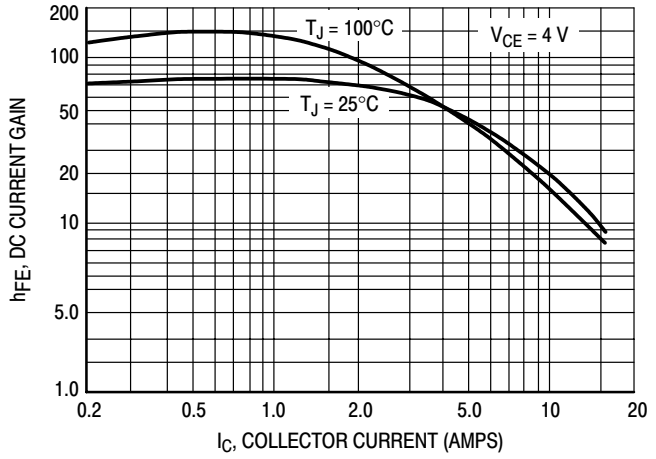


Figure 4. DC Current Gain

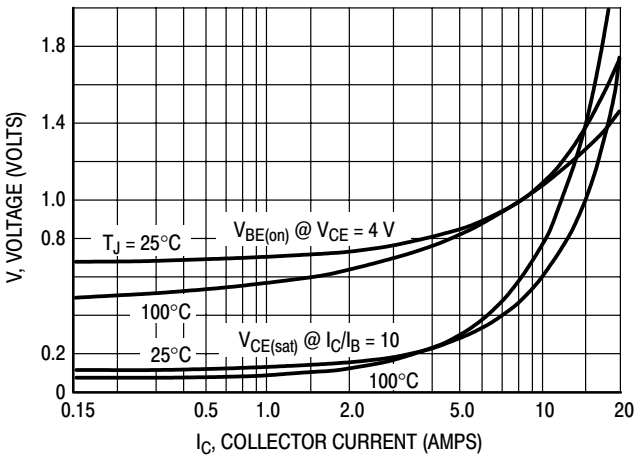


Figure 5. “On” Voltage

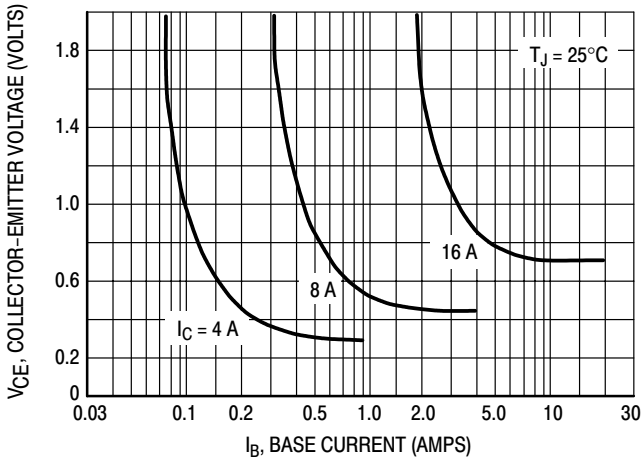


Figure 6. Collector Saturation Region

PNP
MJ15023
MJ15025 *

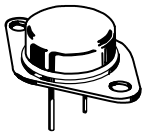
*ON Semiconductor Preferred Device

Silicon Power Transistors

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  2 A @ 80 V
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Base Voltage	V_{CBO}	350	400	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector–Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			
(I_C = 100 mAdc, I_B = 0)	MJ15023		200	—	
	MJ15025		250	—	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15023		—	250	
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15025		—	250	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJ15023		—	500	
(V_{CE} = 200 Vdc, I_B = 0)	MJ15025		—	500	
Emitter Cutoff Current		I_{EBO}	—	500	μAdc
(V_{CE} = 5 Vdc, I_B = 0)	Both				
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive))			5	—	
(V_{CE} = 80 Vdc, t = 0.5 s (non–repetitive))			2	—	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 8 Adc, V_{CE} = 4 Vdc)			15	60	
(I_C = 16 Adc, V_{CE} = 4 Vdc)			5	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			—	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)				4.0	
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.2	Vdc
(I_C = 8 Adc, V_{CE} = 4 Vdc)					
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	4	—	MHz
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Output Capacitance		C_{ob}	—	600	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

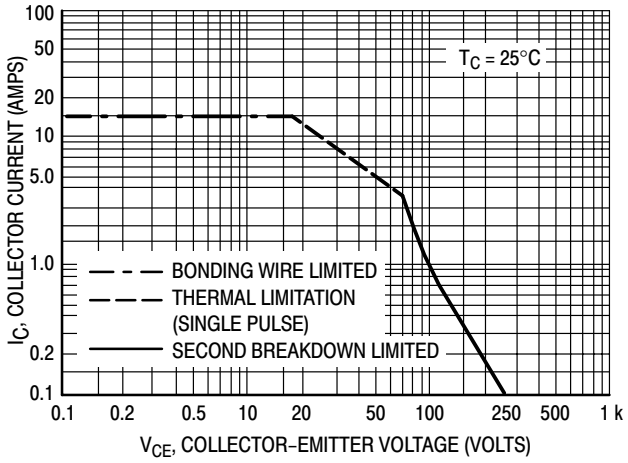


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

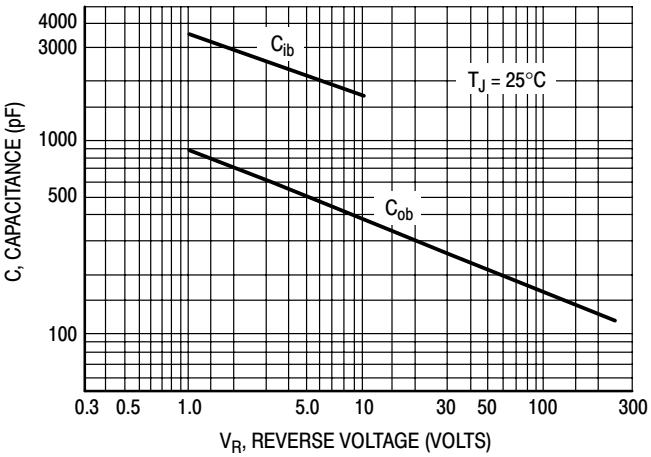


Figure 2. Capacitances

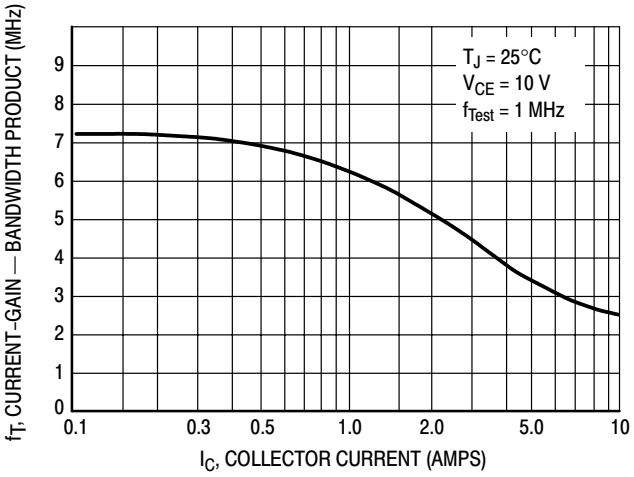


Figure 3. Current–Gain — Bandwidth Product

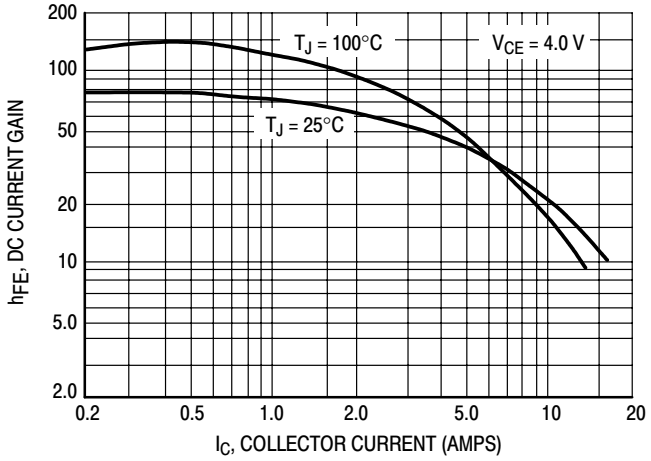


Figure 4. DC Current Gain

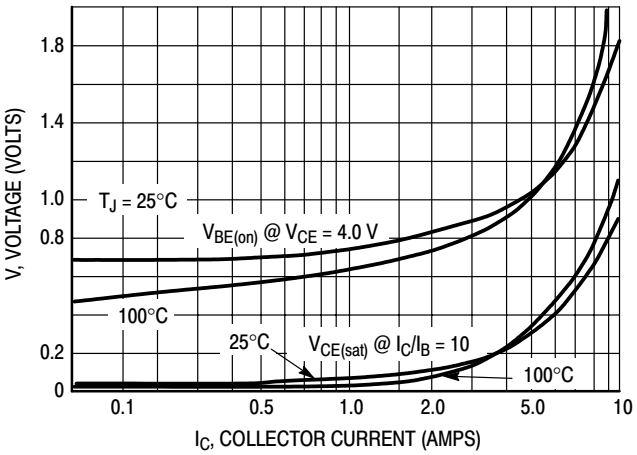


Figure 5. “On” Voltages

PNP
MJ21193*
NPN
MJ21194*

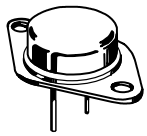
*ON Semiconductor Preferred Device

Silicon Power Transistors

The MJ21193 and MJ21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –
  h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.5 A, 80 V, 1 Second

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 250 WATTS



CASE 1–07 TO–204AA (TO–3)

MAXIMUM RATINGS

Rating	Sym-bol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current — Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%. (continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 3
Publication Order Number:
MJ21193/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive)		5	—	—	
(V_{CE} = 80 Vdc, t = 1 s (non–repetitive)		2.5	—	—	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}			75	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		25	—		
(I_C = 16 Adc, I_B = 5 Adc)		8	—		
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)		—	—	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)		—	—	4	
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output	T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched		—	0.8	—	
ed					
(Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched		—	0.08	—	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJ21193

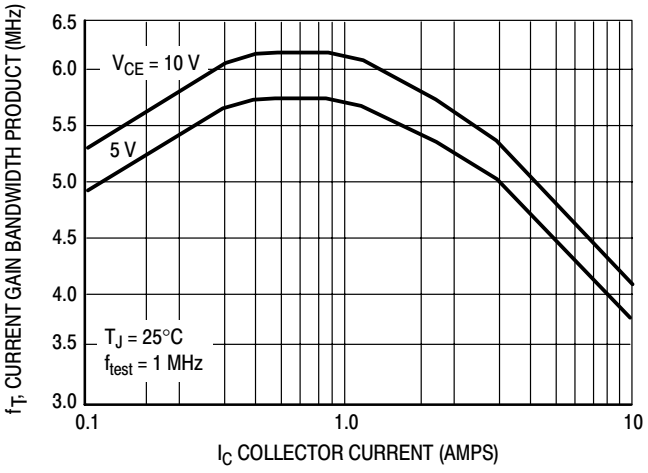


Figure 1. Typical Current Gain Bandwidth Product

NPN MJ21194

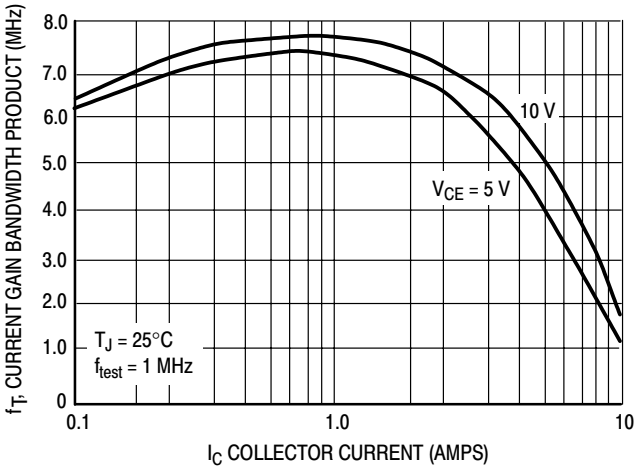


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJ21193

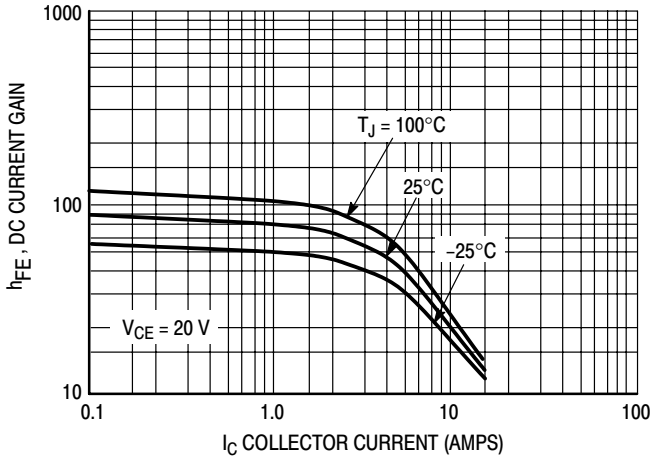


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJ21194

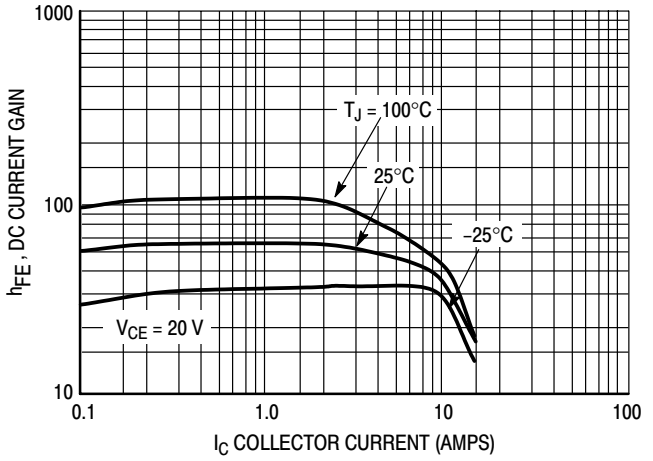


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJ21193

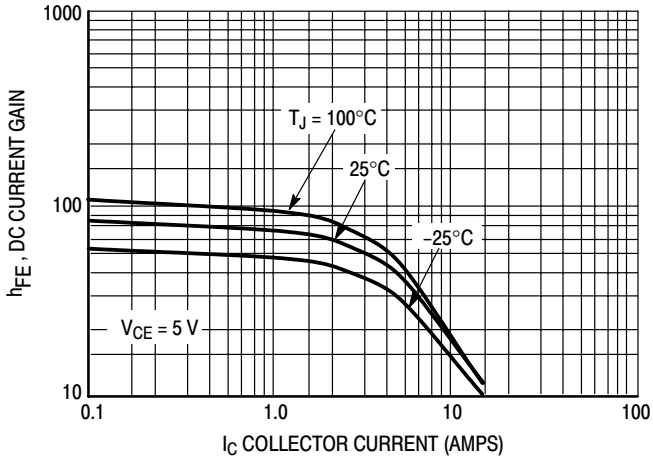


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ21194

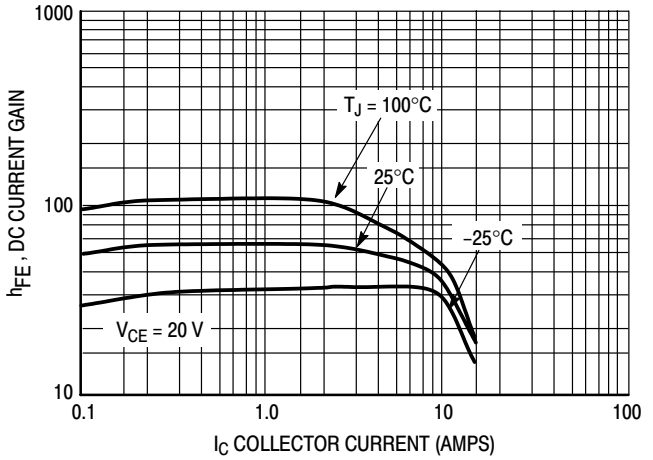


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJ21193

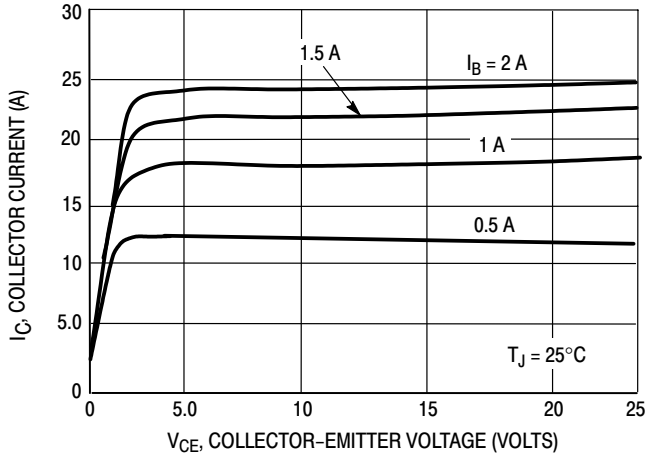


Figure 7. Typical Output Characteristics

NPN MJ21194

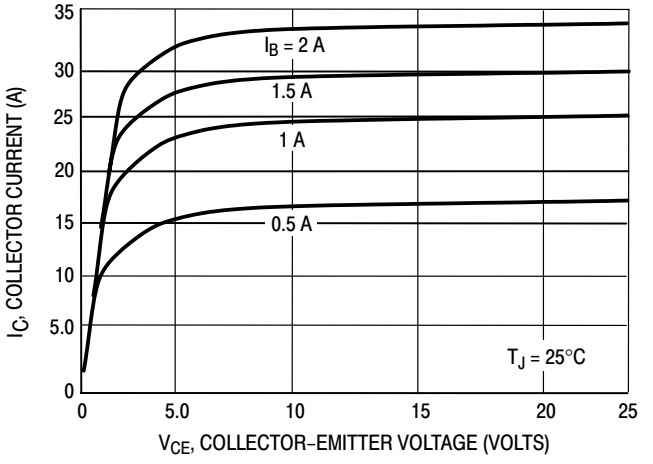


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21193

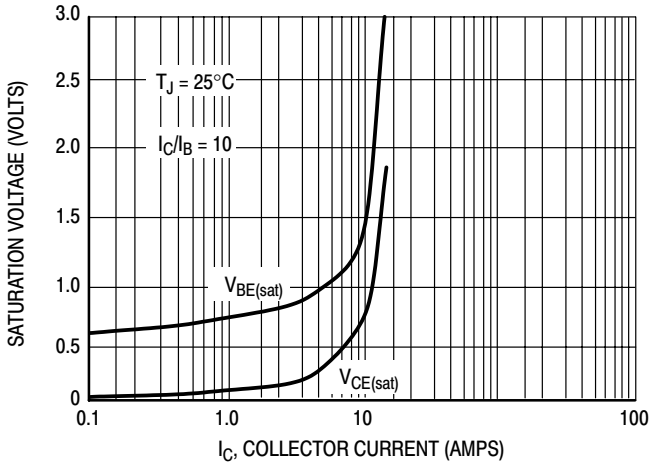


Figure 9. Typical Saturation Voltages

NPN MJ21194

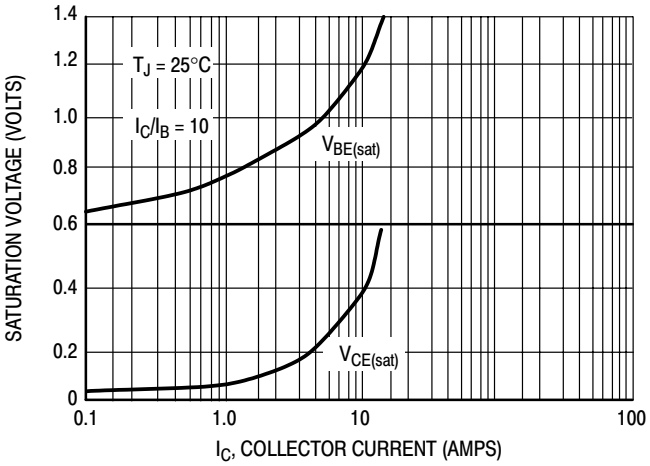


Figure 10. Typical Saturation Voltages

PNP MJ21193

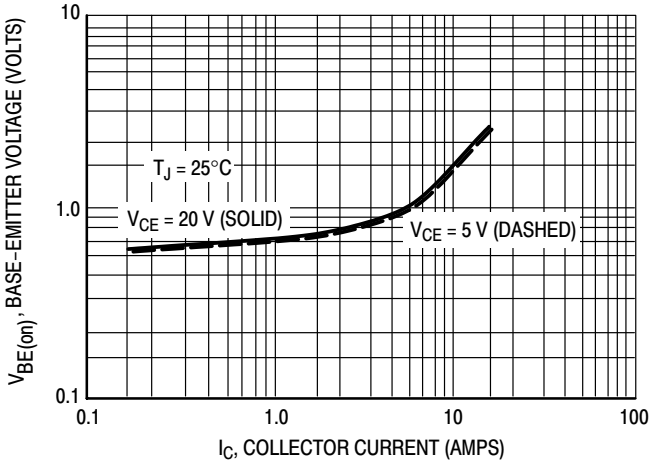


Figure 11. Typical Base–Emitter Voltage

NPN MJ21194

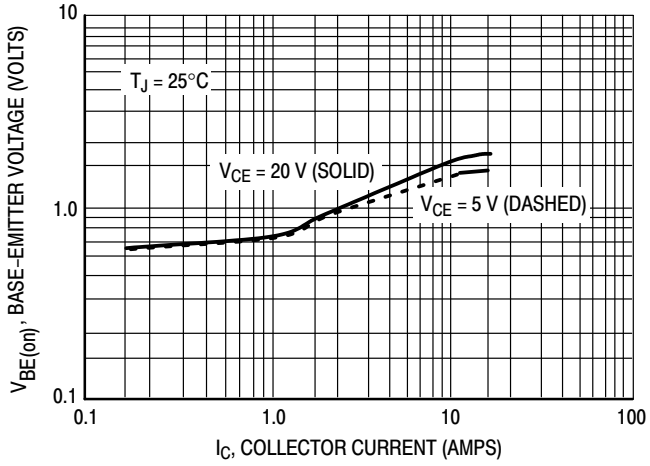


Figure 12. Typical Base–Emitter Voltage

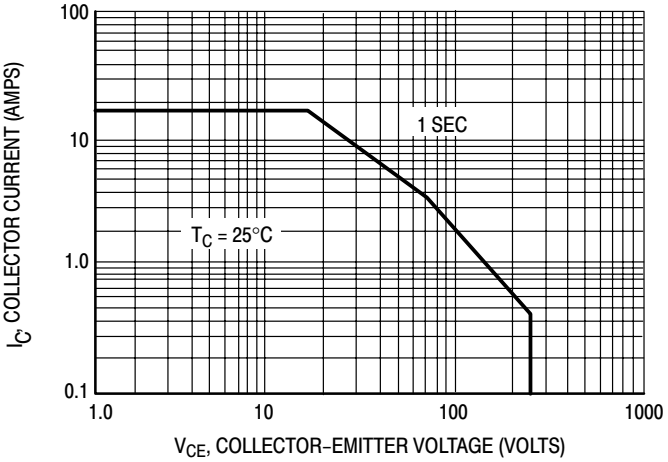


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

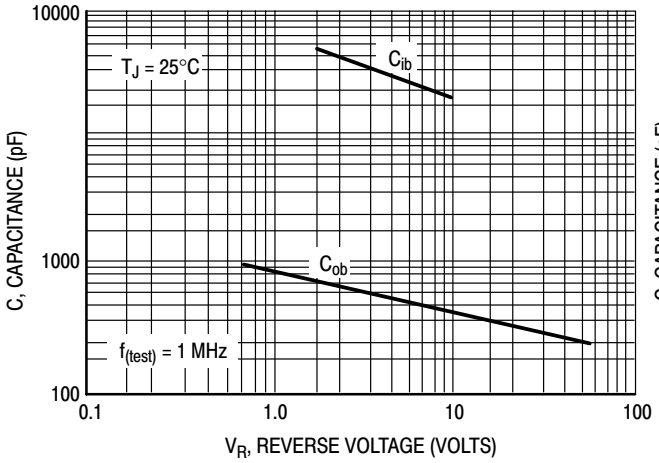


Figure 14. MJ21193 Typical Capacitance

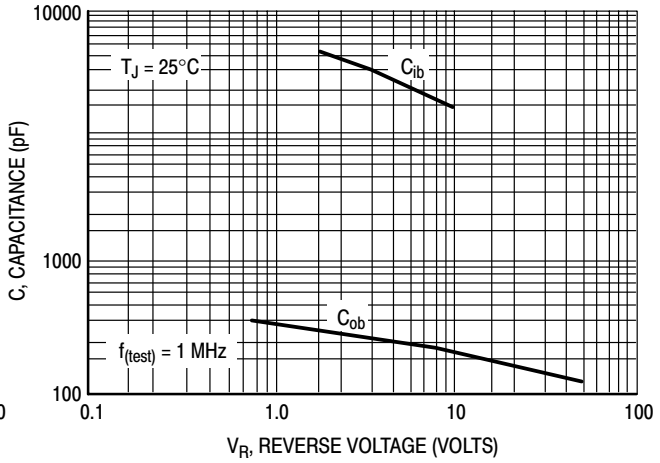


Figure 15. MJ21194 Typical Capacitance

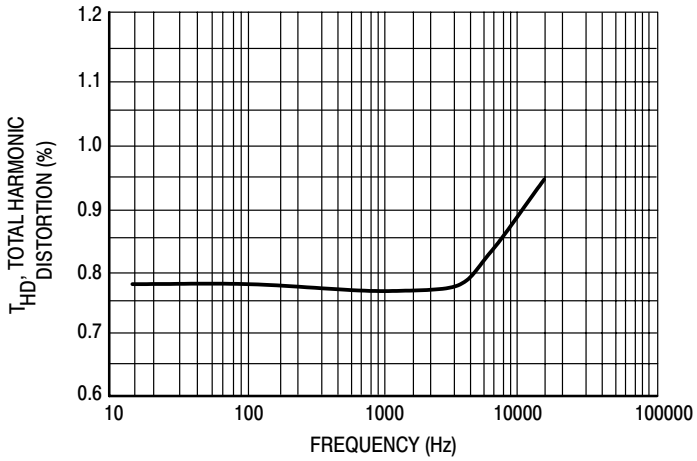


Figure 16. Typical Total Harmonic Distortion

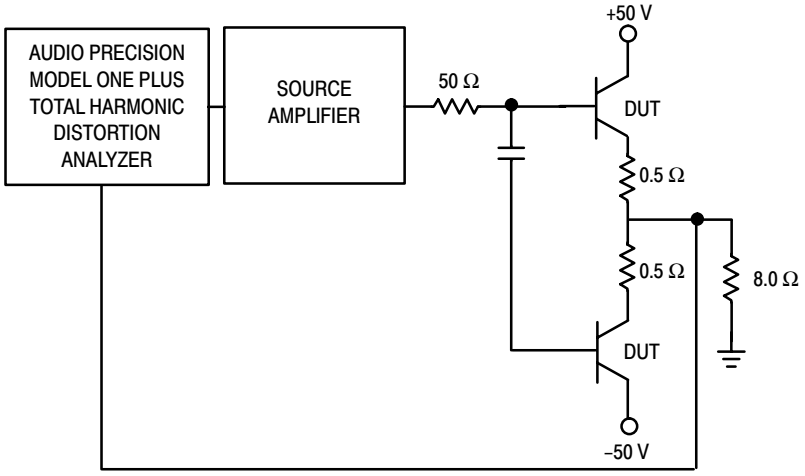


Figure 17. Total Harmonic Distortion Test Circuit

Silicon Power Transistors

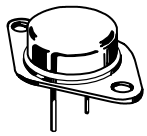
PNP
MJ21195*
NPN
MJ21196*

*ON Semiconductor Preferred Device

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –
  h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Second

16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Sym-bol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current — Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C ± 5°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 2
Publication Order Number:
MJ21195/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non–repetitive) (V_{CE} = 80 Vdc, t = 1 s (non–repetitive)	$I_{S/b}$	 5 2.5	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, V_{CE} = 5 Vdc)	h_{FE}	 25 8	 — —	75	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 — —	 1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 — —	 0.8 0.08	 — —	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJ21195

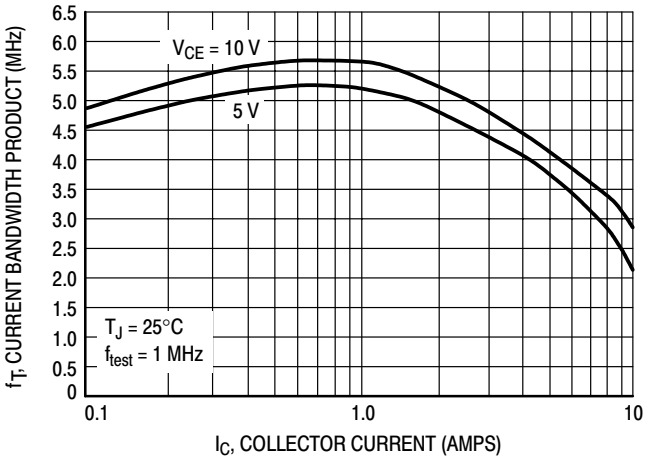


Figure 1. Typical Current Gain Bandwidth Product

NPN MJ21196

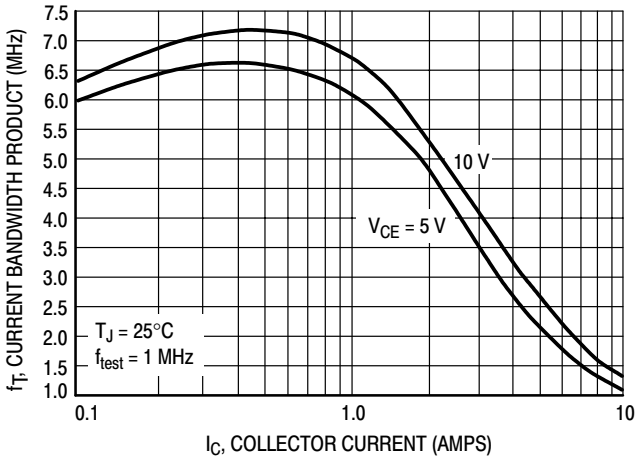


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJ21195

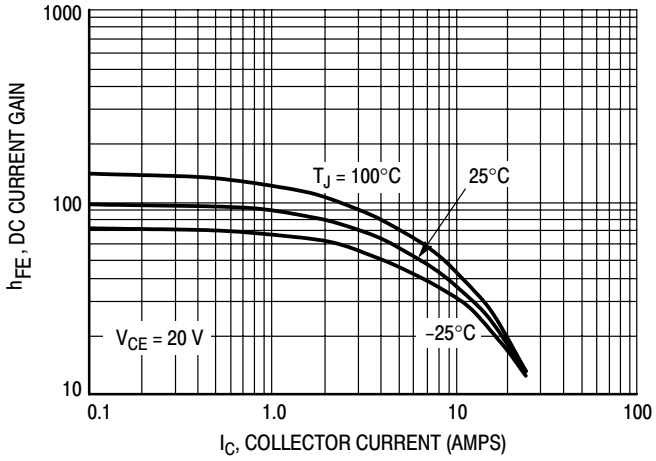


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJ21196

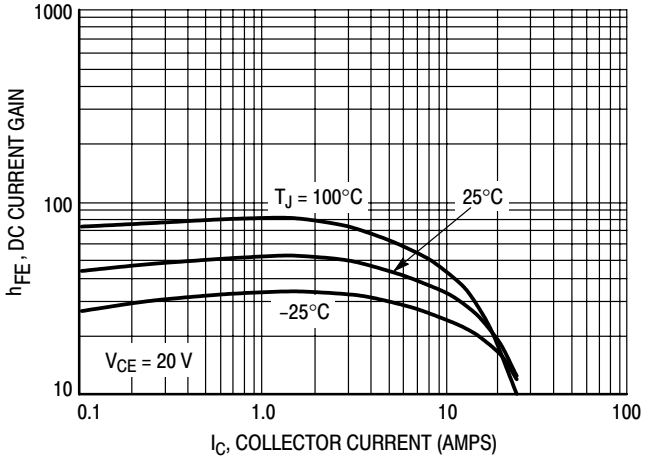


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJ21195

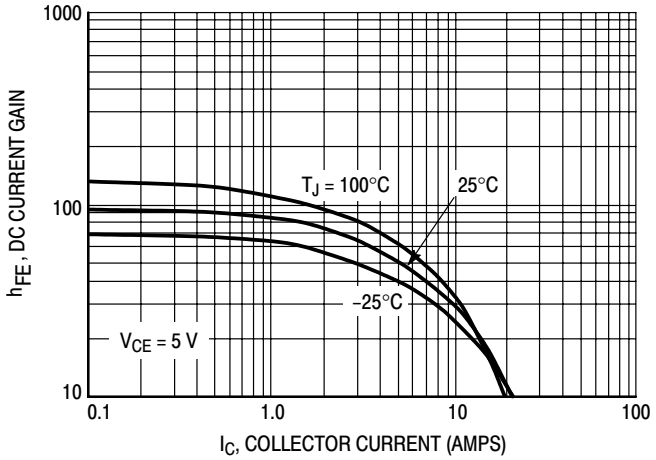


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ21196

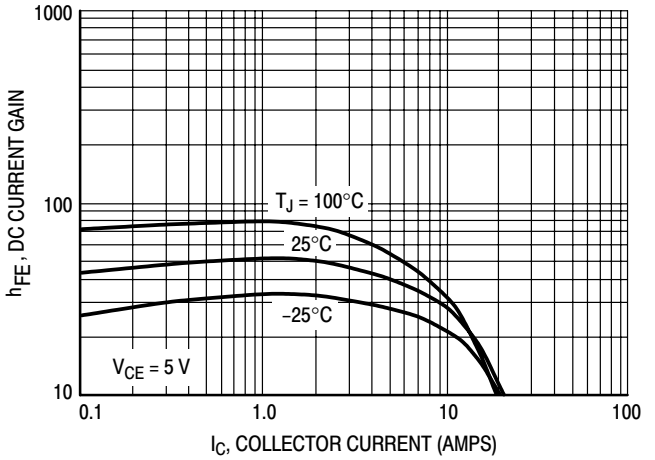


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJ21195

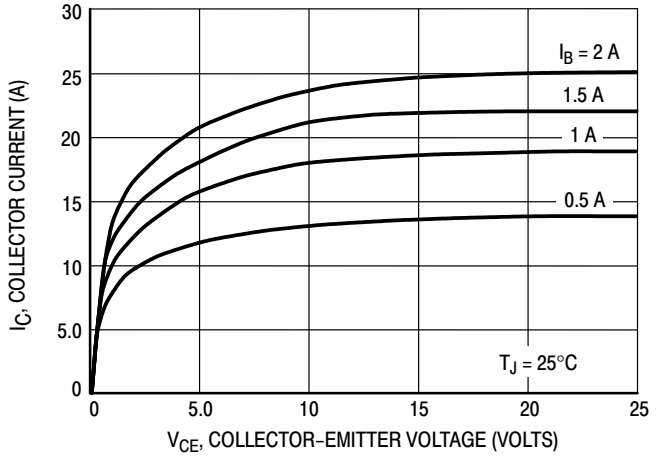


Figure 7. Typical Output Characteristics

NPN MJ21196

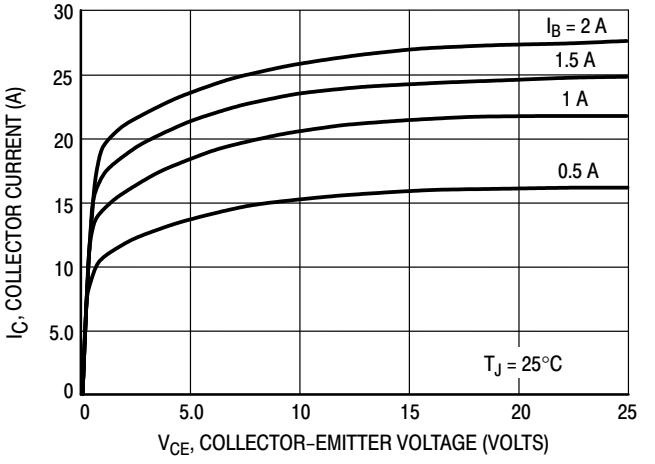


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21195

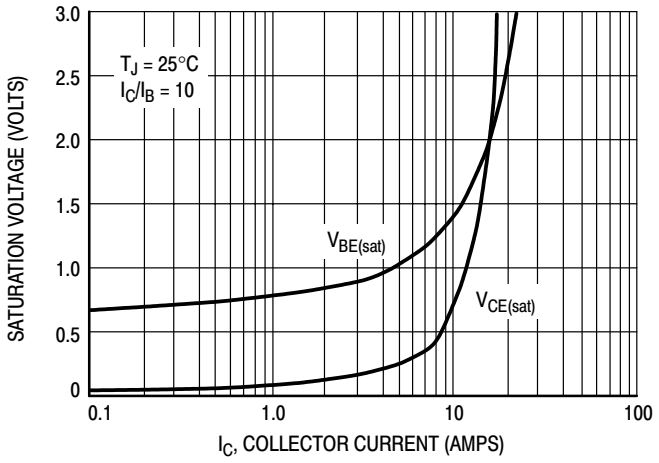


Figure 9. Typical Saturation Voltages

NPN MJ21196

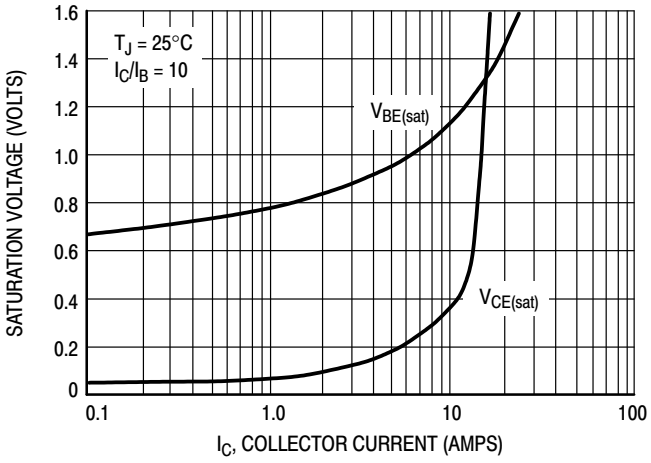


Figure 10. Typical Saturation Voltages

PNP MJ21195

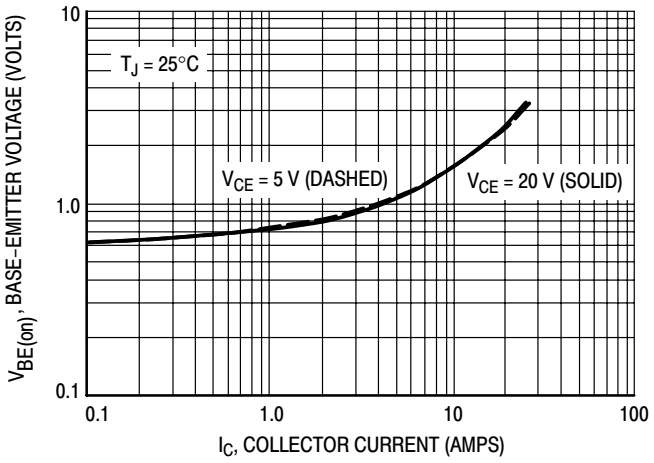


Figure 11. Typical Base–Emitter Voltage

NPN MJ21196

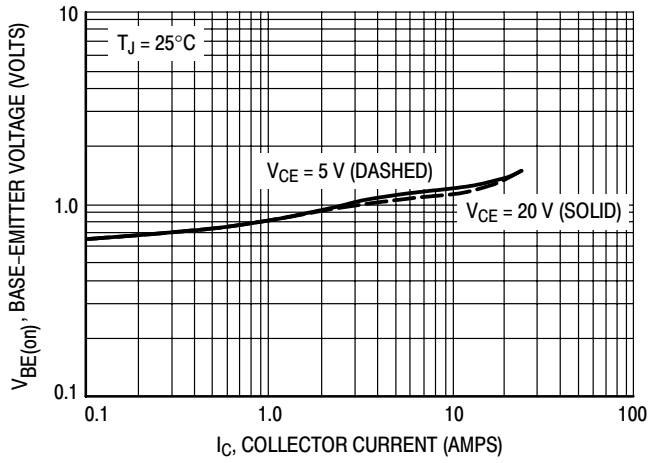


Figure 12. Typical Base–Emitter Voltage

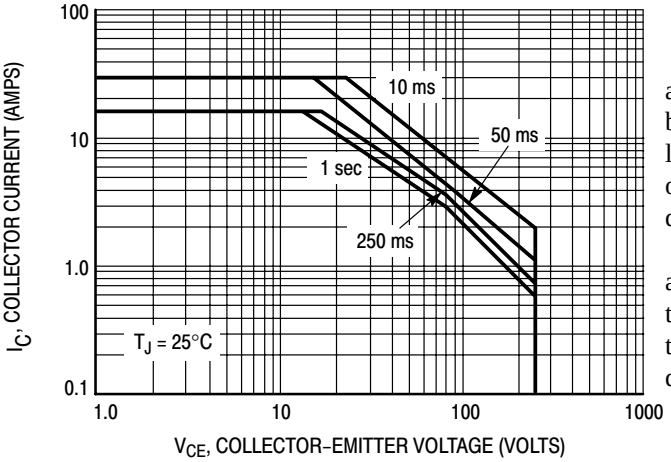


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

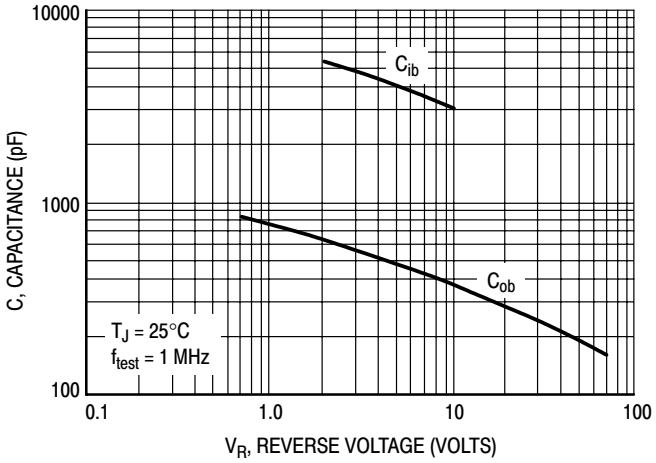


Figure 14. MJ21195 Typical Capacitance

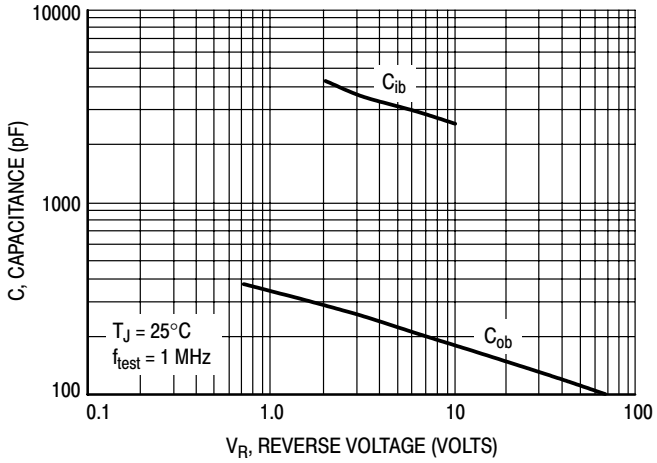


Figure 15. MJ21196 Typical Capacitance

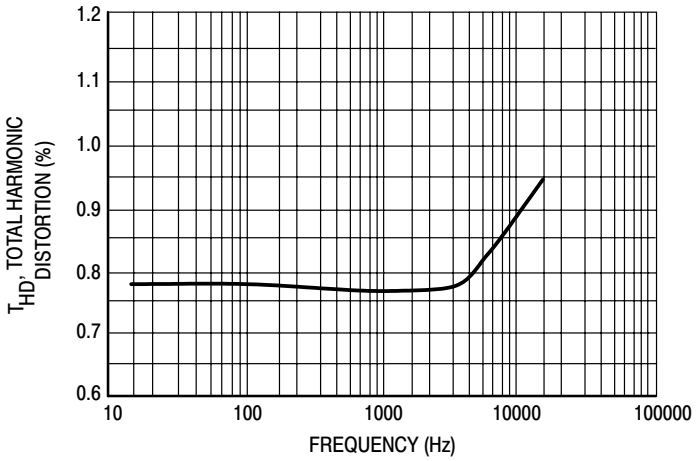


Figure 16. Typical Total Harmonic Distortion

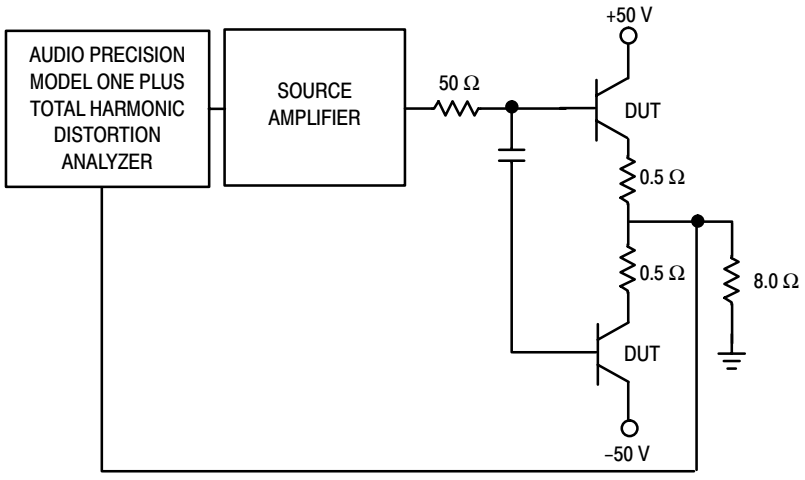


Figure 17. Total Harmonic Distortion Test Circuit

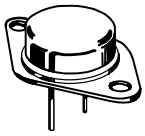
MJ4502

High–Power PNP Silicon Transistor

30 AMPERE
POWER TRANSISTOR
PNP SILICON
100 VOLTS
200 WATTS

. . . for use as an output device in complementary audio amplifiers to 100–Watts music power per channel.

- High DC Current Gain —
  h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the NPN MJ802



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	90	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

MAXIMUM RATINGS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

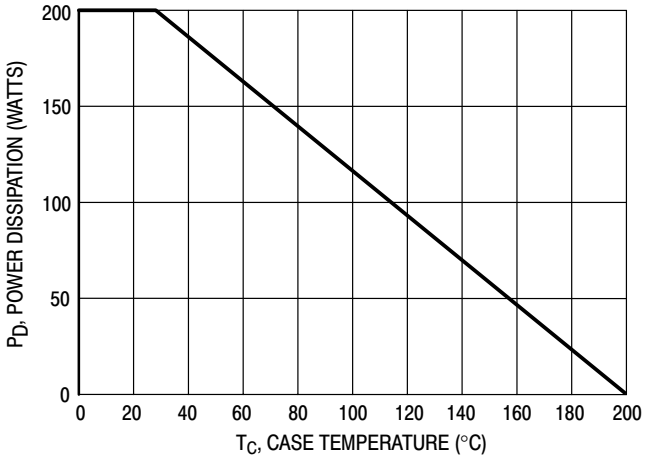


Figure 1. Power–Temperature Derating Curve

April, 2001 – Rev. 9
Publication Order Number:
MJ4502/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage[1] (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{(BR)CER}$	100	—	Vdc
Collector–Emitter Sustaining Voltage[1] (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter–Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base–Emitter “On” Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Collector–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	—	MHz

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

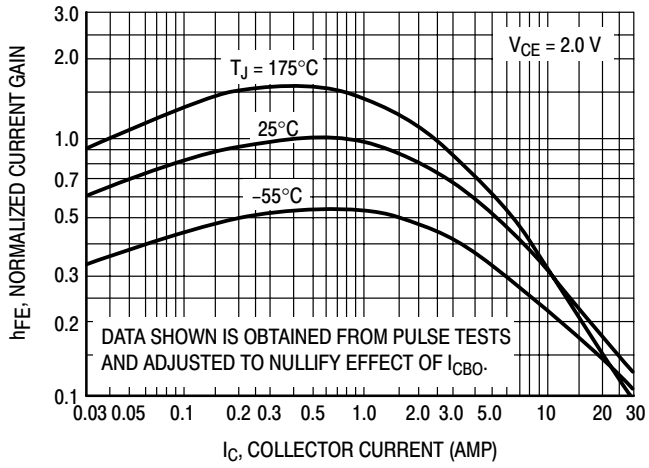


Figure 2. DC Current Gain

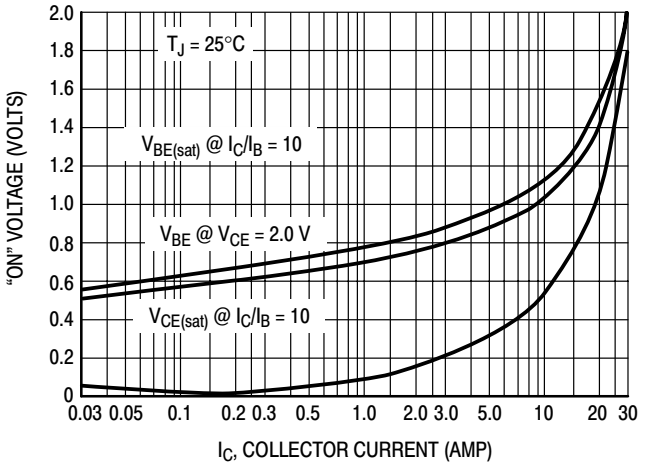


Figure 3. “On” Voltages

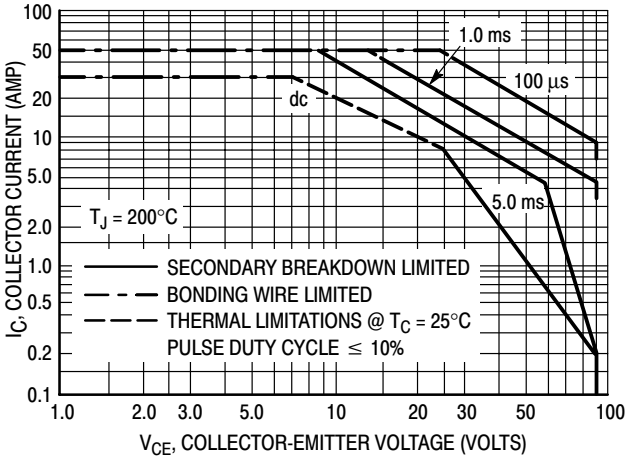


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

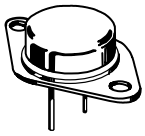
MJ802

High-Power NPN Silicon Transistor

30 AMPERE
POWER TRANSISTOR
NPN SILICON
100 VOLTS
200 WATTS

. . . for use as an output device in complementary audio amplifiers to 100–Watts music power per channel.

- High DC Current Gain —
  h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	90	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

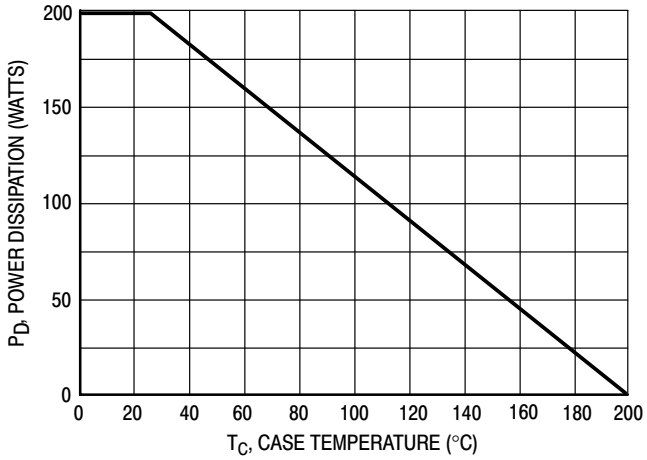


Figure 1. Power–Temperature Derating Curve

April, 2001 – Rev. 9
Publication Order Number:
M J802/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage[1] (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	—	Vdc
Collector–Emitter Sustaining Voltage[1] (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter–Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain[1] (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base–Emitter “On” Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Collector–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	—	MHz

[1]Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.

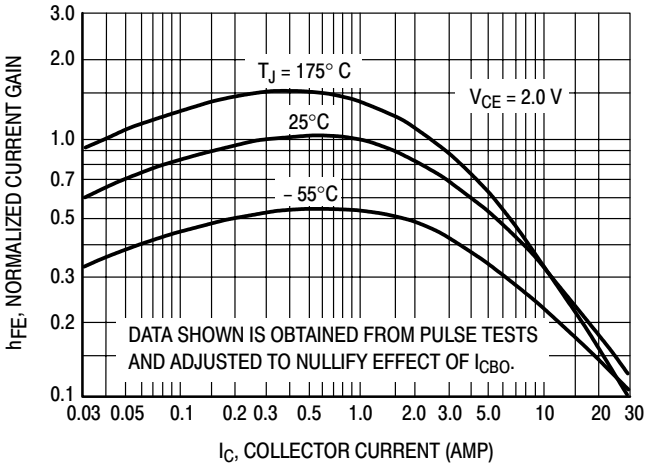


Figure 2. DC Current Gain

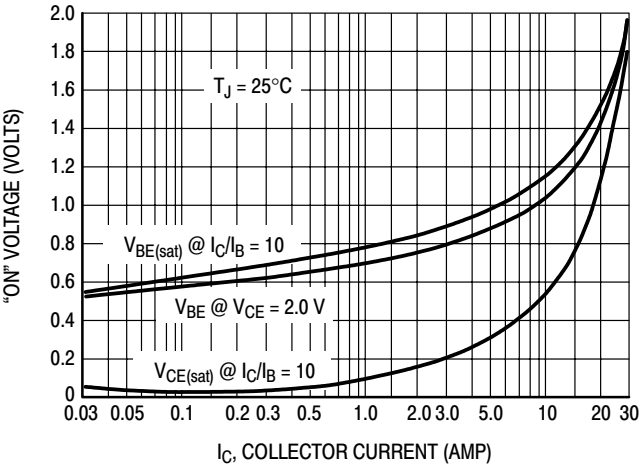


Figure 3. "On" Voltages

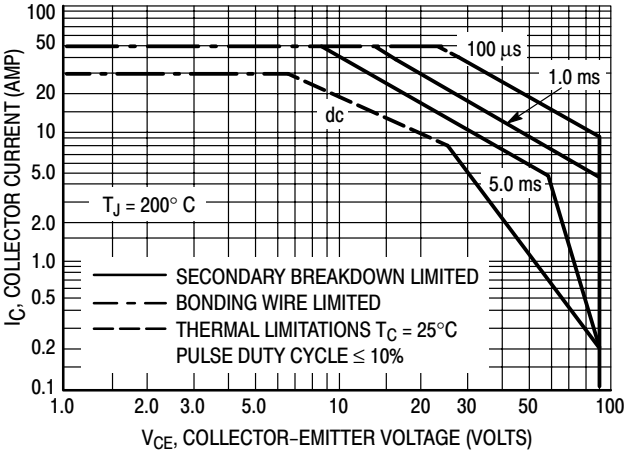


Figure 4. Active Region Safe Operating Area

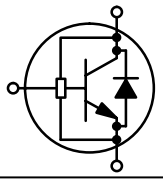
The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power temperature derating must be observed for both steady state and pulse power conditions.

MJB18004D2T4

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

D2PAK For Surface Mount

POWER TRANSISTORS
5 AMPERES
1000 VOLTS
75 WATTS



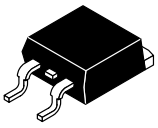
The MJB18004D2T4 is state–of–art High Speed High gain Bipolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

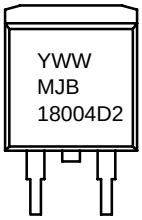
- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- “6 Sigma” Process Providing Tight and Reproductible Parameter Spreads

It’s characteristics make it also suitable for PFC application.

MARKING DIAGRAM



D^2PAK
CASE 418B
STYLE 1



Y = Year
WW = Work Week

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W
Junction to Ambient, When Mounted With the Minimun Recommended Pad Size.	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	547		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	1000	1100		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.9 0.8	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.45 0.75	0.75 1	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.9 1.6	1.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.25 0.28	0.5 0.6	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 10	28 14		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	8 6		
(I_C = 1 Adc, V_{CE} = 2.5 Vdc)	@ T_C = 25°C @ T_C = 125°C		18 14	28 20		
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc I_{B1} = 100 mA V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	9 16	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		3.1 9	
	I_C = 2 Adc I_{B1} = 0.4 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		11 18	
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		1.4 8	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 1 Adc)		@ T_C = 25°C @ T_C = 125°C	V_{EC}		0.96 0.72	1.5	V
(I_{EC} = 2 Adc)		@ T_C = 25°C @ T_C = 125°C			1.15 0.8	1.7	
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/μs)		@ T_C = 25°C	t_{fr}		440		ns
(I_F = 1 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
(I_F = 2 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		60	100	pF
Input Capacitance (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			C_{ib}		450	750	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 1 Adc V_{CC} = 250 Vdc	@ T_C = 25°C	t_{on}		500	750	ns
Turn–off Time		@ T_C = 25°C	t_{off}	1.1		1.4	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		100 150	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.6	1.3	μs
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		120 500	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	1.85	 2.6	2.15	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 2.5 Adc I_{B1} = 500 mAdc I_{B2} = 500 mAdc V_Z = 350 V L_C = 300 μH	@ T_C = 25°C @ T_C = 125°C	t_f		130 300	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.12 2.6	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		355 750	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 400 mAdc I_{B2} = 400 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		95 230	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 2.9	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		300 700	450	ns
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		70 100	90	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.7 1.05	0.9	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		75 160	120	ns

TYPICAL STATIC CHARACTERISTICS

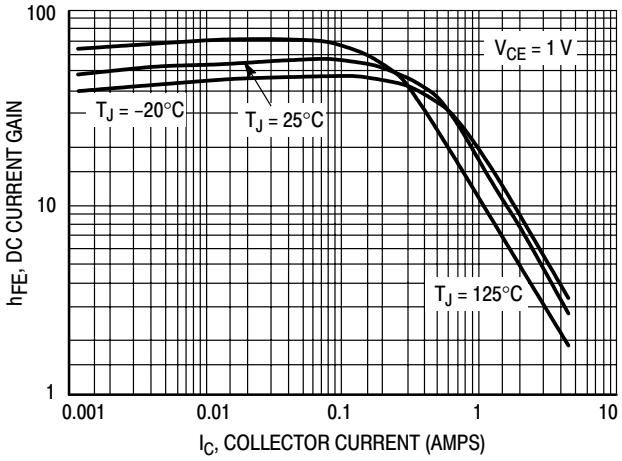


Figure 1. DC Current Gain @ 1 Volt

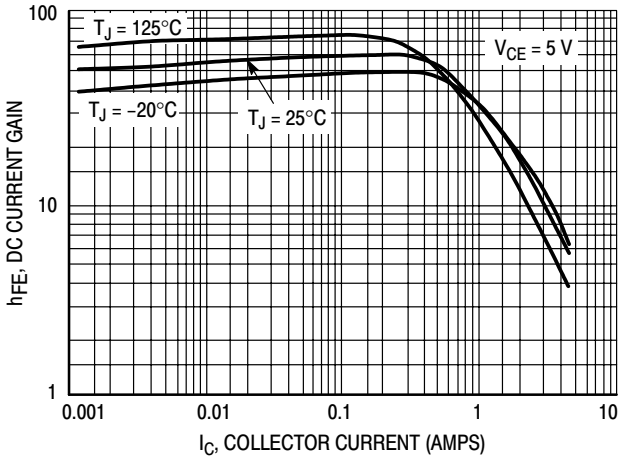


Figure 2. DC Current Gain @ 5 Volt

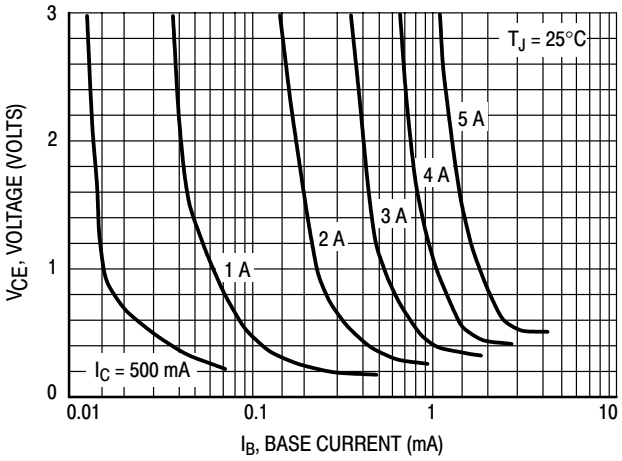


Figure 3. Collector Saturation Region

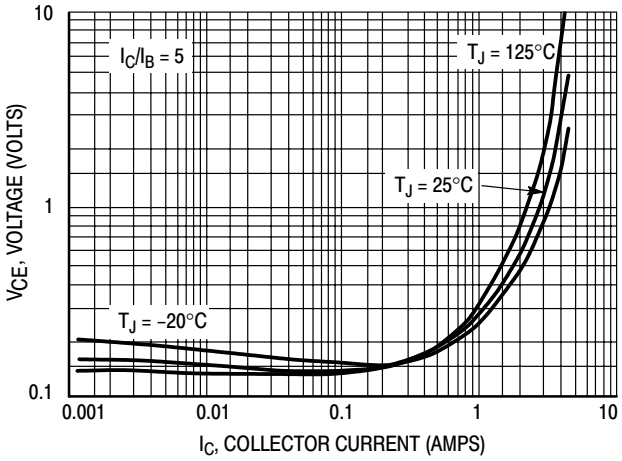


Figure 4. Collector–Emitter Saturation Voltage

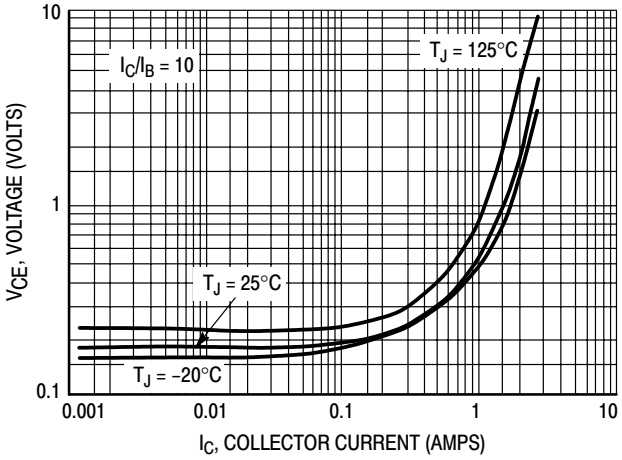


Figure 5. Collector–Emitter Saturation Voltage

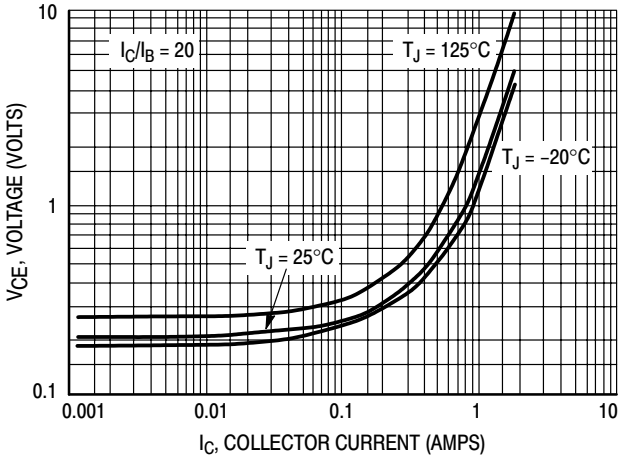


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

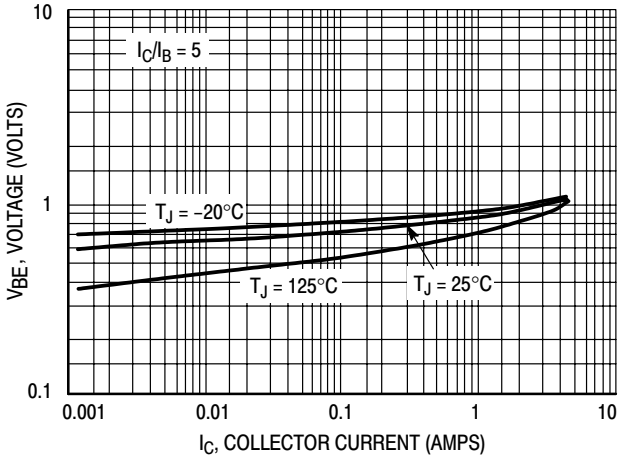


Figure 7. Base–Emitter Saturation Region

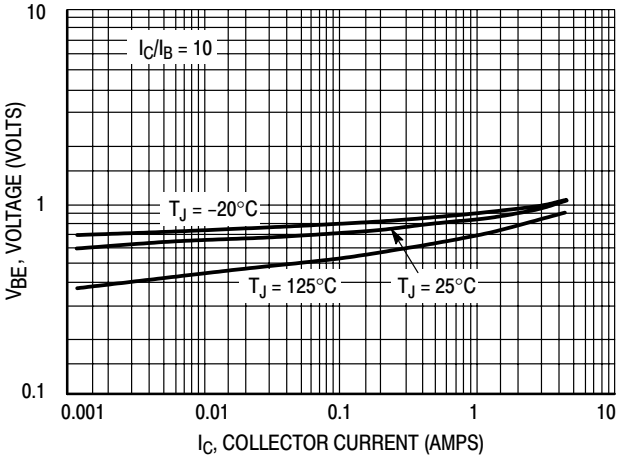


Figure 8. Base–Emitter Saturation Region

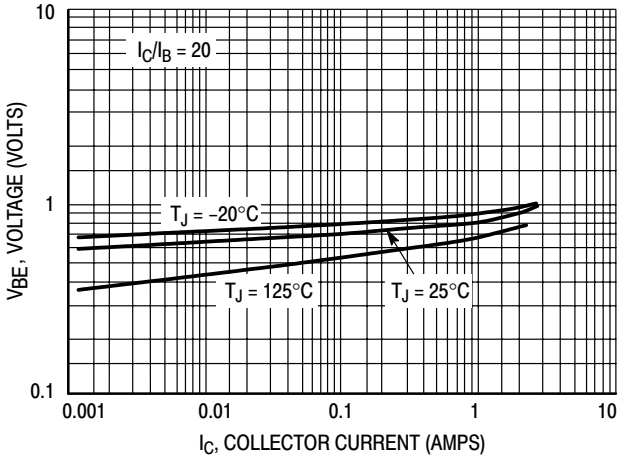


Figure 9. Base–Emitter Saturation Region

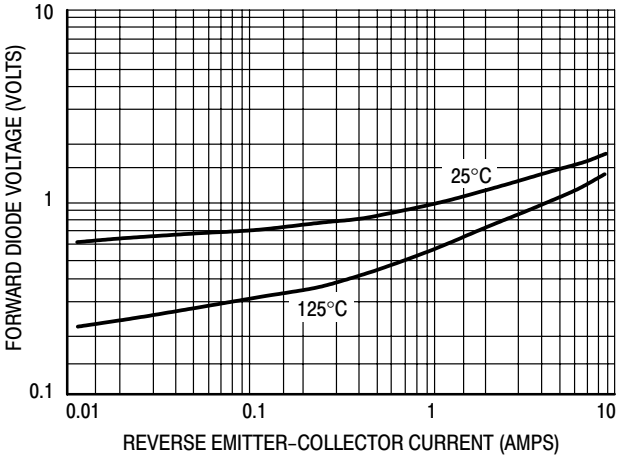


Figure 10. Forward Diode Voltage

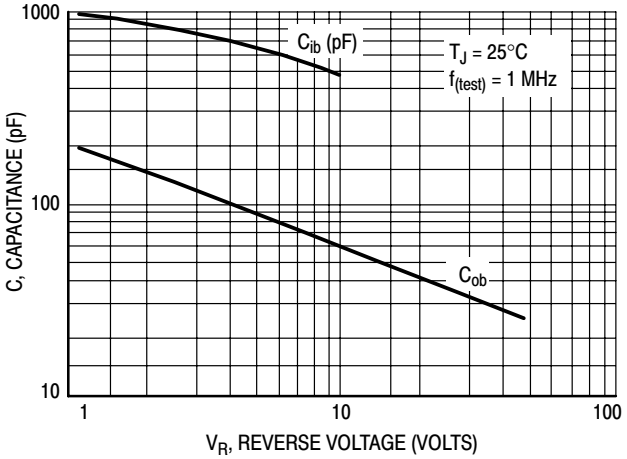


Figure 11. Capacitance

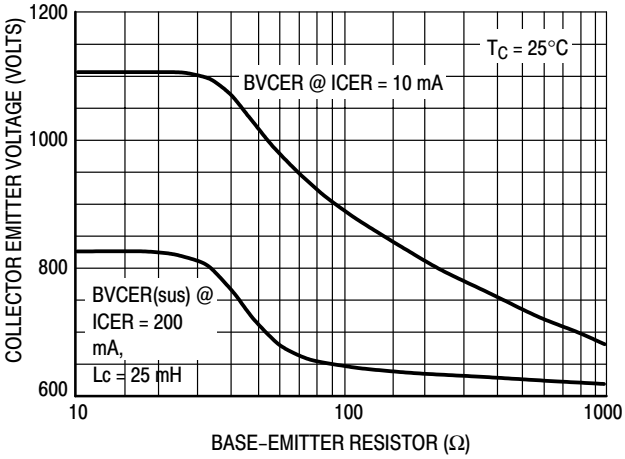


Figure 12. BVCER = f(R_{BE})

TYPICAL SWITCHING CHARACTERISTICS

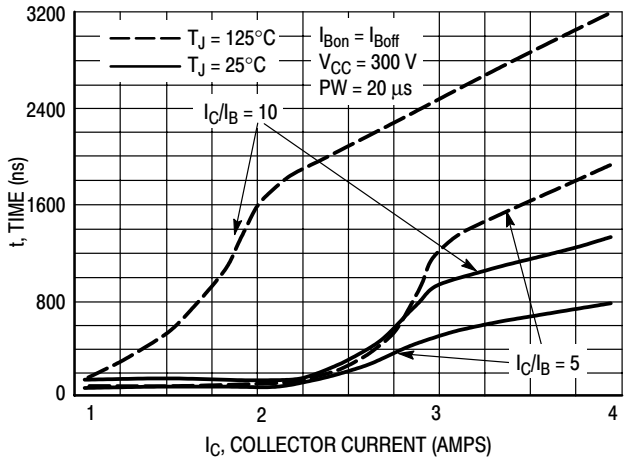


Figure 13. Resistive Switch Time, t_{on}

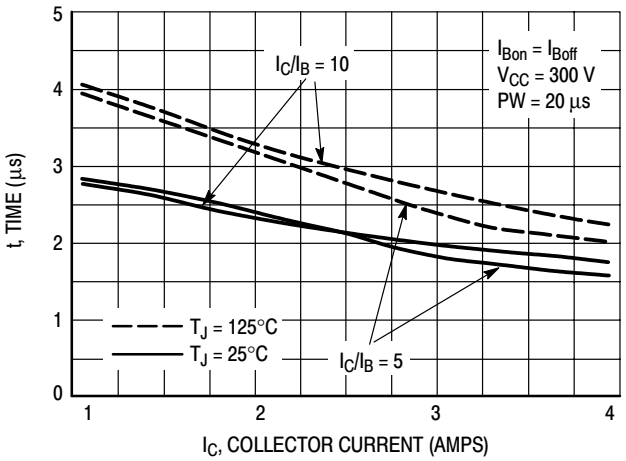


Figure 14. Resistive Switch Time, t_{off}

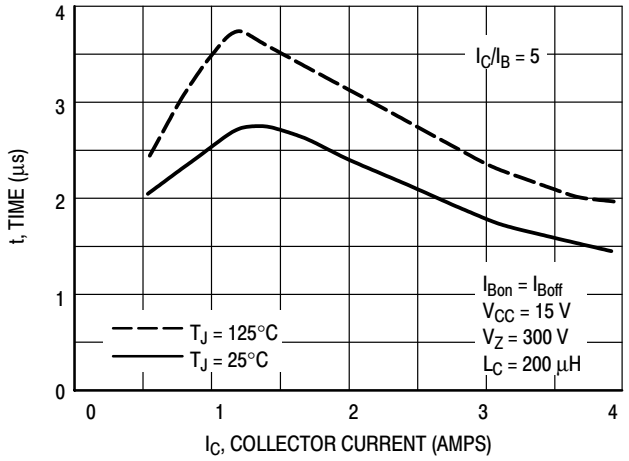


Figure 15. Inductive Storage Time, t_{si} @ I_C/I_B = 5

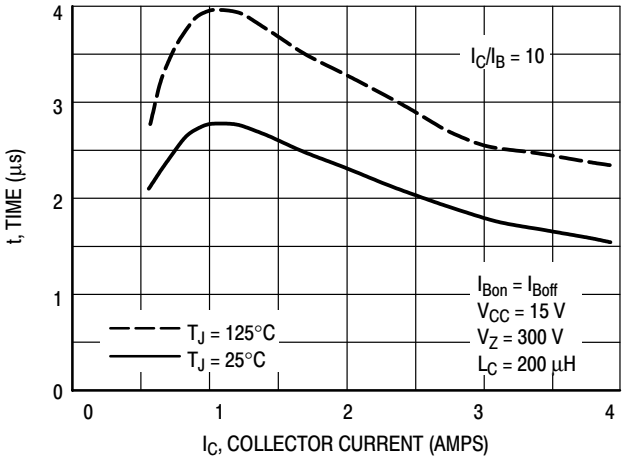


Figure 16. Inductive Storage Time, t_{si} @ I_C/I_B = 10

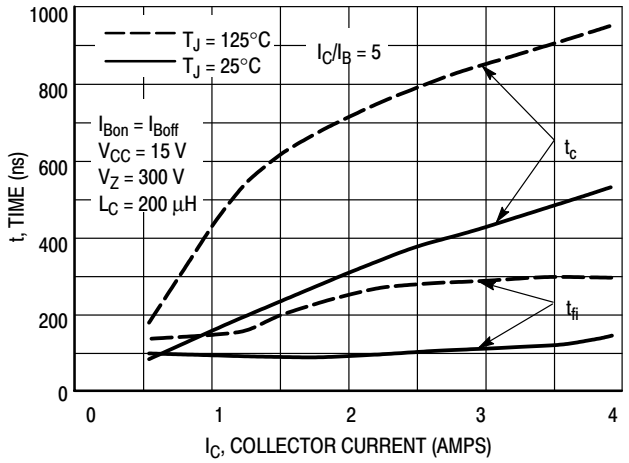


Figure 17. Inductive Switching Time, t_c and t_{fi} @ I_C/I_B = 5

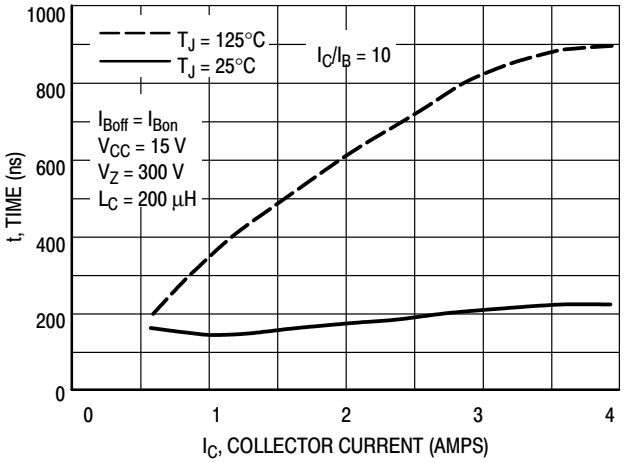


Figure 18. Inductive Switching Time, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

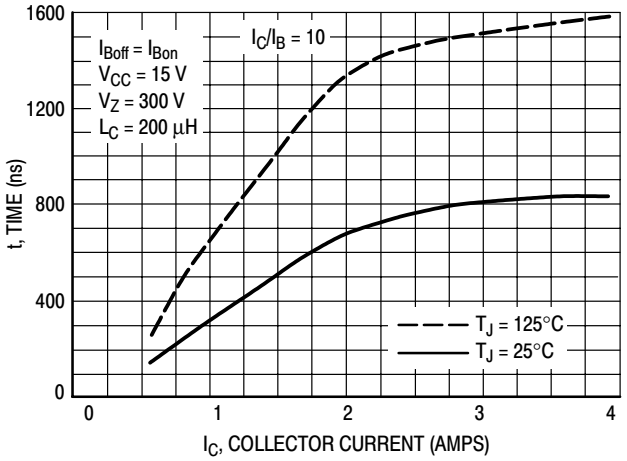


Figure 19. Inductive Switching, t_c @ I_C/I_B = 10

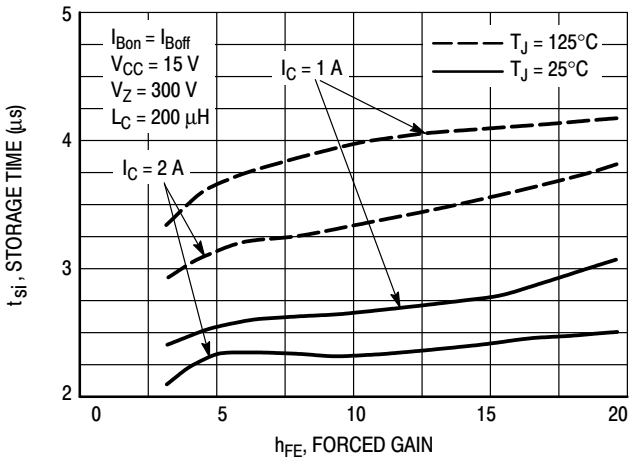


Figure 20. Inductive Storage Time

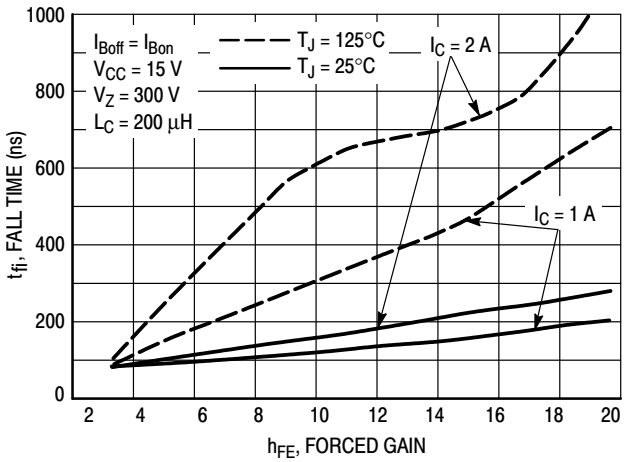


Figure 21. Inductive Fall Time

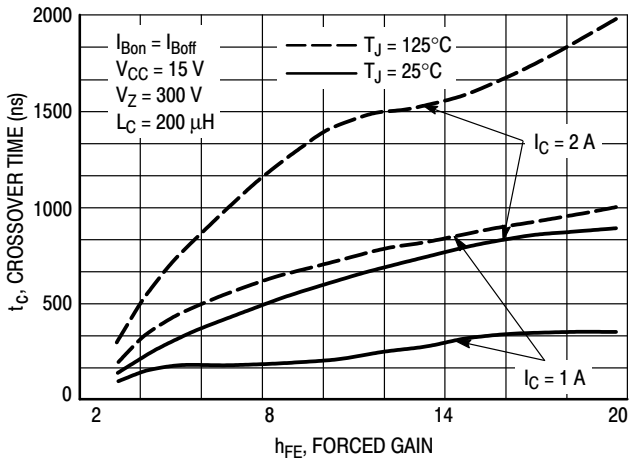


Figure 22. Inductive Crossover Time

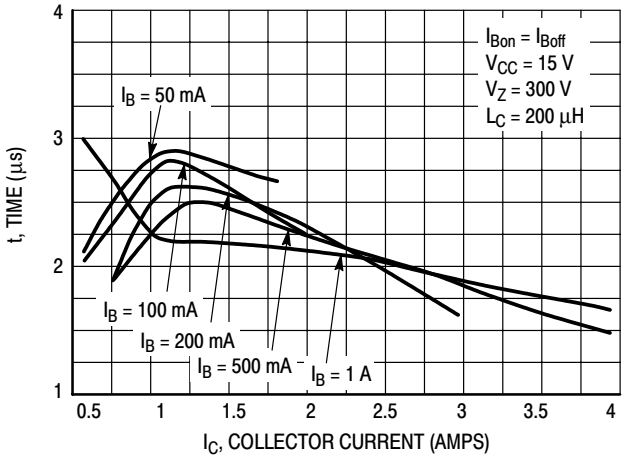


Figure 23. Inductive Storage Time, t_{si}

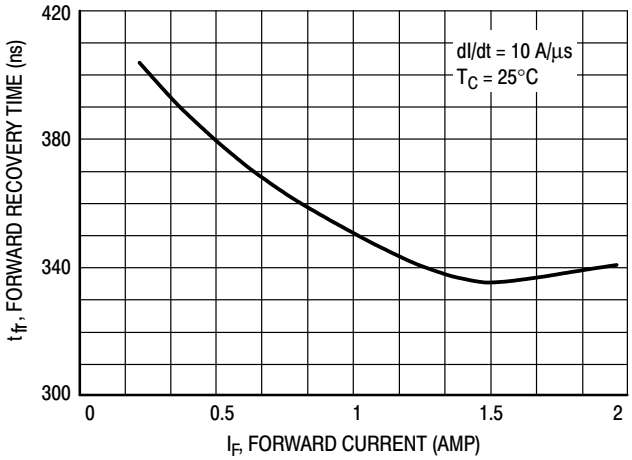


Figure 24. Forward Recovery Time, T_{FR}

TYPICAL SWITCHING CHARACTERISTICS

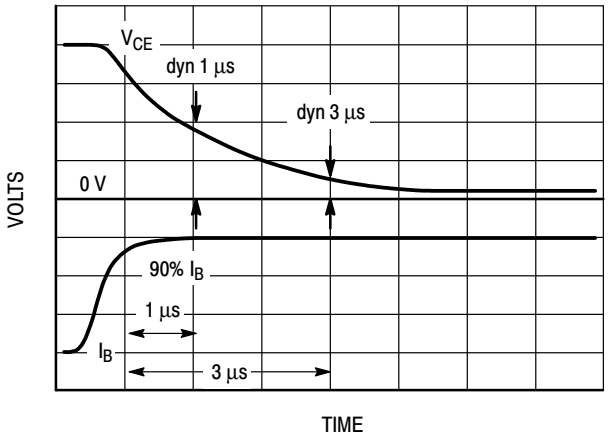


Figure 25. Dynamic Saturation Voltage Measurements

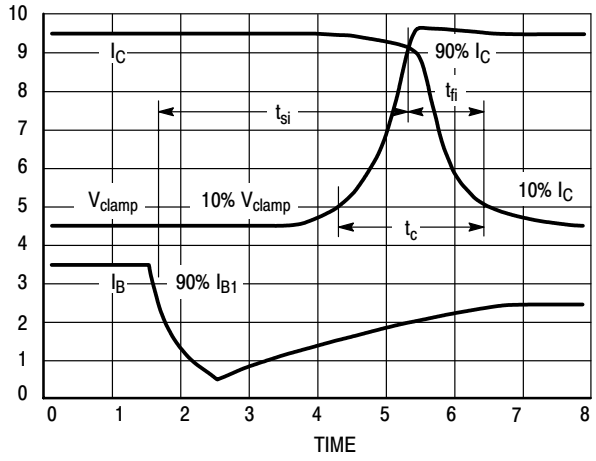


Figure 26. Inductive Switching Measurements

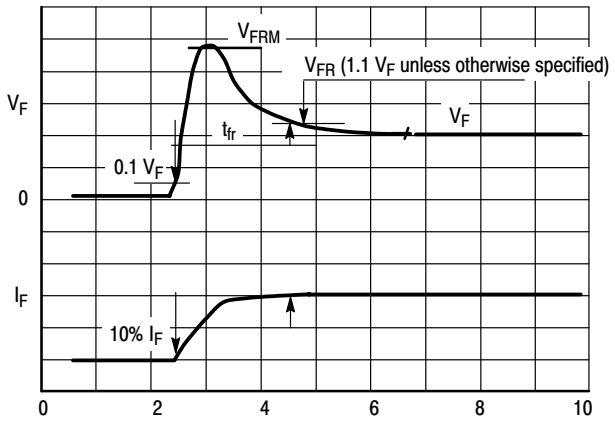
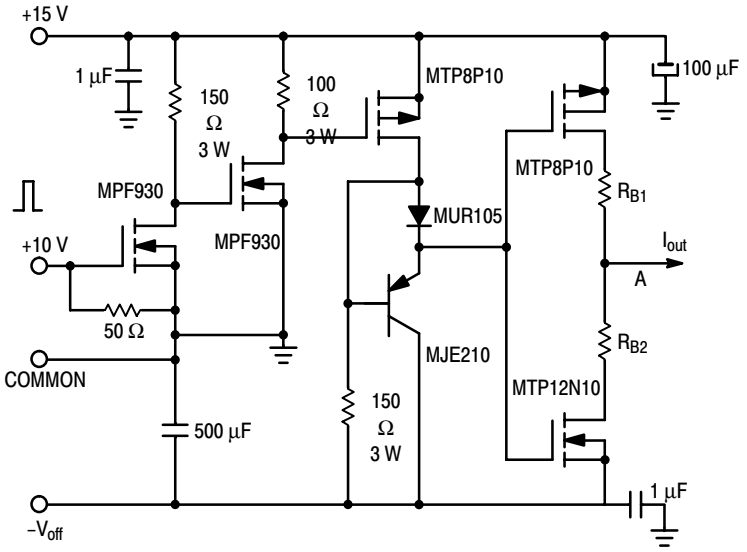
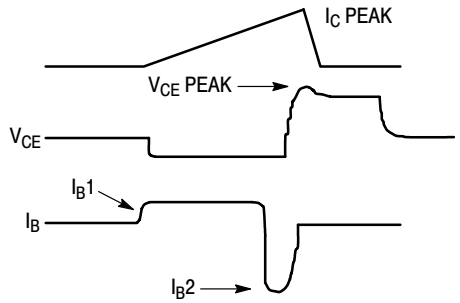


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	RB1 selected for desired Ib1	RB1 selected for desired Ib1

TYPICAL CHARACTERISTICS

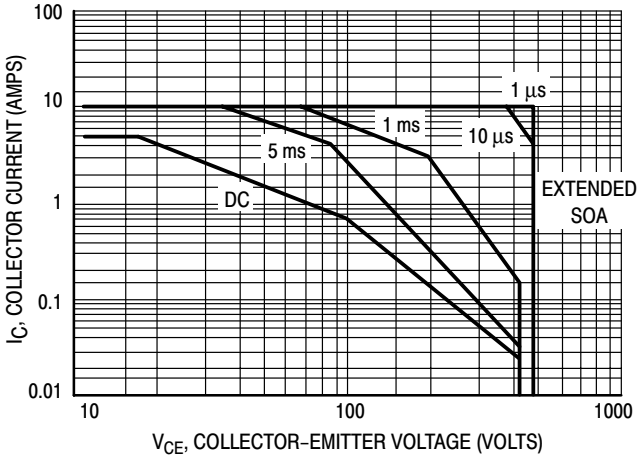


Figure 28. Forward Bias Safe Operating Area

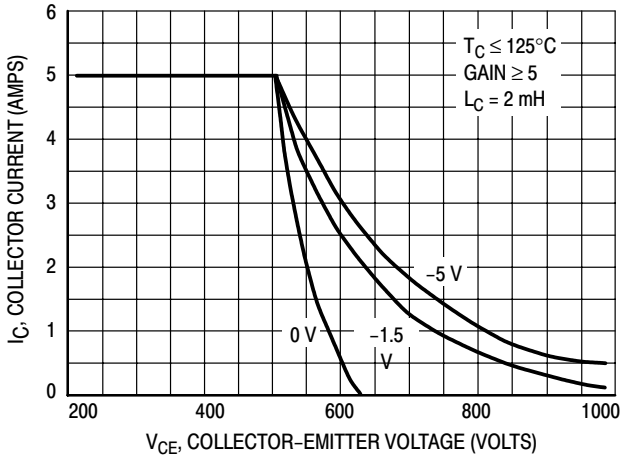


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

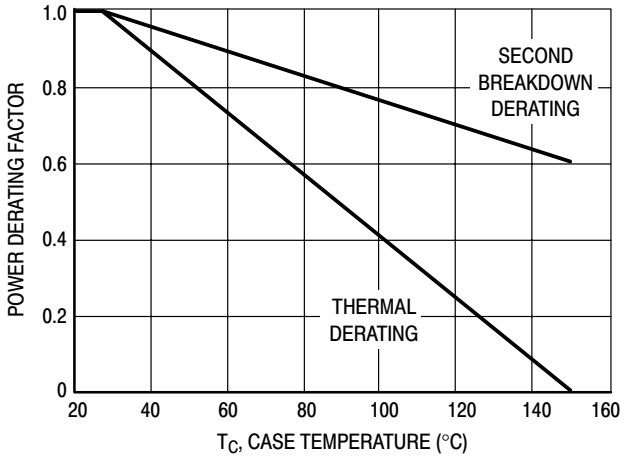


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

T_J(pk) may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

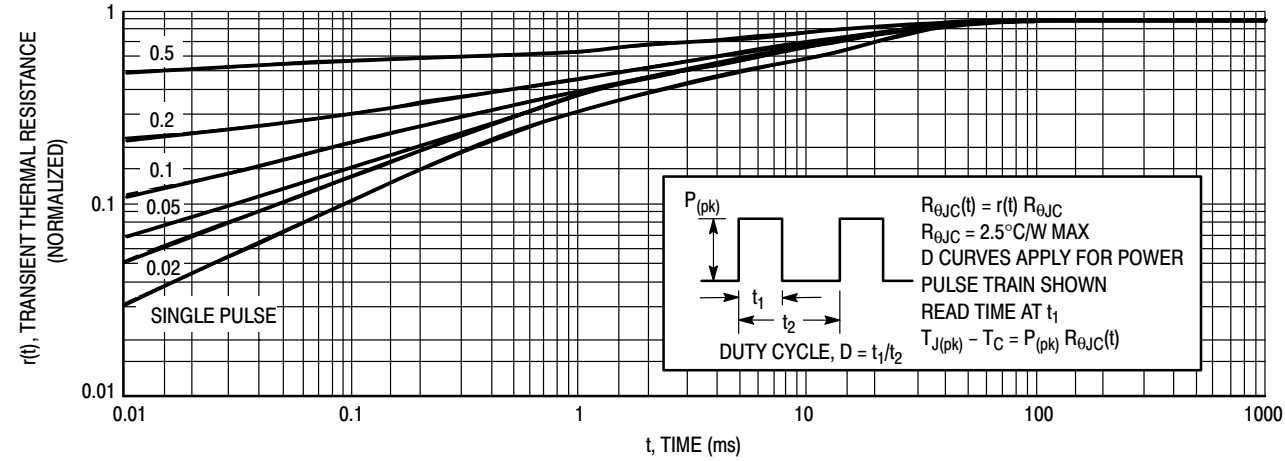
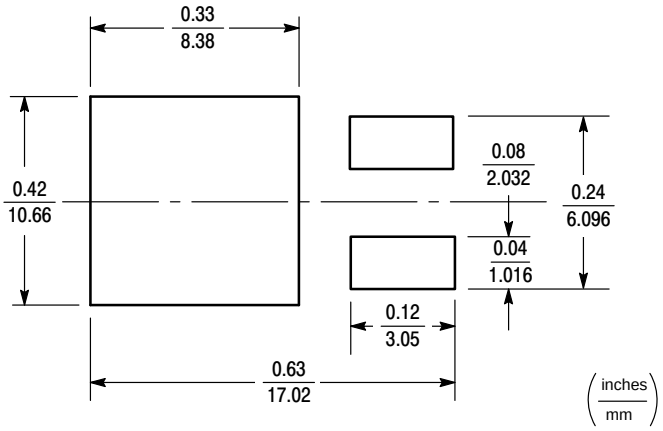


Figure 31. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJB18004D2T4

INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus Collector pad area is shown in Figure 32

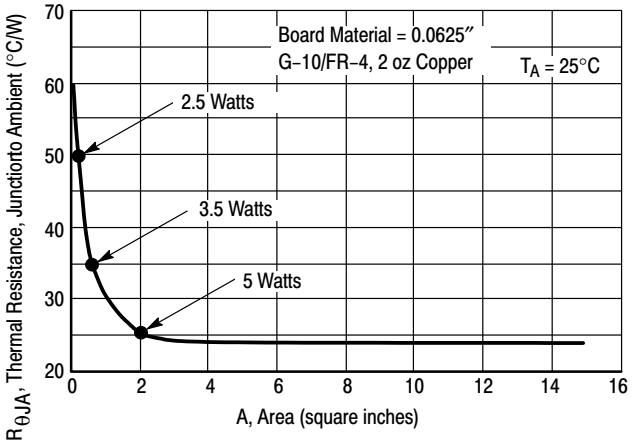


Figure 32. Thermal Resistance versus Collector Pad Area for the D²PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 33 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

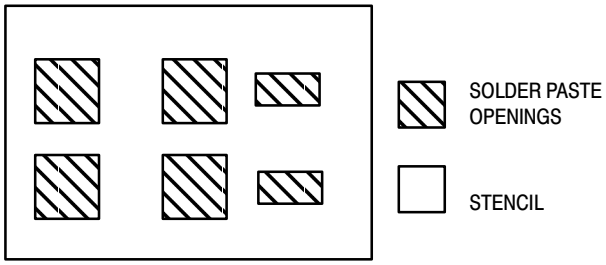


Figure 33. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 34 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

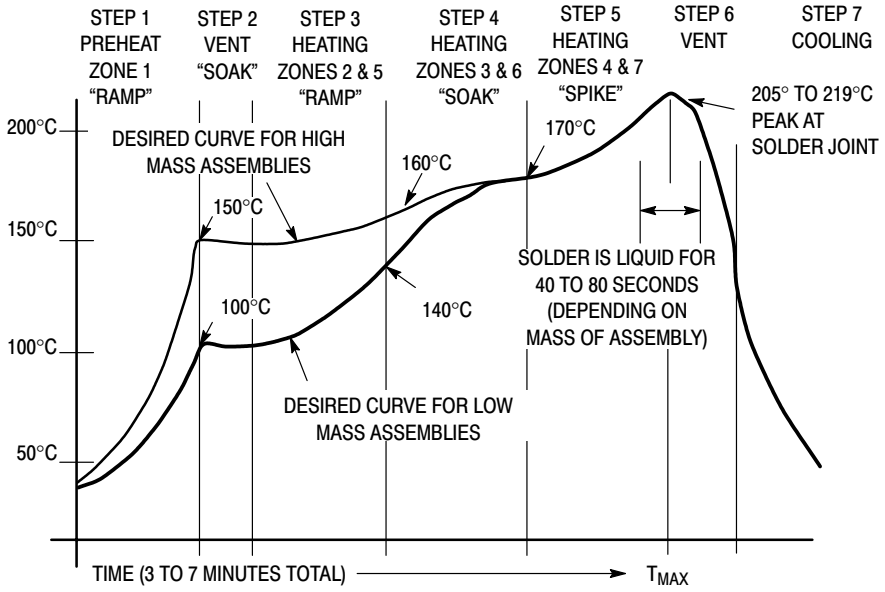


Figure 34. Typical Solder Heating Profile

MJB41C (NPN), MJB42C (PNP)

Preferred Devices

Complementary Silicon Plastic Power Transistors

D²PAK for Surface Mount

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape & Reel (“T4” Suffix)
- Electrically the Same as TIP41 and T1P42 Series

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous – Peak	I_C	6.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Unclamped Inductive Load Energy (Note 1.)	E	62.5	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds	T_L	260	°C

1. I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω
2. When surface mounted to an FR–4 board using the minimum recommended pad size.

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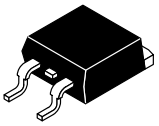
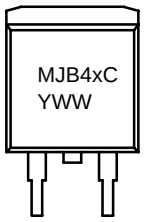
COMPLEMENTARY SILICON POWER TRANSISTORS 6 AMPERES 100 VOLTS 65 WATTS

MARKING DIAGRAM



D²PAK CASE 418B STYLE 1



MJB4xC = Specific Device Code
x = 1 or 2
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJB41C	D²PAK	50 Units/Rail
MJB41CT4	D²PAK	800/Tape & Reel
MJB42C	D²PAK	50 Units/Rail
MJB42CT4	D²PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 3.) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	–	100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	50	μAdc
ON CHARACTERISTICS (Note 3.)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	30 15	– 75	–
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	–	1.5	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	3.0	–	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	–	–

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

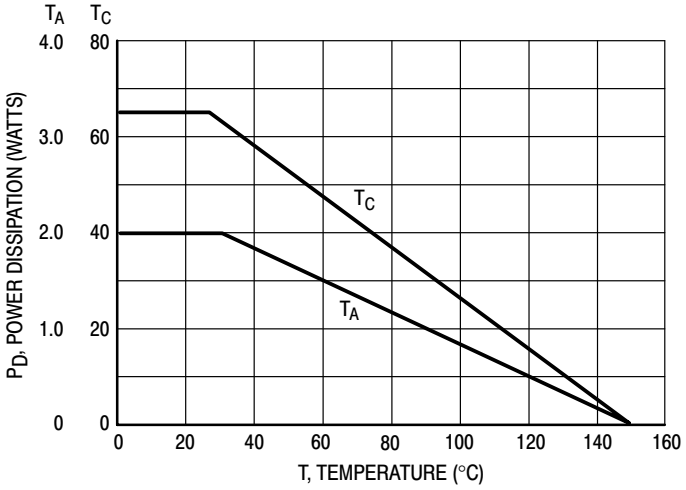
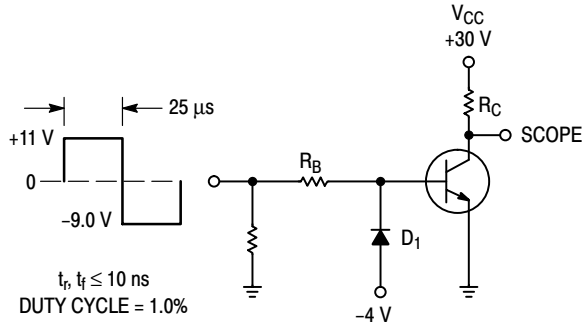


Figure 35. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Figure 36. Switching Time Test Circuit

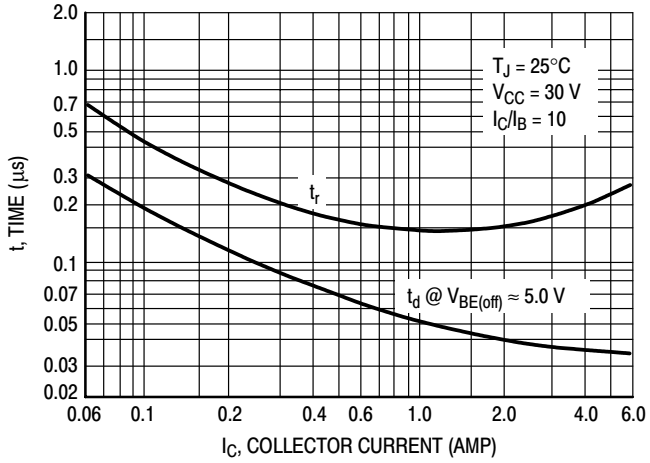


Figure 37. Turn–On Time

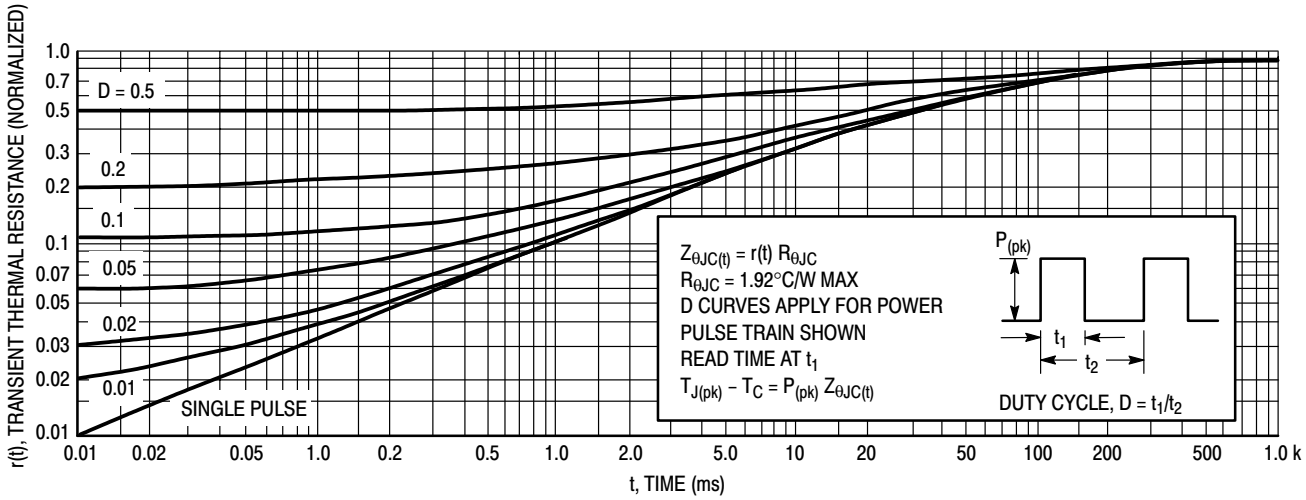


Figure 38. Thermal Response

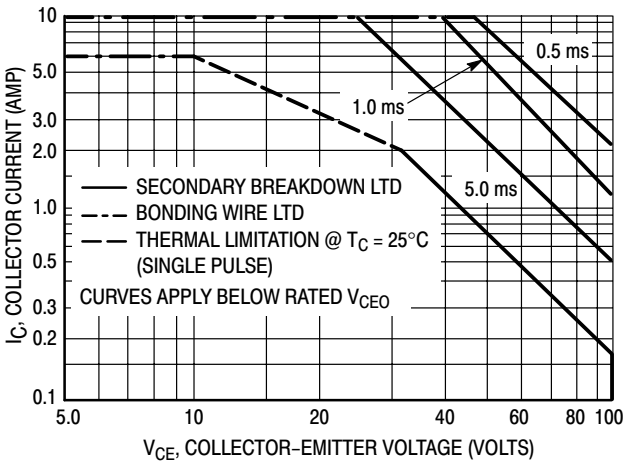


Figure 39. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

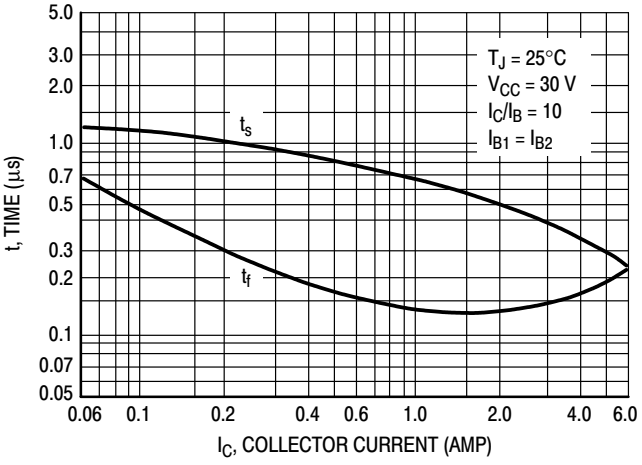


Figure 40. Turn−Off Time

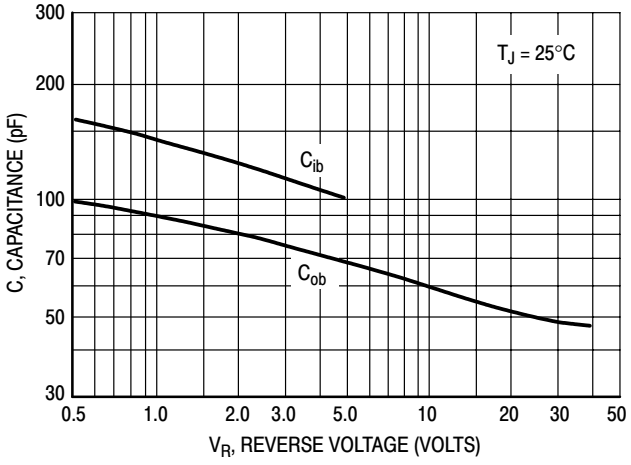


Figure 41. Capacitance

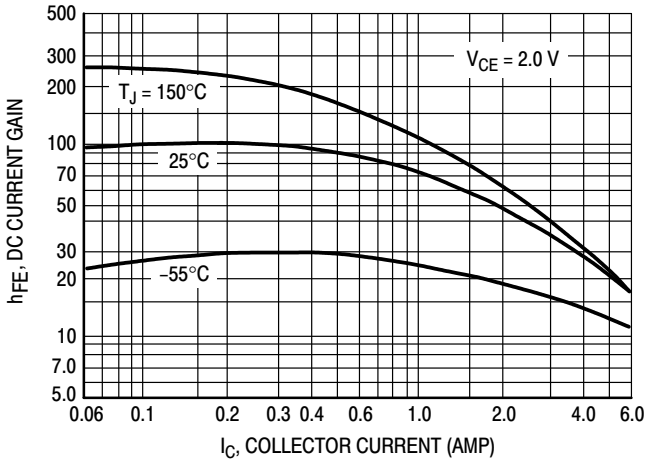


Figure 42. DC Current Gain

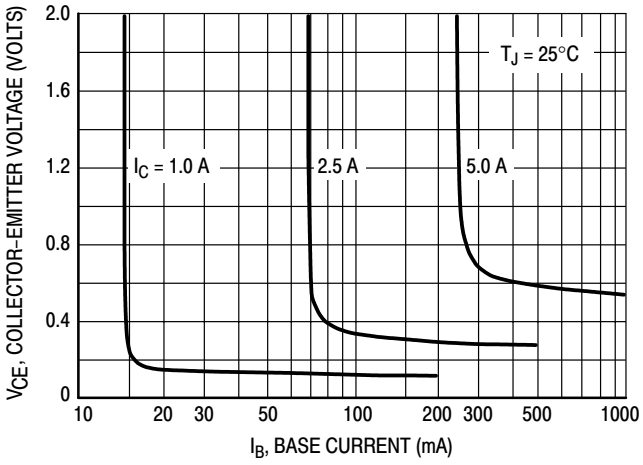


Figure 43. Collector Saturation Region

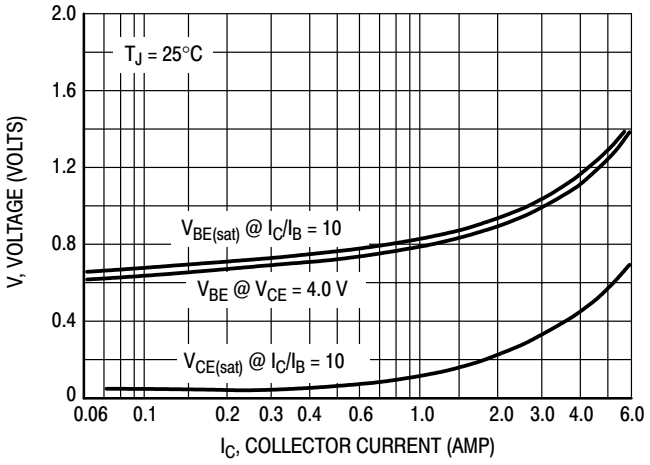


Figure 44. “On” Voltages

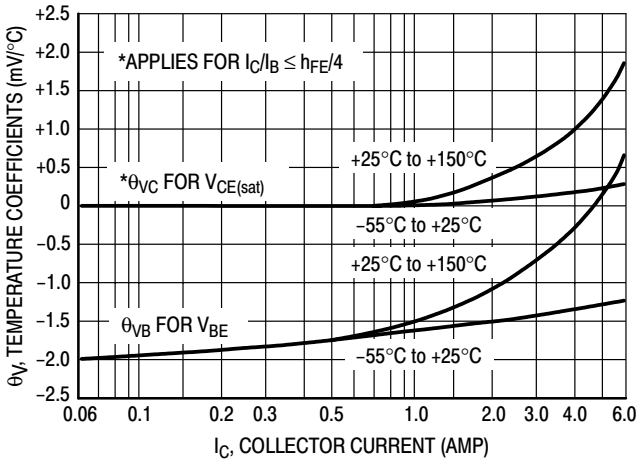


Figure 45. Temperature Coefficients

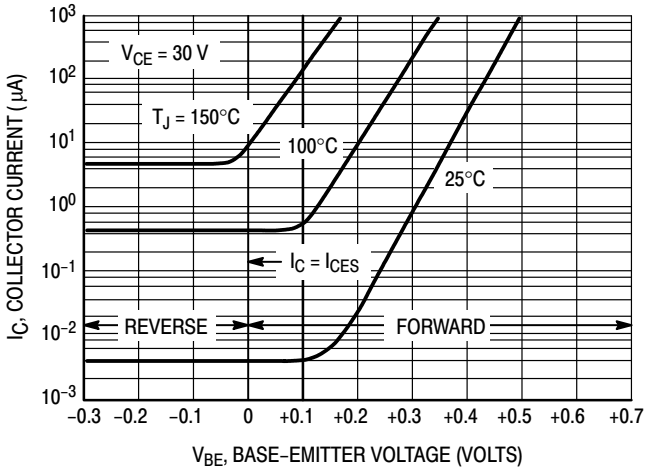


Figure 46. Collector Cut−Off Region

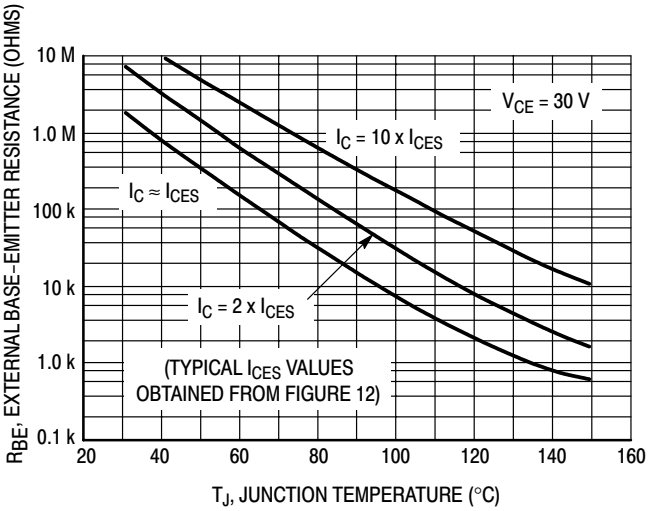
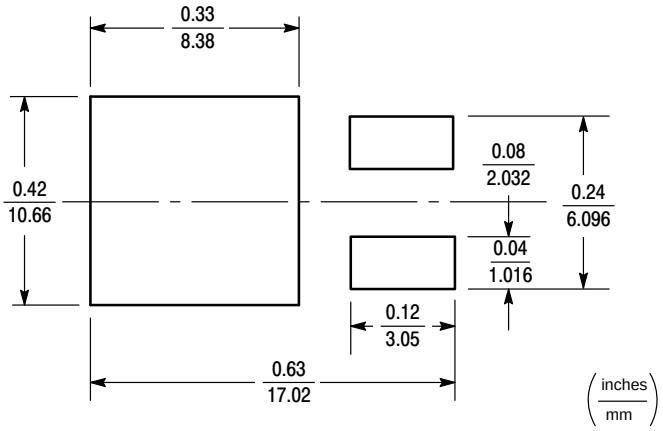


Figure 47. Effects of Base−Emitter Resistance

INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus Collector pad area is shown in Figure 48

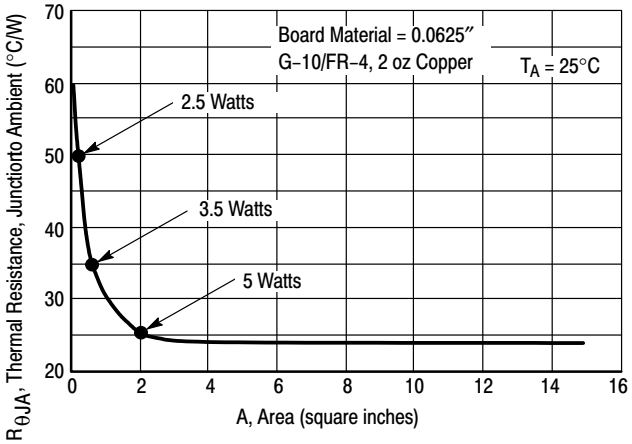


Figure 48. Thermal Resistance versus Collector Pad Area for the D²PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 49 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

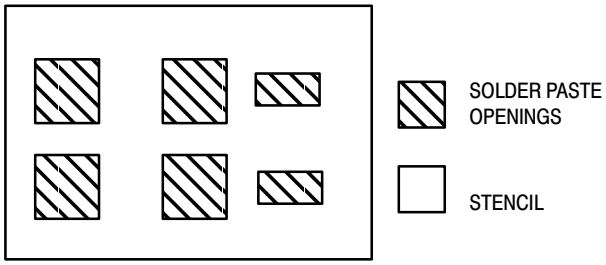


Figure 49. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 50 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

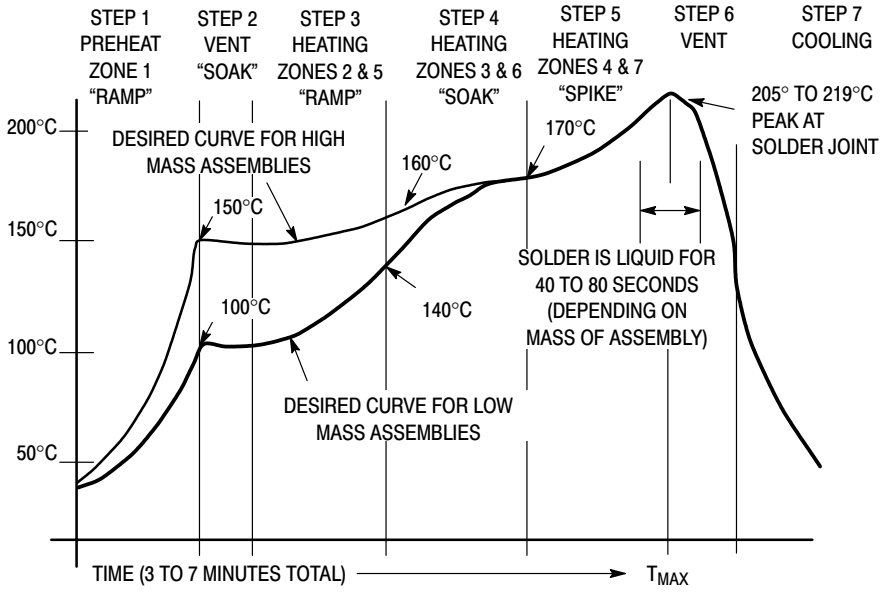


Figure 50. Typical Solder Heating Profile

MJB44H11 (NPN), MJB45H11 (PNP)

Preferred Devices

Complementary Power Transistors

D^2PAK for Surface Mount

. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

ON Semiconductor™

http://onsemi.com

SILICON POWER TRANSISTORS
10 AMPERES
80 VOLTS
50 WATTS

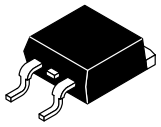
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current – Continuous – Peak	I_C	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 50 1.67	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

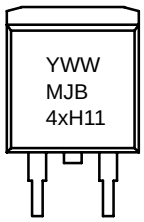
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

MARKING DIAGRAM



D^2PAK
CASE 418B
STYLE 1



Y = Year
WW = Work Week
MJB4xH11 = Specific Device Code
x = 4 or 5

ORDERING INFORMATION

Device	Package	Shipping
MJB44H11	D^2PAK	50 Units/Rail
MJB44H11T4	D^2PAK	800/Tape & Reel
MJB45H11	D^2PAK	50 Units/Rail
MJB45H11T4	D^2PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	–	–	10	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	–	–	50	μA
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	–	–	1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	–	–	–
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	–	–	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJB44H11 MJB45H11	C_{cb}	– –	130 230	– –	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJB44H11 MJB45H11	f_T	– –	50 40	– –	MHz
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJB44H11 MJB45H11	$t_d + t_r$	– –	300 135	– –	ns
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJB44H11 MJB45H11	t_s	– –	500 500	– –	ns
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJB44H11 MJB45H11	t_f	– –	140 100	– –	ns

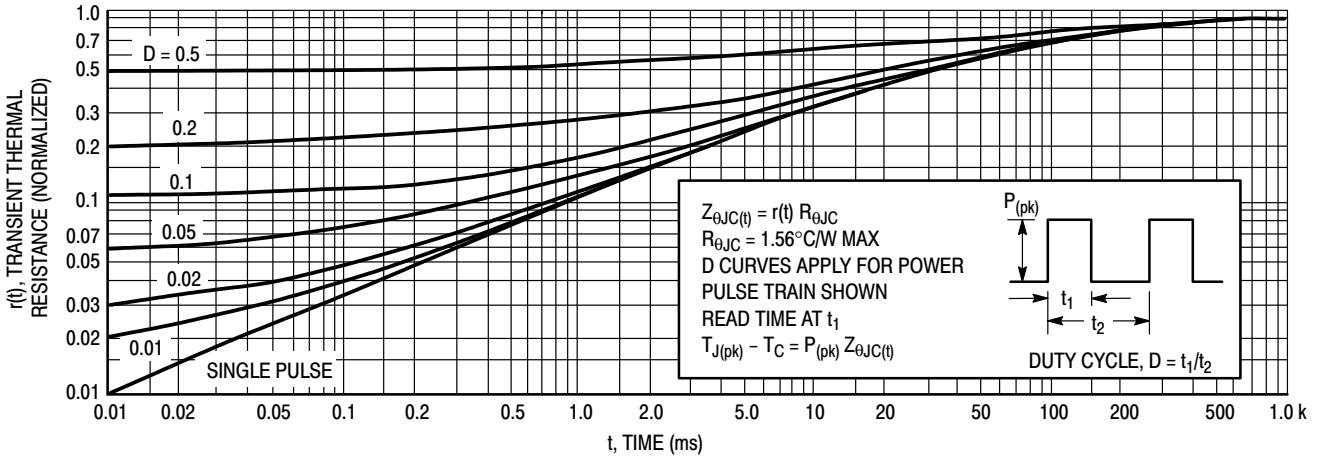


Figure 1. Thermal Response

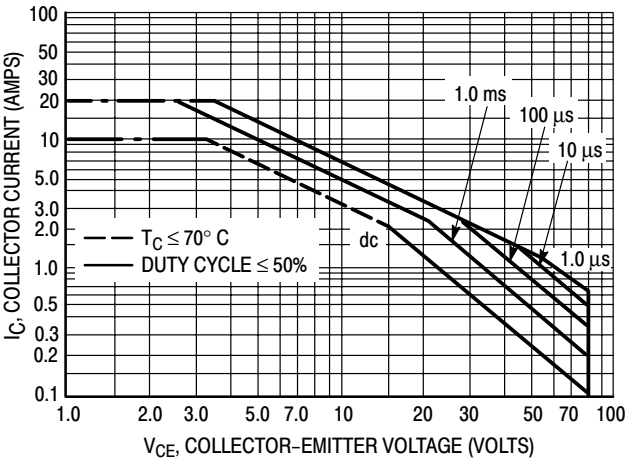


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

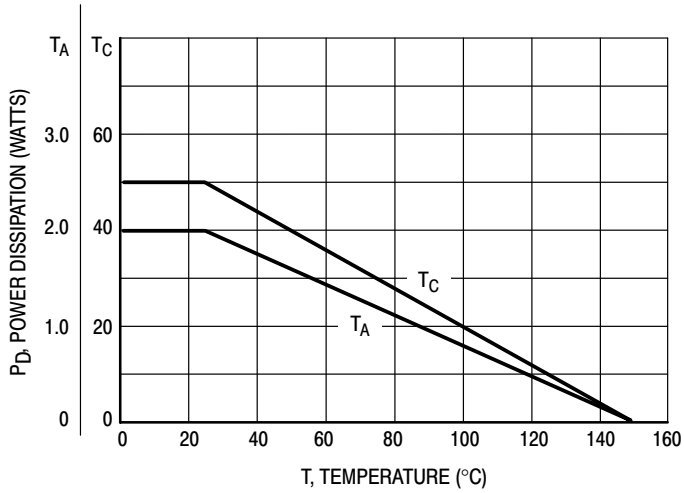


Figure 3. Power Derating

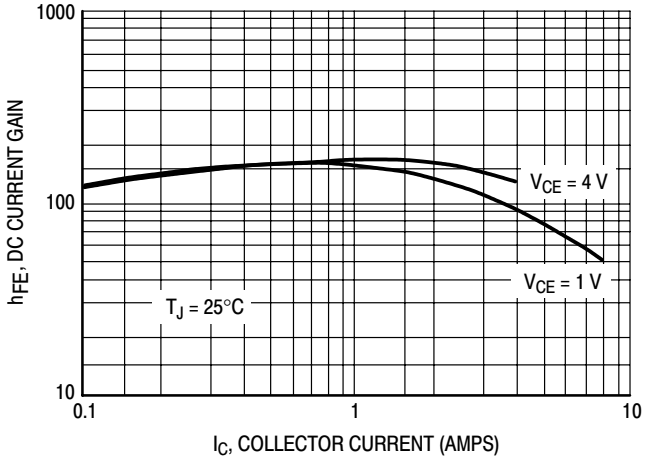


Figure 4. MJB44H11 DC Current Gain

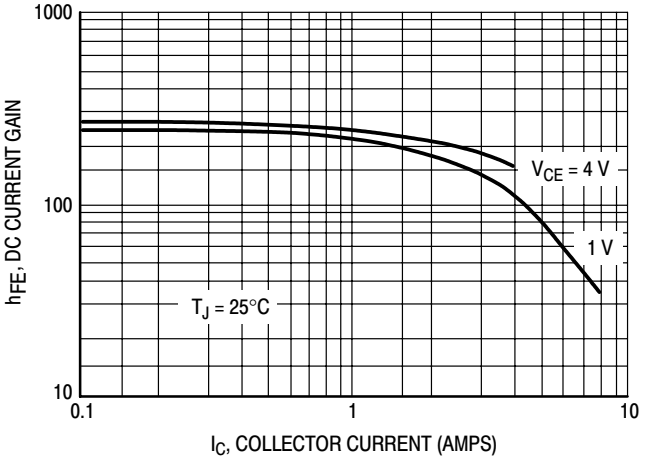


Figure 5. MJB45H11 DC Current Gain

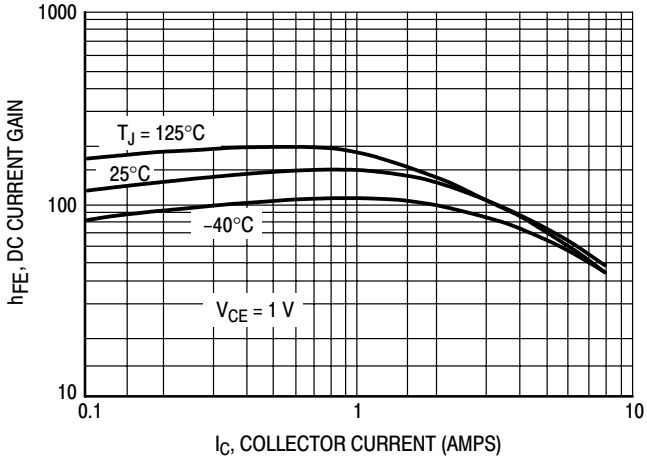


Figure 6. MJB44H11 Current Gain versus Temperature

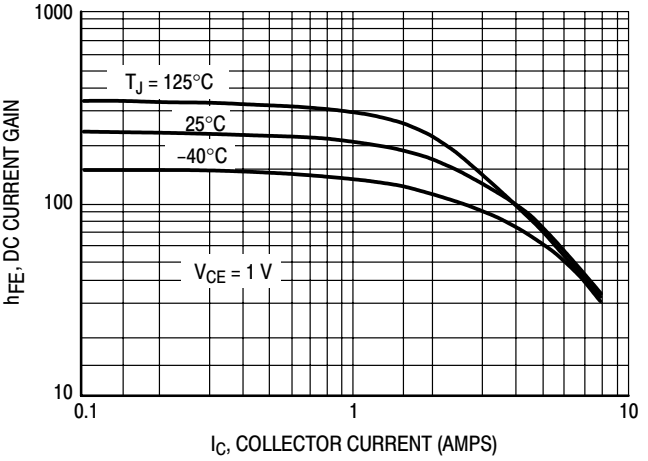


Figure 7. MJB45H11 Current Gain versus Temperature

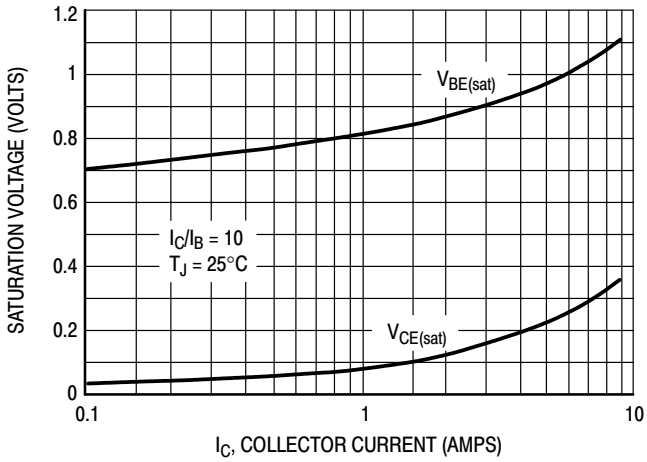


Figure 8. MJB44H11 On–Voltages

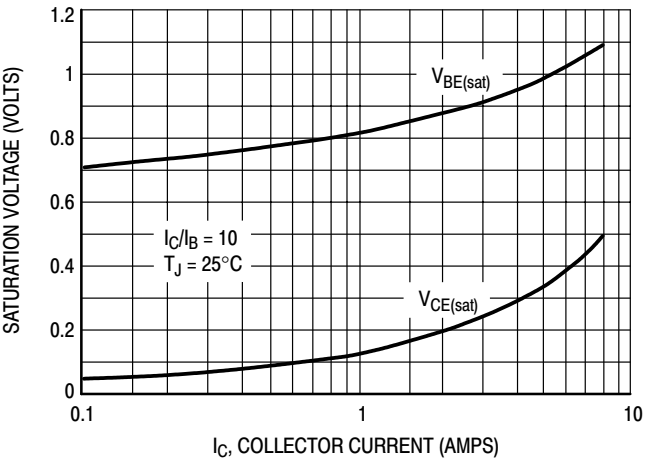


Figure 9. MJB45H11 On–Voltages

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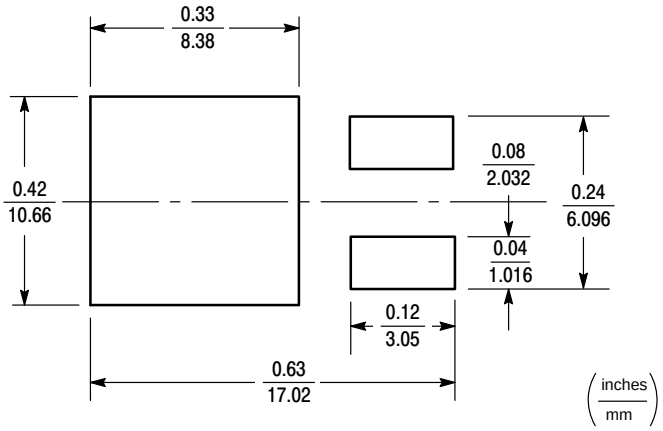

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$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus Collector pad area is shown in Figure 10

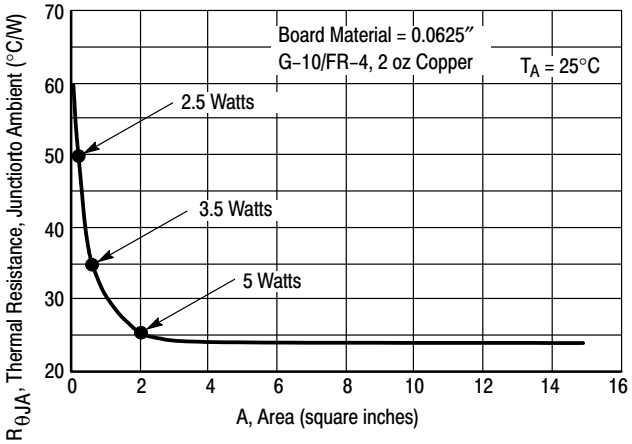


Figure 10. Thermal Resistance versus Collector Pad Area for the D²PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 11 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

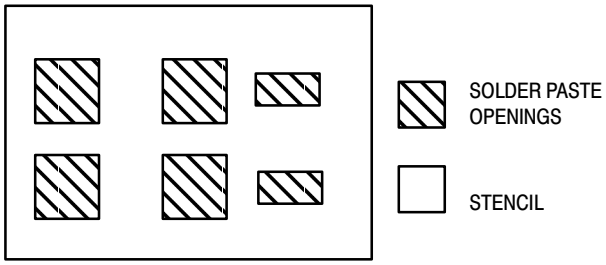


Figure 11. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

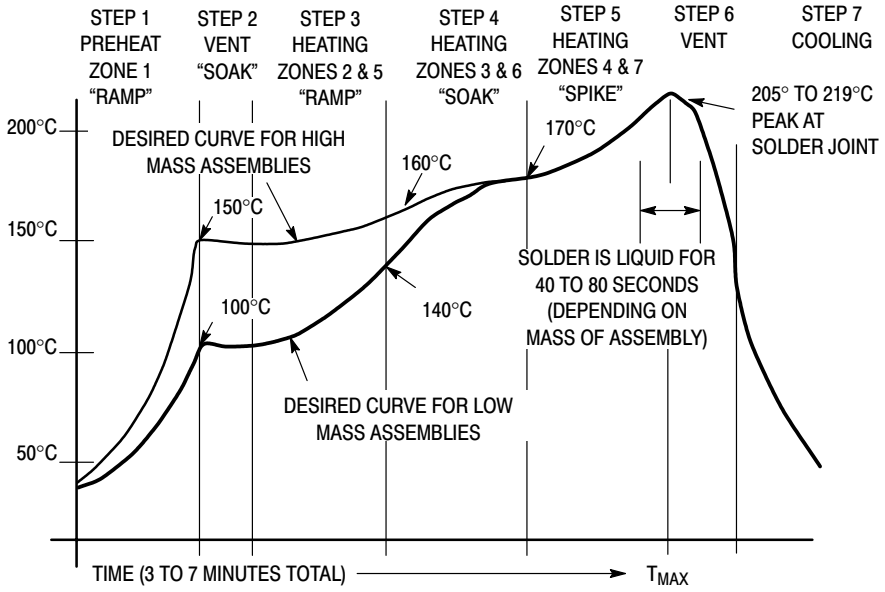


Figure 12. Typical Solder Heating Profile

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

NPN
MJD112*
PNP
MJD117*

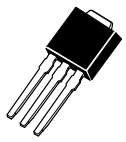
*ON Semiconductor Preferred Device

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Surface Mount Replacements for TIP110–TIP117 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 2.0 Adc
- Complementary Pairs Simplifies Designs

SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS
20 WATTS

CASE 369A–13

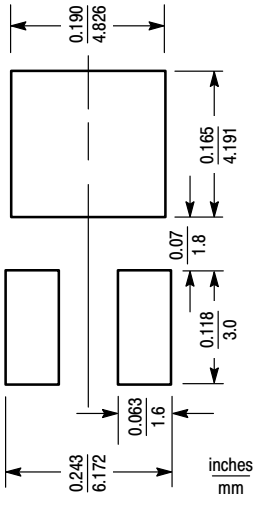


CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	MJD112 MJD117	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
Collector–Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter–Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 2 Adc, V_{CE} = 3 Vdc) (I_C = 4 Adc, V_{CE} = 3 Vdc)	h_{FE}	 500 1000 200	 — 12,000 —	—
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc) (I_C = 4 Adc, I_B = 40 mAdc)	$V_{CE(sat)}$	 — —	 2 3	Vdc
Base–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	—	4	Vdc
Base–Emitter On Voltage (I_C = 2 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	25	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD117 MJD112	C_{ob}	 — —	 200 100	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

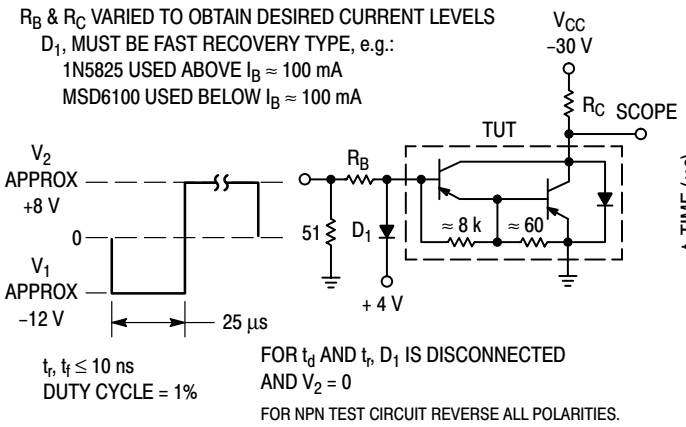


Figure 13. Switching Times Test Circuit

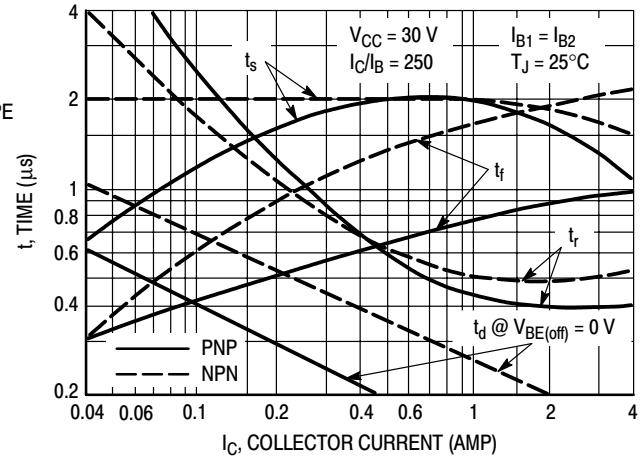


Figure 14. Switching Times

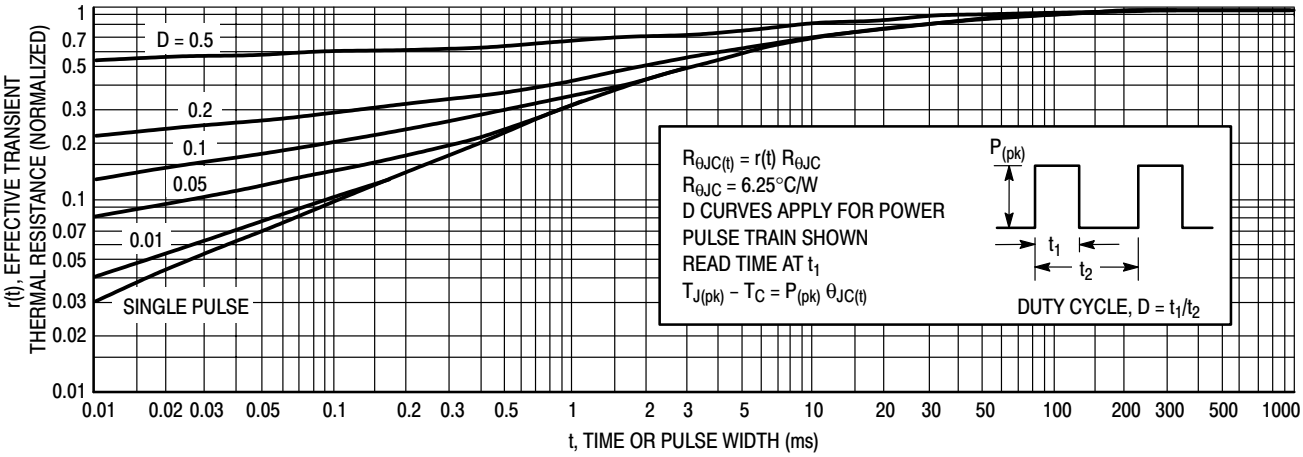


Figure 15. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

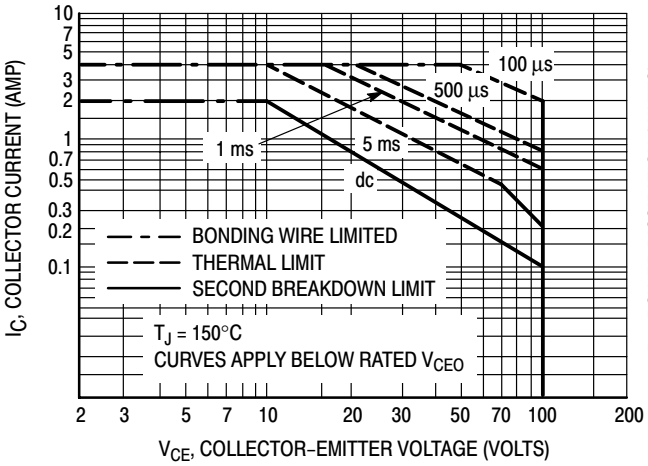


Figure 16. Maximum Rated Forward Biased Safe Operating Area

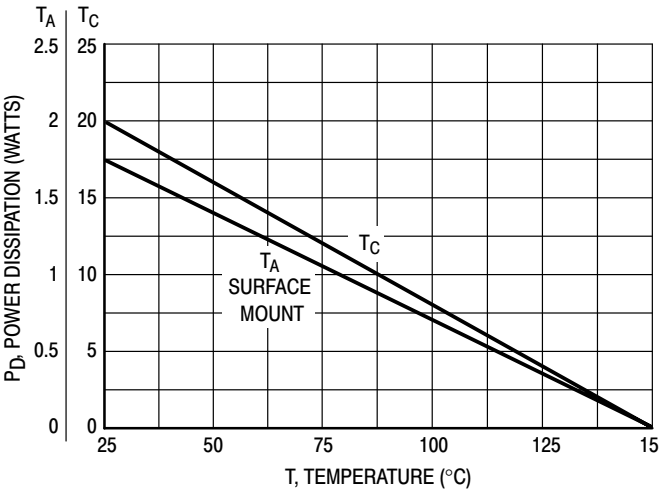


Figure 17. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 17 and 18 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

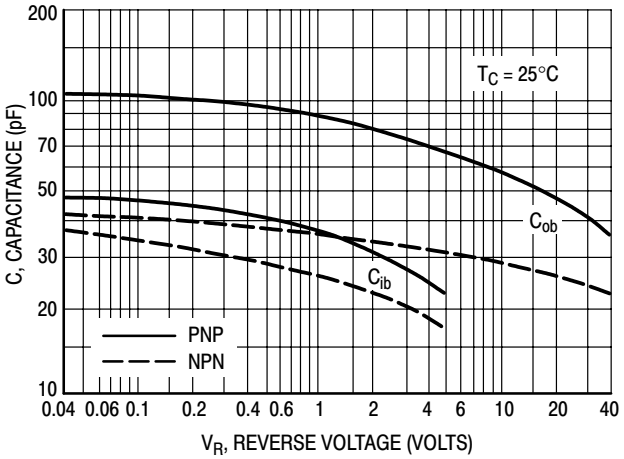


Figure 18. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

NPN MJD112 **PNP MJD117**

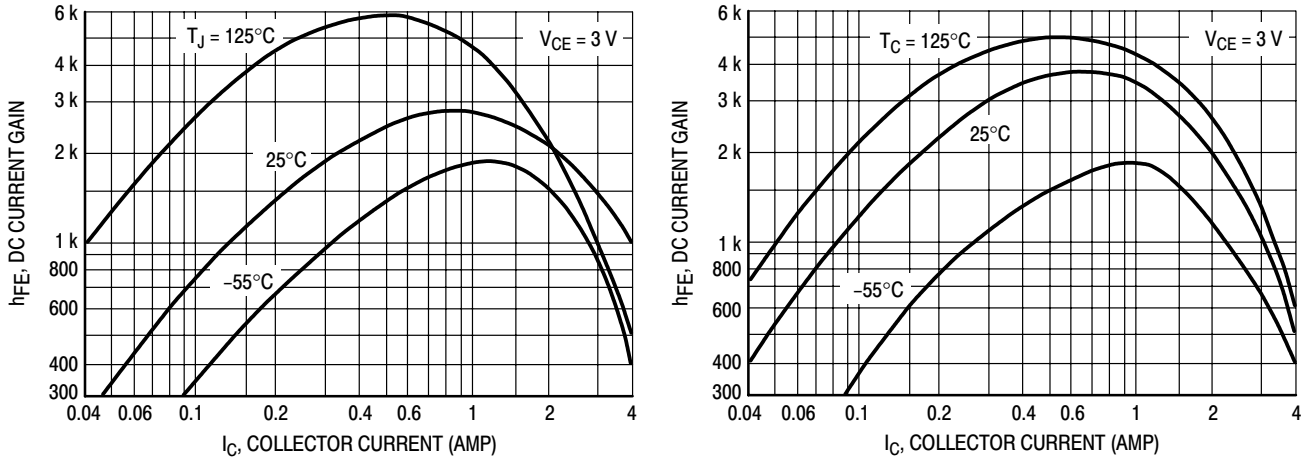


Figure 19. DC Current Gain

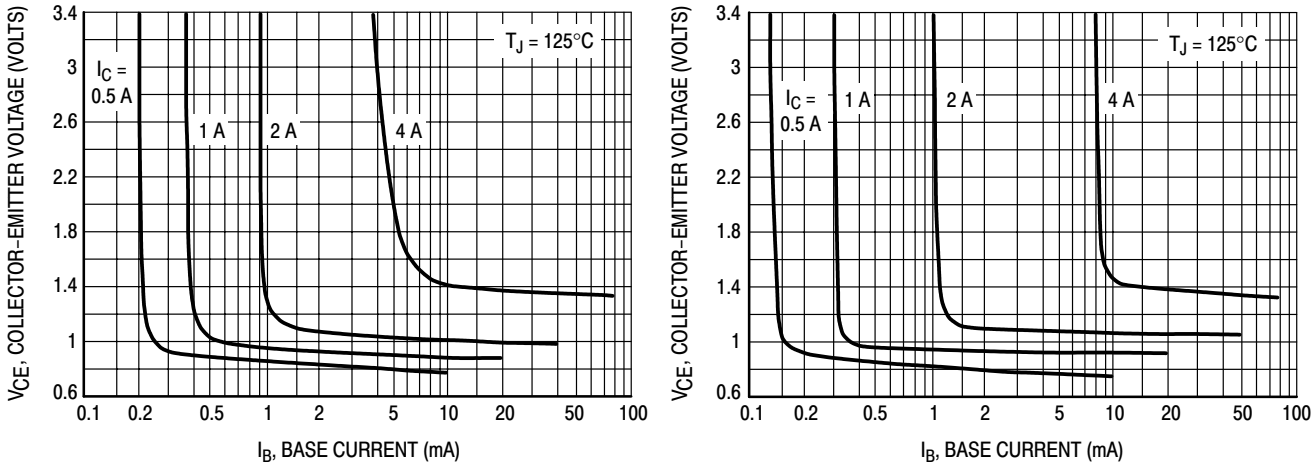


Figure 20. Collector Saturation Region

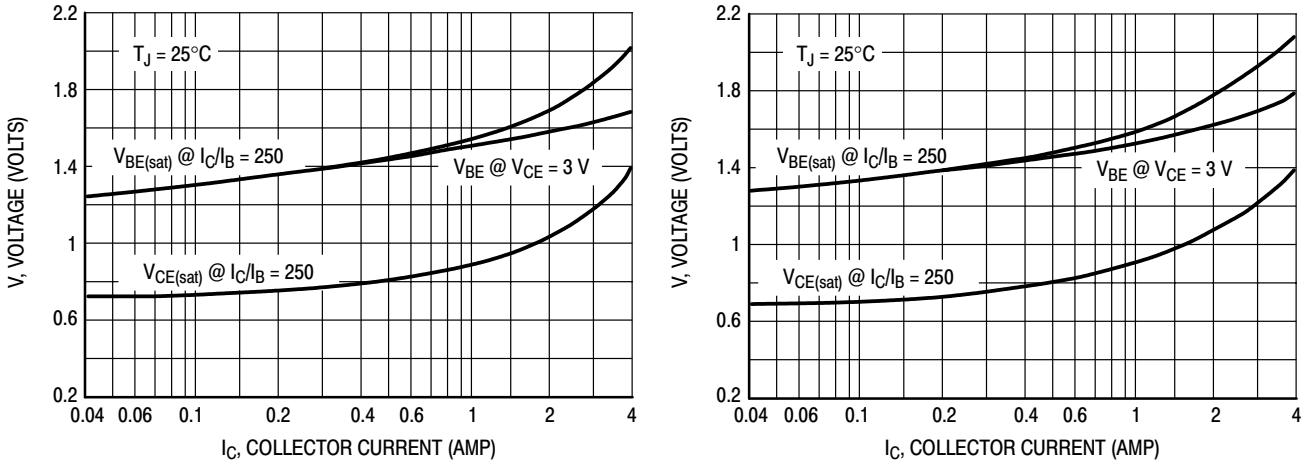


Figure 21. “On Voltages

NPN MJD112 **PNP MJD117**

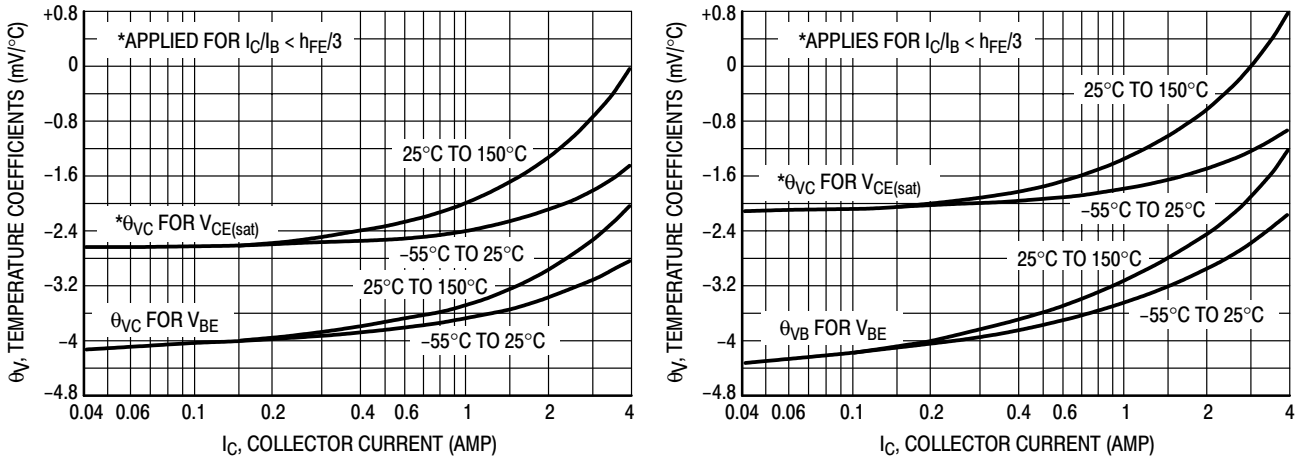


Figure 22. Temperature Coefficients

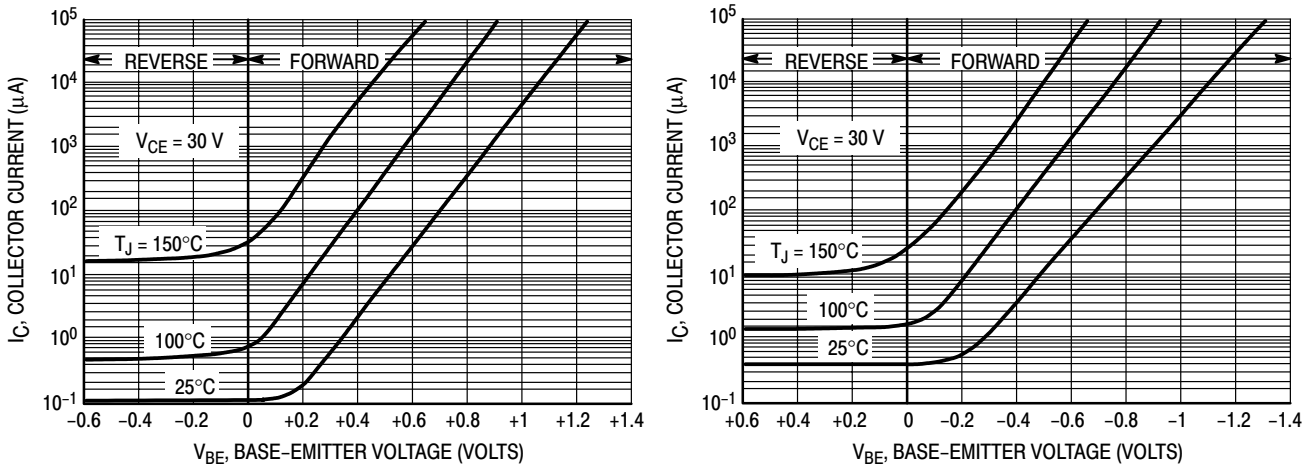


Figure 23. Collector Cut−Off Region

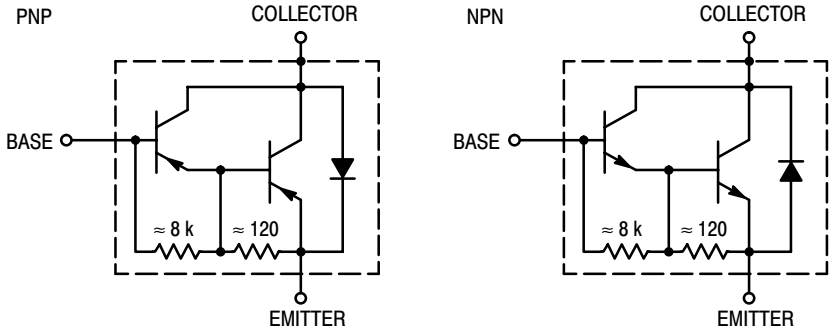


Figure 24. Darlington Schematic

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

NPN
MJD122*
PNP
MJD127*

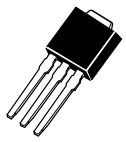
*ON Semiconductor Preferred Device

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("T4" Suffix)
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Complementary Pairs Simplifies Designs

SILICON POWER TRANSISTORS 8 AMPERES 100 VOLTS 20 WATTS

CASE 369A–13



CASE 369–07

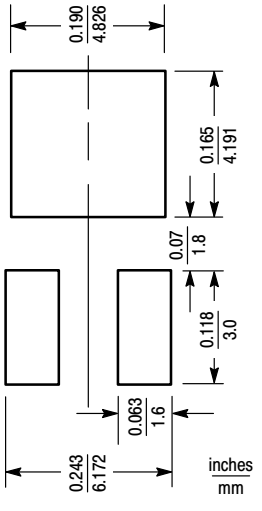
MAXIMUM RATINGS

Rating	Symbol	MJD122 MJD127	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 8 Adc, V_{CE} = 4 Vdc)	h_{FE}	1000 100	12,000 —	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 16 mAdc) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	— —	2 4	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	—	4.5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	$\|h_{fe}\|$	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD127 MJD122	C_{ob}	— —	300 200	pF
Small–Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	300	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

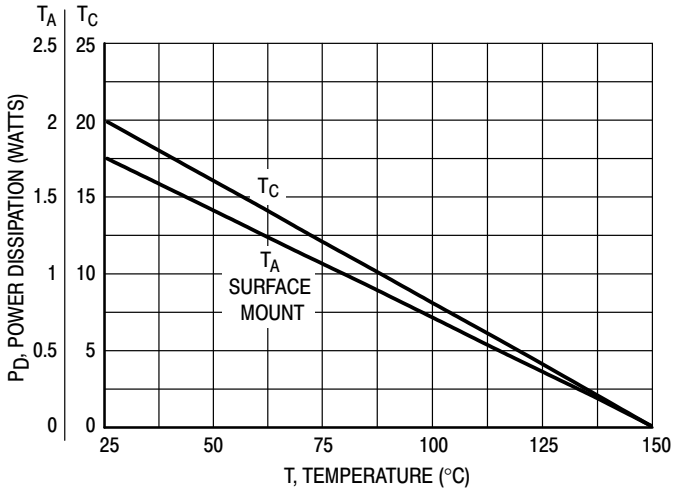


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127 **NPN MJD122**

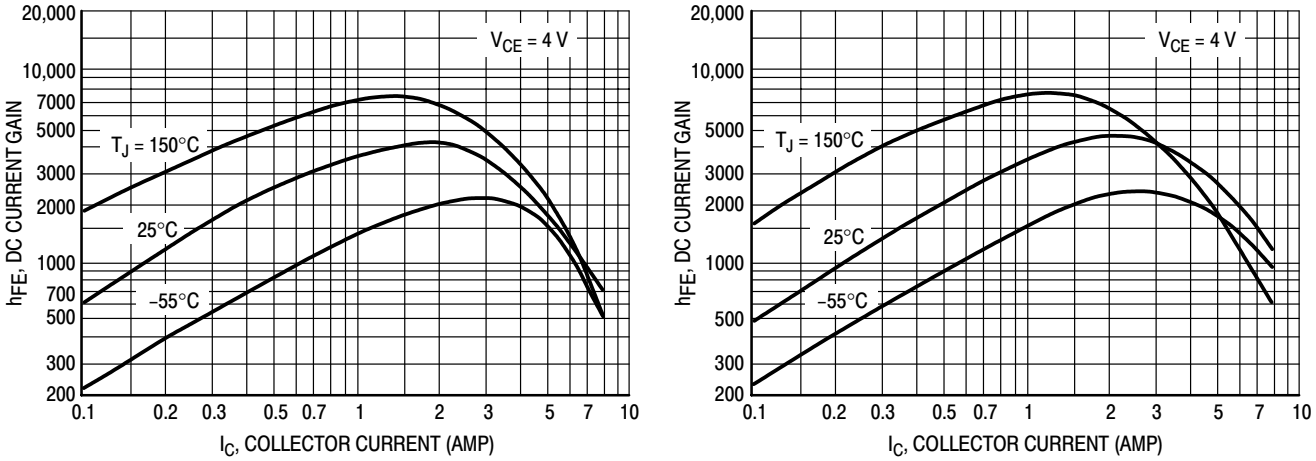


Figure 2. DC Current Gain

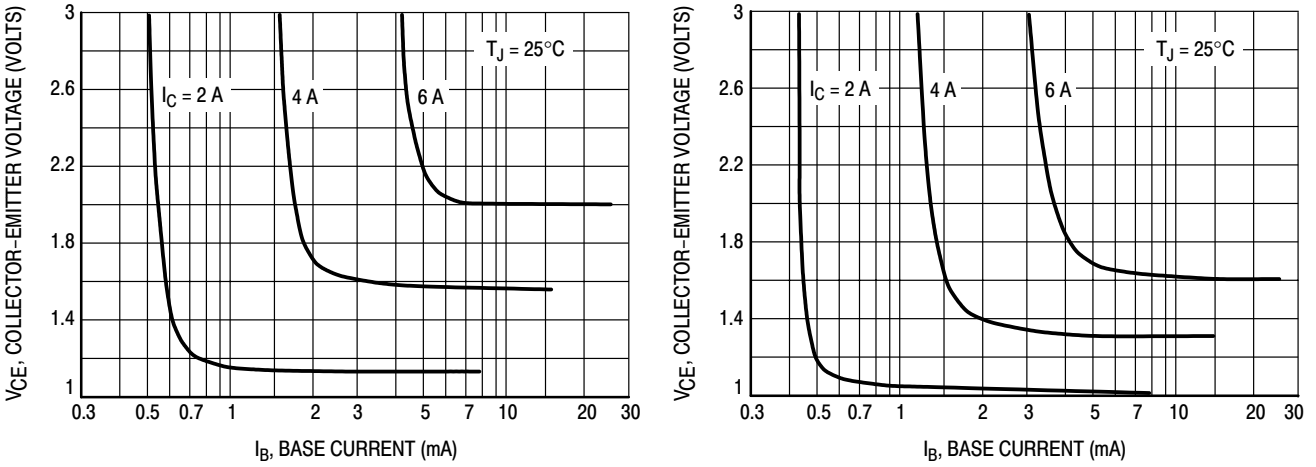


Figure 3. Collector Saturation Region

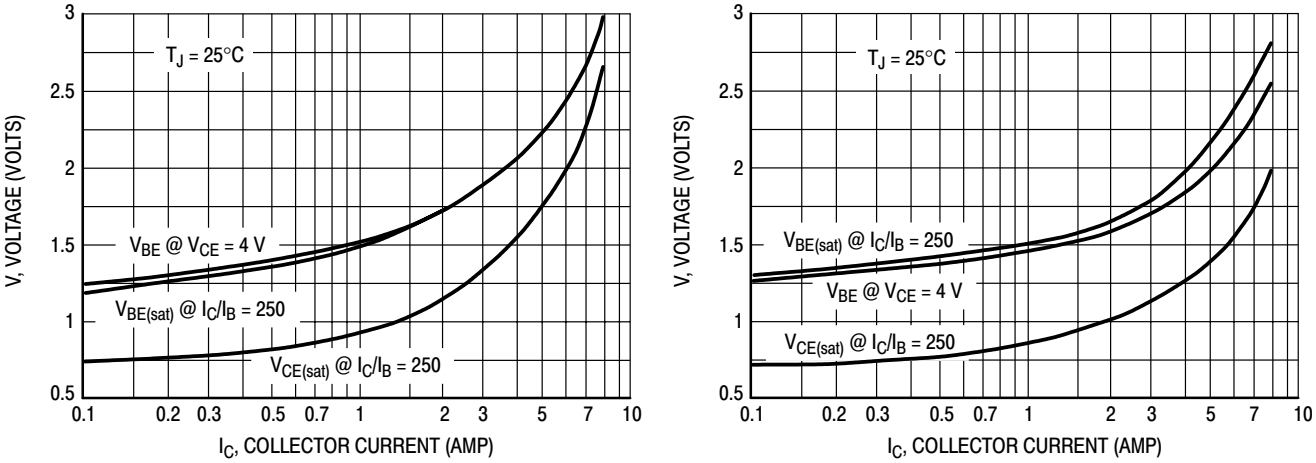


Figure 4. “On” Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127 **NPN MJD122**

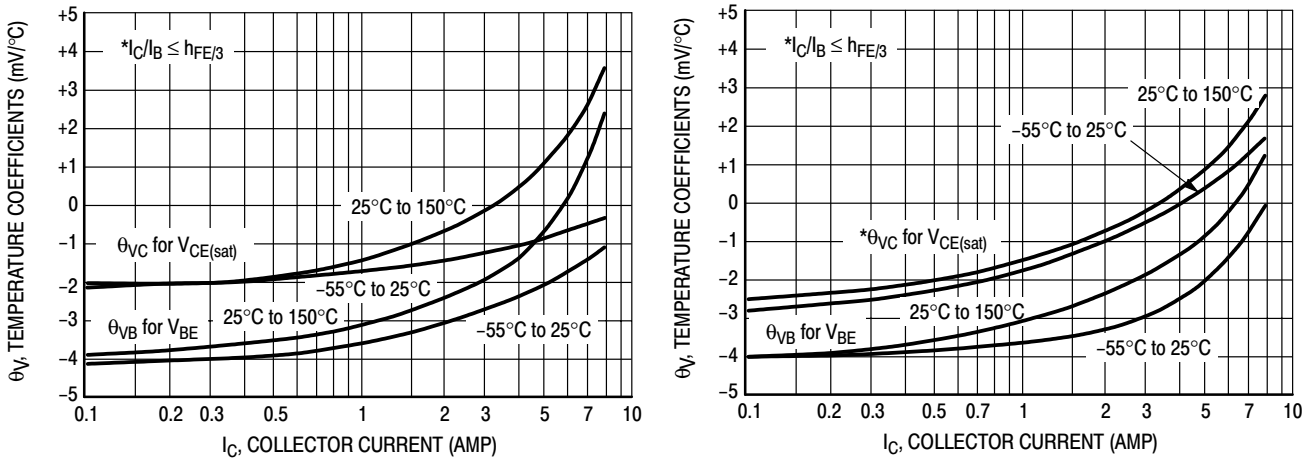


Figure 5. Temperature Coefficients

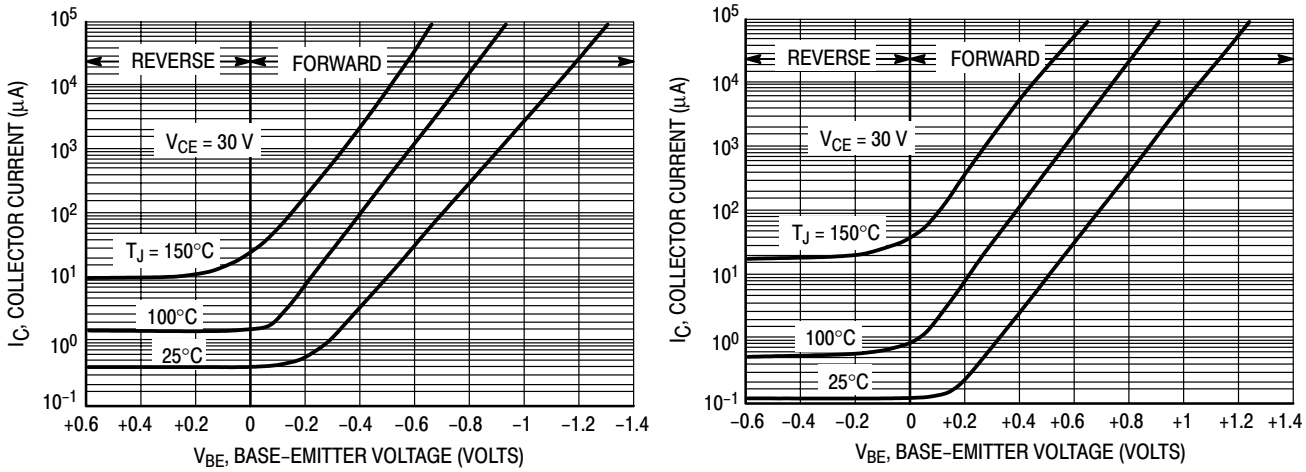


Figure 6. Collector Cut−Off Region

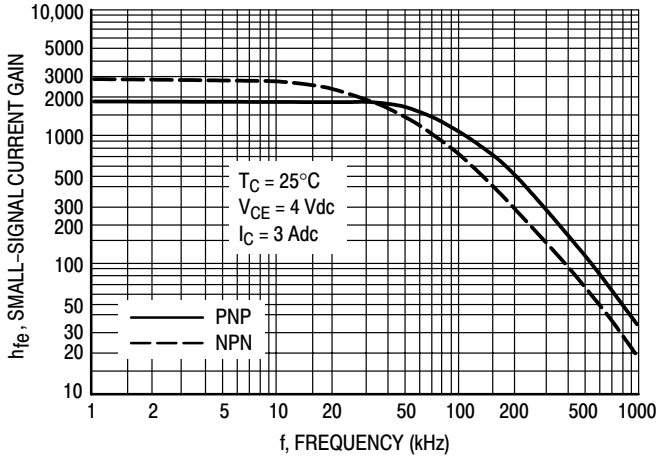


Figure 7. Small−Signal Current Gain

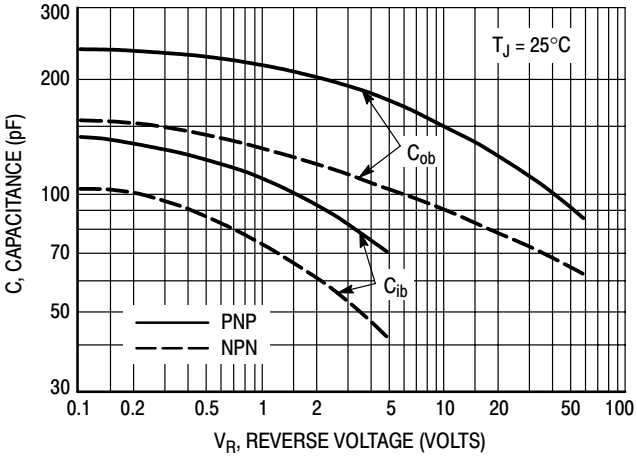


Figure 8. Capacitance

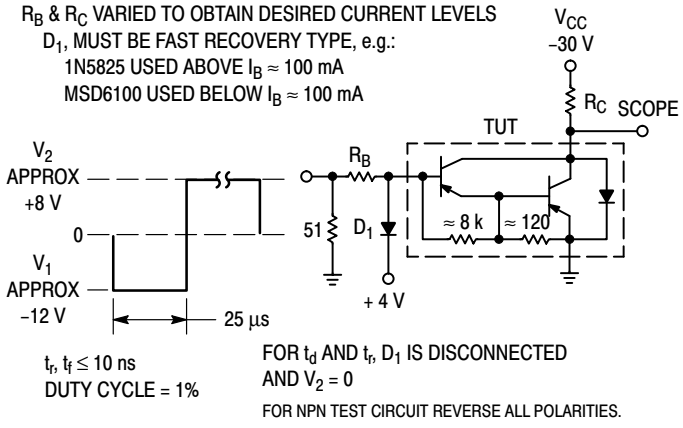


Figure 9. Switching Times Test Circuit

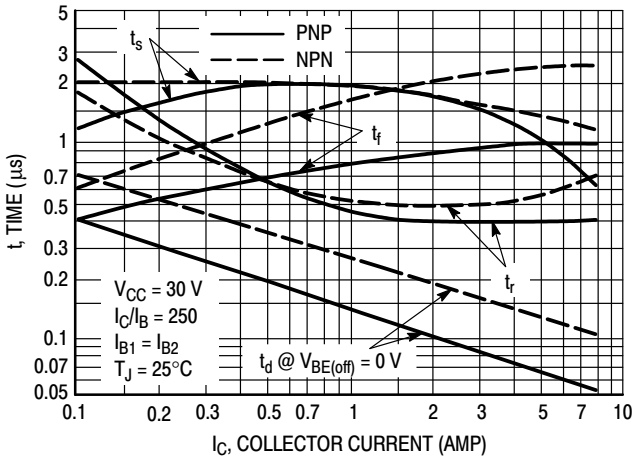


Figure 10. Switching Times

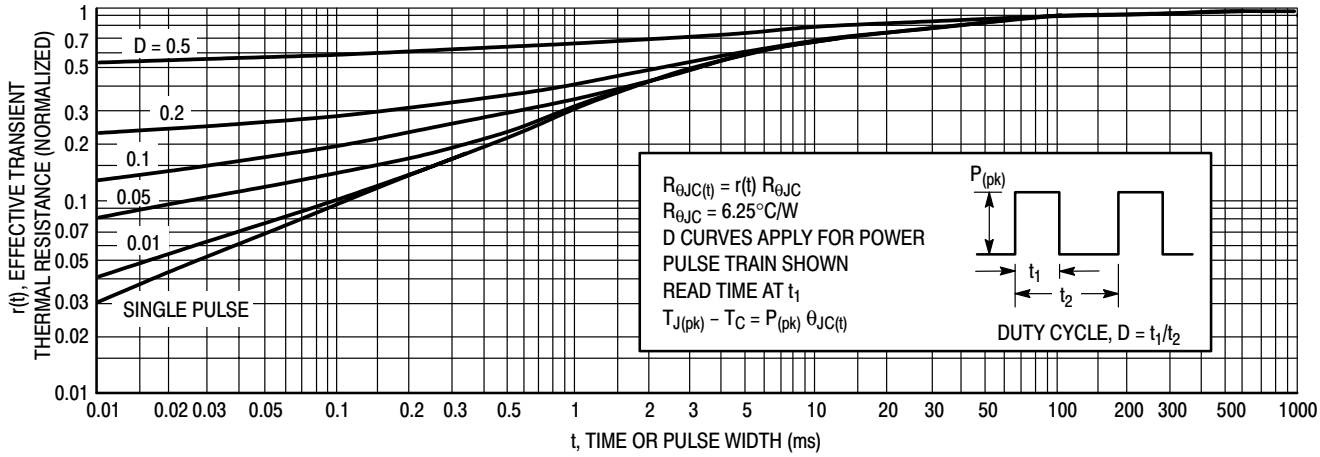


Figure 11. Thermal Response

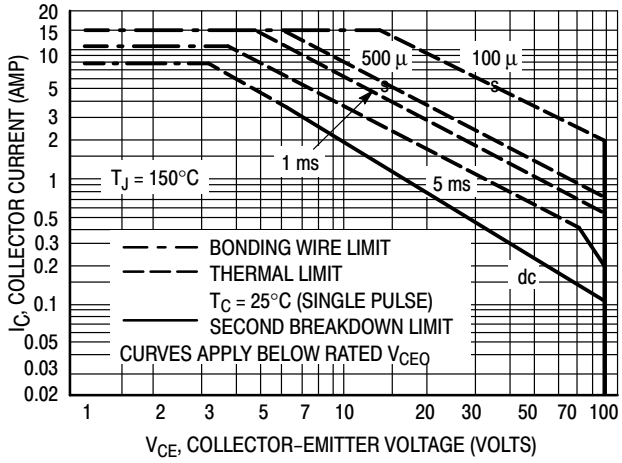


Figure 12. Maximum Forward Bias Safe Operating rea

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

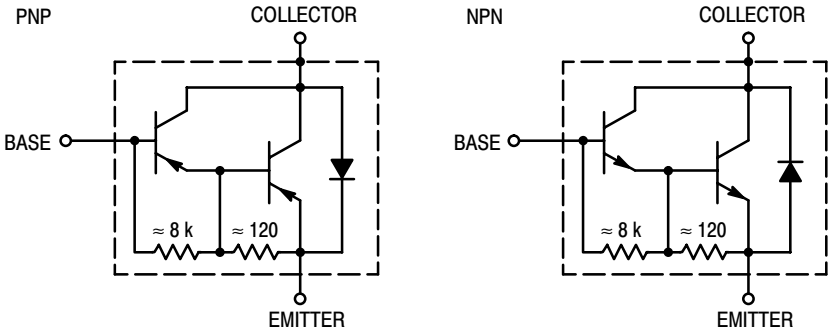


Figure 13. Darlington Schematic

MJD18002D2

Bipolar NPN Transistor

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector–Emitter Diode and Built–In Efficient Antisaturation Network

The MJD18002D2 is a state–of–the–art high speed, high gain bipolar transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no longer a need to guarantee an h_{FE} window.

Main Features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic V_{CEsat}
- Characteristics Make It Suitable for PFC Application
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

Two Versions:

- MJD18002D2–1: Case 369 for Insertion Mode
- MJD18002D2: Case 369A for Surface Mount Mode

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	11	Vdc
Collector Current – Continuous – Peak (Note 1.)	I_C I_{CM}	2.0 5.0	Adc
Base Current – Continuous – Peak (Note 1.)	I_B I_{BM}	1.0 2.0	Adc

THERMAL CHARACTERISTICS

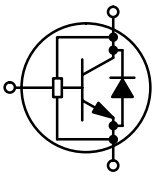
Characteristic	Symbol	Value	Unit
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to +150	°C
Thermal Resistance – Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Thermal Resistance – Junction–to–Ambient	$R_{\theta JA}$	71.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 sec.	T_L	260	°C

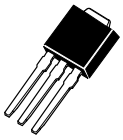
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%

ON Semiconductor™

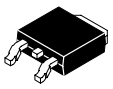
http://onsemi.com

2 AMPERES
1000 VOLTS
50 WATTS
POWER TRANSISTOR



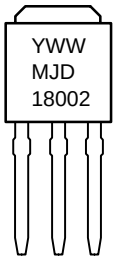


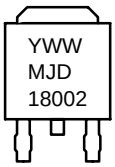
DPAK
CASE 369
STYLE 1



DPAK
CASE 369A
STYLE 1

MARKING DIAGRAMS





Y = Year
WW = Work Week
MJD18002
= Device Code

ORDERING INFORMATION

Device	Package	Shipping
MJD18002D2–1	DPAK	75 Units/Rail
MJD18002D2T4	DPAK	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	570	–	Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	1000	1100	–	Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	11	14	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C	I_{CES}	–	–	100	μAdc
	@ T_C = 125°C		–	–	500	
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C		–	–	100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	–	500	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C		–	0.78	1.0	
(I_C = 1.0 Adc, I_B = 0.2 Adc)	@ T_C = 25°C		–	0.87	1.1	
Collector–Emitter Saturation Voltage	@ T_C = 25°C	$V_{CE(sat)}$	–	0.36	0.6	Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 125°C		–	0.50	1.0	
(I_C = 1.0 Adc, I_B = 0.2 Adc)	@ T_C = 25°C		–	0.40	0.75	
	@ T_C = 125°C		–	0.65	1.2	
DC Current Gain	@ T_C = 25°C	h_{FE}	14	25	–	–
(I_C = 0.4 Adc, V_{CE} = 1.0 Vdc)	@ T_C = 125°C		8.0	15	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	@ T_C = 25°C		6.0	10	–	
	@ T_C = 125°C		4.0	6.0	–	
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_t	–	13	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	–	50	100	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}	–	340	500	pF
DIODE CHARACTERISTICS						
Forward Diode Voltage		V_{EC}				Vdc
(I_{EC} = 1.0 Adc)	@ T_C = 25°C		–	1.2	1.5	
(I_{EC} = 0.4 Adc)	@ T_C = 25°C		–	1.0	1.3	
	@ T_C = 125°C		–	0.6	–	
Forward Recovery Time		t_{fr}				ns
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C		–	517	–	
(I_F = 1.0 Adc, di/dt = 10 A/μs)	@ T_C = 25°C		–	480	–	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage Determinated 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.4 Adc, I_{B1} = 40 mA, V_{CC} = 300 Vdc	@ 1 μs	@ T_C = 25°C	$V_{CE(dsat)}$	–	7.4	–	V
		@ 3 μs	@ T_C = 25°C		–	2.5	–	
	I_C = 1 Adc, I_{B1} = 0.2 A, V_{CC} = 300 Vdc	@ 1 μs	@ T_C = 25°C		–	11.7	–	
		@ 3 μs	@ T_C = 25°C		–	1.3	–	
SWITCHING CHARACTERISTICS: Resistive Load (D.C.S. 10%, Pulse Width = 40 μs)								
Turn–on Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 200 mAdc, V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}	– –	225 375	350 –	ns
Turn–off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}	0.8 –	– 1.5	1.1 –	μs
Turn–on Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc, V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}	– –	100 94	150 –	ns
Turn–off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}	0.95 –	– 1.5	1.25 –	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 0.2 Adc		@ T_C = 25°C @ T_C = 125°C	t_f	– –	130 120	175 –	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s	0.4 –	– 0.7	0.7 –	μs
Cross–over Time			@ T_C = 25°C @ T_C = 125°C	t_c	– –	110 100	175 –	ns
Fall Time	I_C = 0.8 Adc, I_{B1} = 160 mAdc, I_{B2} = 160 mAdc		@ T_C = 25°C @ T_C = 125°C	t_f	– –	130 140	175 –	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s	2.1 –	– 3.0	2.4 –	μs
Cross–over Time			@ T_C = 25°C @ T_C = 125°C	t_c	– –	275 350	350 –	ns
Fall Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc		@ T_C = 25°C @ T_C = 125°C	t_f	– –	100 100	150 –	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s	– –	1.05 1.45	1.2 –	μs
Cross–over Time			@ T_C = 25°C @ T_C = 125°C	t_c	– –	100 115	150 –	ns

Typical Static Characteristics

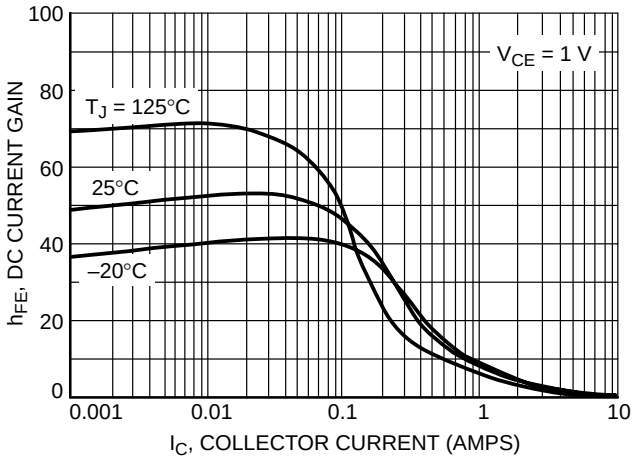


Figure 1. DC Current Gain @ 1 V

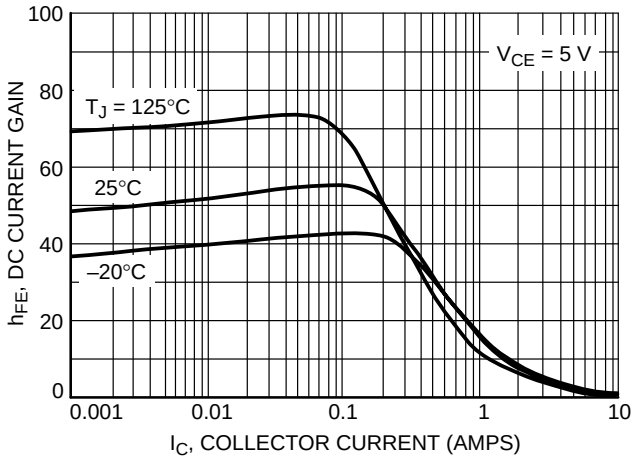


Figure 2. DC Current Gain @ 5 V

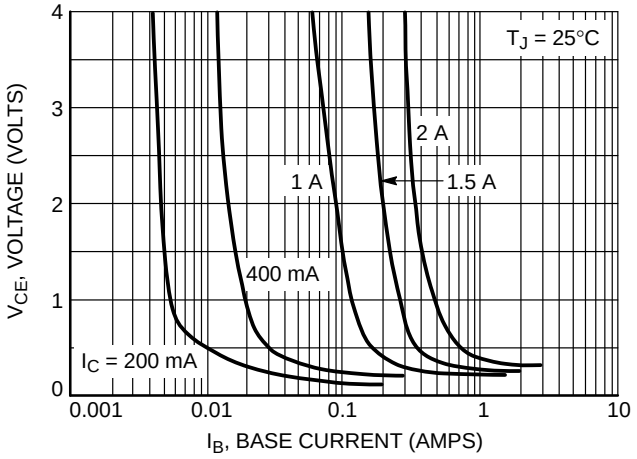


Figure 3. Collector Saturation Region

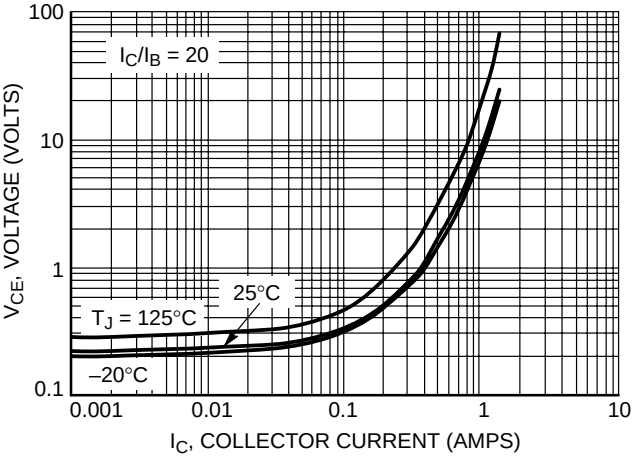


Figure 4. Collector–Emitter Saturation Voltage

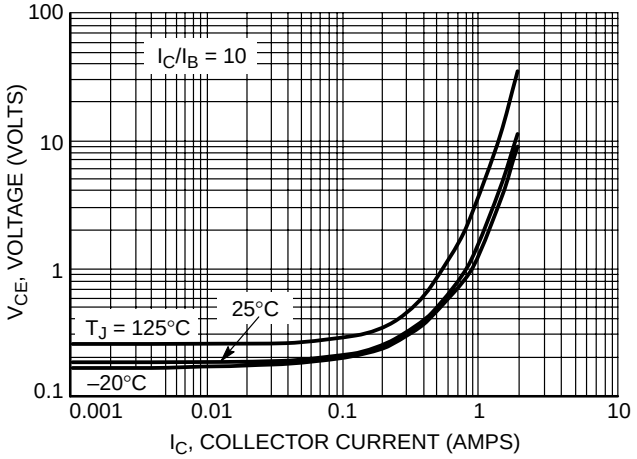


Figure 5. Collector–Emitter Saturation Voltage

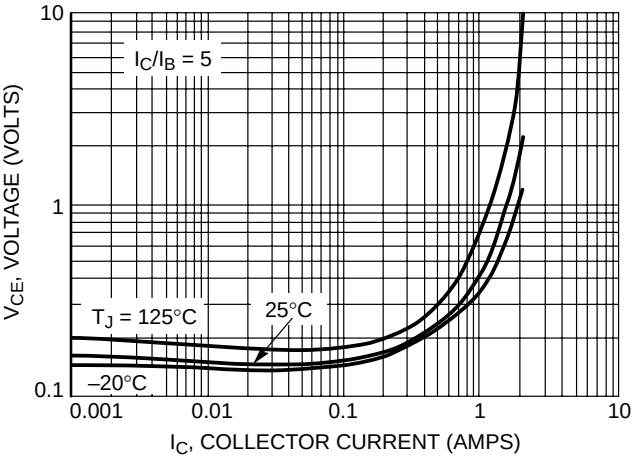


Figure 6. Collector–Emitter Saturation Voltage

Typical Static Characteristics

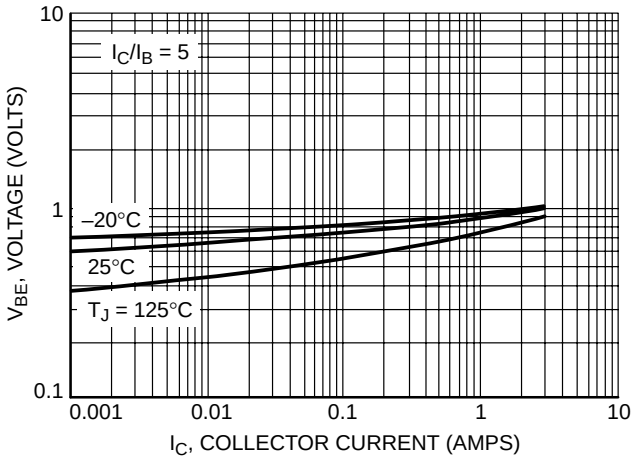


Figure 7. Base–Emitter Saturation Region I_C/I_B = 5

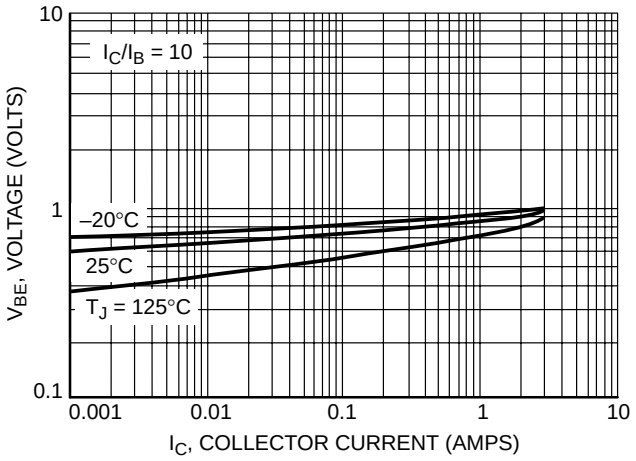


Figure 8. Base–Emitter Saturation Region I_C/I_B = 10

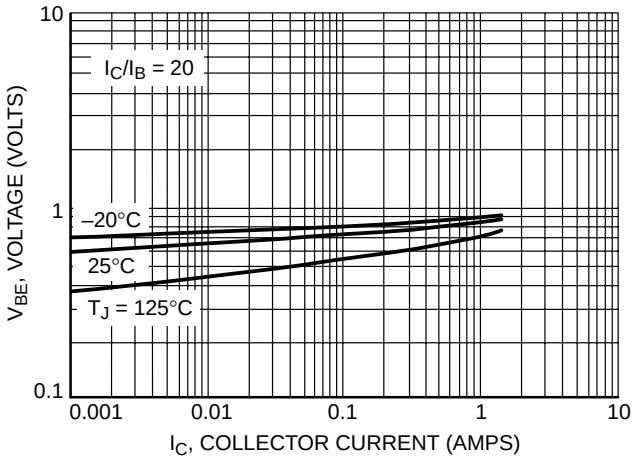


Figure 9. Base–Emitter Saturation Region I_C/I_B = 20

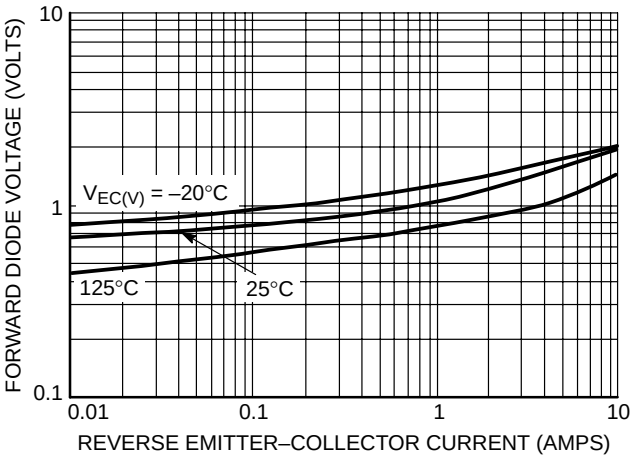


Figure 10. Forward Diode Voltage

Typical Switching Characteristics

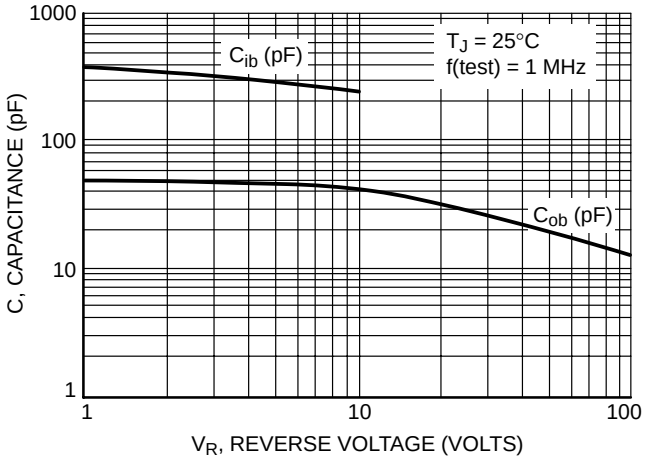


Figure 11. Capacitance

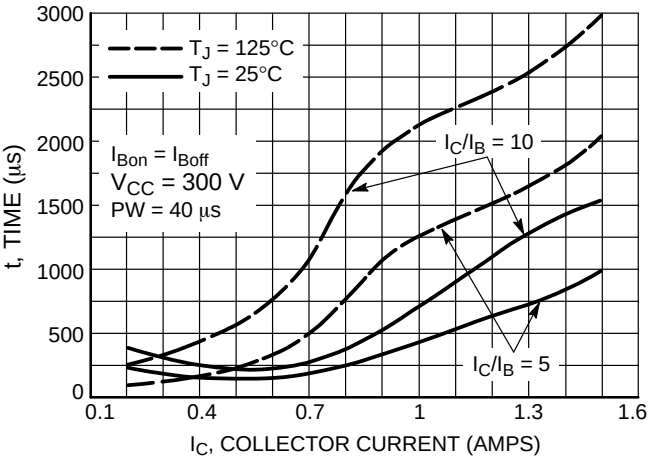


Figure 12. Resistive Switch Time, t_{on}

Typical Switching Characteristics

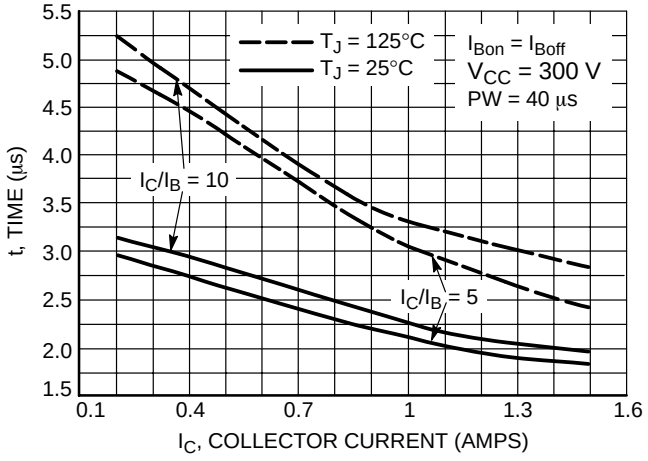


Figure 13. Resistive Switch Time, t_{off}

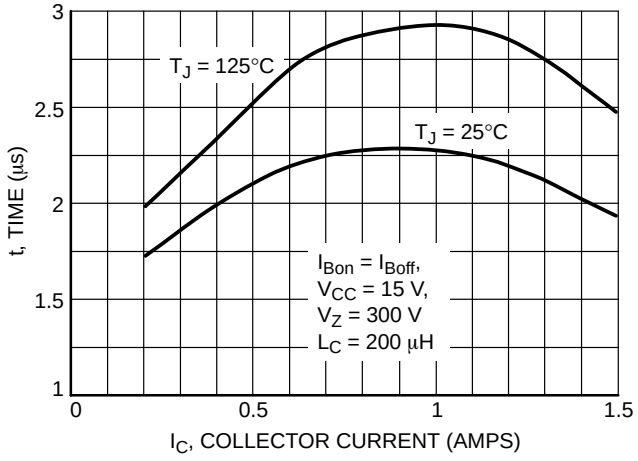


Figure 14. Inductive Storage Time, t_{si} @ I_C/I_B = 5

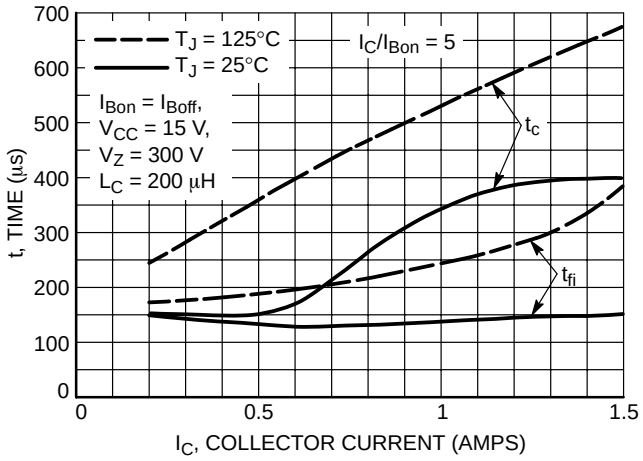


Figure 15. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

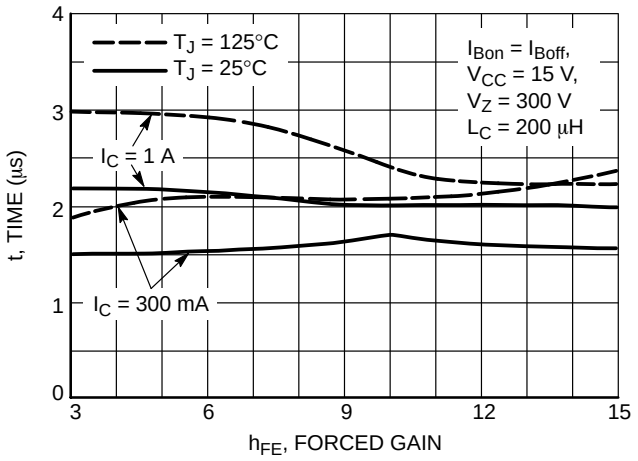


Figure 16. Inductive Storage Time

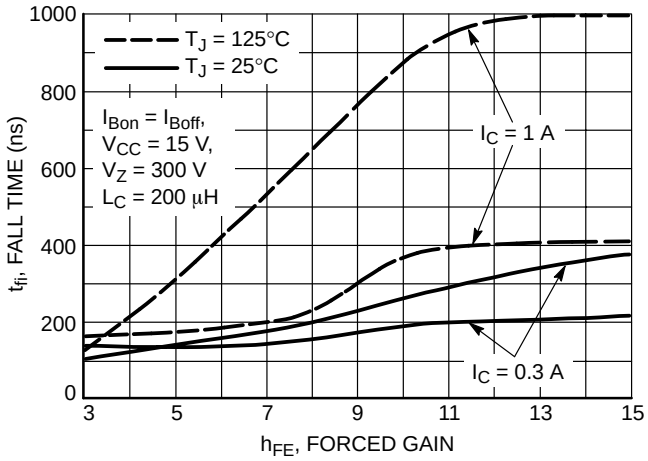


Figure 17. Inductive Fall Time

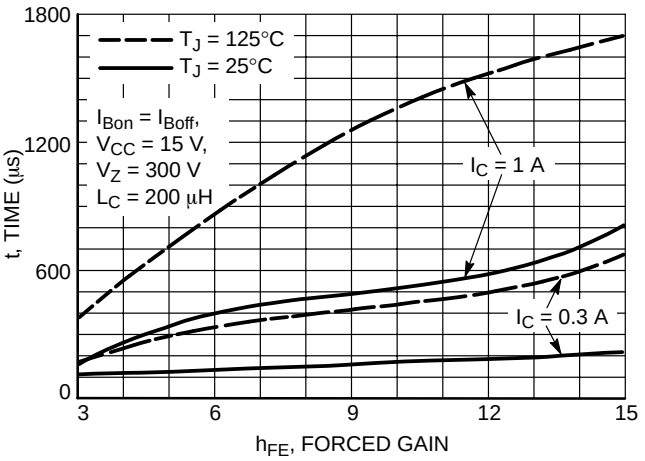


Figure 18. Inductive Cross–Over Time

Typical Switching Characteristics

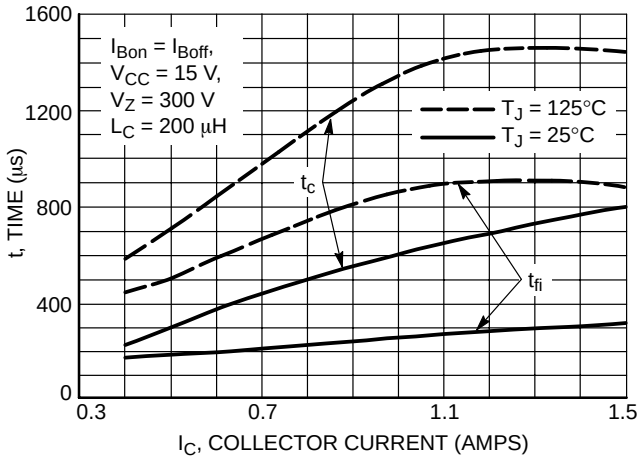


Figure 19. Inductive Switching Time, t_{fi} & T_C @ G = 10

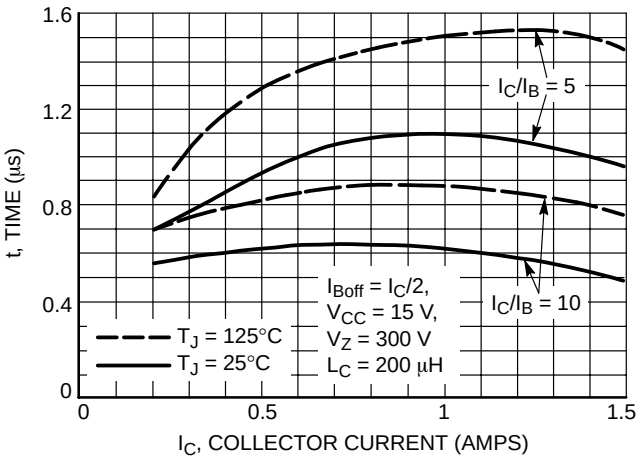


Figure 20. Inductive Switching Time, t_{si}

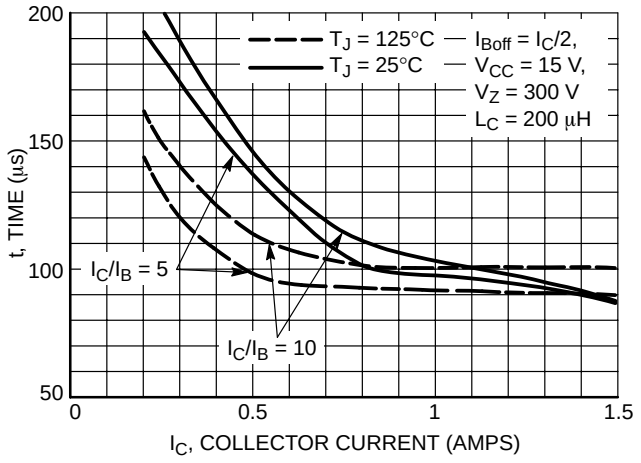


Figure 21. Inductive Storage Time, t_{fi}

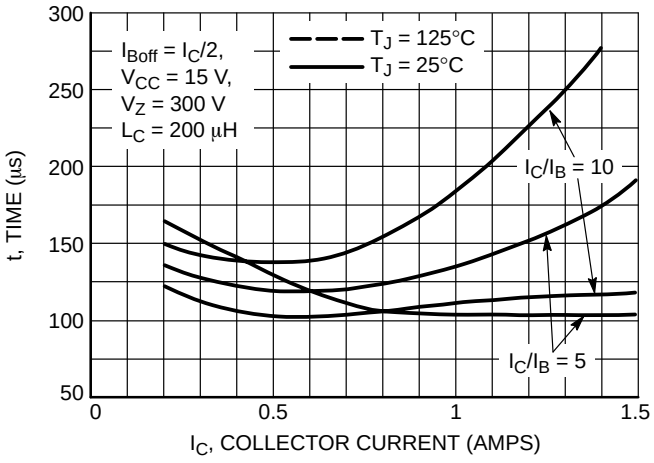


Figure 22. Inductive Storage Time, t_c

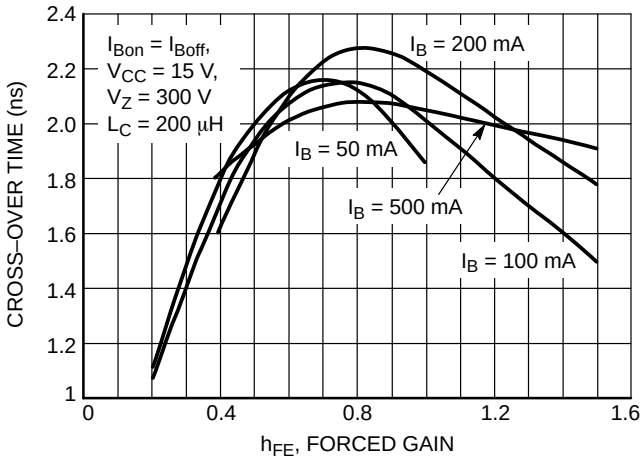


Figure 23. Inductive Storage Time, t_{si}

Figure 24. Dynamic Saturation Voltage Measurements

Typical Switching Characteristics

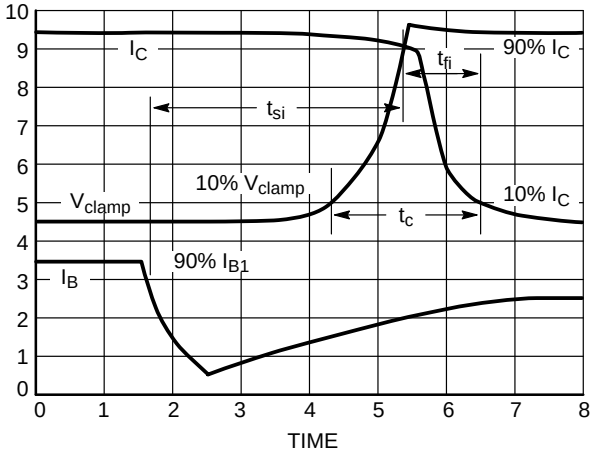
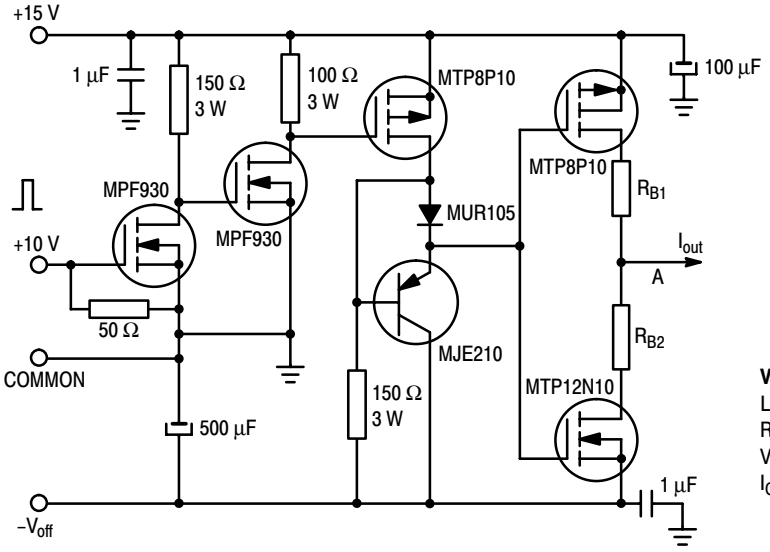
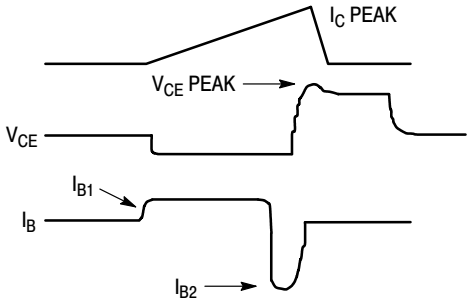


Figure 25. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	**Inductive Switching**	**RBSOA**
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

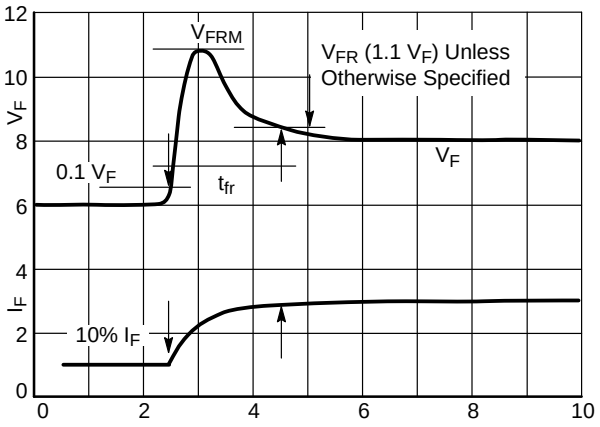


Figure 26. t_{fr} Measurement

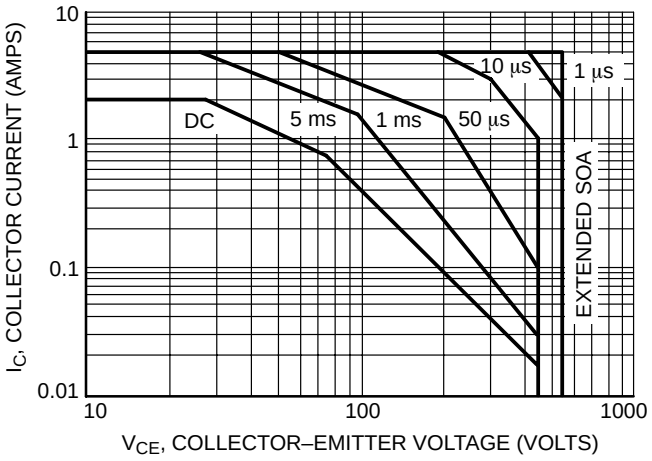


Figure 27. Forward Bias Safe Operating Area

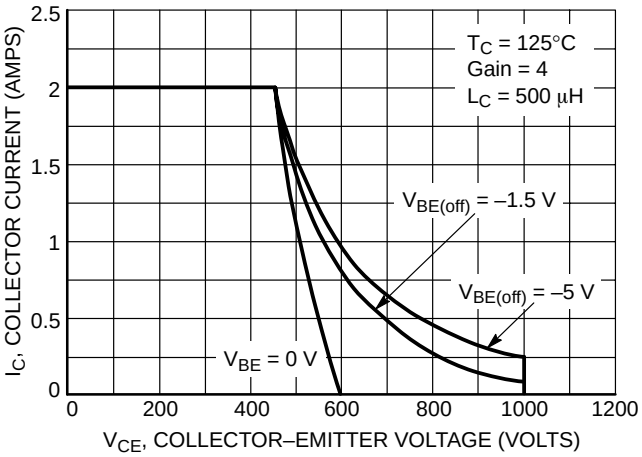


Figure 28. Reverse Bias Safe Operating Area

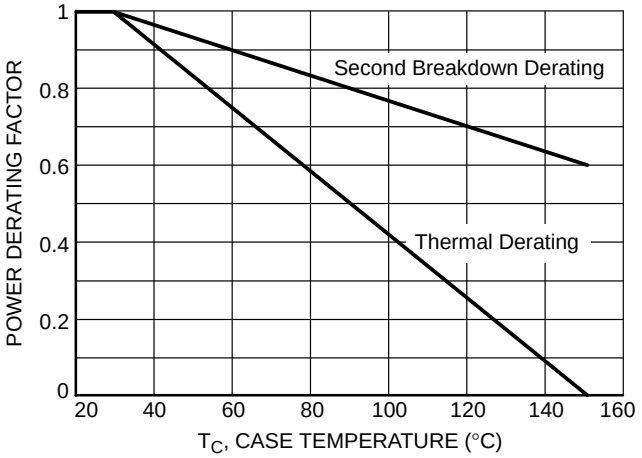


Figure 29. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 27 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second Breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 27 may be found at any case temperature by using the appropriate curve on Figure 29.

$T_{J(pk)}$ may be calculated from the data in Figure 30. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 28). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

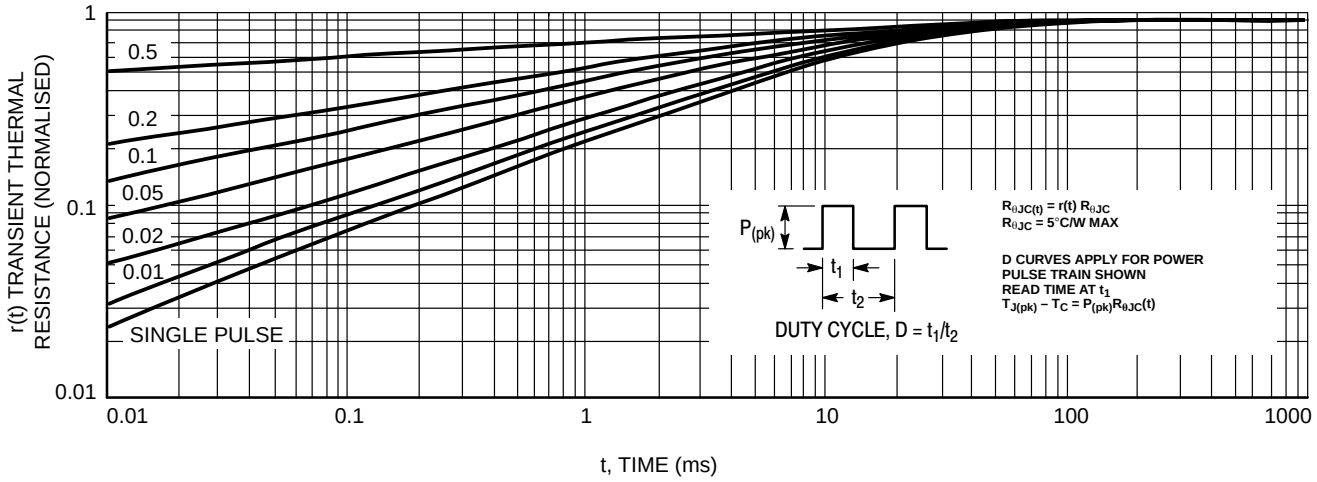


Figure 30. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJD18002D2

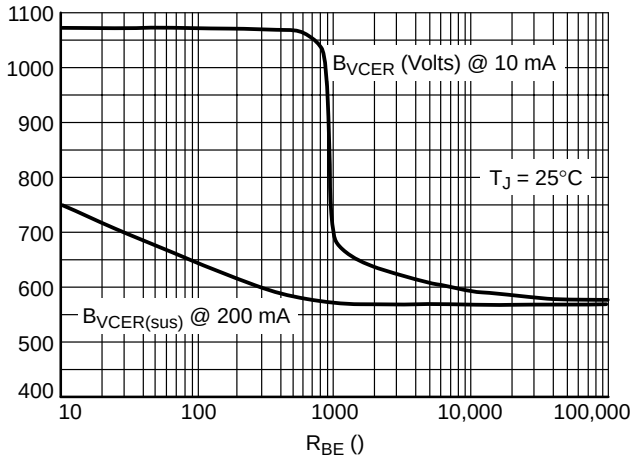


Figure 31. B_{VCER}

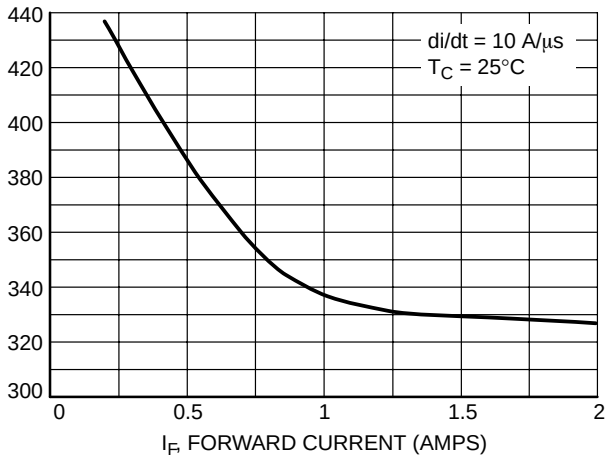


Figure 32. Forward Recovery Time, t_{fr}

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 33 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

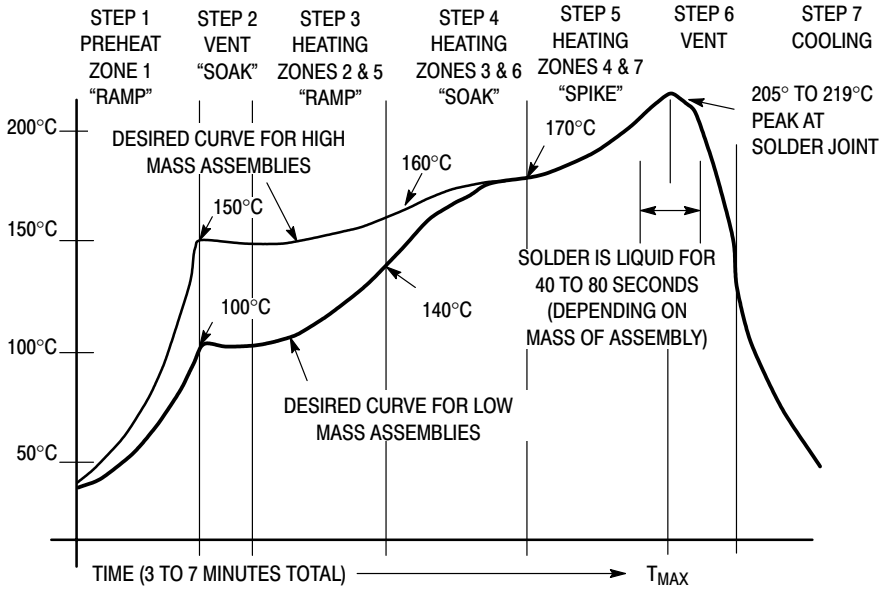


Figure 33. Typical Solder Heating Profile

Complementary Plastic Power Transistors

NPN/PNP Silicon DPAK For Surface Mount Applications

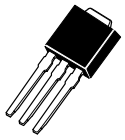
NPN
MJD200
PNP
MJD210

SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS

. . . designed for low voltage, low–power, high–gain audio amplifier applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2 Adc
  = 10 (Min) @ I_C = 5 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“–1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current–Gain — Bandwidth Product —
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage —
  I_{CBO} = 100 nAdc @ Rated V_{CB}

CASE 369A–13

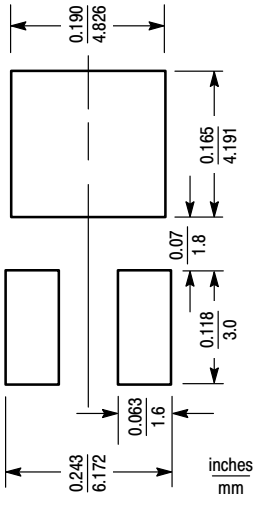


CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	40	Vdc
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Emitter–Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Junction to Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 — —	 100 100	nAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}	—	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (2) (I_C = 500 mAdc, V_{CE} = 1 Vdc) (I_C = 2 Adc, V_{CE} = 1 Vdc) (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	 70 45 10	 — 180 —	—
Collector–Emitter Saturation Voltage (2) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 200 mAdc) (I_C = 5 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	 — — —	 0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 2 Adc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (3) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob} MJD200 MJD210	 — —	 80 120	pF

*When surface mounted on minimum pad sizes recommended.

(continued)

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.

(3) $f_T = |h_{fe}| \bullet f_{test}$.

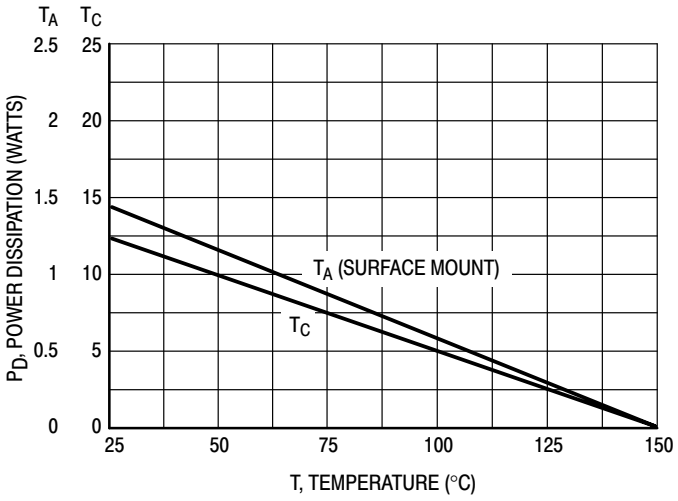


Figure 34. Power Derating

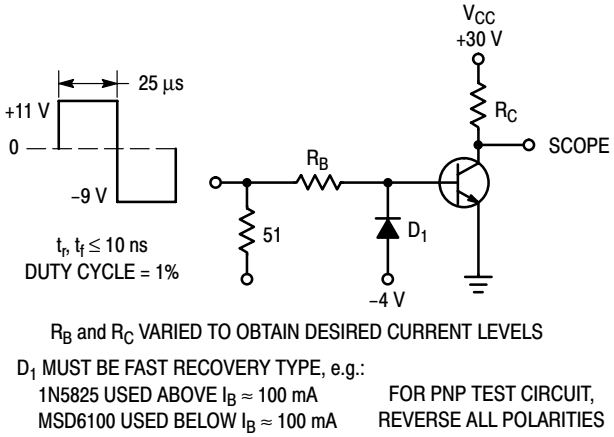


Figure 35. Switching Time Test Circuit

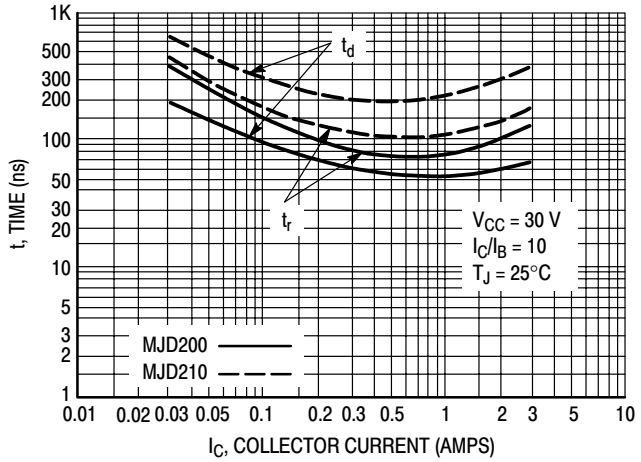


Figure 36. Turn−On Time

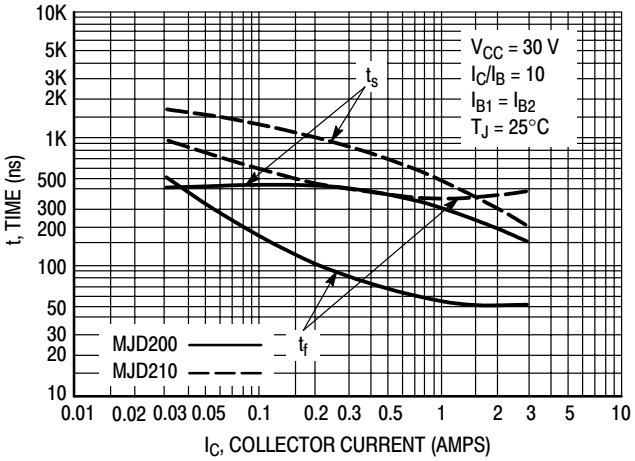
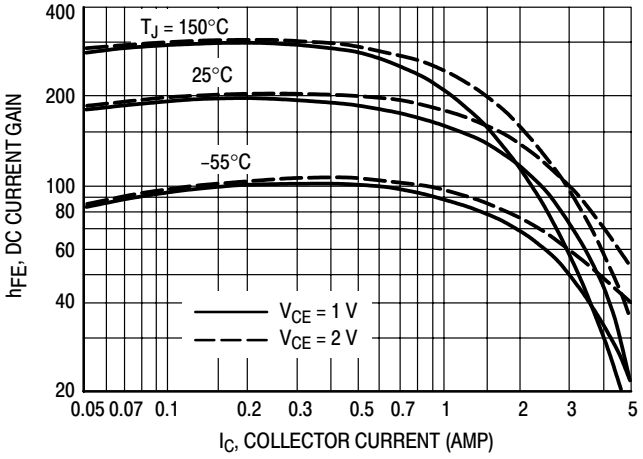


Figure 37. Turn−Off Time

NPN
MJD200



PNP
MJD210

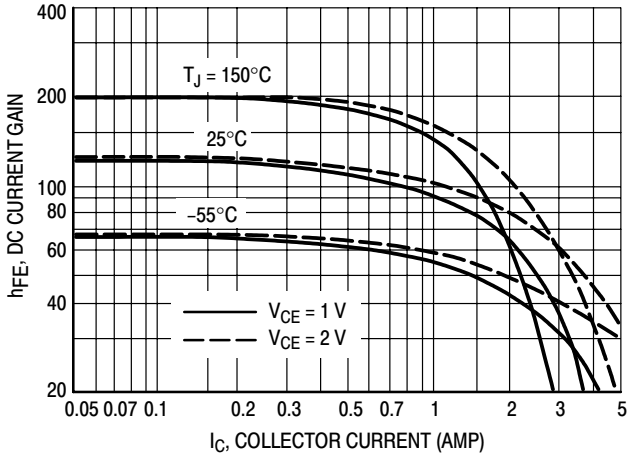
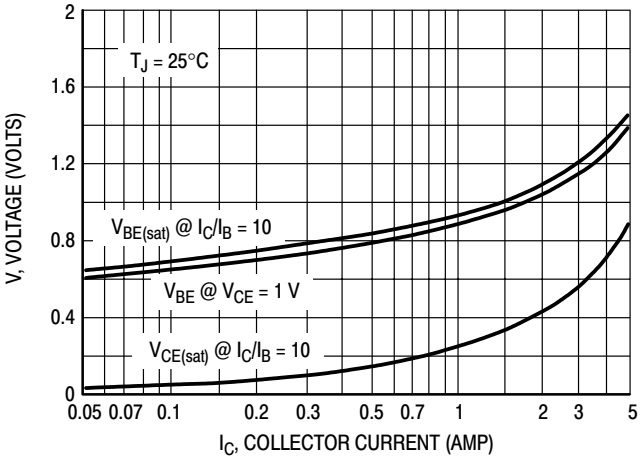


Figure 38. DC Current Gain



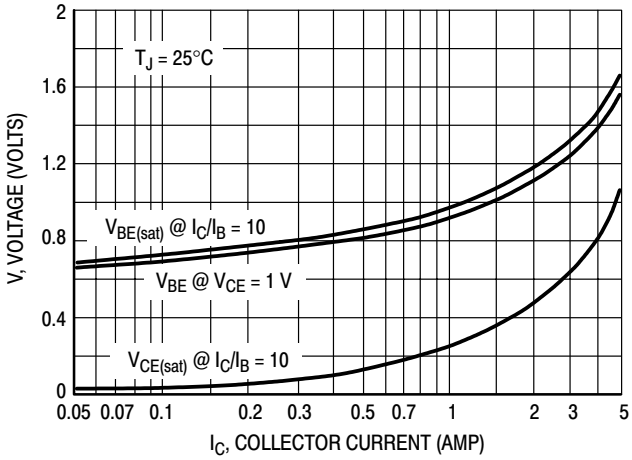
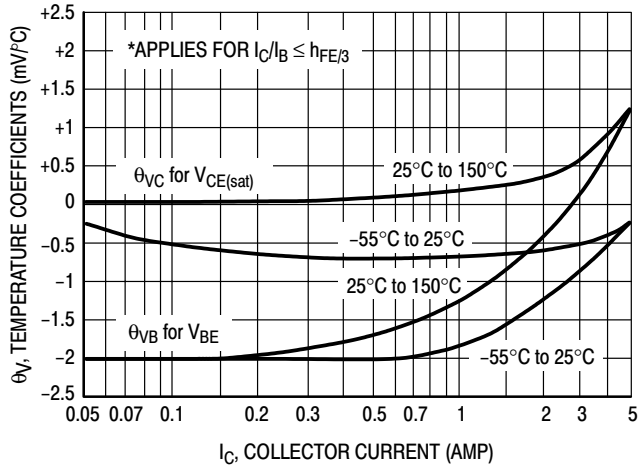


Figure 39. “On” Voltage



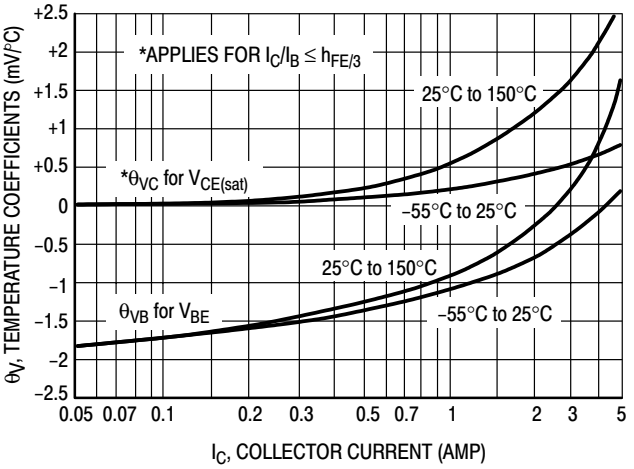


Figure 40. Temperature Coefficients

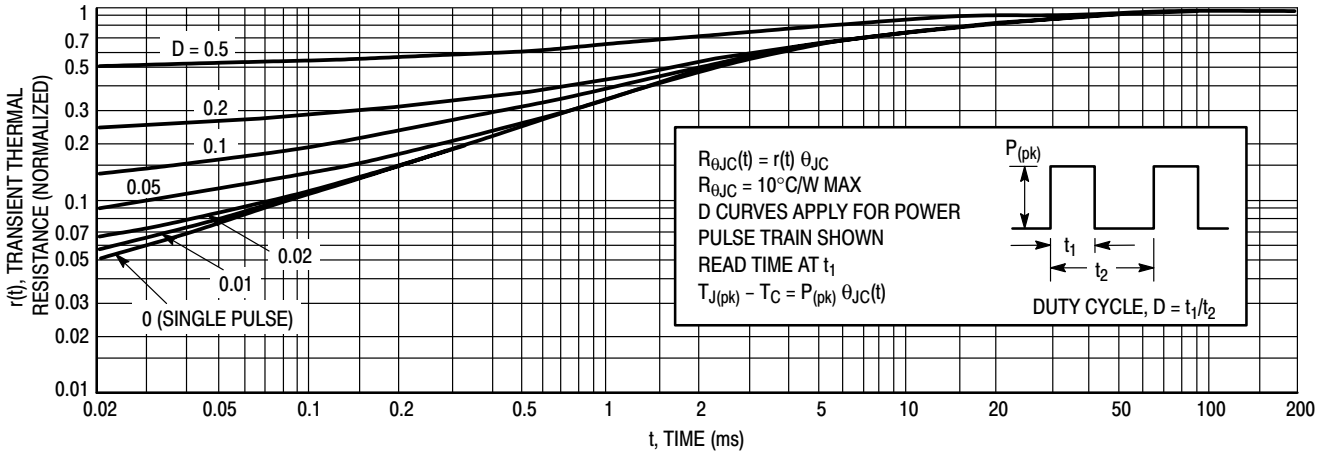


Figure 41. Thermal Response

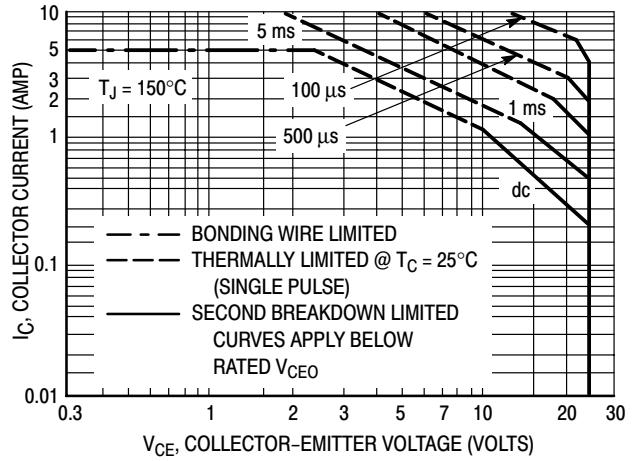


Figure 42. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 42 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Case 369 may be ordered by adding a "–1" suffix to the device title (i.e. MJD200–1)

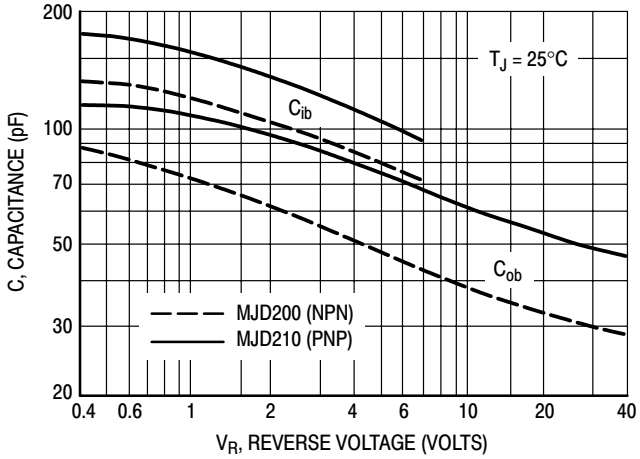


Figure 43. Capacitance

MJD243 (NPN), MJD253 (PNP)

MJD243 is a Preferred Device

Complementary Silicon Plastic Power Transistor

DPAK for Surface Mount Applications

. . . designed for low voltage, low–power, high–gain audio amplifier applications.

- Collector–Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain –
  h_{FE} = 40 (Min) @ I_C = 200 mAdc
  = 15 (Min) @ I_C = 1.0 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Low Collector–Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.6 Vdc (Max) @ I_C = 1.0 Adc
- High Current–Gain – Bandwidth Product –
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage –
  I_{CBO} = 100 nAdc @ Rated V_{CB}

MAXIMUM RATINGS

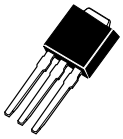
Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current – Continuous – Peak	I_C	4 8	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C (Note 1.) Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

1. When surface mounted on minimum pad sizes recommended.

ON Semiconductor™

http://onsemi.com

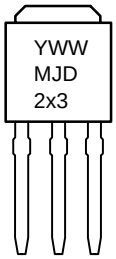
4 AMPERES
100 VOLTS
12.5 WATTS
POWER TRANSISTOR

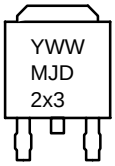


DPAK
CASE 369
STYLE 1

DPAK
CASE 369A
STYLE 1

MARKING DIAMONDS





Y = Year
WW = Work Week
MJD2x3 = Device Code
x = 4 or 5

ORDERING INFORMATION

Device	Package	Shipping
MJD243–1	DPAK	75 Units/Rail
MJD243T4	DPAK	3000/Tape & Reel
MJD253–1	DPAK	75 Units/Rail
MJD253T4	DPAK	3000/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

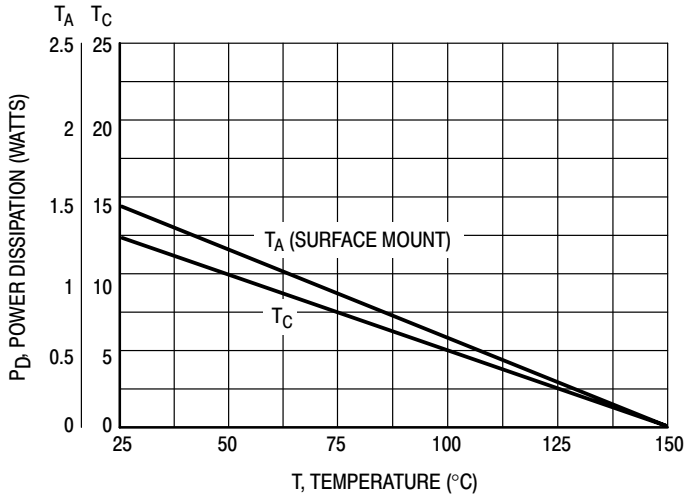


Figure 1. Power Derating

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Junction to Ambient (Note 2.)	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 3.) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	– –	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
DC Current Gain (Note 3.) (I_C = 200 mAdc, V_{CE} = 1 Vdc) (I_C = 1 Adc, V_{CE} = 1 Vdc)	h_{FE}	40 15	180 –	–
Collector–Emitter Saturation Voltage (Note 3.) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	 – –	 0.3 0.6	Vdc
Base–Emitter Saturation Voltage (Note 3.) (I_C = 2 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	–	1.8	Vdc
Base–Emitter On Voltage (Note 3.) (I_C = 500 mAdc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain – Bandwidth Product (Note 4.) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	50	pF

2. When surface mounted on minimum pad sizes recommended.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$.

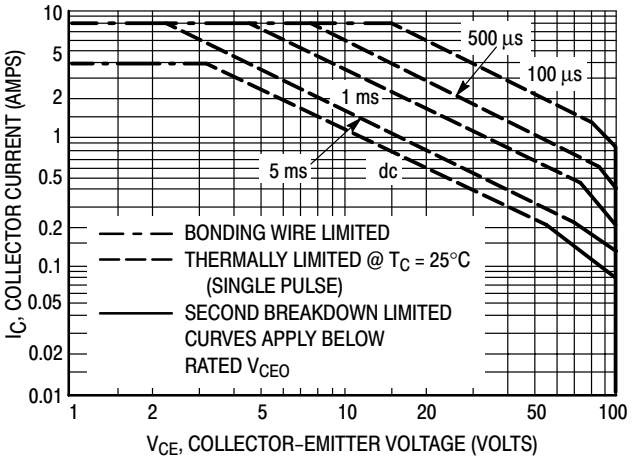


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

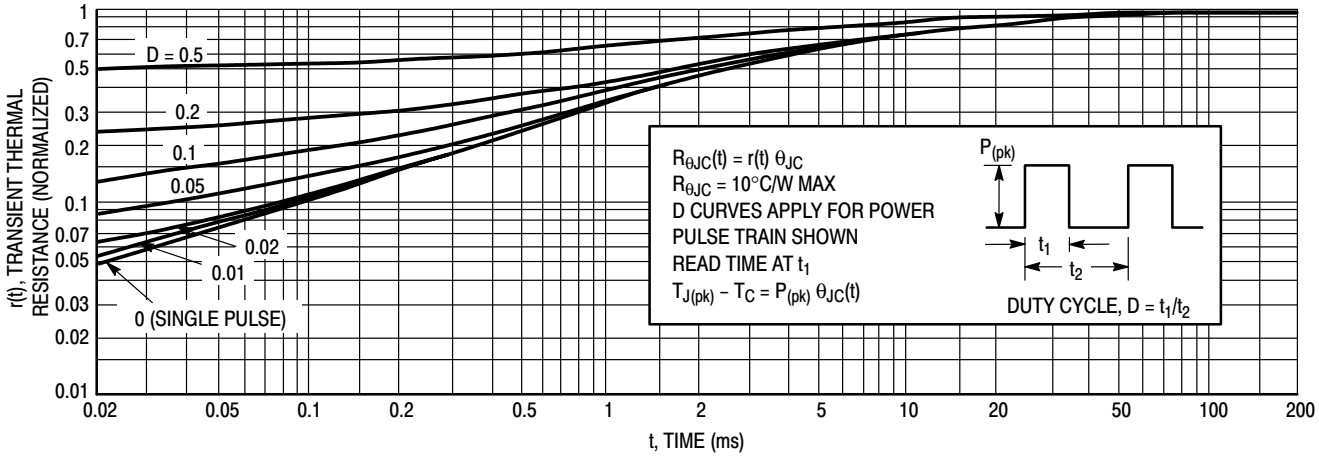
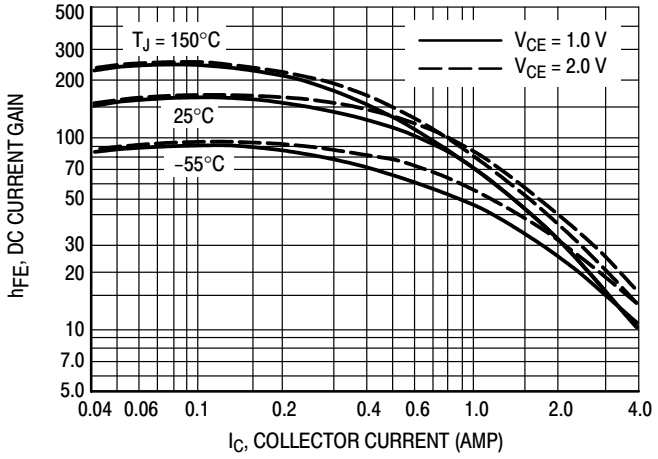


Figure 3. Thermal Response

NPN
MJD243



PNP
MJD253

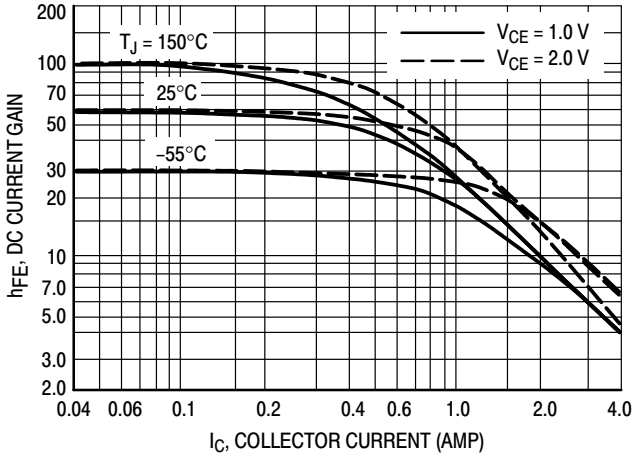
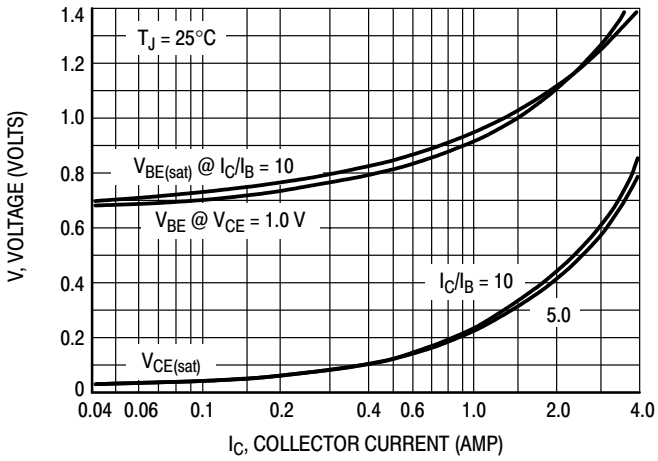


Figure 4. DC Current Gain



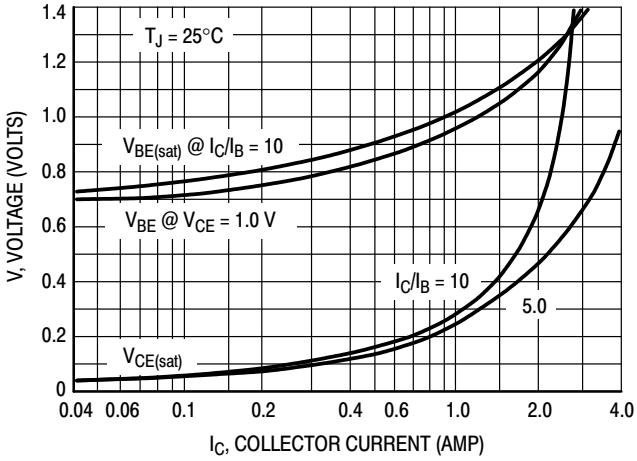
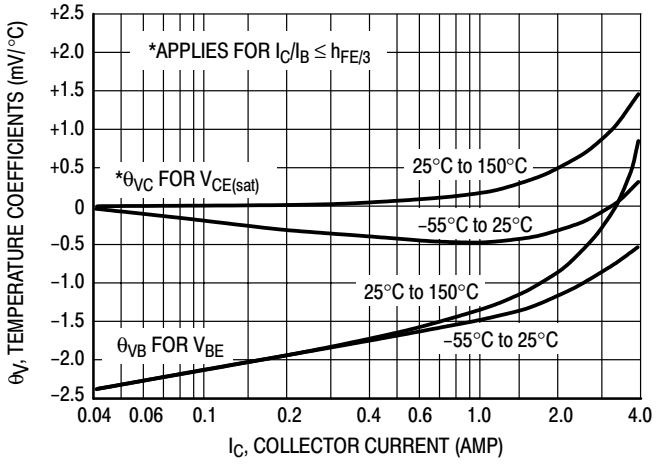


Figure 5. “On” Voltages



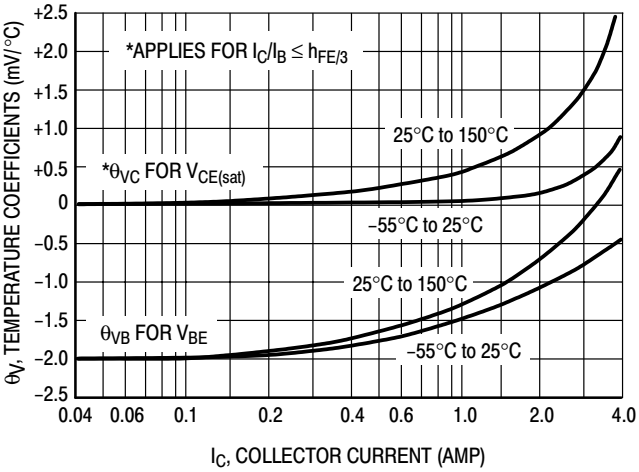
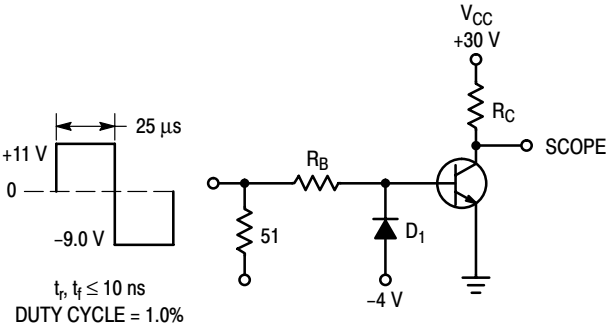


Figure 6. Temperature Coefficients



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 7. Switching Time Test Circuit

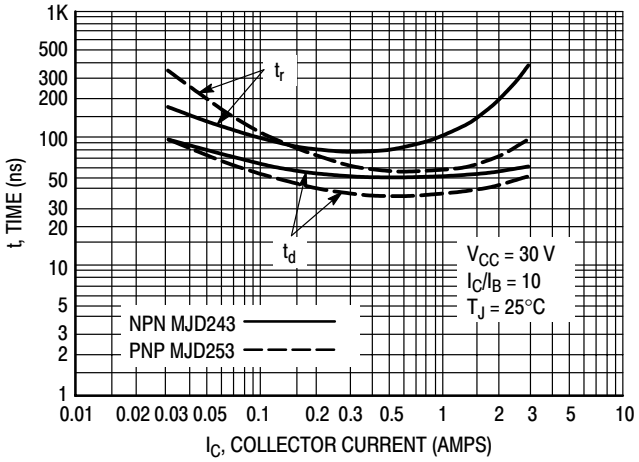


Figure 8. Turn–On Time

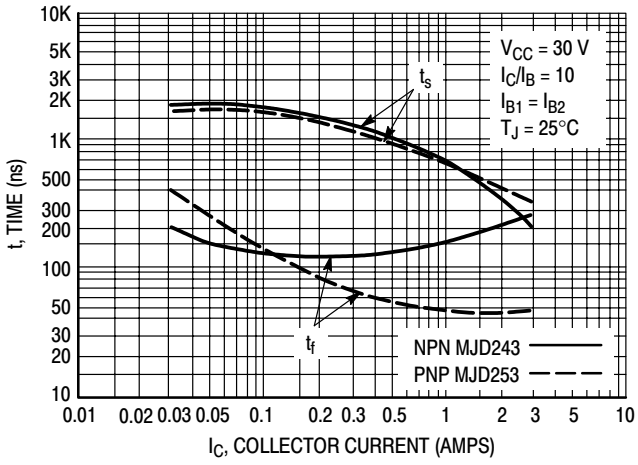


Figure 9. Turn–Off Time

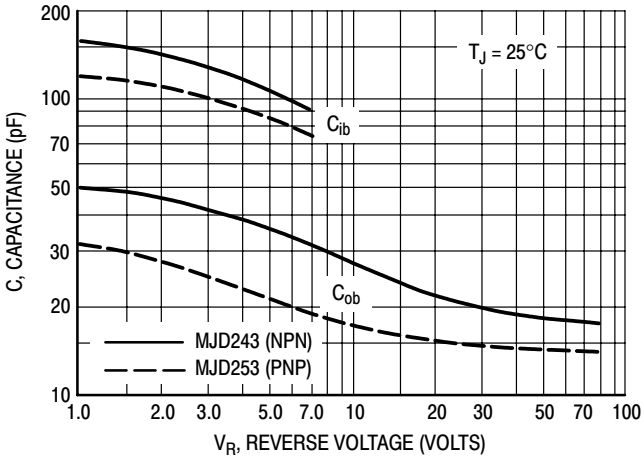


Figure 10. Capacitance

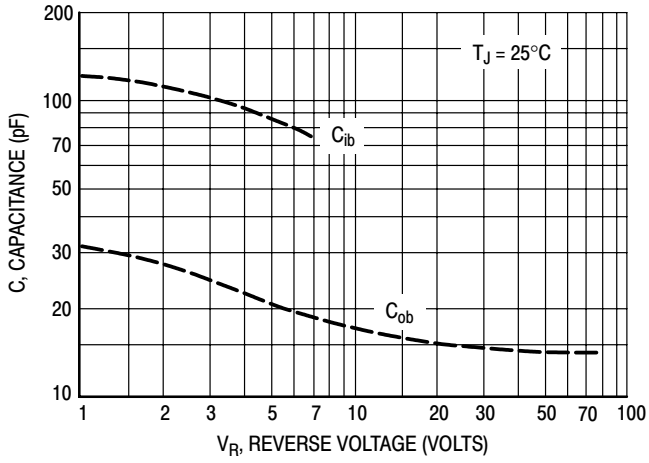


Figure 11. Capacitance

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

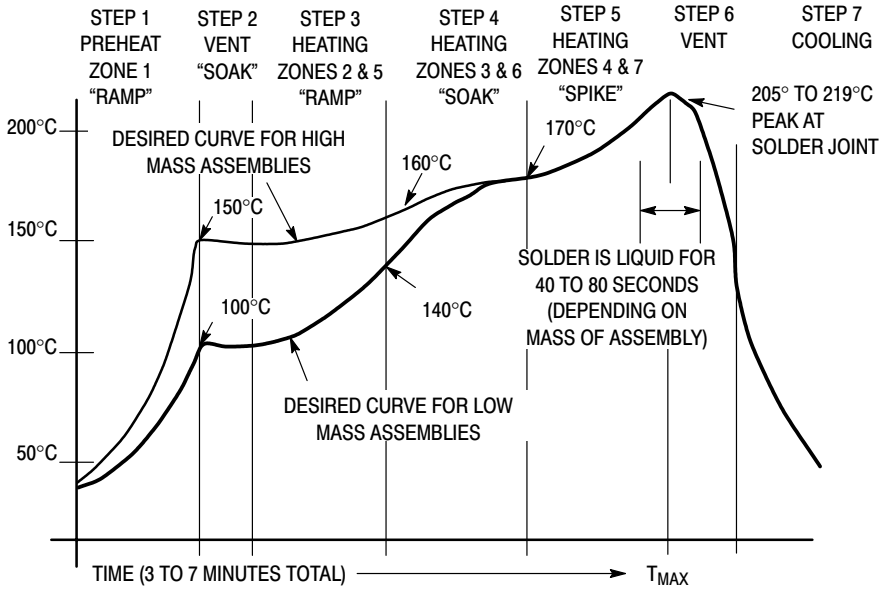


Figure 12. Typical Solder Heating Profile

Complementary Power Transistors

DPAK For Surface Mount Applications

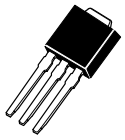
PNP
MJD2955
NPN
MJD3055

SILICON
POWER TRANSISTORS
10 AMPERES
60 VOLTS
20 WATTS

Designed for general purpose amplifier and low speed switching applications.

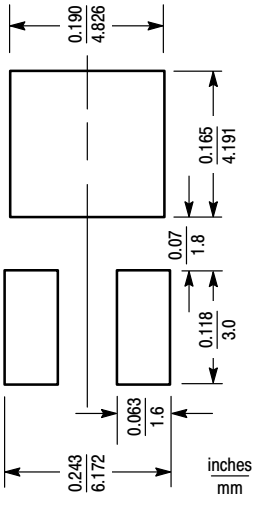
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to MJE2955 and MJE3055
- DC Current Gain Specified to 10 Amperes
- High Current Gain–Bandwidth Product —
  f_T = 2.0 MHz (Min) @ I_C
  = 500 mAdc

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CB}	70	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D†	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.
†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 0.02 2	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 0.02 2	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	 20 5	 100 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 8	Vdc
Base–Emitter On Voltage (1) (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

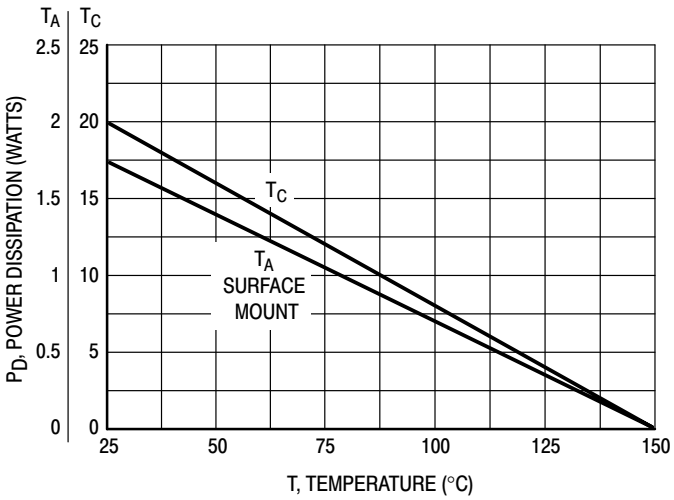


Figure 1. Power Derating

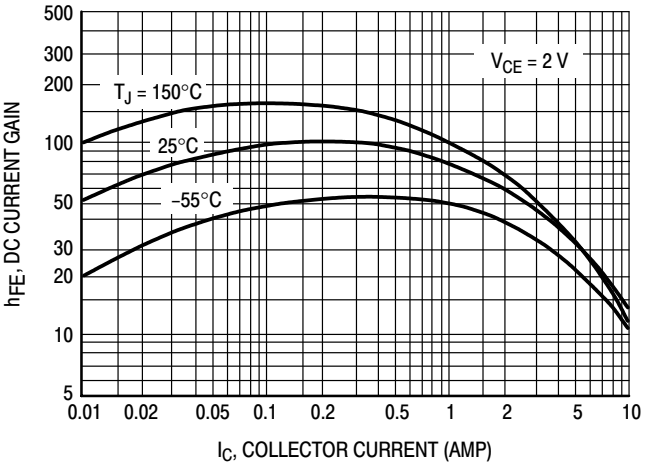


Figure 2. DC Current Gain

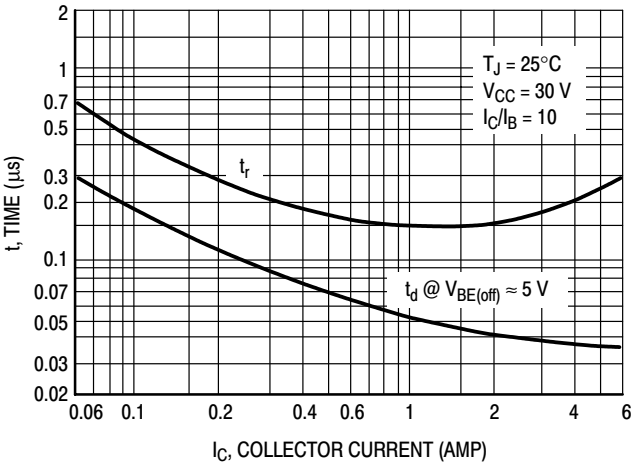


Figure 3. Turn−On Time

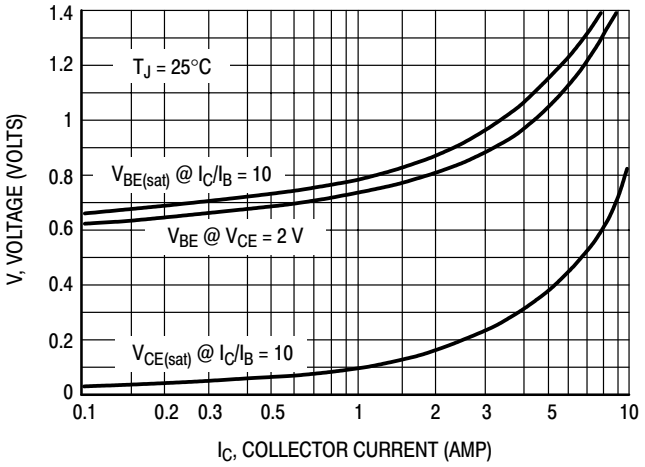


Figure 4. “On” Voltages, MJD3055

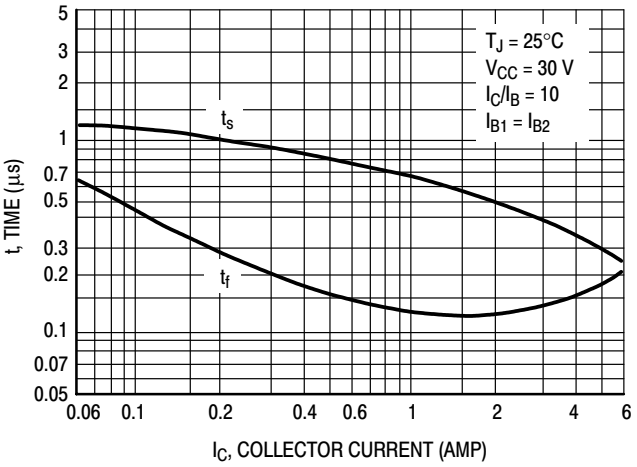


Figure 5. Turn−Off Time

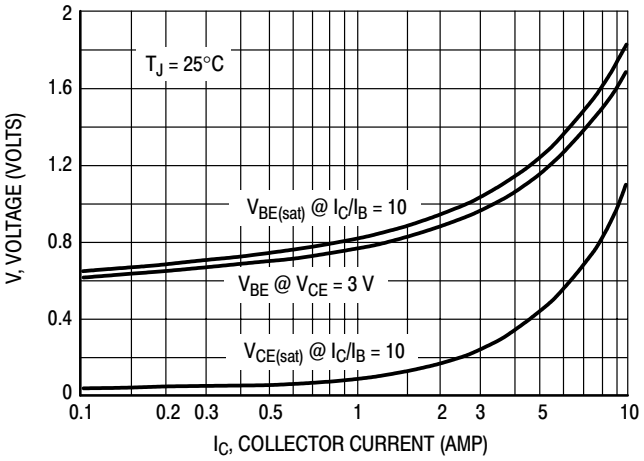


Figure 6. "On" Voltages, MJD2955

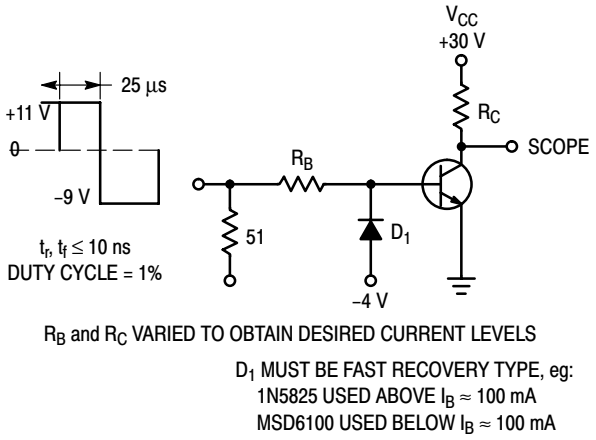


Figure 7. Switching Time Test Circuit

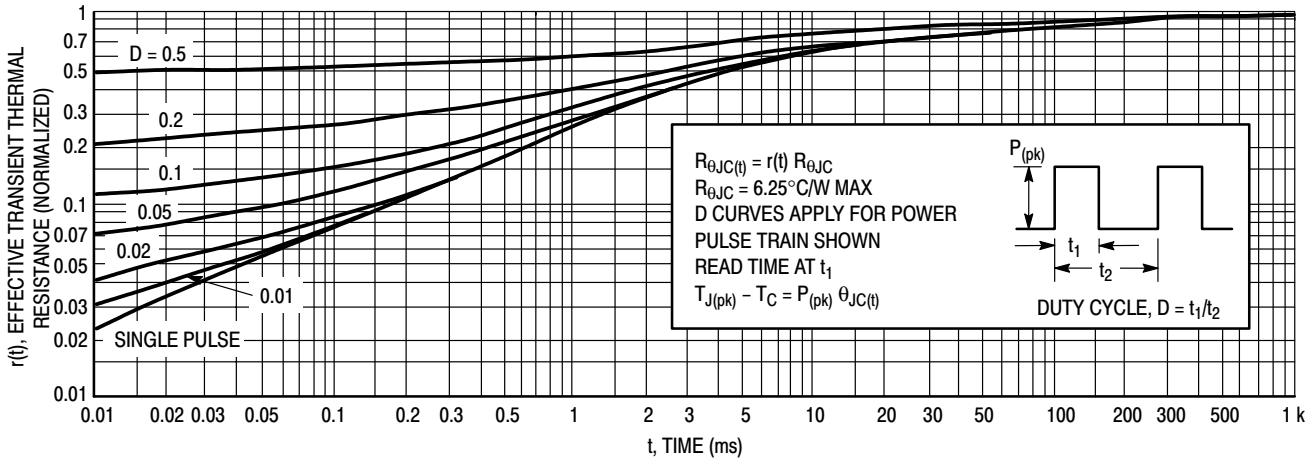


Figure 8. Thermal Response

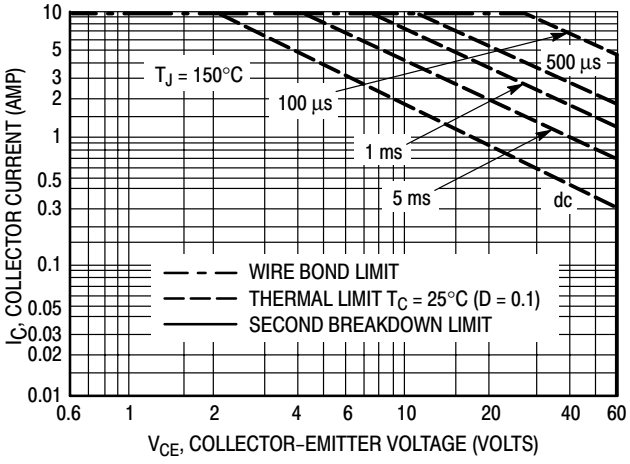


Figure 9. Maximum Forward Bias Safe Operating Area

FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

MJD31C and MJD32C are Preferred Devices

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

ON Semiconductor™

http://onsemi.com

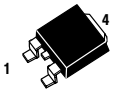
SILICON
POWER TRANSISTORS
3 AMPERES
40 AND 100 VOLTS
15 WATTS

MAXIMUM RATINGS

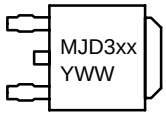
Rating	Symbol	MJD31 MJD32	MJD31C MJD32C	Unit
Collector–Emitter Voltage	V_{CEO}	40	100	Vdc
Collector–Base Voltage	V_{CB}	40	100	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current – Continuous Peak	I_C	3 5		Adc
Base Current	I_B	1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 15 0.12		 Watts W/°C
Total Power Dissipation (Note 1.) @ T_A = 25°C Derate above 25°C	P_D	 1.56 0.012		 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

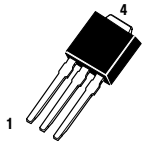
1. These ratings are applicable when surface mounted on the minimum pad size recommended.

MARKING DIAGRAMS

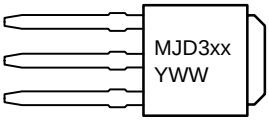


DPAK
CASE 369A
STYLE 1





DPAK
STRAIGHT LEADS
CASE 369
STYLE 1



MJD3xx = Specific Device Code
xx = 1, 1C, 2 or 2C
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 437 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	°C/W
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

2. These ratings are applicable when surface mounted on the minimum pad size recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 3.)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	MJD31, MJD32		40	–	
	MJD31C, MJD32C		100	–	
Collector Cutoff Current		I_{CEO}	–	50	μAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJD31, MJD32				
(V_{CE} = 60 Vdc, I_B = 0)	MJD31C, MJD32C				
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		ICES	–	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	–	1	mAdc
ON CHARACTERISTICS (Note 3.)					
DC Current Gain		h_{FE}			–
(I_C = 1 Adc, V_{CE} = 4 Vdc)			25	–	
(I_C = 3 Adc, V_{CE} = 4 Vdc)			10	50	
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	–	1.2	Vdc
Base–Emitter On Voltage (I_C = 3 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (Note 4.) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3	–	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

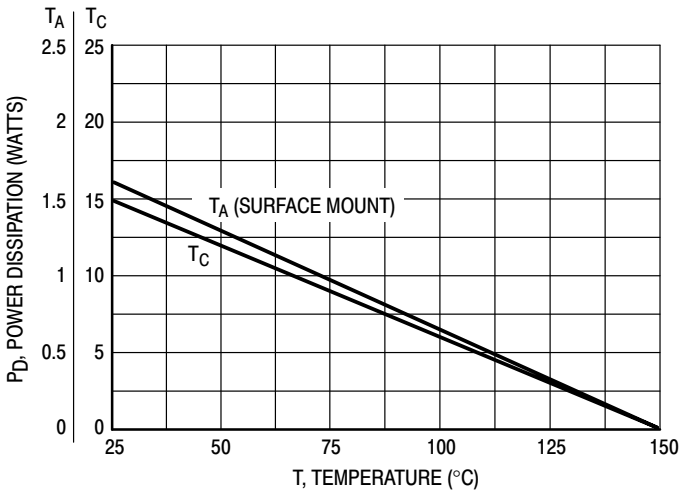
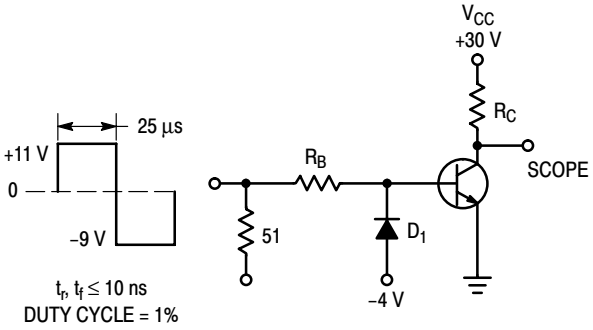


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

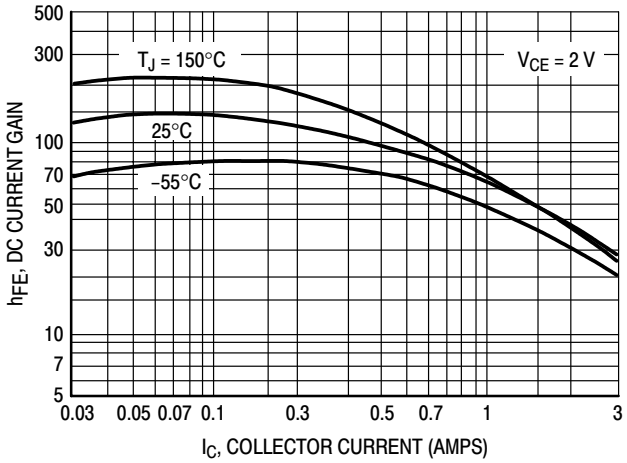


Figure 3. DC Current Gain

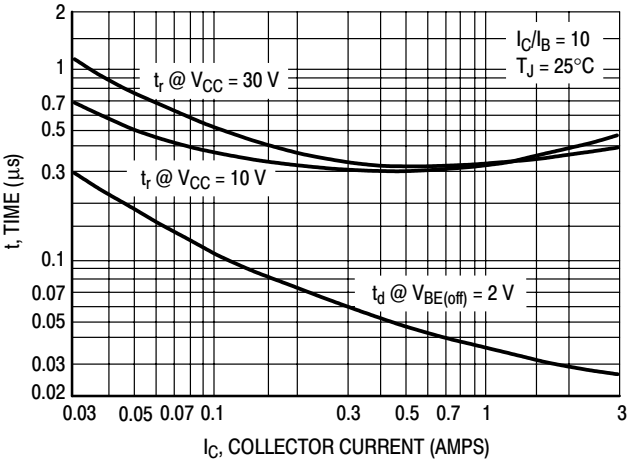


Figure 4. Turn−On Time

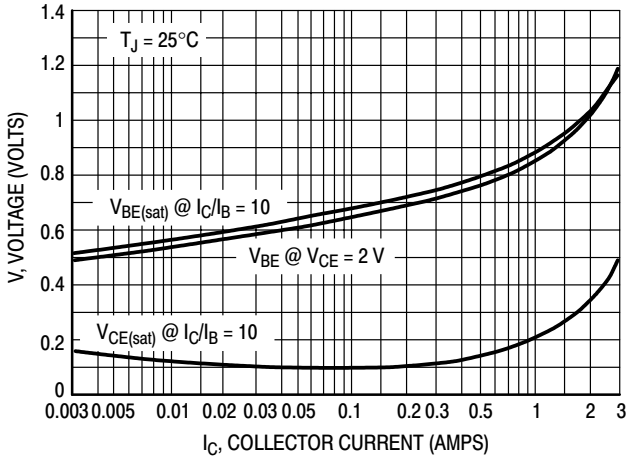


Figure 5. “On” Voltages

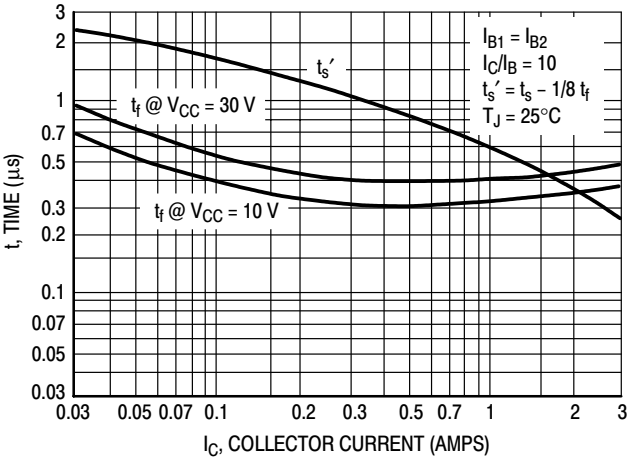


Figure 6. Turn−Off Time

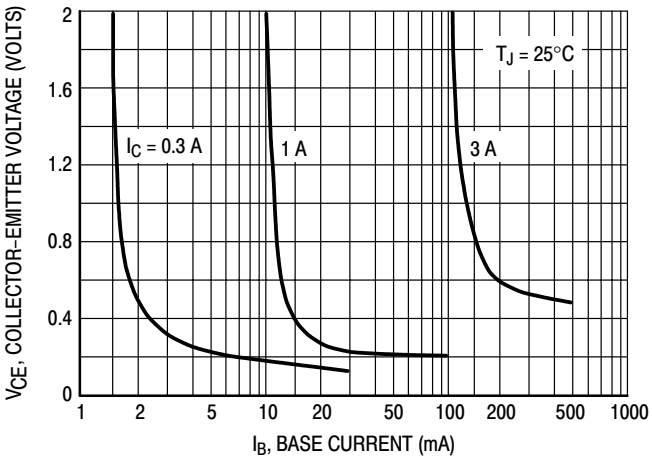


Figure 7. Collector Saturation Region

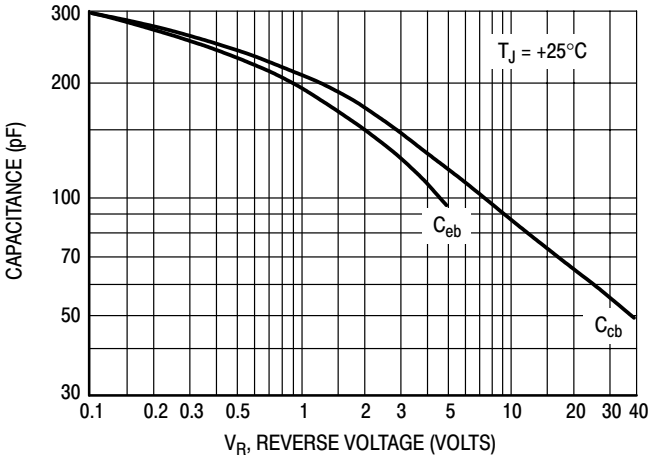


Figure 8. Capacitance

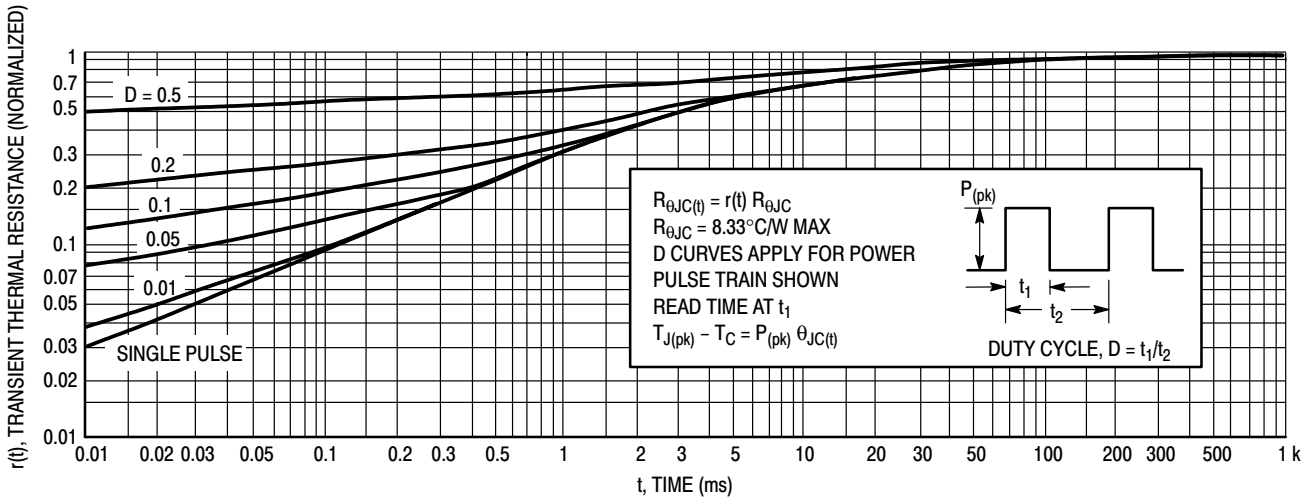


Figure 9. Thermal Response

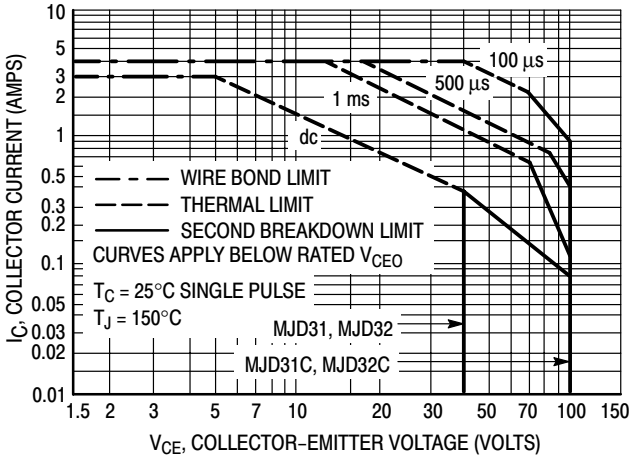
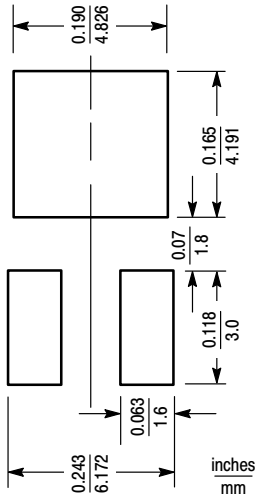


Figure 10. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ORDERING INFORMATION

Device	Package	Shipping
MJD31C	DPAK	75 Units / Rail
MJD31CRL	DPAK	1800 Tape & Reel
MJD31CT4	DPAK	2500 Tape & Reel
MJD31C–1	DPAK Straight Leads	75 Units / Rail
MJD31T4	DPAK	2500 Tape & Reel
MJD32C	DPAK	75 Units / Rail
MJD32CRL	DPAK	1800 Tape & Reel
MJD32CT4	DPAK	2500 Tape & Reel
MJD32C–1	DPAK Straight Leads	75 Units / Rail
MJD32RL	DPAK	1800 Tape & Reel
MJD32T4	DPAK	2500 Tape & Reel

High Voltage Power Transistors
DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

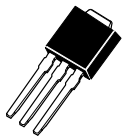
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) — $V_{CEO(sus)}$
- 0.5 A Rated Collector Current

NPN
MJD340*
PNP
MJD350*

*ON Semiconductor Preferred Device

SILICON
POWER TRANSISTORS
0.5 AMPERE
300 VOLTS
15 WATTS

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Collector–Base Voltage	V_{CB}	300	Vdc
Emitter–Base Voltage	V_{EB}	3	Vdc
Collector Current — Continuous — Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

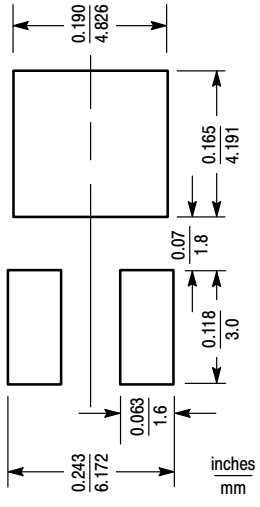
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 1 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

*When surface mounted on minimum pad sizes recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

TYPICAL CHARACTERISTICS

MJD340

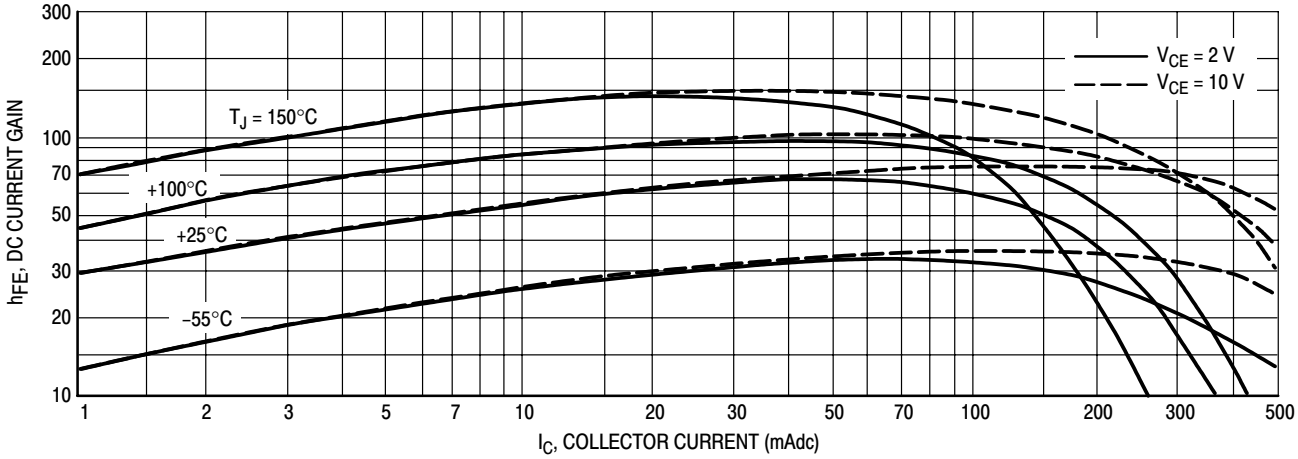


Figure 1. DC Current Gain

MJD340

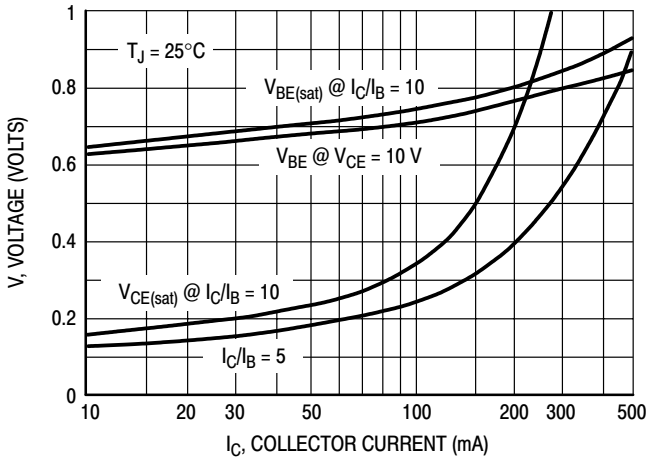


Figure 2. “On” Voltages

MJD350

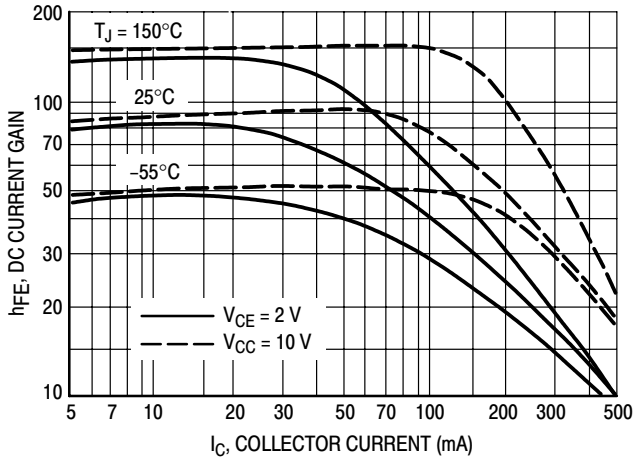


Figure 3. DC Current Gain

MJD350

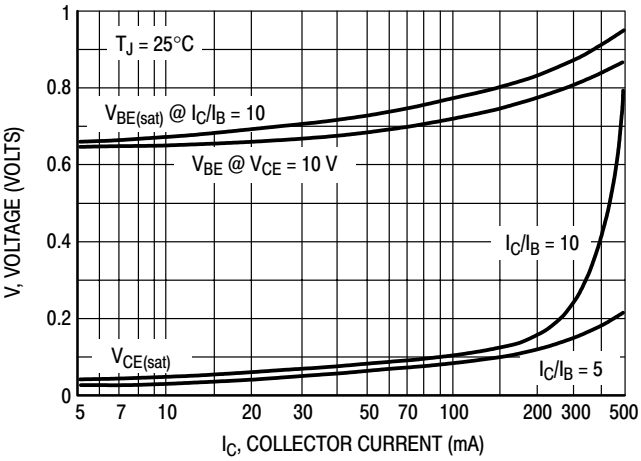


Figure 4. “On” Voltages

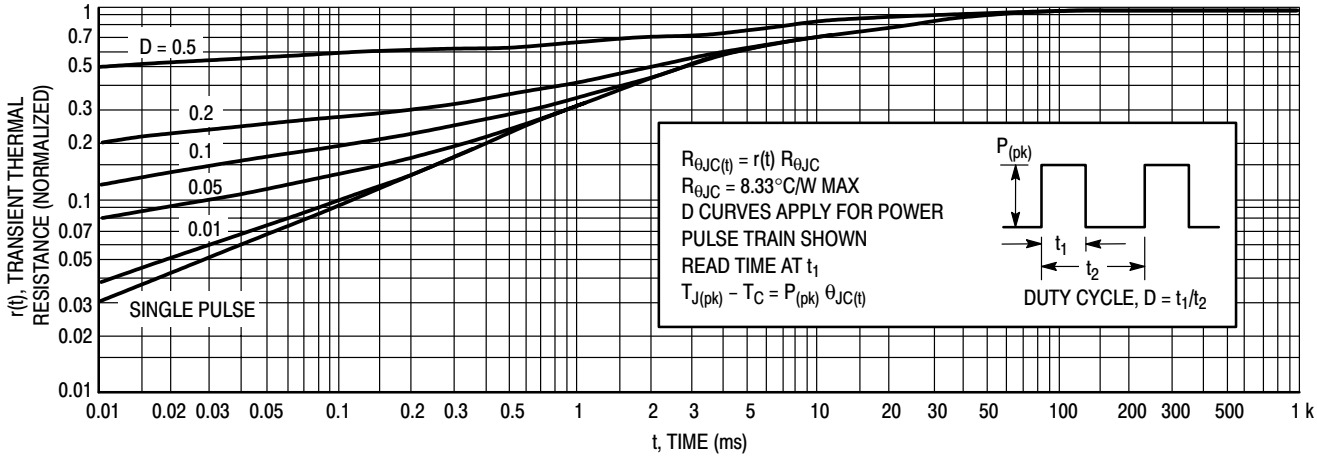


Figure 5. Thermal Response

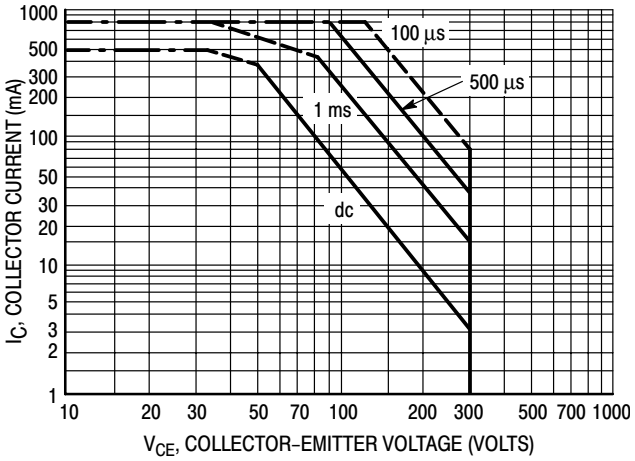


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

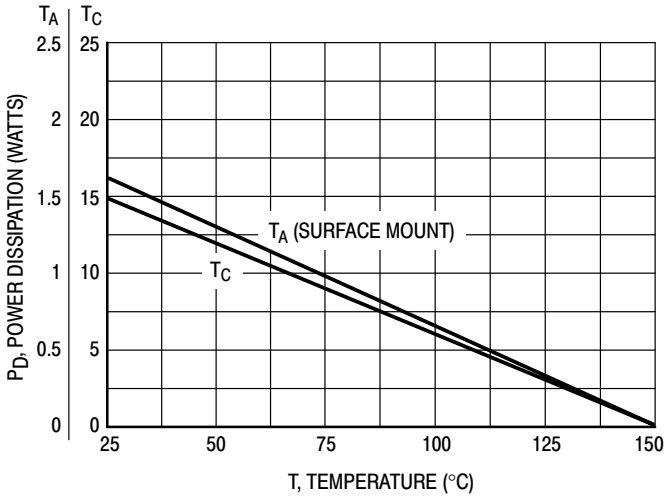


Figure 7. Power Derating

Complementary Power Transistors

DPAK For Surface Mount Applications

NPN
MJD41C*
PNP
MJD42C*

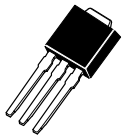
*ON Semiconductor Preferred Device

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built–in Base–Emitter Resistors

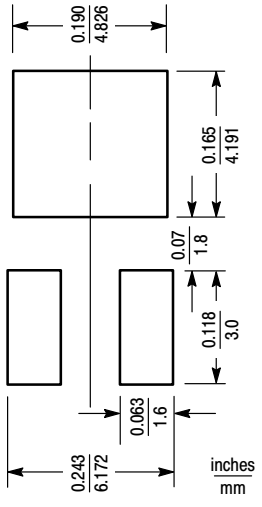
SILICON POWER TRANSISTORS 6 AMPERES 100 VOLTS 20 WATTS

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD41C MJD42C	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	6 10	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

*These ratings are applicable when surface mounted on the minimum pad size recommended.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)	h_{FE}	 30 15	 — 75	—
Collector–Emitter Saturation Voltage (I_C = 6 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

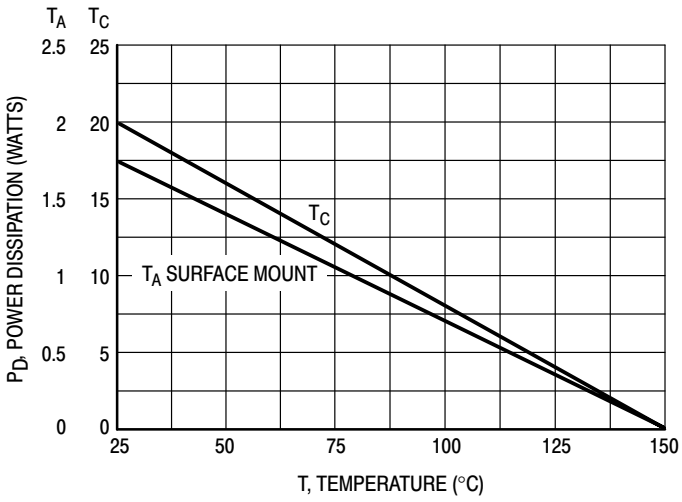
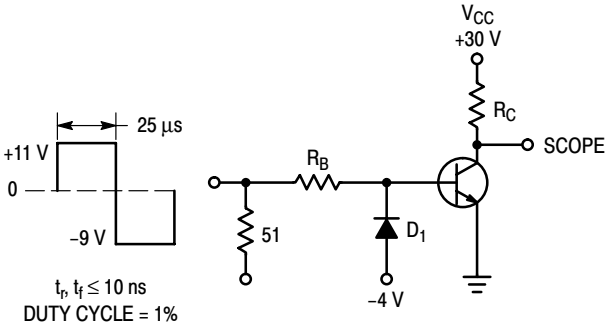


Figure 8. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
MSB5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
REVERSE ALL POLARITIES FOR PNP.

Figure 9. Switching Time Test Circuit

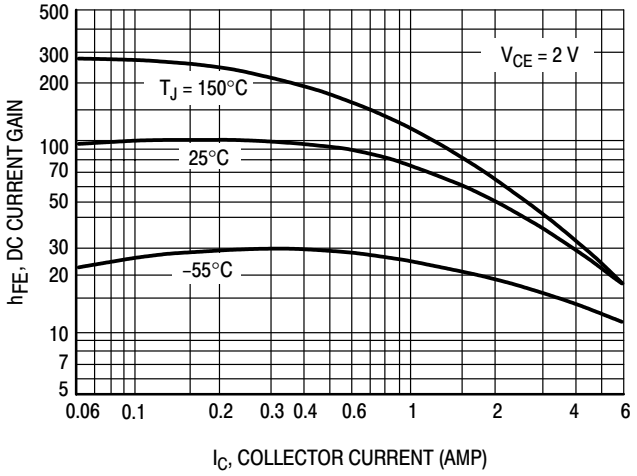


Figure 10. DC Current Gain

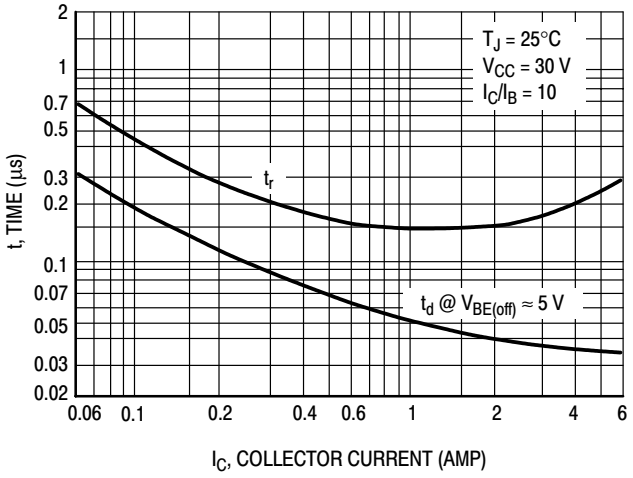


Figure 11. Turn−On Time

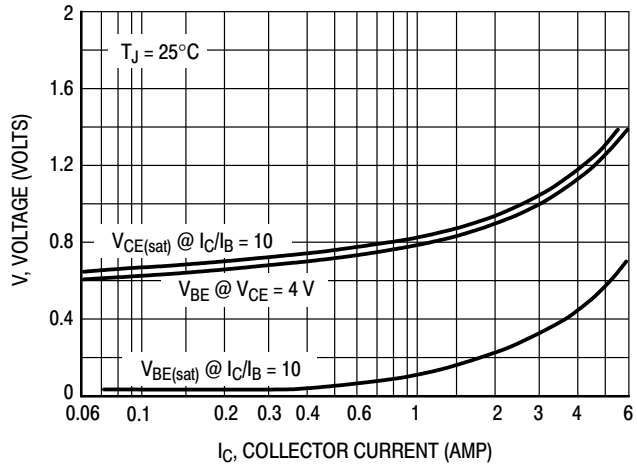


Figure 12. “On” Voltages

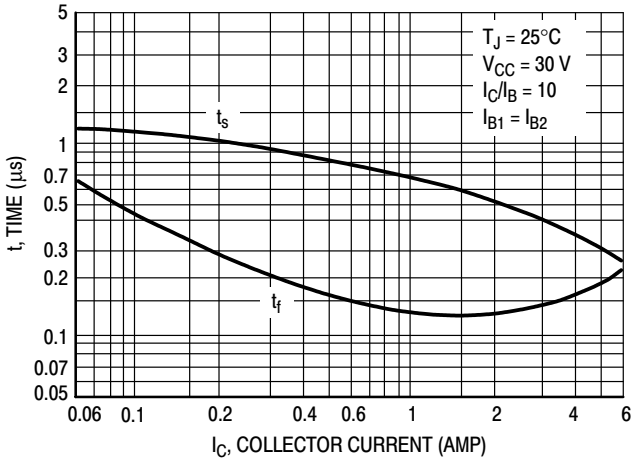


Figure 13. Turn−Off Time

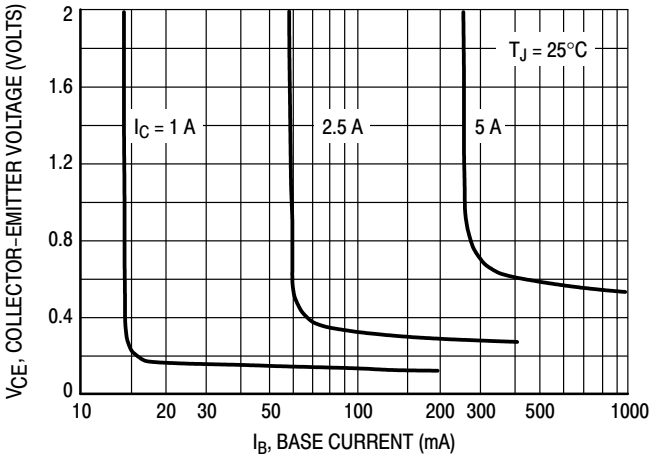


Figure 14. Collector Saturation Region

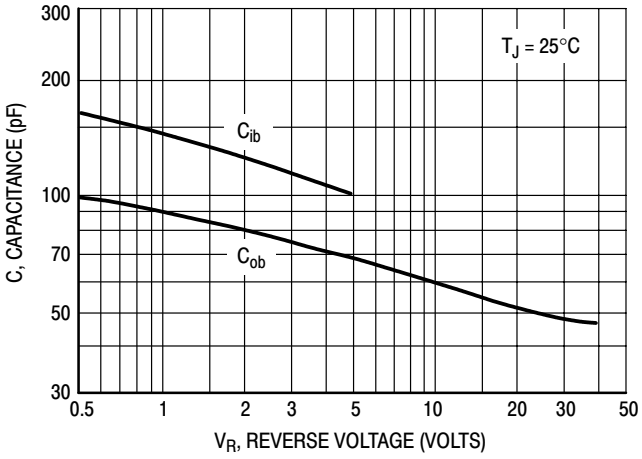


Figure 15. Capacitance

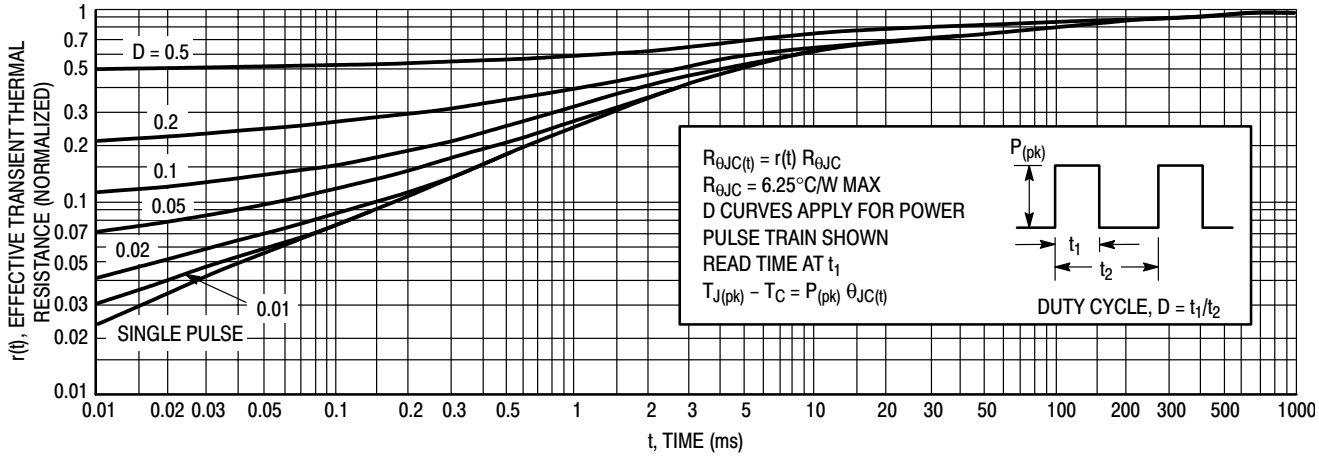


Figure 16. Thermal Response

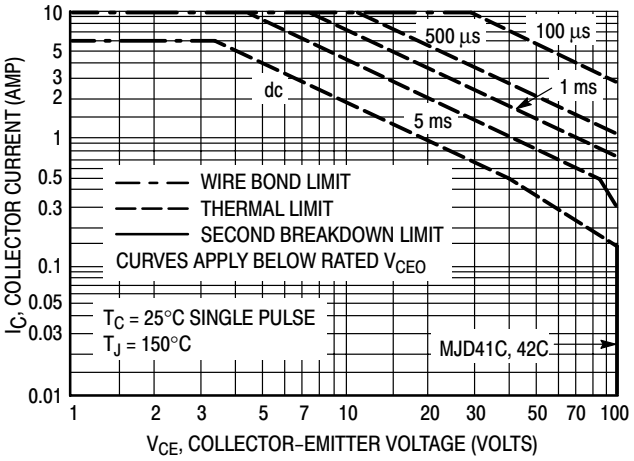


Figure 17. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 17 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD44E3*

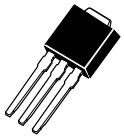
*ON Semiconductor Preferred Device

Darlington Power Transistor
DPAK For Surface Mount Application

. . . for general purpose power and switching output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount ("T4" Suffix)
- Electrically Similar to Popular D44E3 Device
- High DC Gain — 1000 Min @ 5.0 Adc
- Low Sat. Voltage — 1.5 V @ 5.0 Adc
- Compatible With Existing Automatic Pick & Place Equipment

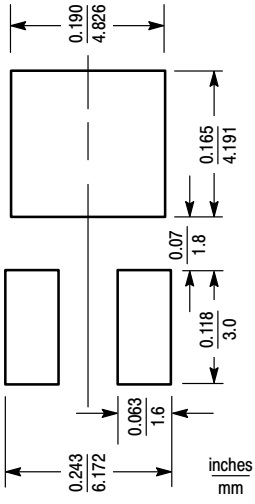
NPN DARLINGTON SILICON POWER TRANSISTOR 10 AMPERES 80 VOLTS 20 WATTS



CASE 369–07

CASE 369A–13

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 20 0.16	 Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	 1.75 0.014	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 7 Vdc)	I_{EBO}	—	—	1	μA
ON CHARACTERISTICS					
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 10 mAdc) (I_C = 10 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	 — —	 — —	 1.5 2	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	—	2.5	Vdc
DC Current Gain (V_{CE} = 5 Vdc, I_C = 5 Adc)	h_{FE}	1000	—	—	—
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	C_{cb}	—	—	130	pF
SWITCHING TIMES					
Delay and Rise Times (I_C = 10 Adc, I_{B1} = 20 mAdc)	$t_d + t_r$	—	0.6	—	μs
Storage Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_s	—	2	—	μs
Fall Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_f	—	0.5	—	μs

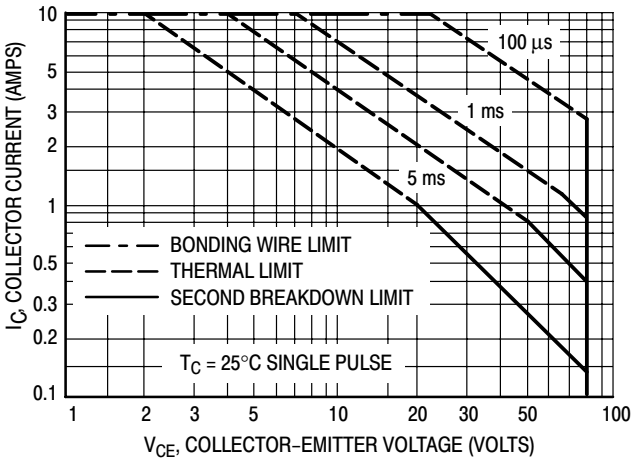


Figure 1. Maximum Forward Bias Safe Operating Area

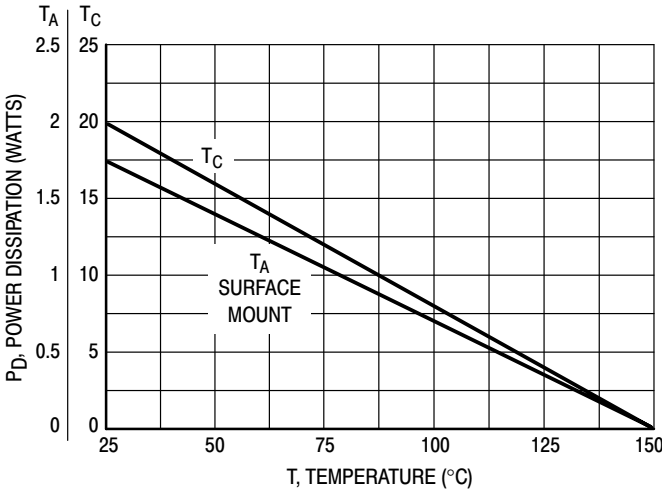


Figure 2. Power Derating

Complementary Power Transistors

DPAK For Surface Mount Applications

NPN
MJD44H11*
PNP
MJD45H11*

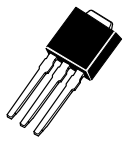
*ON Semiconductor Preferred Device

. . . for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount ("T4" Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Volt Max @ 8.0 Amperes
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

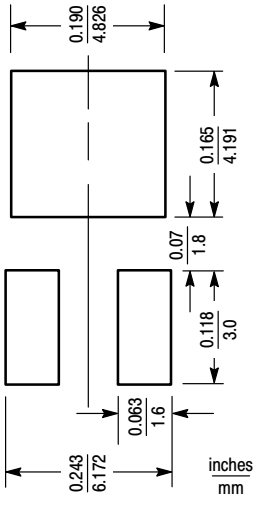
SILICON POWER TRANSISTORS 8 AMPERES 80 VOLTS 20 WATTS

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	D44H11 or D45H11	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 20 0.16	 Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	 1.75 0.014	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	—	—	50	μA
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	—	—	—
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	—	—	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJD44H11 MJD45H11	C_{cb}	— —	130 230	— —	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJD44H11 MJD45H11	f_T	— —	50 40	— —	MHz
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJD44H11 MJD45H11	$t_d + t_r$	— —	300 135	— —	ns
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t_s	— —	500 500	— —	ns
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t_f	— —	140 100	— —	ns

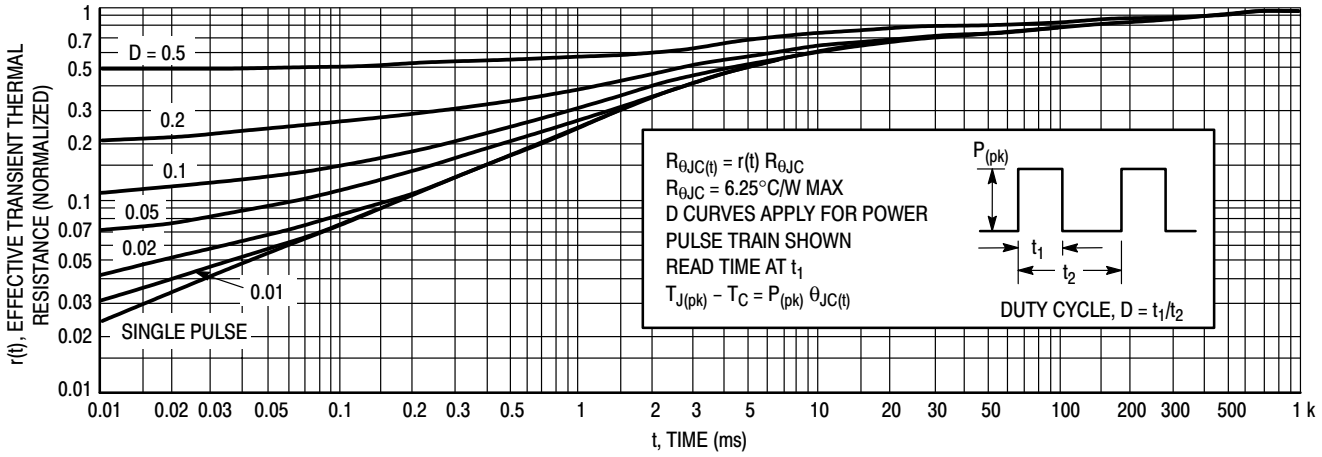


Figure 1. Thermal Response

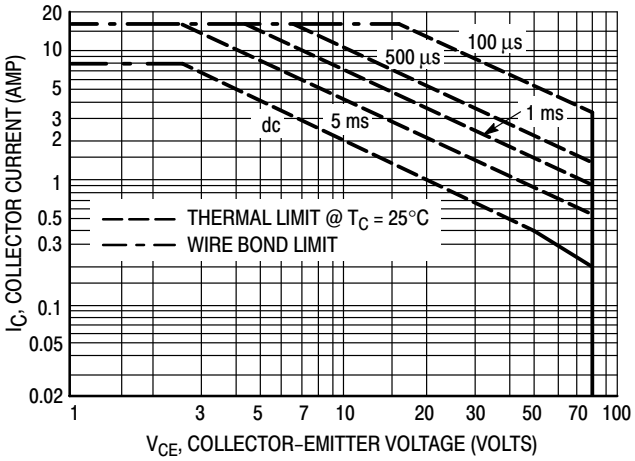


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

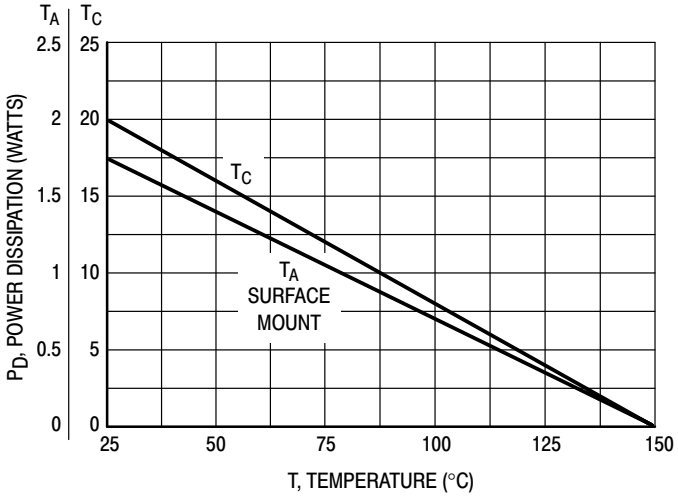


Figure 3. Power Derating

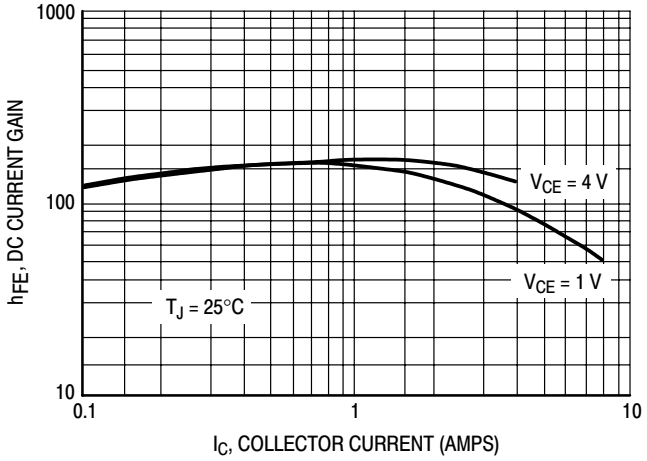


Figure 4. MJD44H11 DC Current Gain

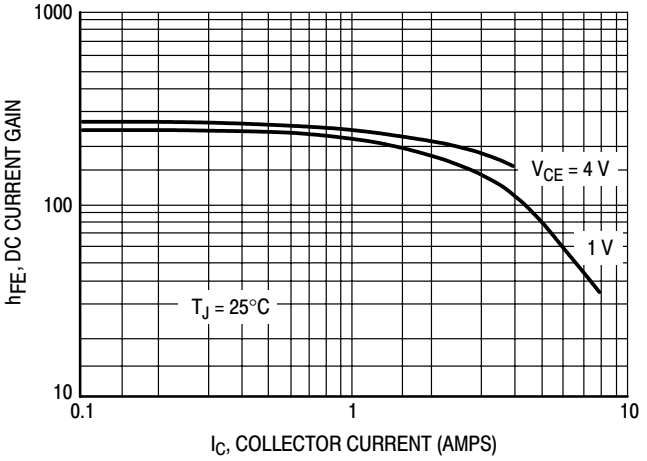


Figure 5. MJD45H11 DC Current Gain

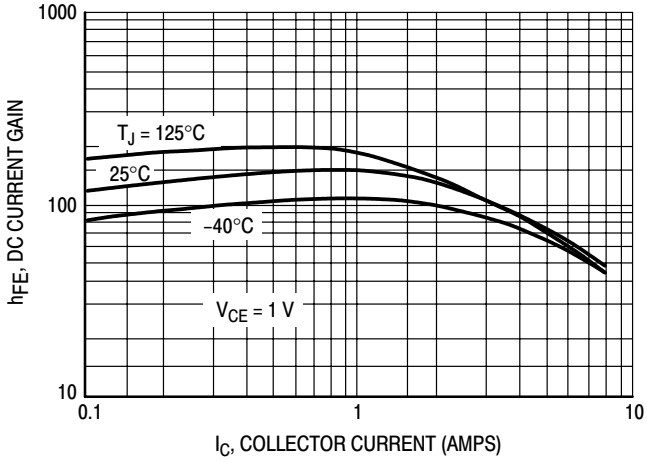


Figure 6. MJD44H11 Current Gain versus Temperature

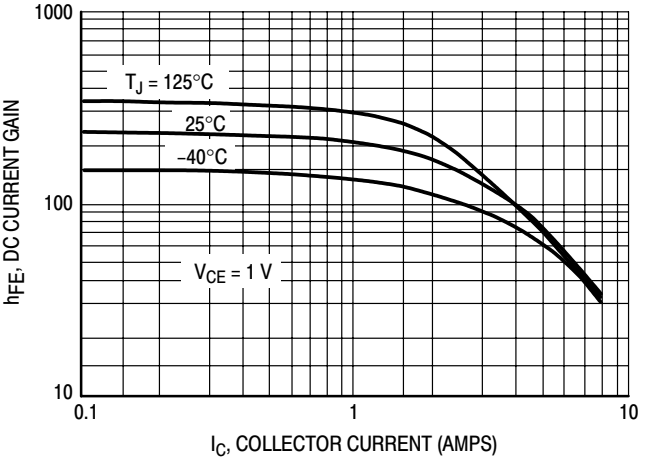


Figure 7. MJD45H11 Current Gain versus Temperature

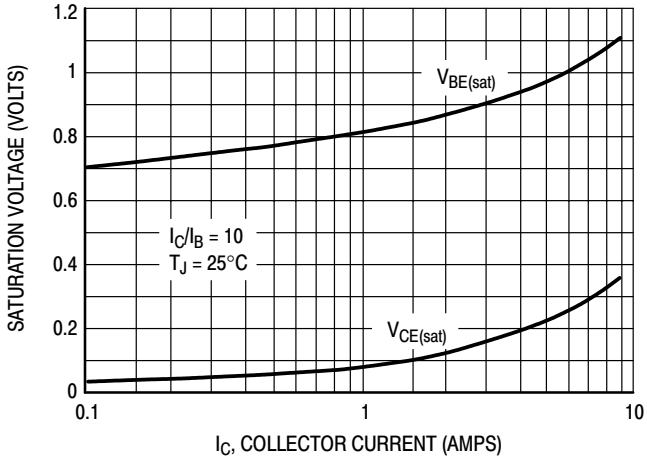


Figure 8. MJD44H11 On−Voltages

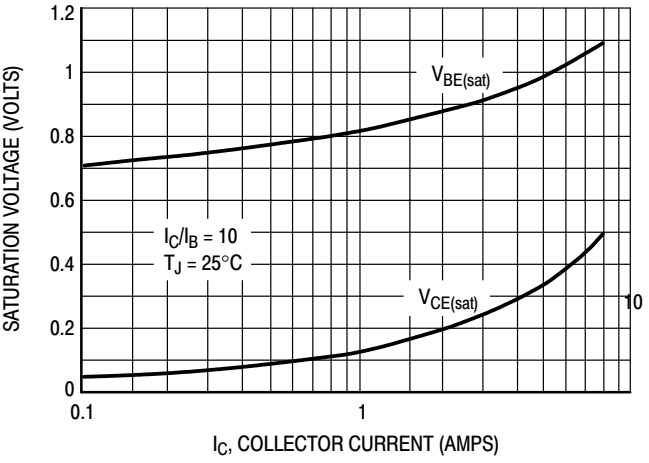


Figure 9. MJD45H11 On−Voltages

High Voltage Power Transistors
DPAK For Surface Mount Applications

MJD47*
MJD50*

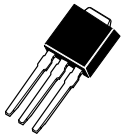
*ON Semiconductor Preferred Device

NPN SILICON
POWER TRANSISTORS
1 AMPERE
250, 400 VOLTS
15 WATTS

Designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

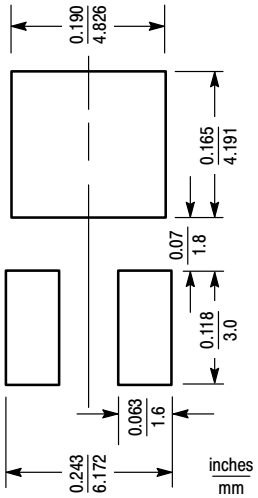
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD47	MJD50	Unit
Collector–Emitter Voltage	V_{CEO}	250	400	Vdc
Collector–Base Voltage	V_{CB}	350	500	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	1 2		Adc
Base Current	I_B	0.6		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.0125		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJD47 MJD50	$V_{CEO(sus)}$	250 400	— —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJD47 MJD50	I_{CEO}	 — —	 0.2 0.2	mAdc

*When surface mounted on minimum pad sizes recommended. (continued)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
MJD47/D

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	 MJD47 MJD50	I_{CES}	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 —	—
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2 MHz)		f_T	10	—	MHz
Small–Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

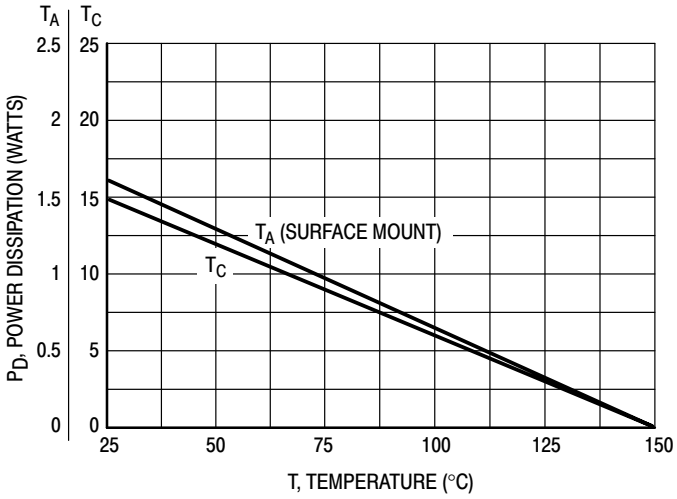


Figure 1. Power Derating

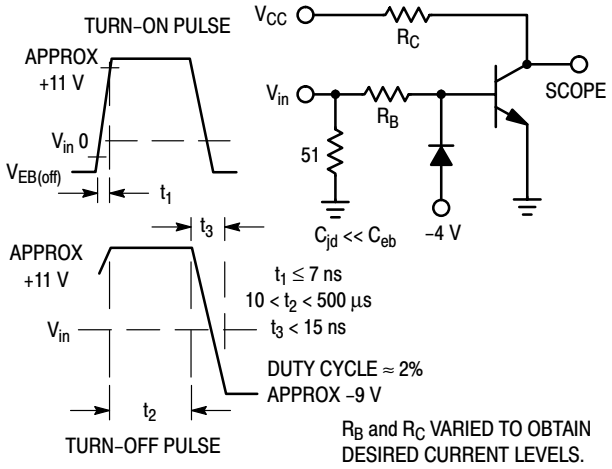


Figure 2. Switching Time Equivalent Circuit

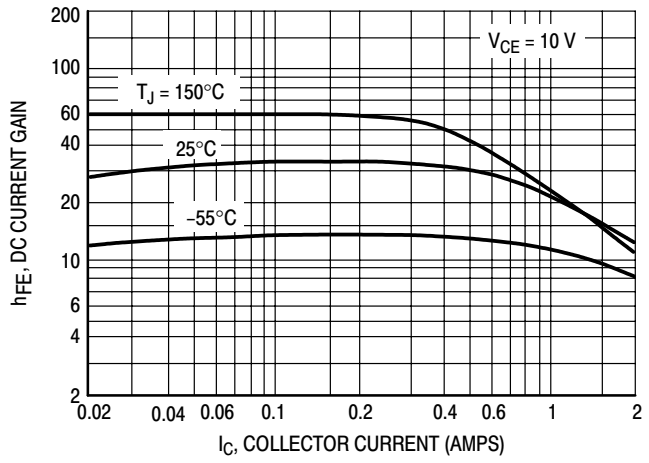


Figure 3. DC Current Gain

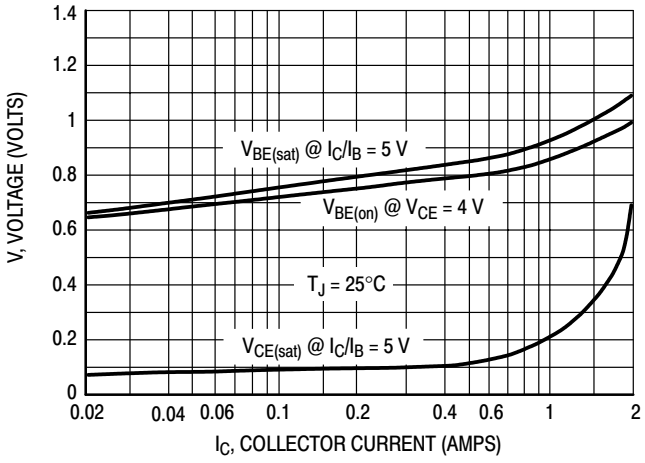


Figure 4. “On” Voltages

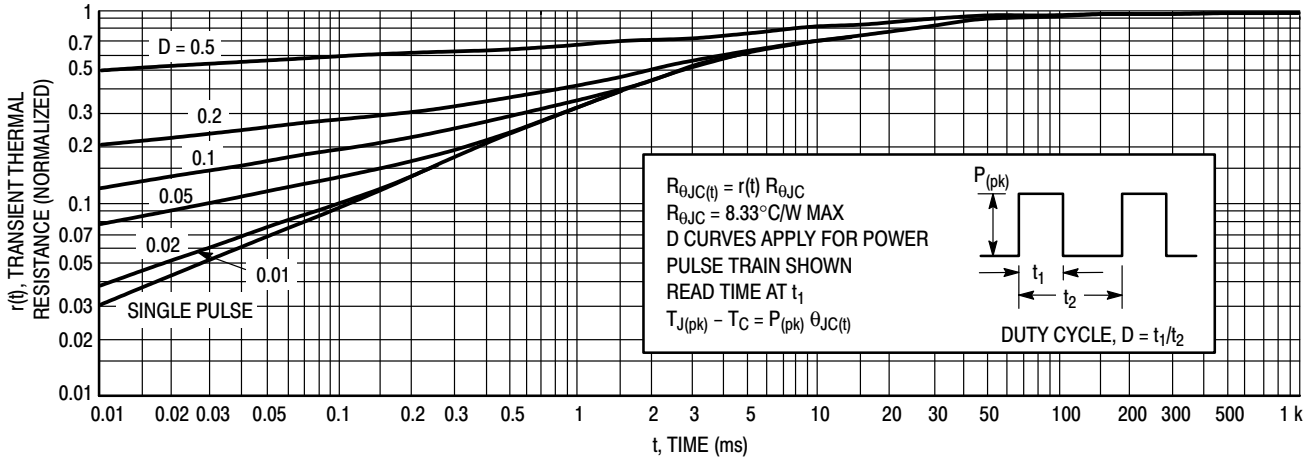


Figure 5. Thermal Response

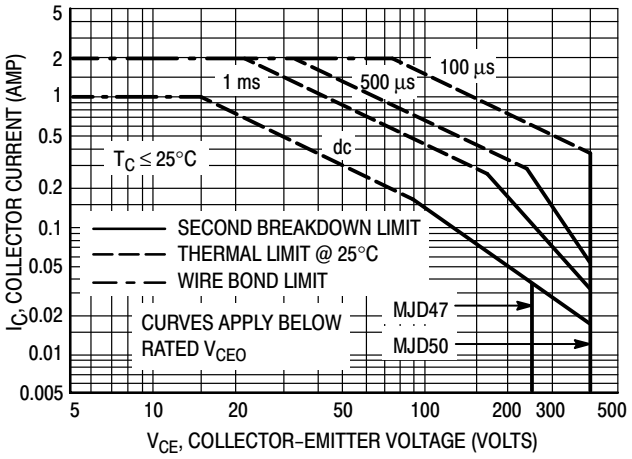


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

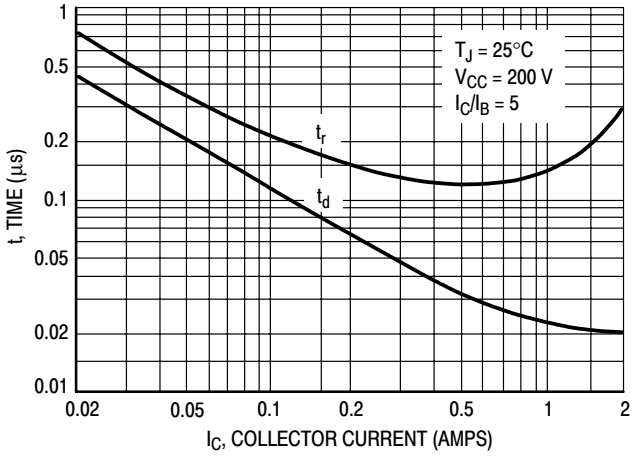


Figure 7. Turn−On Time

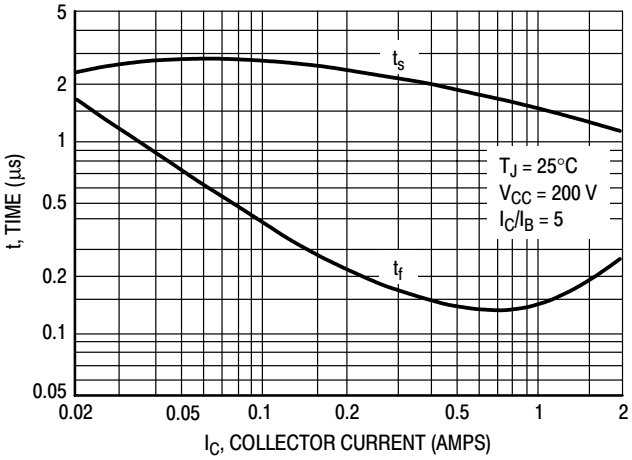


Figure 8. Turn-Off Time

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

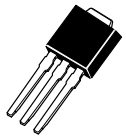
NPN
MJD6036
PNP
MJD6039

SILICON
POWER TRANSISTORS
4 AMPERES
80 VOLTS
20 WATTS

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Available on 16 mm Tape and Reel for Automatic Handling ("T4" Suffix)
- Surface Mount Replacements for 2N6034–2N6039 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Complementary Pairs Simplifies Designs

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

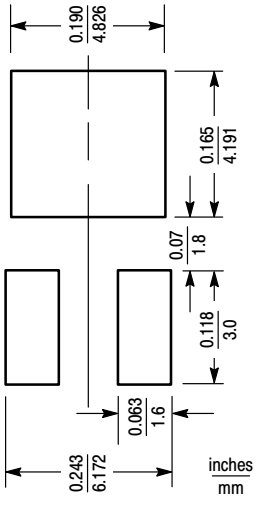
Rating	Symbol	MJD6036 MJD6039	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CB}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	100	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)		$V_{CEO(sus)}$	80	—	Vdc
Collector–Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)		I_{CEO}	—	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc) (I_C = 2 Adc, V_{CE} = 4 Vdc)		h_{FE}	 1000 500	 — —	—
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc)		$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 2 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	25	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJD6036 MJD6039	C_{ob}	 —	 200 100	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

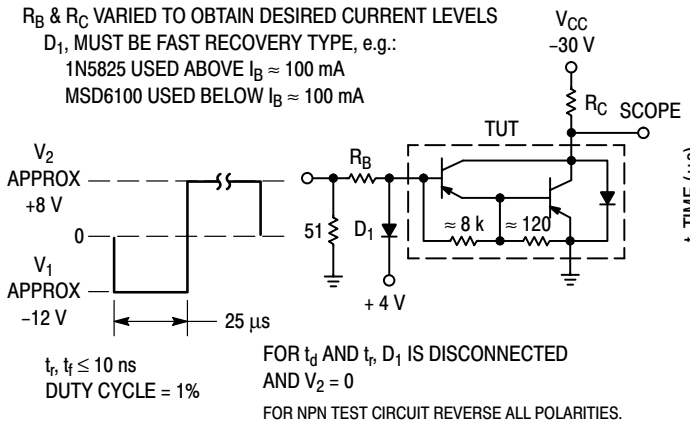


Figure 9. Switching Times Test Circuit

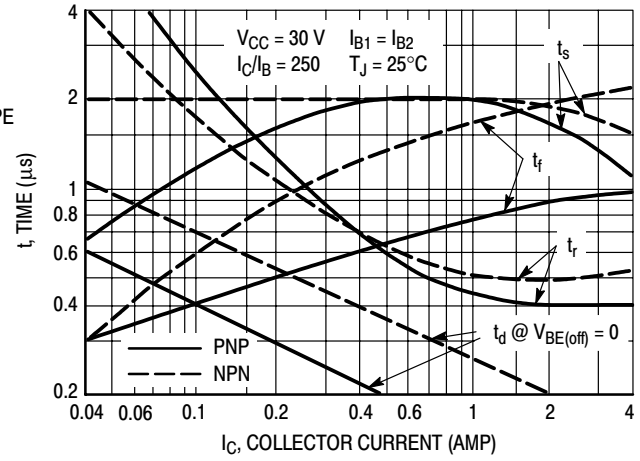


Figure 10. Switching Times

TYPICAL ELECTRICAL CHARACTERISTICS

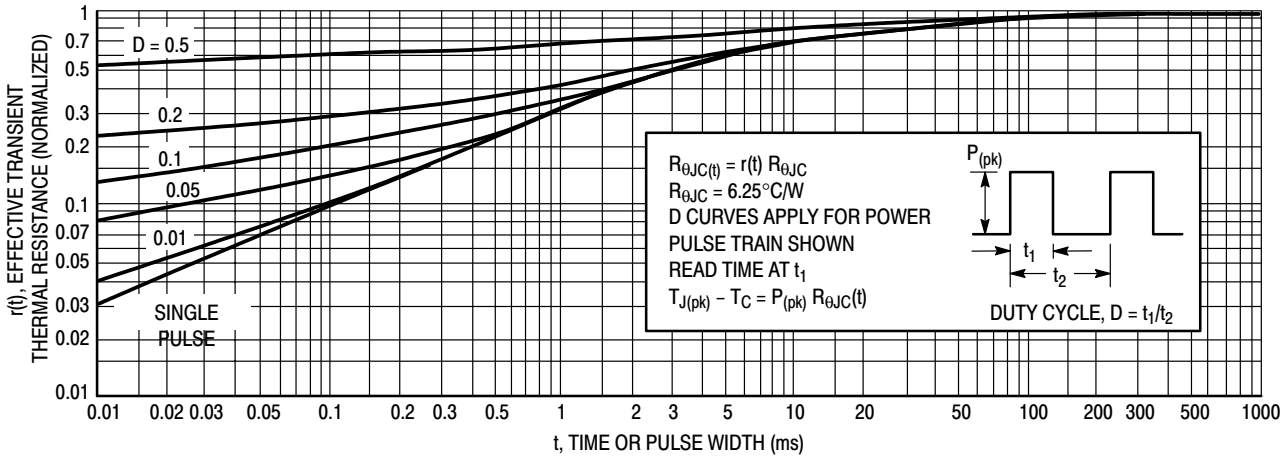


Figure 11. Thermal Response

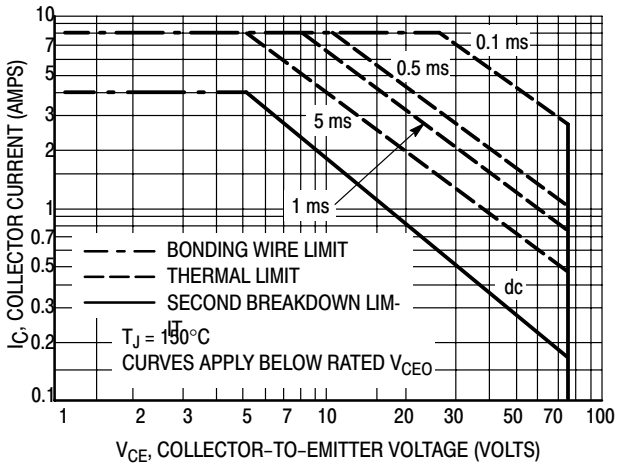


Figure 12. Maximum Rated Forward Biased Safe Operating Area

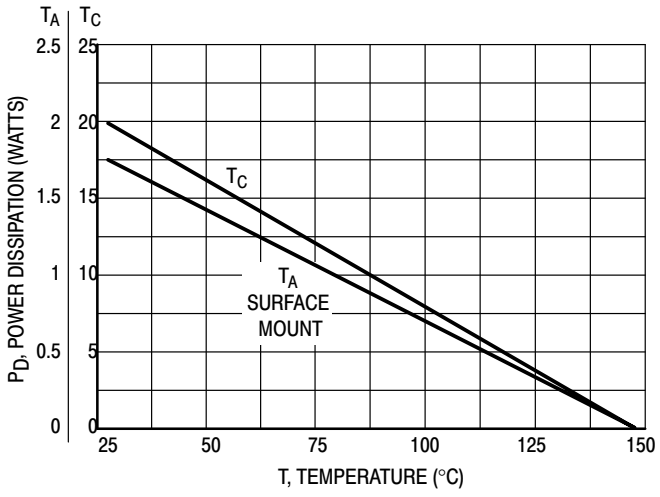


Figure 13. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14 and 15 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

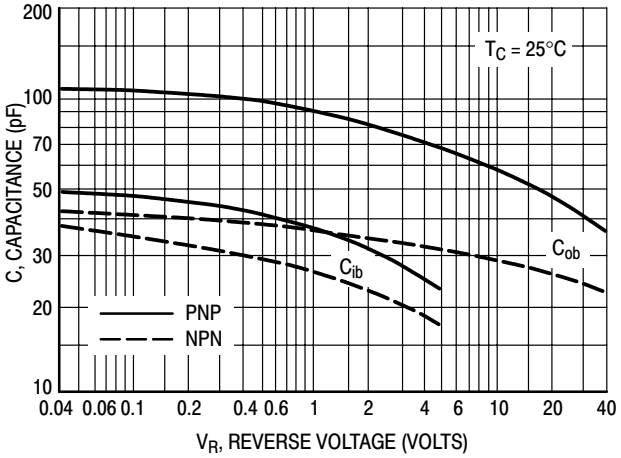


Figure 14. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD6036 **NPN MJD6039**

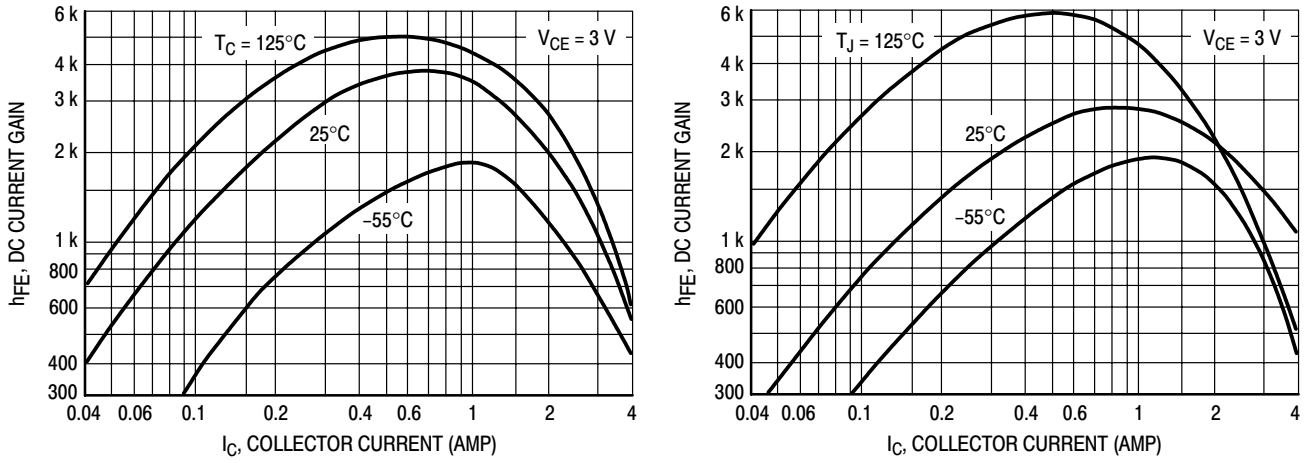


Figure 15. DC Current Gain

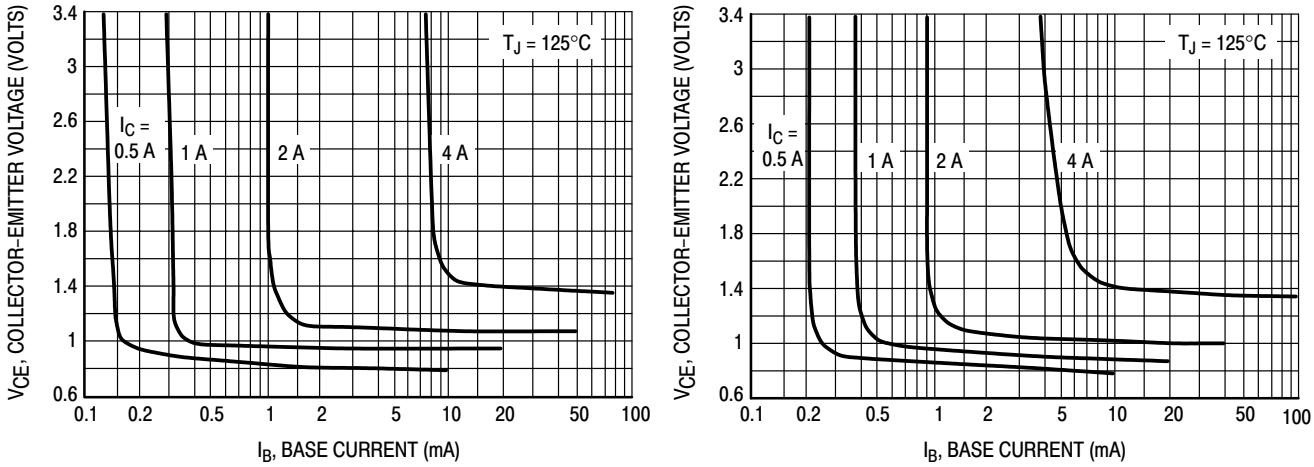


Figure 16. Collector Saturation Region

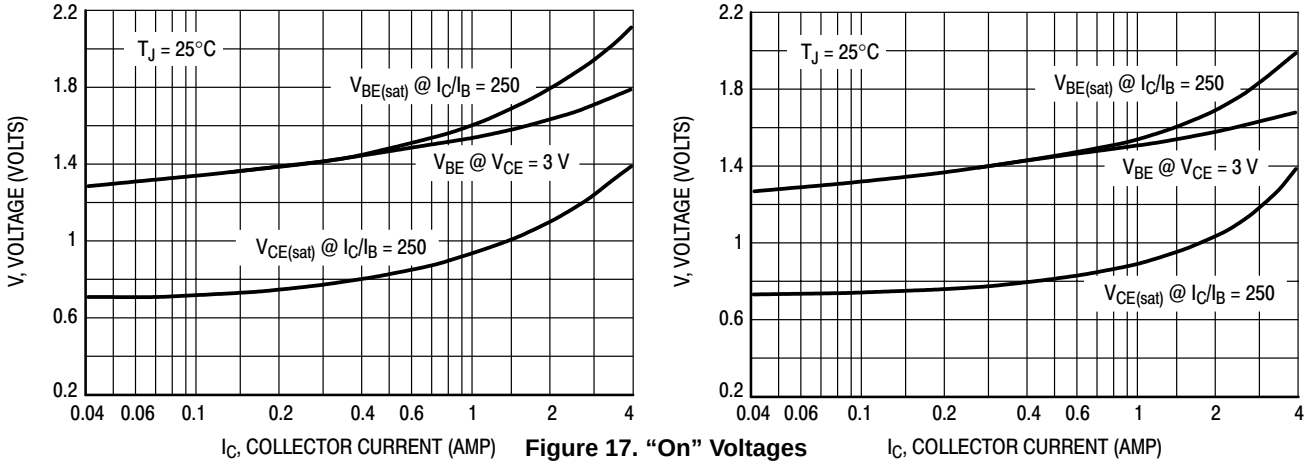


Figure 17. “On” Voltages

PNP MJD6036 **NPN MJD6039**

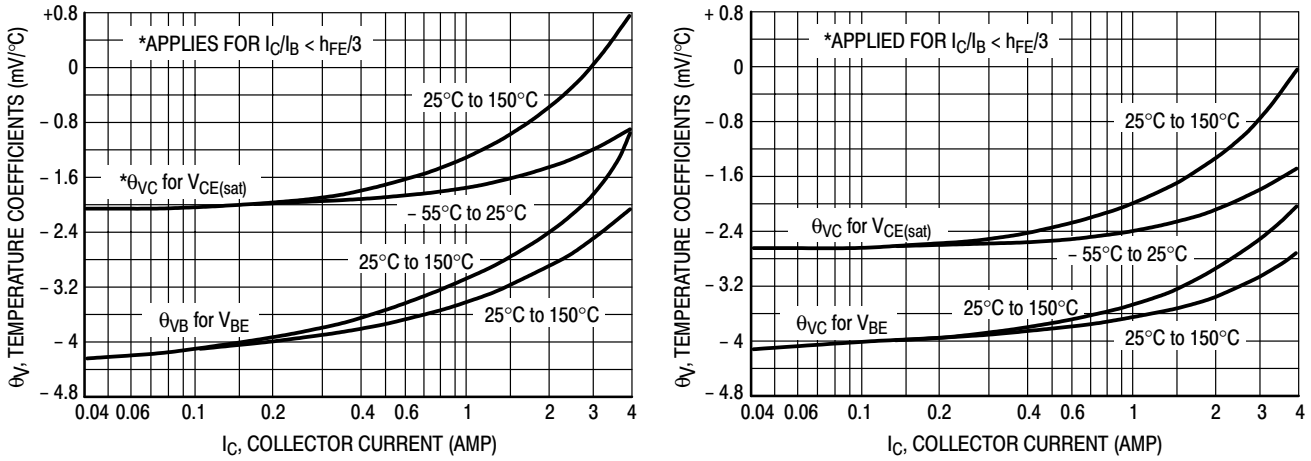


Figure 18. Temperature Coefficients

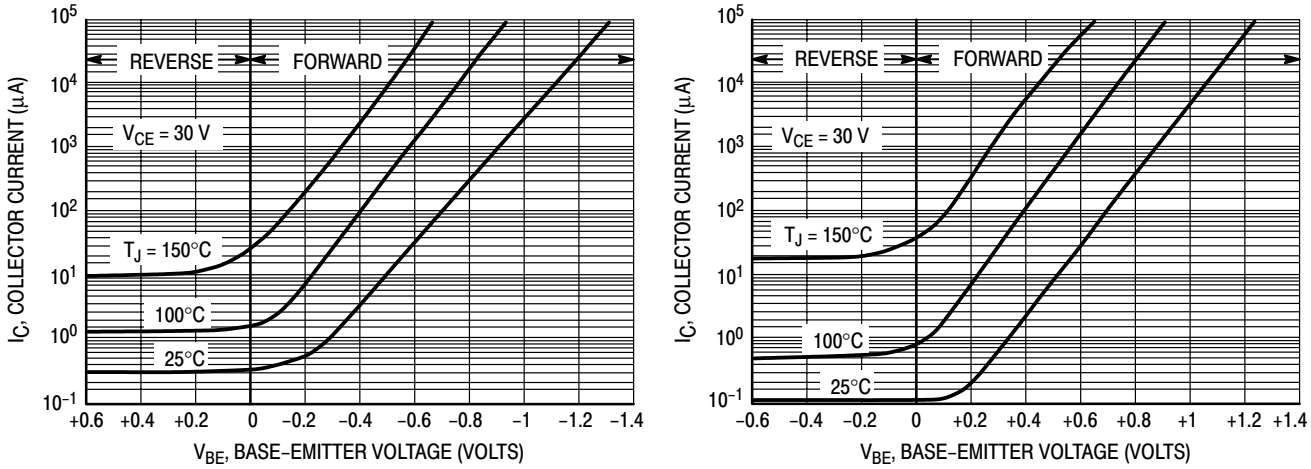


Figure 19. Collector Cut–Off Region

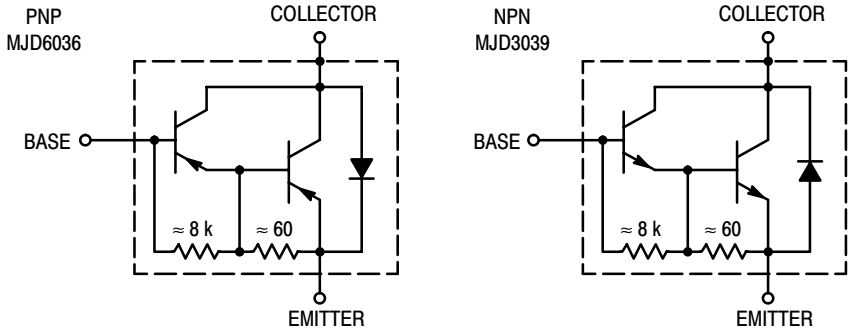


Figure 20. Darlington Schematic

MJE13003

SWITCHMODE™ Series NPN Silicon Power Transistor

These devices are designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C
  t_c @ 1 A, 100°C is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous – Peak (Note 1.)	I_C I_{CM}	1.5 3	Adc
Base Current – Continuous – Peak (Note 1.)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current – Continuous – Peak (Note 1.)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.4 11.2	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

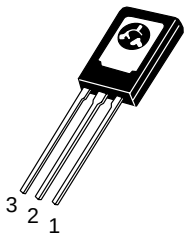
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	°C/W
Maximum Load Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ON Semiconductor™

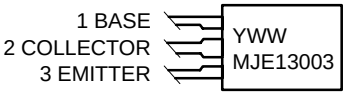
http://onsemi.com

1.5 AMPERES
NPN SILICON POWER TRANSISTORS
300 AND 400 VOLTS
40 WATTS



TO–225
CASE 77
STYLE 3

MARKING DIAGRAM



Y = Year
WW = Work Week
MJE13003 = Device Code

ORDERING INFORMATION

Device	Package	Shipping
MJE13003	TO–225	500 Units/Box

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 5..)						
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with bass forward biased		$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 12			
ON CHARACTERISTICS (Note 5..)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc) (I_C = 1 Adc, V_{CE} = 2 Vdc)		h_{FE}	8 5	– –	40 25	–
Collector–Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1.5 Adc, I_B = 0.5 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – – –	– – – –	0.5 1 3 1	Vdc
Base–Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{BE(sat)}$	– – –	– – –	1 1.2 1.1	Vdc
DYNAMIC CHARACTERISTICS						
Current–Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	21	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.05	0.1	μs
Rise Time		t_r	–	0.5	1	μs
Storage Time		t_s	–	2	4	μs
Fall Time		t_f	–	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	(I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.7	4	μs
Crossover Time		t_c	–	0.29	0.75	μs
Fall Time		t_{fi}	–	0.15	–	μs

5. Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

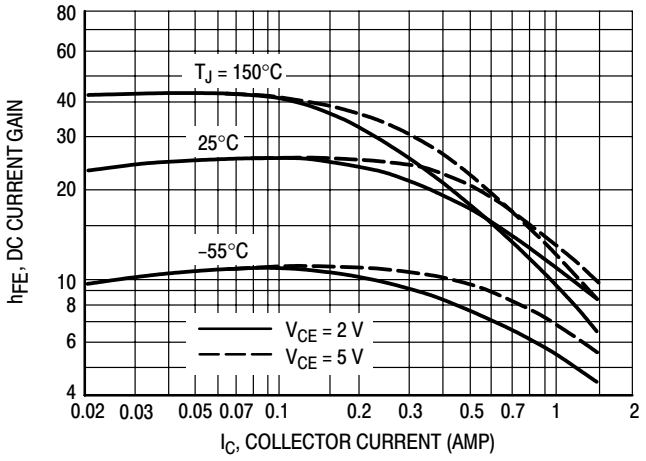


Figure 1. DC Current Gain

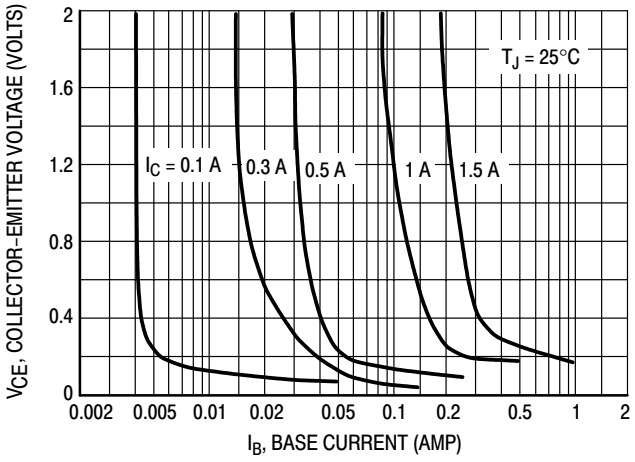


Figure 2. Collector Saturation Region

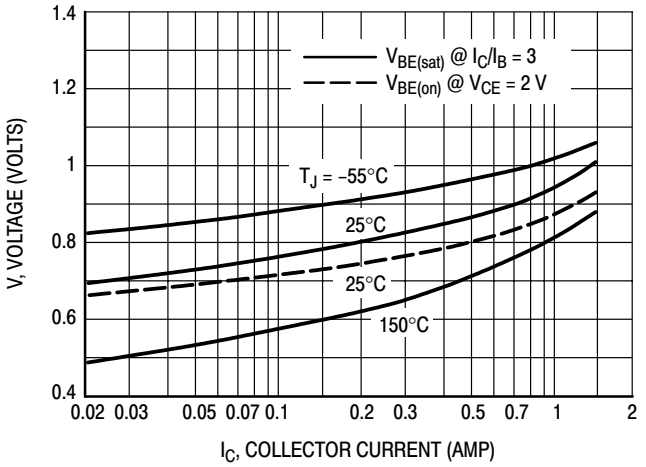


Figure 3. Base−Emitter Voltage

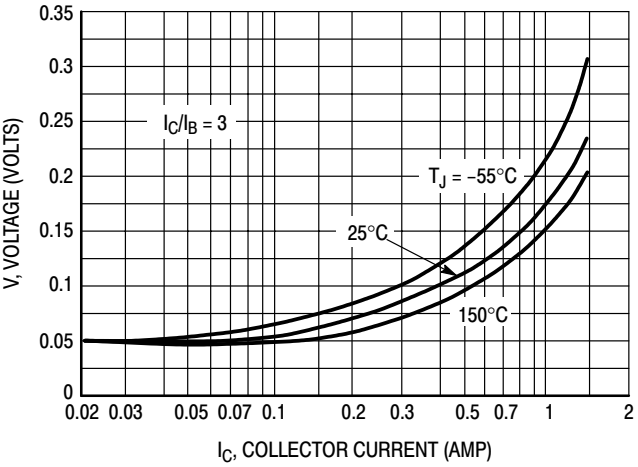


Figure 4. Collector−Emitter Saturation Region

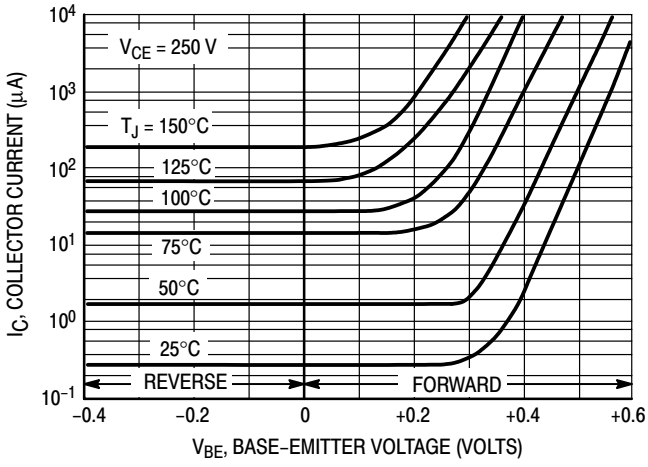


Figure 5. Collector Cutoff Region

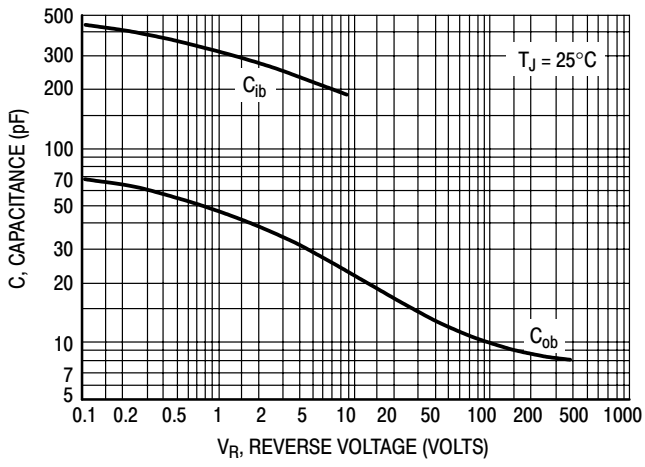
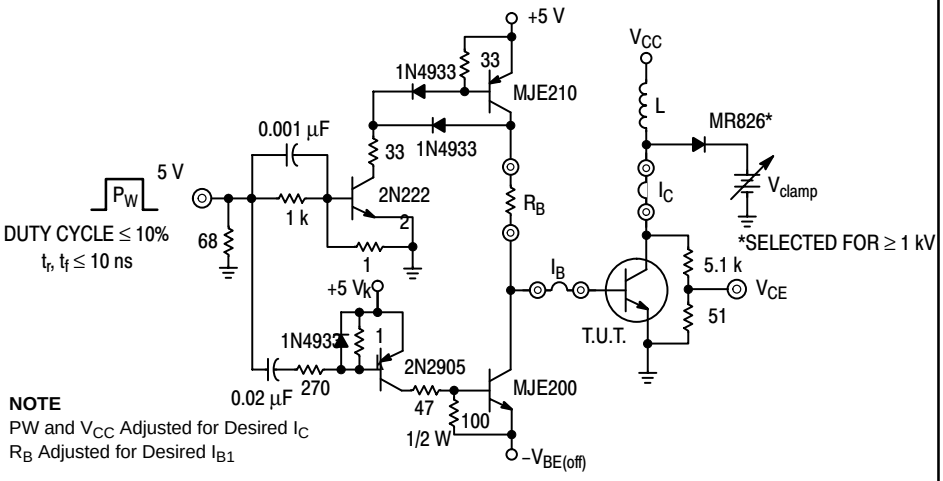
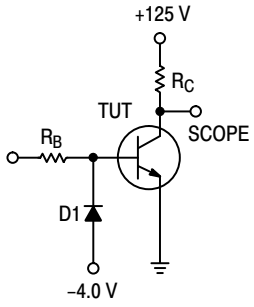
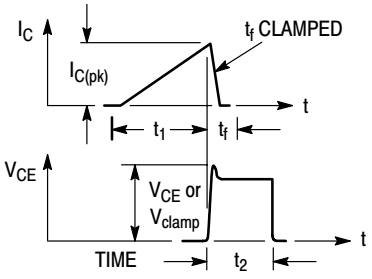
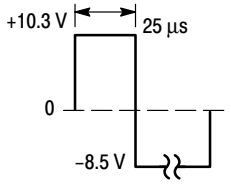


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2 A L_{coil} = 50 mH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 or Equiv. R_B = 47 Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

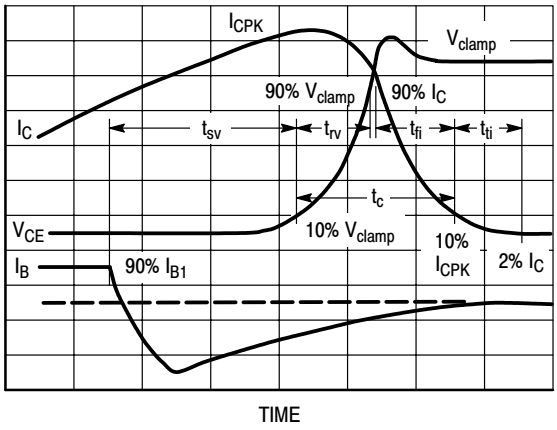


Figure 7. Inductive Switching Measurements

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25 100	1.3 1.6	0.23 0.26	0.30 0.30	0.35 0.40	0.30 0.36
1	25 100	1.5 1.7	0.10 0.13	0.14 0.26	0.05 0.06	0.16 0.29
1.5	25 100	1.8 3	0.07 0.08	0.10 0.22	0.05 0.08	0.16 0.28

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

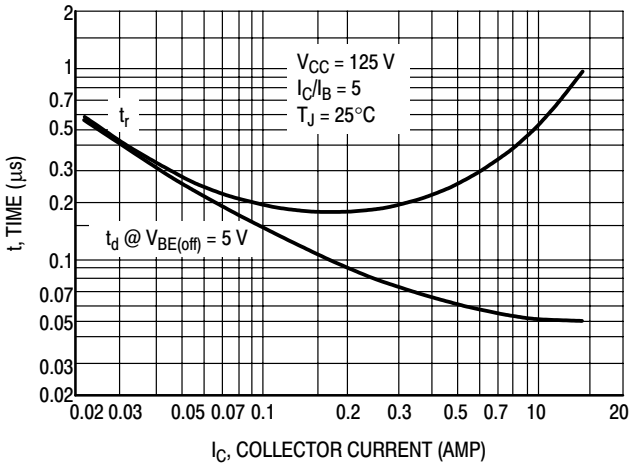


Figure 8. Turn–On Time

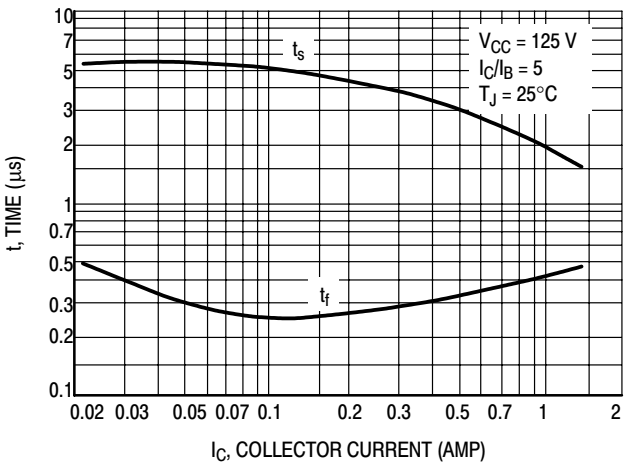


Figure 9. Turn–Off Time

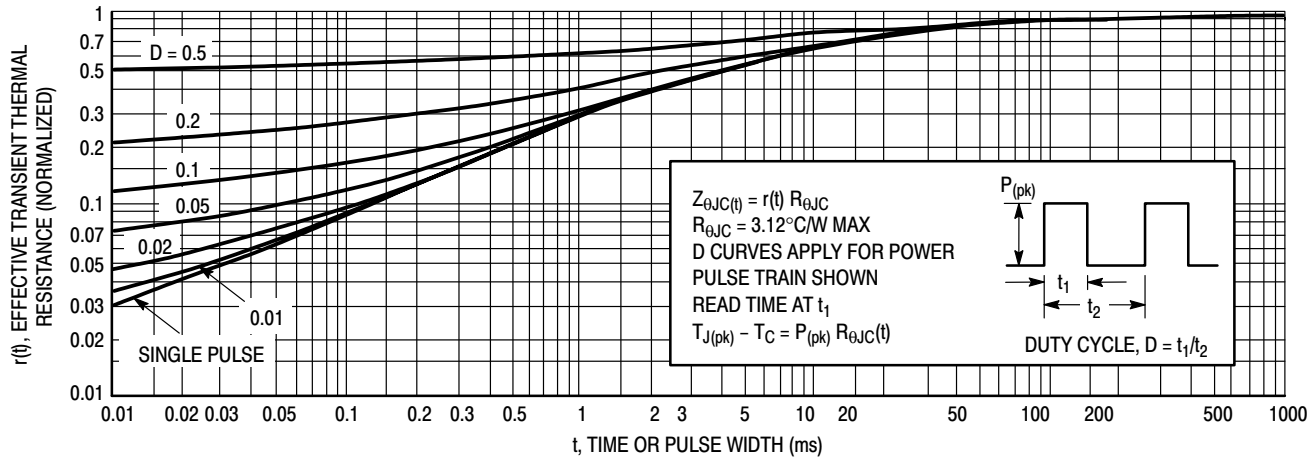


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

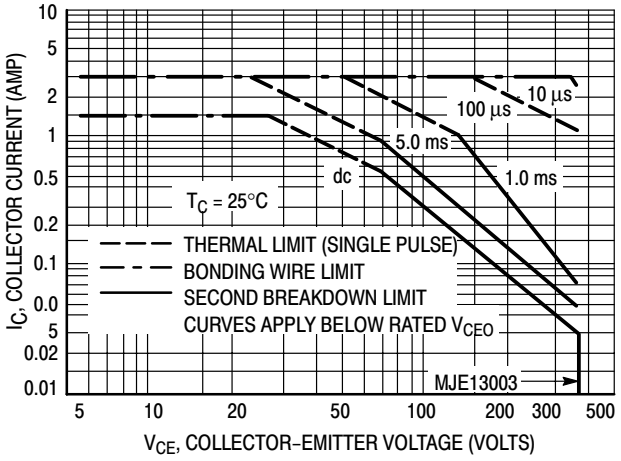


Figure 11. Active Region Safe Operating Area

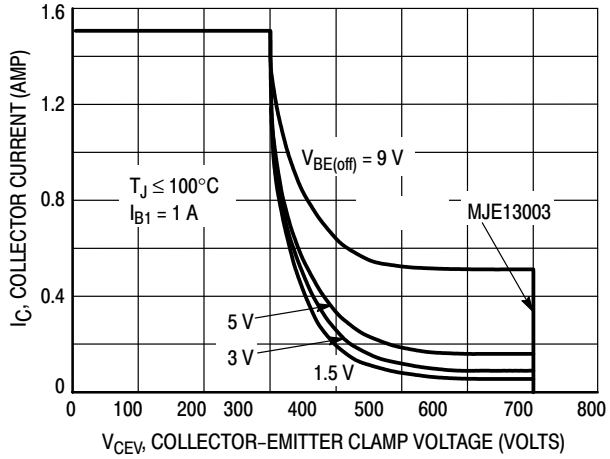


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

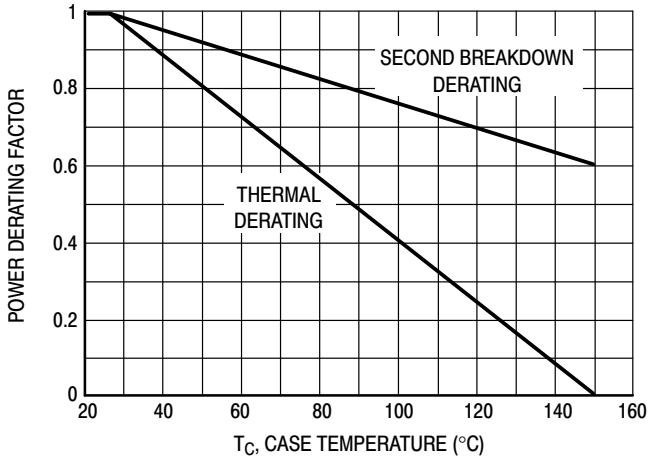


Figure 13. Forward Bias Power Derating

MJE13005*

*ON Semiconductor Preferred Device

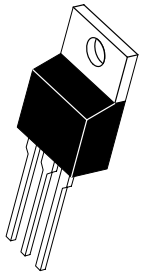
SWITCHMODE™ Series NPN Silicon Power Transistors

These devices are designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

4 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
75 WATTS

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
  t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	6 12	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 600	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		—	—	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 11		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 12		
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				—
(I_C = 1 Adc, V_{CE} = 5 Vdc)		10	—	60	
(I_C = 2 Adc, V_{CE} = 5 Vdc)		8	—	40	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)		—	—	0.5	
(I_C = 2 Adc, I_B = 0.5 Adc)		—	—	0.6	
(I_C = 4 Adc, I_B = 1 Adc)		—	—	1	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		—	—	1	
Base–Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)		—	—	1.2	
(I_C = 2 Adc, I_B = 0.5 Adc)		—	—	1.6	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	65	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 2)					
Delay Time	t_d	—	0.025	0.1	μs
Rise Time	t_r	—	0.3	0.7	μs
Storage Time	t_s	—	1.7	4	μs
Fall Time	t_f	—	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)					
Voltage Storage Time	t_{sv}	—	0.9	4	μs
Crossover Time	t_c	—	0.32	0.9	μs
Fall Time	t_{fi}	—	0.16	—	μs

(V_{CC} = 125 Vdc, I_C = 2 A, I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)

(I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

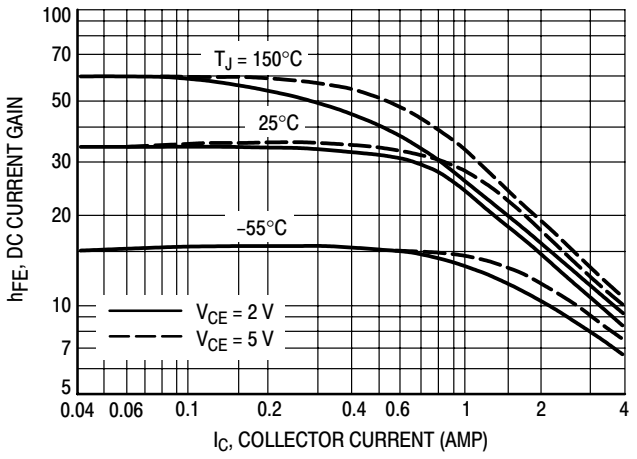


Figure 1. DC Current Gain

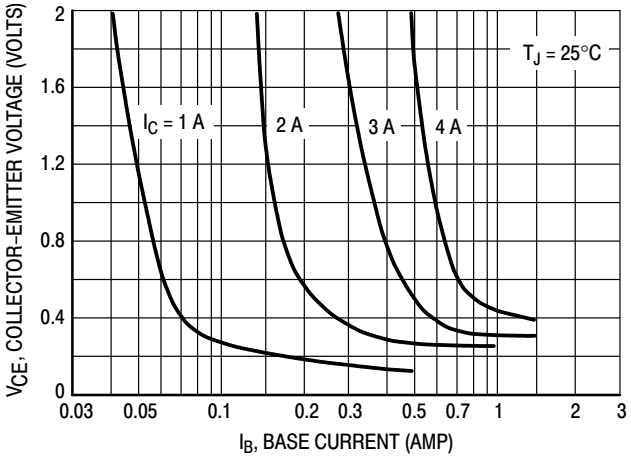


Figure 2. Collector Saturation Region

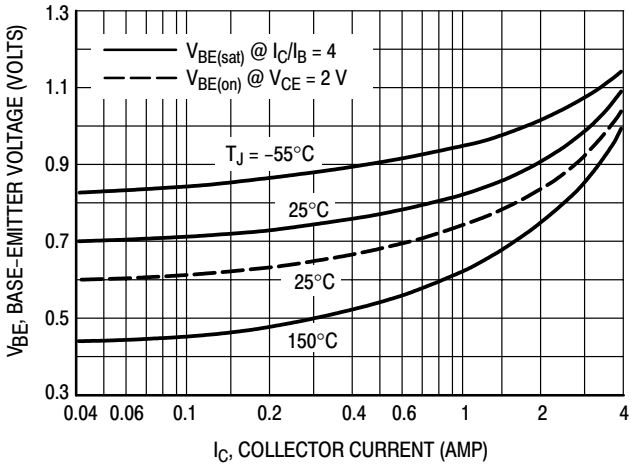


Figure 3. Base−Emitter Voltage

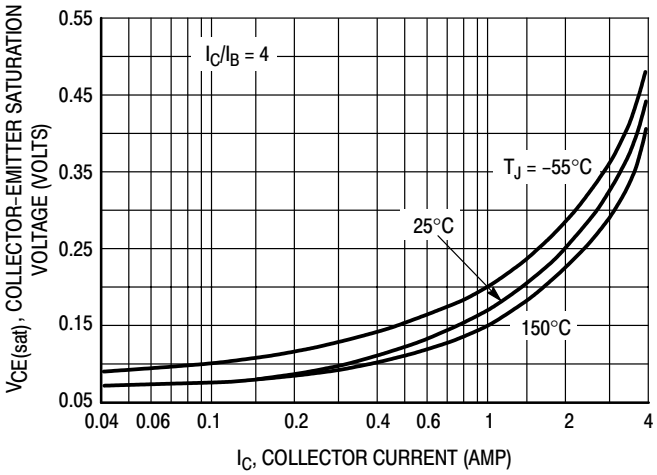


Figure 4. Collector−Emitter Saturation Voltage

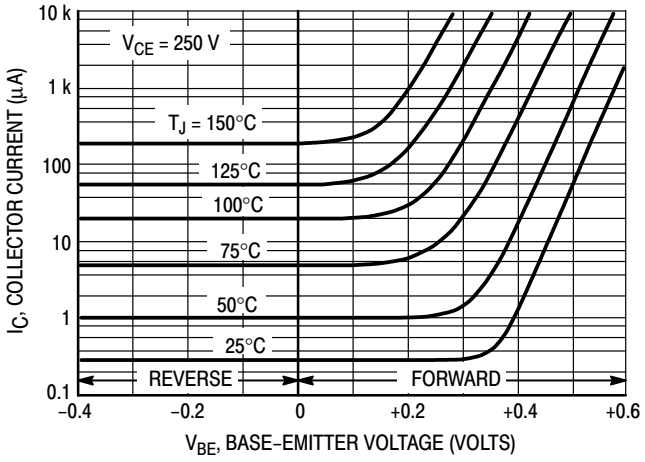


Figure 5. Collector Cutoff Region

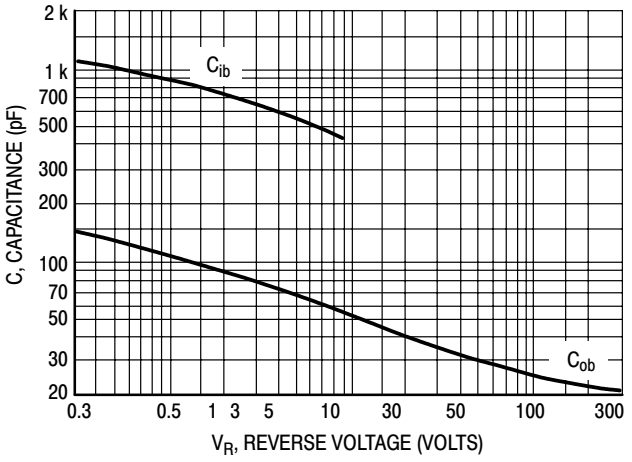


Figure 6. Capacitance

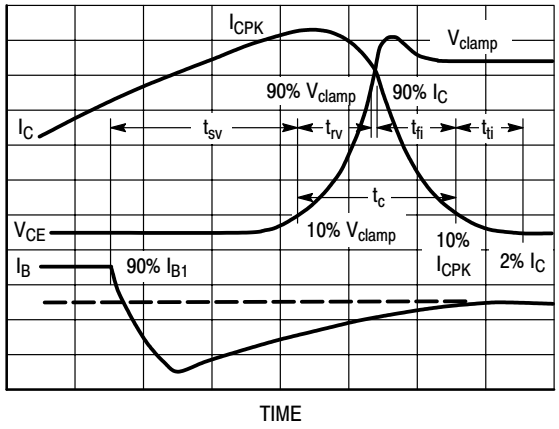


Figure 7. Inductive Switching Measurements

Table 1. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25 100	600 900	70 110	100 240	80 130	180 320
3	25 100	650 950	60 100	140 330	60 100	200 350
4	25 100	550 850	70 110	160 350	100 160	220 390

NOTE: All Data recorded in the inductive Switching Circuit In Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

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t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

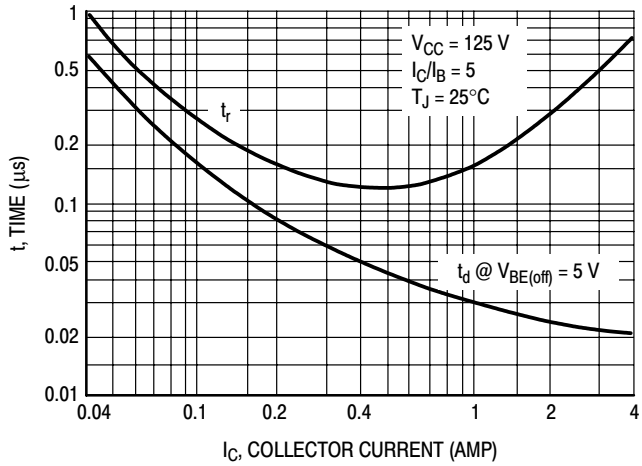


Figure 8. Turn–On Time

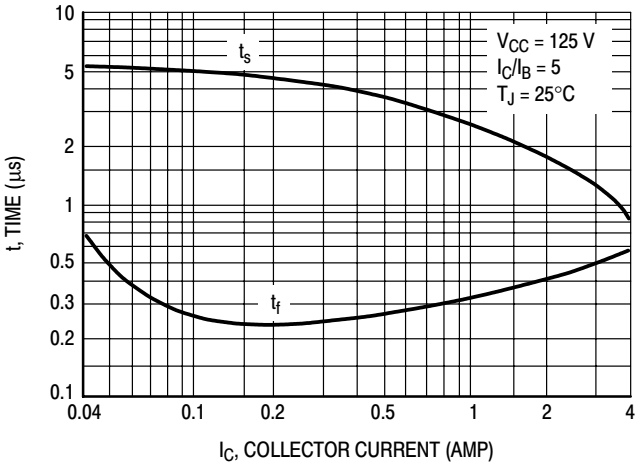
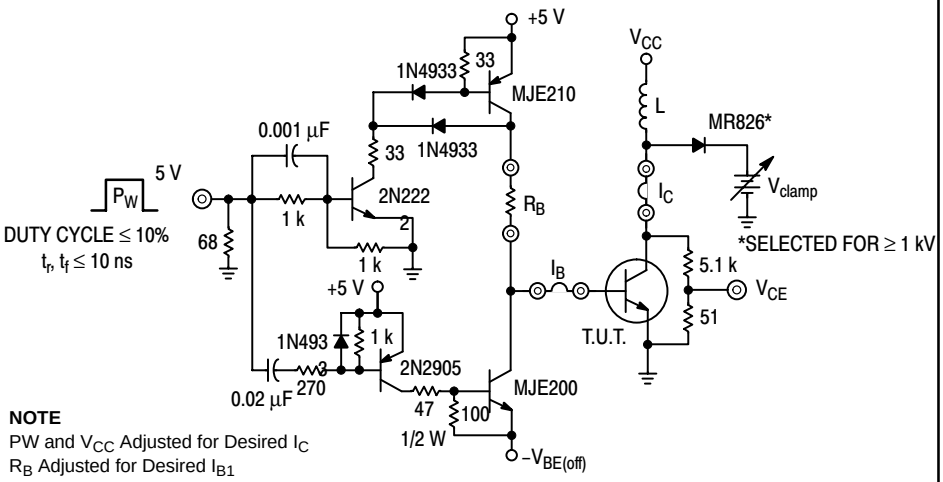
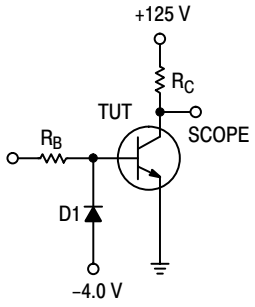
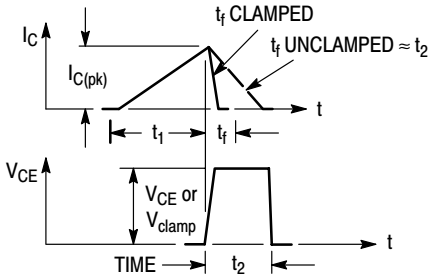
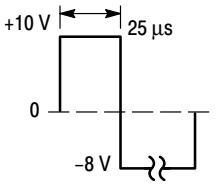


Figure 9. Turn–Off Time

Table 2. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20 A L_{coil} = 200 µH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 62 Ω D1 = 1N5820 or Equiv. R_B = 22 Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

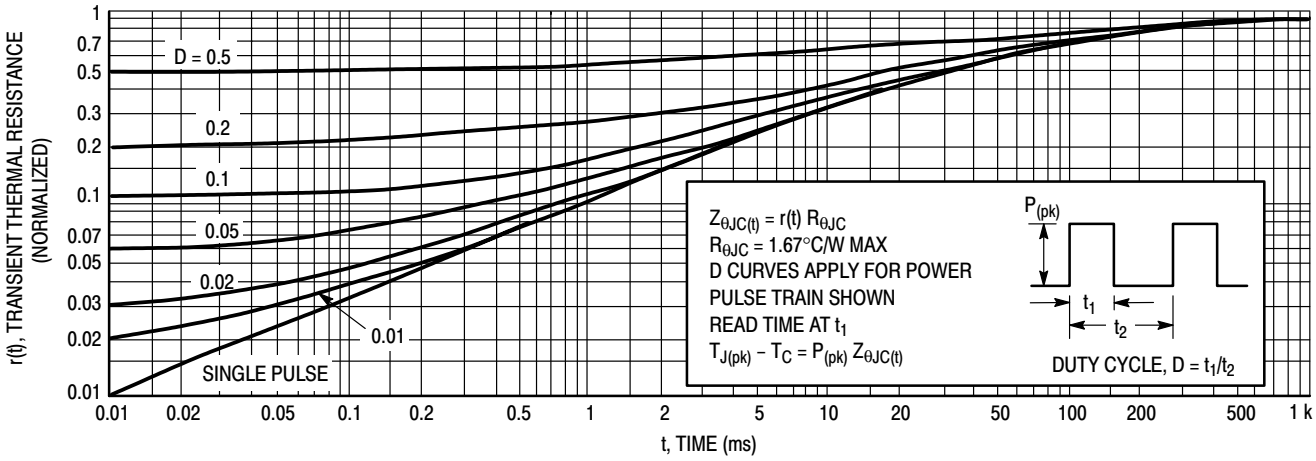


Figure 10. Typical Thermal Response [$Z_{\theta JC}(t)$]

SAFE OPERATING AREA INFORMATION

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

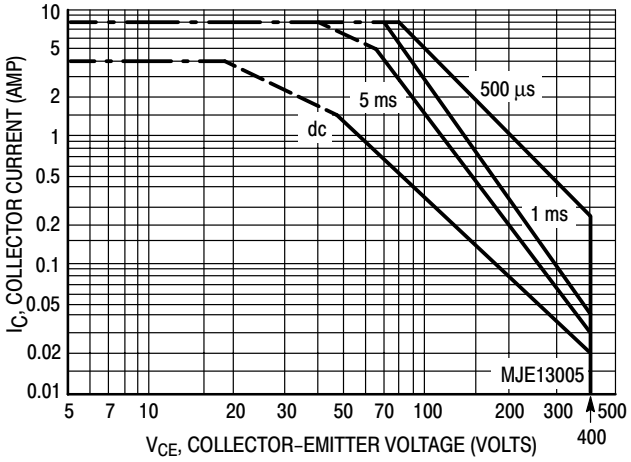


Figure 11. Forward Bias Safe Operating Area

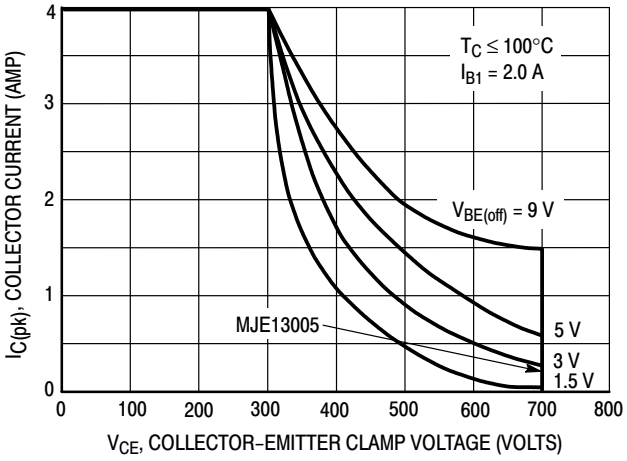


Figure 12. Reverse Bias Switching Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

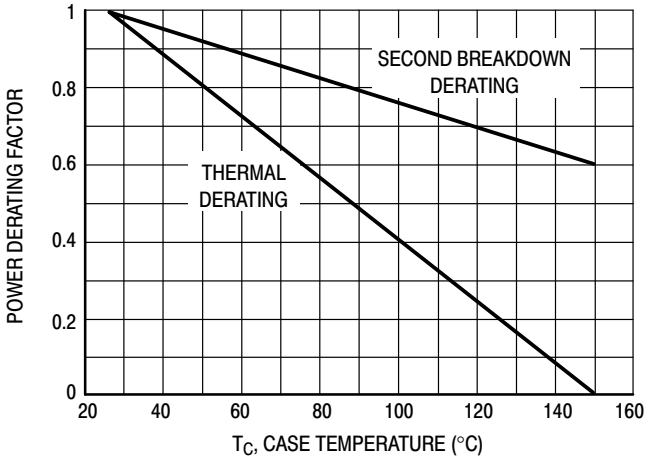


Figure 13. Forward Bias Power Derating

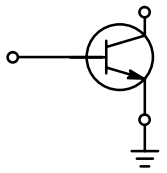
MJE13007

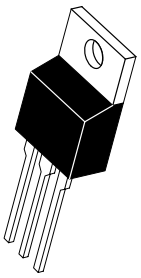
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE13007 is designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Standard TO–220

POWER TRANSISTOR
8.0 AMPERES
400 VOLTS
80 WATTS





CASE 221A–09
TO–220AB
MJE13007

MAXIMUM RATINGS

Rating	Symbol	MJE13007	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.56 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

May, 2001 – Rev. 3
Publication Order Number:
MJE13007/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**							
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current			I_{CES}				mAdc
(V_{CES} = 700 Vdc)				—	—	0.1	
(V_{CES} = 700 Vdc, T_C = 125°C)				—	—	1.0	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)			I_{EBO}	—	—	100	μAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased			—	See Figure 7			
***ON CHARACTERISTICS**							
DC Current Gain			h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)				8.0	—	40	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)				5.0	—	30	
Collector–Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	2.0	
(I_C = 8.0 Adc, I_B = 2.0 Adc)				—	—	3.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	3.0	
Base–Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.2	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	1.5	
DYNAMIC CHARACTERISTICS							
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)			f_T	4.0	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 125 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 25 μs, Duty Cycle ≤ 1.0%)		t_d	—	0.025	0.1	μs
Rise Time			t_r	—	0.5	1.5	
Storage Time			t_s	—	1.8	3.0	
Fall Time			t_f	—	0.23	0.7	
Inductive Load, Clamped (Table 1)							
Voltage Storage Time	V_{CC} = 15 Vdc, I_C = 5.0 A, V_{clamp} = 300 Vdc	T_C = 25°C	t_{sv}	—	1.2	2.0	μs
		T_C = 100°C		—	1.6	3.0	
Crossover Time	$I_{B(on)}$ = 1.0 A, $I_{B(off)}$ = 2.5 A, L_C = 200 μH	T_C = 25°C	t_c	—	0.15	0.30	μs
		T_C = 100°C		—	0.21	0.50	
Fall Time		T_C = 25°C	t_{fi}	—	0.04	0.12	μs
		T_C = 100°C		—	0.10	0.20	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

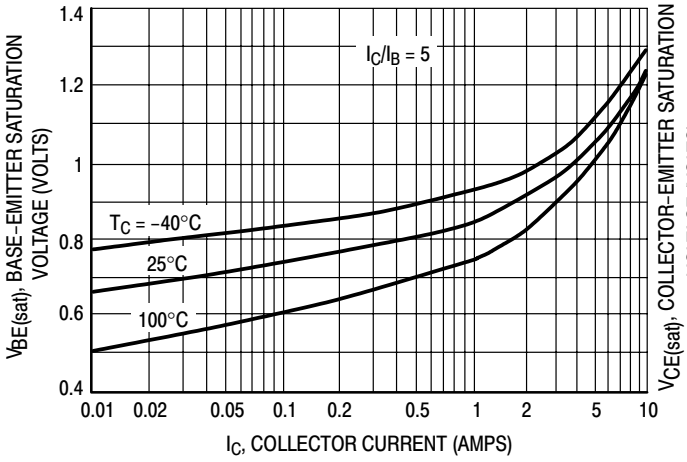


Figure 1. Base–Emitter Saturation Voltage

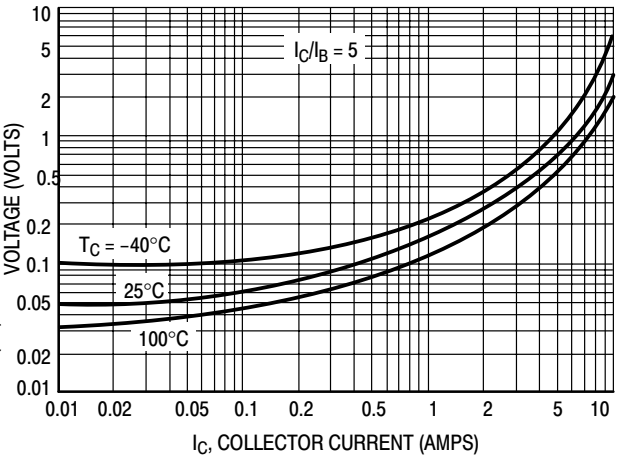


Figure 2. Collector–Emitter Saturation Voltage

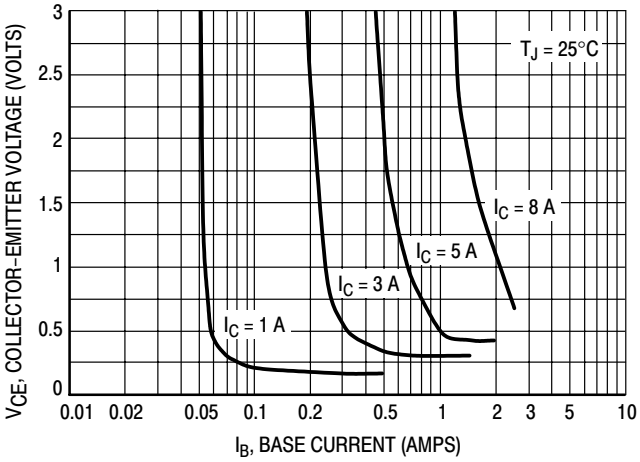


Figure 3. Collector Saturation Region

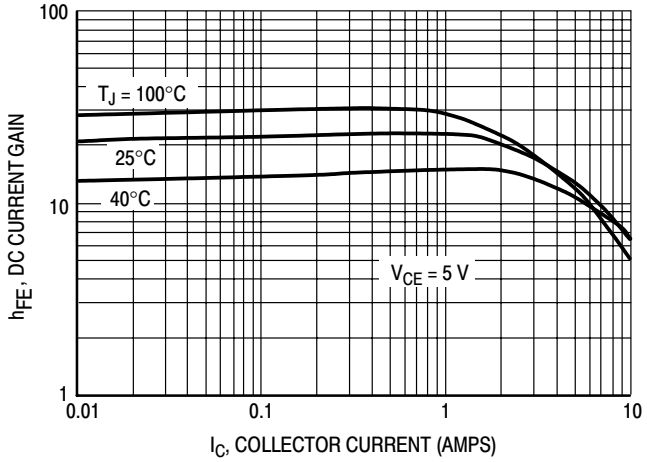


Figure 4. DC Current Gain

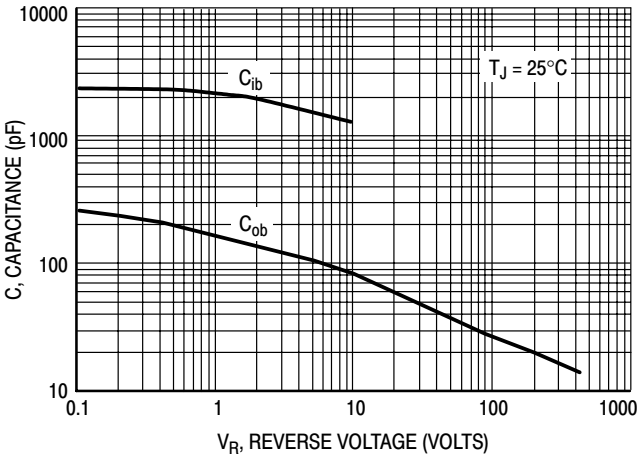


Figure 5. Capacitance

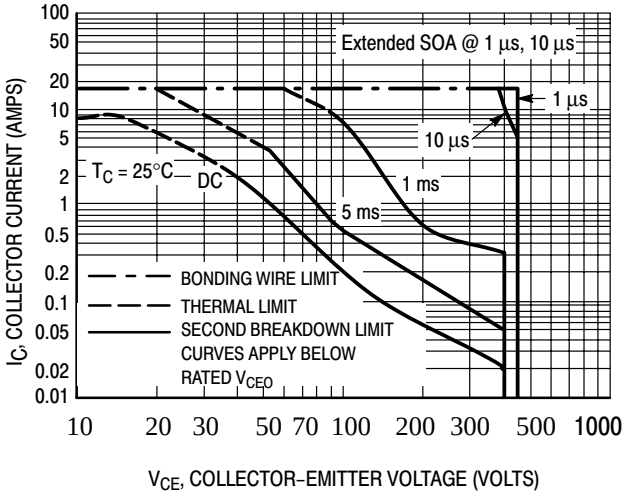


Figure 6. Maximum Forward Bias Safe Operating Area

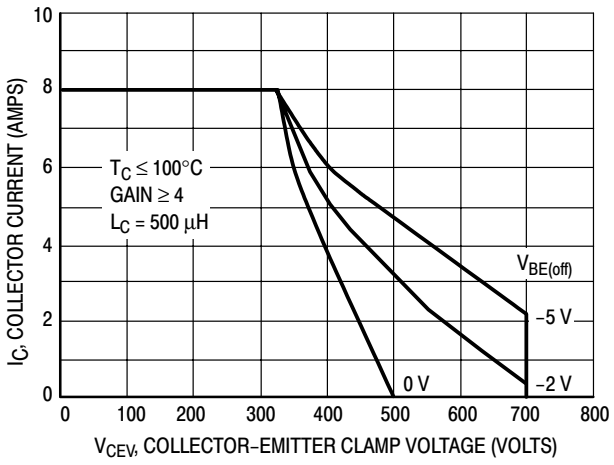


Figure 7. Maximum Reverse Bias Switching Safe Operating Area

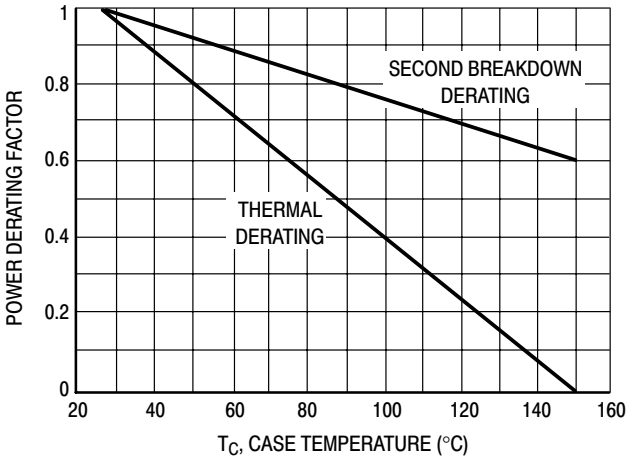


Figure 8. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 8.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 7) is discussed in the applications information section.

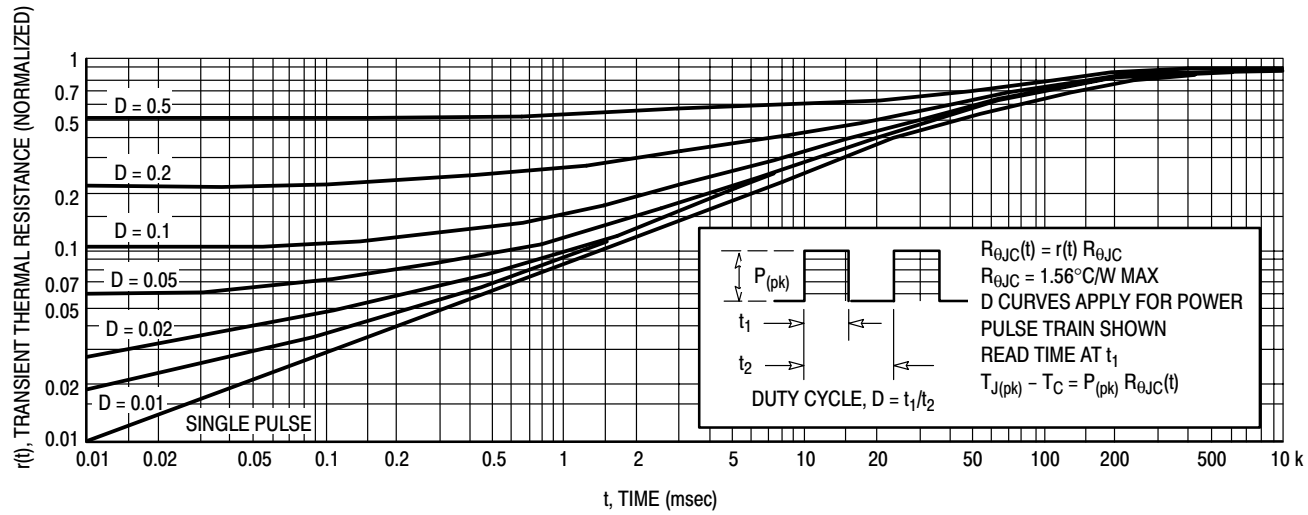


Figure 9. Typical Thermal Response for MJE13007

SPECIFICATION INFORMATION FOR SWITCHMODE APPLICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

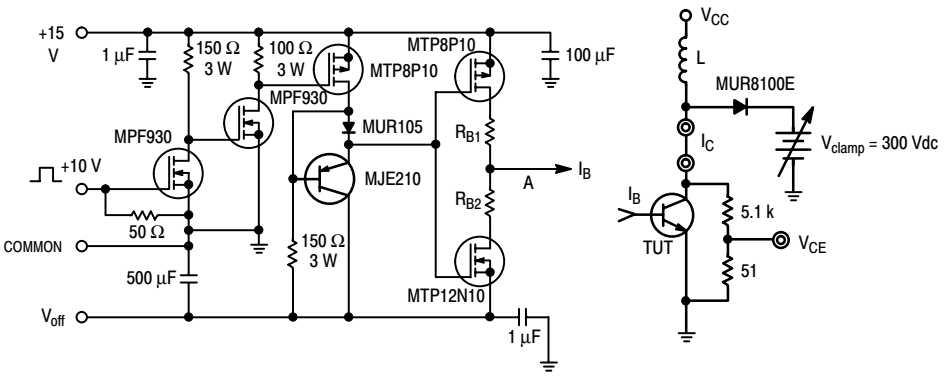
Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

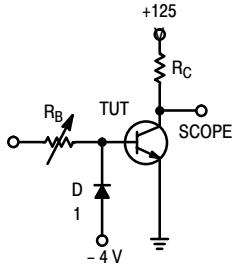
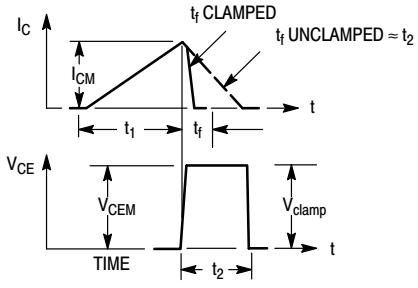
The sustaining or active region voltage requirements in switching applications occur during turn–on and turn–off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn–on and the pulsed forward bias SOA curves (Figure 6) are the proper design limits.

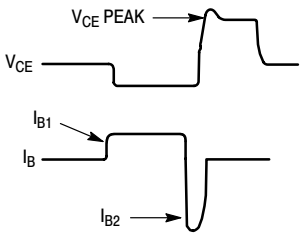
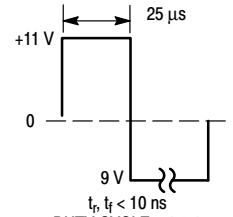
For inductive loads, high voltage and current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 7) which represents voltage–current conditions that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

(1) For detailed information on specific switching applications, see ON Semiconductor Application Note AN719, AN873, AN875, AN951.

Table 1. Test Conditions For Dynamic Performance

<table>
<tr><td>TEST CIRCUITS</td><td>REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING</td><td>RESISTIVE SWITCHING</td></tr>
<tr><td></td><td> 


</td></tr>
<tr><td>CIRCUIT VALUES</td><td><table>
<tr><th>V(BR)CEO(sus)</th><th>Inductive Switching</th><th>RBSOA</th></tr>
<tr><td>L = 10 mH
RB2 = 8
VCC = 20 Volts
IC(pk) = 100 mA</td><td>L = 200 mH
RB2 = 0
VCC = 15 Volts
RB1 selected for desired IB1</td><td>L = 500 mH
RB2 = 0
VCC = 15 Volts
RB1 selected for desired IB1</td></tr>
</table></td><td>VCC = 125 V
RC = 25 Ω
D1 = 1N5820 OR EQUIV.</td></tr>
<tr><td>TEST WAVEFORMS</td><td> 

t1 ADJUSTED TO OBTAIN IC
$t_1 \approx \frac{L_{coil}\,(I_{CM})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}\,(I_{CM})}{V_{clamp}}$
TEST EQUIPMENT
SCOPE — TEKTRONIX 475 OR EQUIVALENT</td><td>TYPICAL WAVE-FORMS
 
</td><td> 

tr, tf < 10 ns
DUTY CYCLE = 1.0%
RB AND RC ADJUSTED FOR DESIRED IB AND IC</td></tr>
</table>

VOLTAGE REQUIREMENTS (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn–off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn–on and within the reverse bias SOA curve during turn–off are considered safe, with the following assumptions:

3. The device thermal limitations are not exceeded.
4. The turn–on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 6).
5. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 7).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5.0 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base–emitter junction during turn–off. The reverse biased switching characteristics for inductive loads are shown in Figures 12 and 13 and resistive loads in Figures 10 and 11. Usually the inductive load components will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (see Table 1) providing correlation between test procedures and actual use conditions.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and any coil driver, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 12 to aid in the visual identity of these terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222A:

$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$

Typical inductive switching times are shown in Figure 13. In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

SWITCHING PERFORMANCE

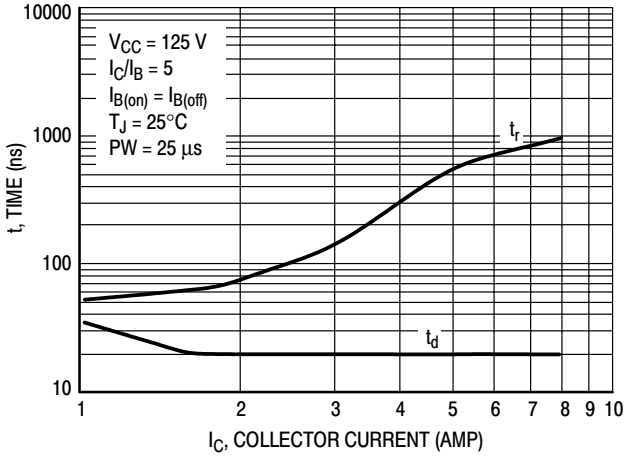


Figure 10. Turn–On Time (Resistive Load)

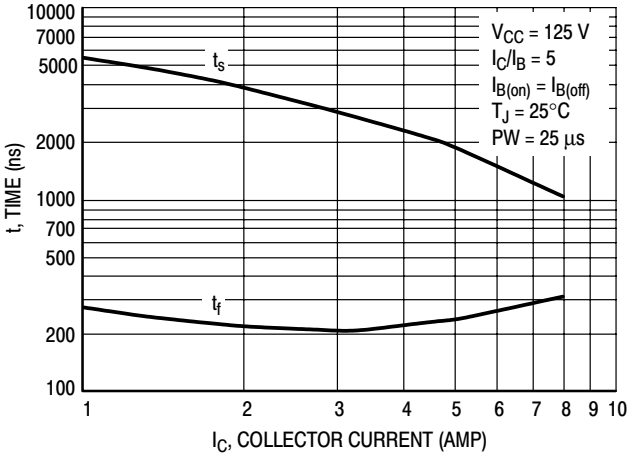


Figure 11. Turn–Off Time (Resistive Load)

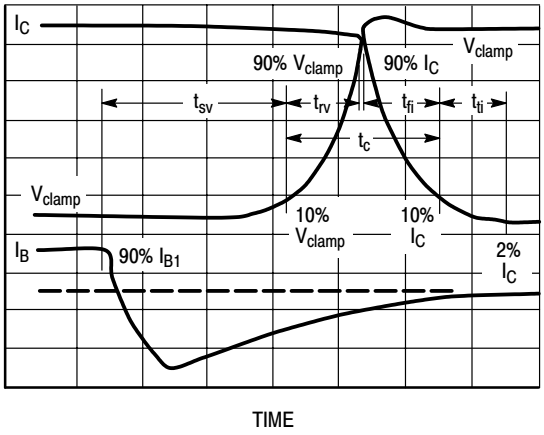


Figure 12. Inductive Switching Measurements

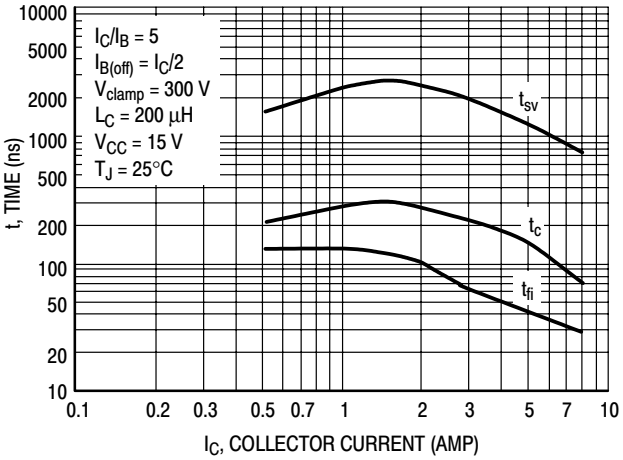
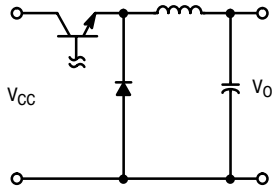
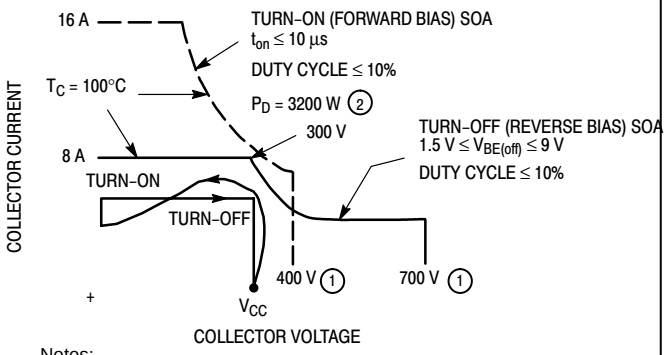
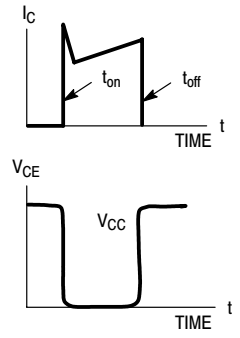
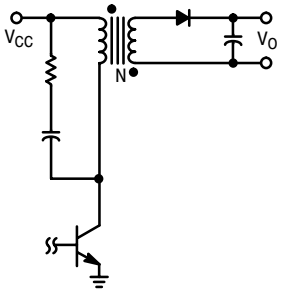
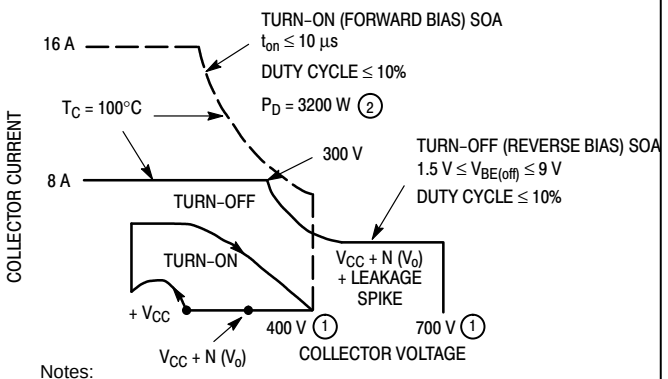
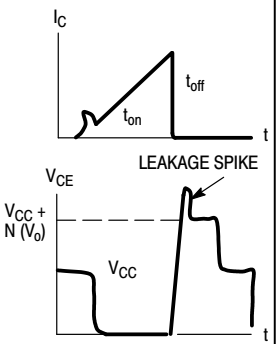
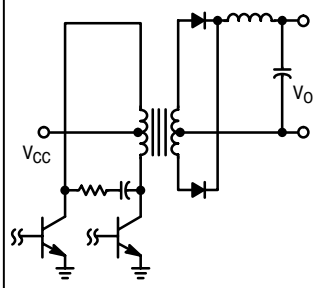
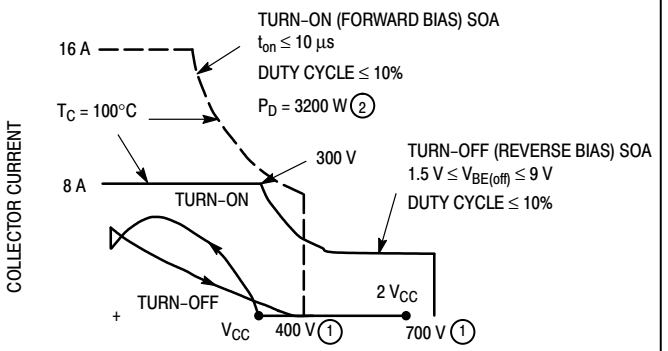
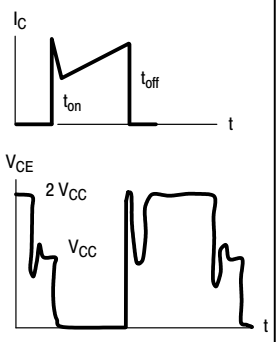
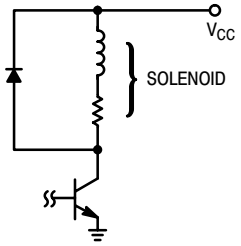
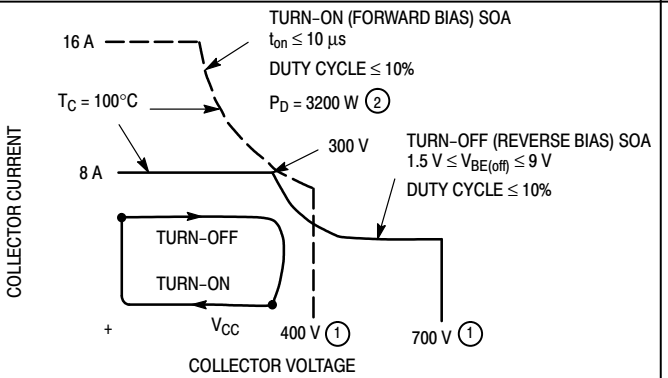
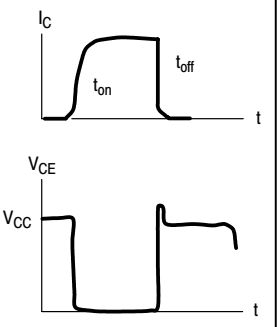


Figure 13. Typical Inductive Switching Times

Table 2. Applications Examples of Switching Circuits

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
B	**FLYBACK INVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
C	**PUSH−PULL INVERTER/CONVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	

MJE13009*

*ON Semiconductor Preferred Device

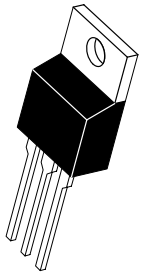
SWITCHMODE™ Series NPN Silicon Power Transistors

The MJE13009 is designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C
  t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

12 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
100 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 800	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		—	—	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	—	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				
(I_C = 5 Adc, V_{CE} = 5 Vdc)		8	—	40	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6	—	30	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		—	—	1	
(I_C = 8 Adc, I_B = 1.6 Adc)		—	—	1.5	
(I_C = 12 Adc, I_B = 3 Adc)		—	—	3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		—	—	2	
Base–Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		—	—	1.2	
(I_C = 8 Adc, I_B = 1.6 Adc)		—	—	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	180	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	t_d	—	0.06	0.1	μs
Rise Time	t_r	—	0.45	1	μs
Storage Time	t_s	—	1.3	3	μs
Fall Time	t_f	—	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	t_{sv}	—	0.92	2.3	μs
Crossover Time	t_c	—	0.12	0.7	μs

(V_{CC} = 125 Vdc, I_C = 8 A, I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs, Duty Cycle ≤ 1%)

(I_C = 8 A, V_{clamp} = 300 Vdc, I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

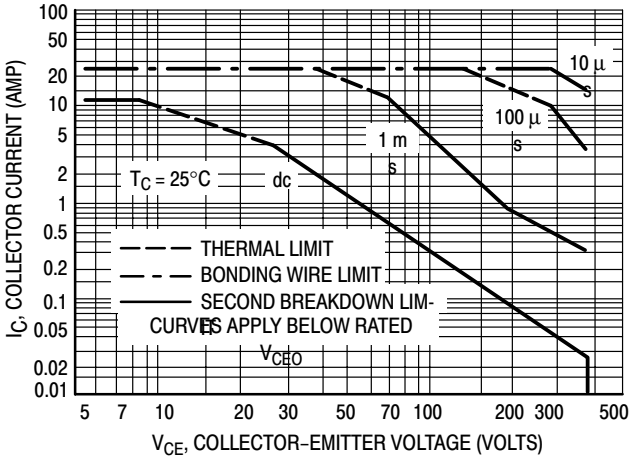


Figure 1. Forward Bias Safe Operating Area

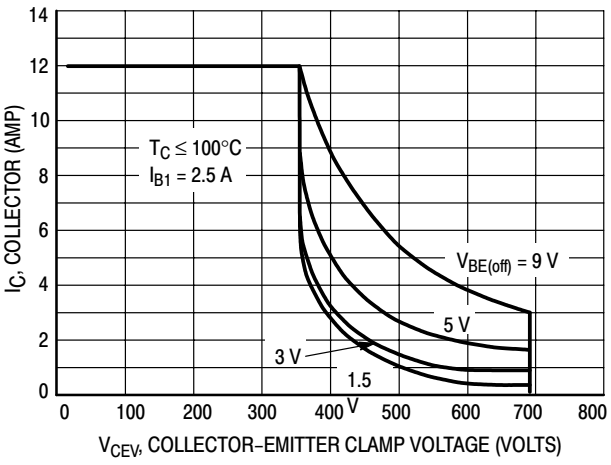


Figure 2. Reverse Bias Switching Safe Operating Area

The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

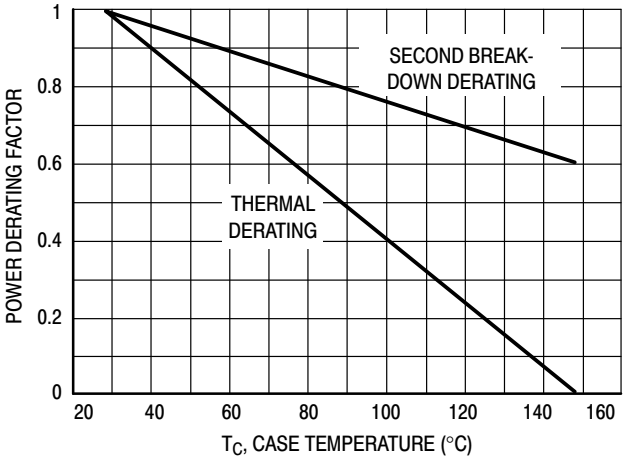


Figure 3. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

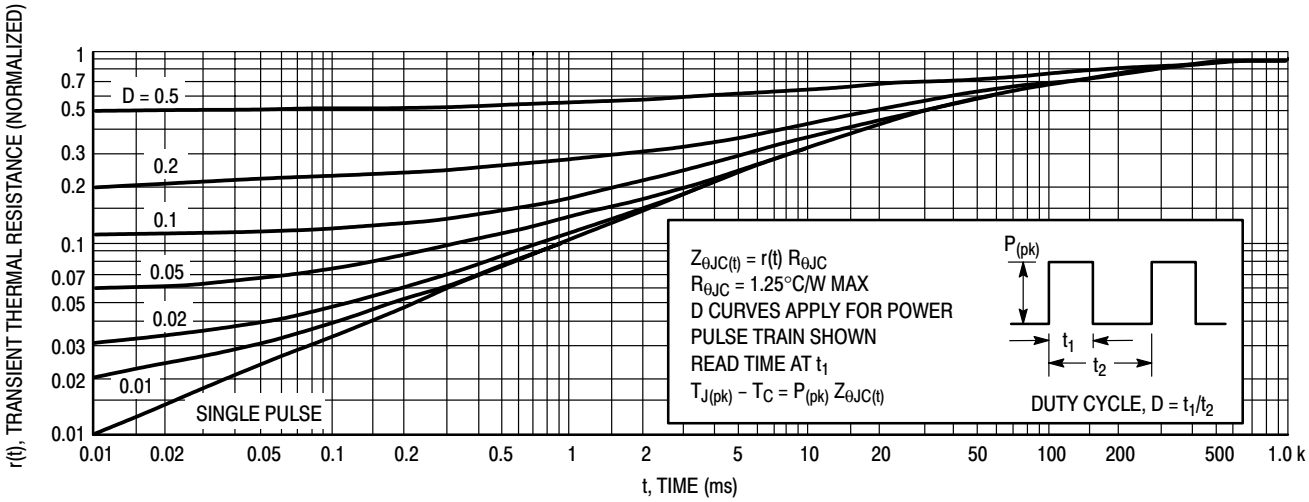


Figure 4. Typical Thermal Response [$Z_{\theta JC}(t)$]

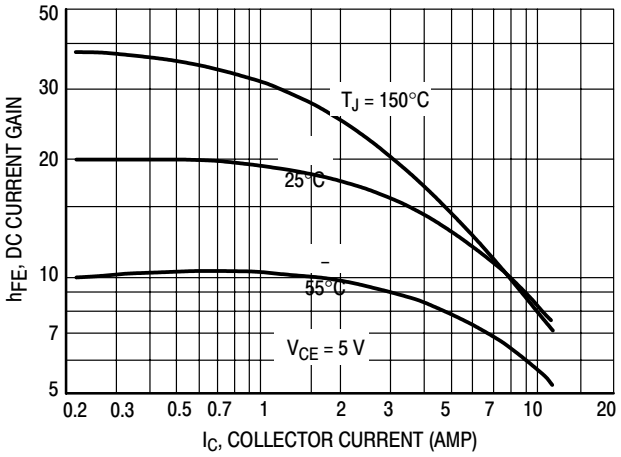


Figure 5. DC Current Gain

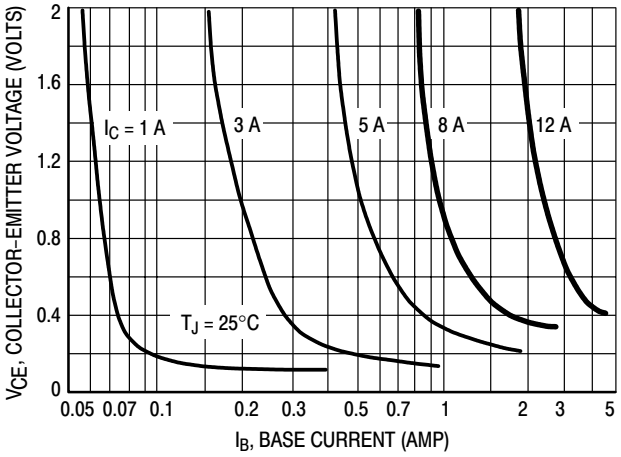


Figure 6. Collector Saturation Region

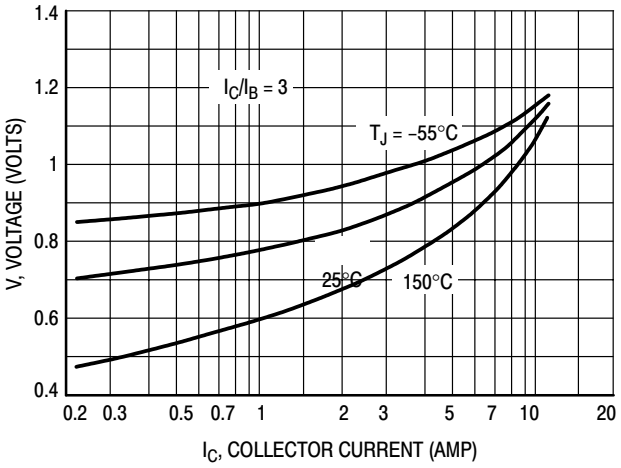


Figure 7. Base−Emitter Saturation Voltage

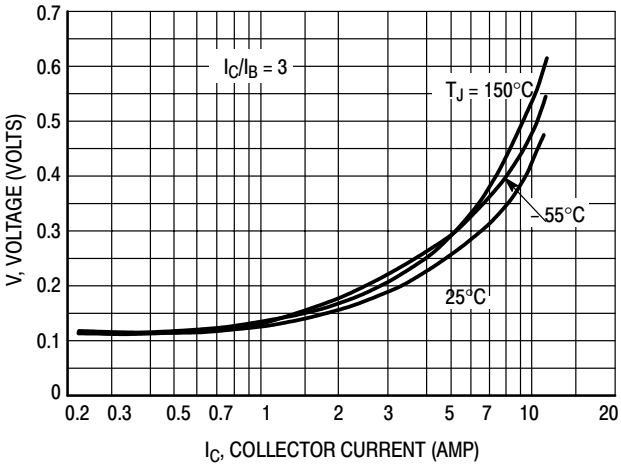


Figure 8. Collector−Emitter Saturation Voltage

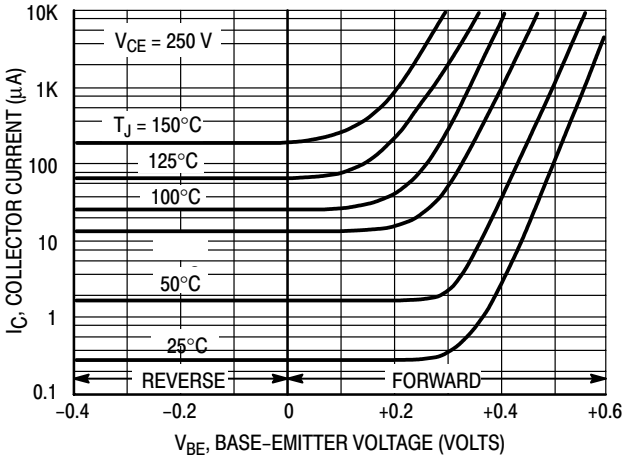


Figure 9. Collector Cutoff Region

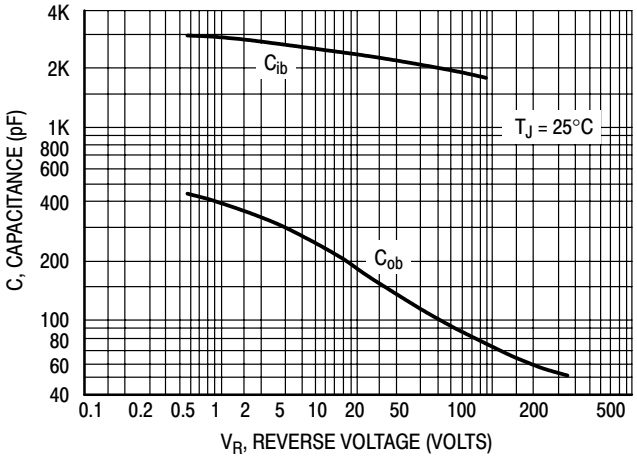
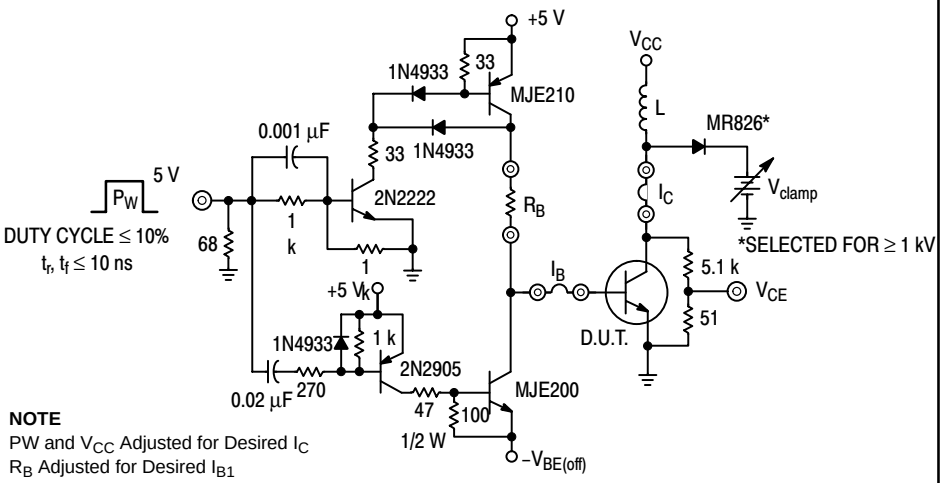
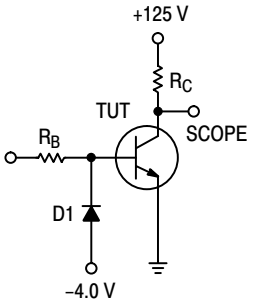
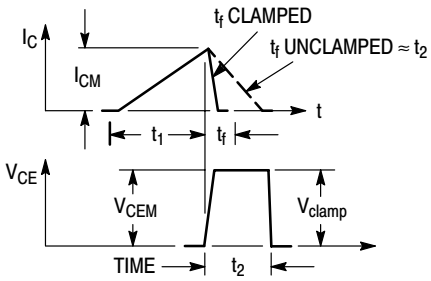
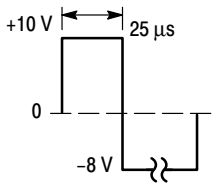


Figure 10. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20 A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15 Ω D1 = 1N5820 or Equiv. R_B = Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn–on and turn–off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn–on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage–current conditions that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn–off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn–on and within the reverse bias SOA curve during turn–off are considered safe, with the following assumptions:

6. The device thermal limitations are not exceeded.
7. The turn–on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
8. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base–emitter junction during turn–off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

(1) For detailed information on specific switching applications, see ON Semiconductor Application Notes AN–719, AN–767.

RESISTIVE SWITCHING PERFORMANCE

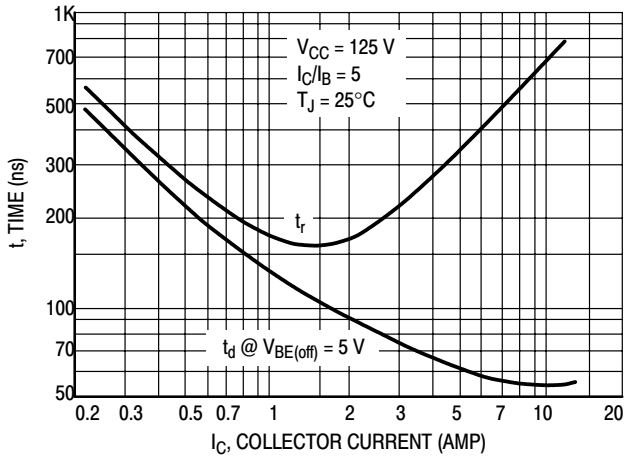


Figure 11. Turn–On Time

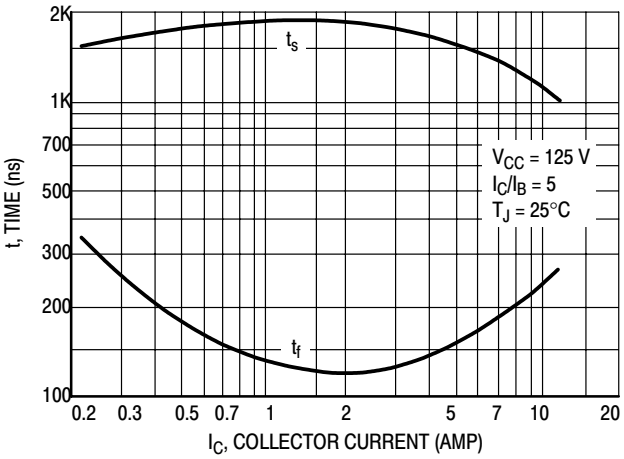


Figure 12. Turn–Off Time

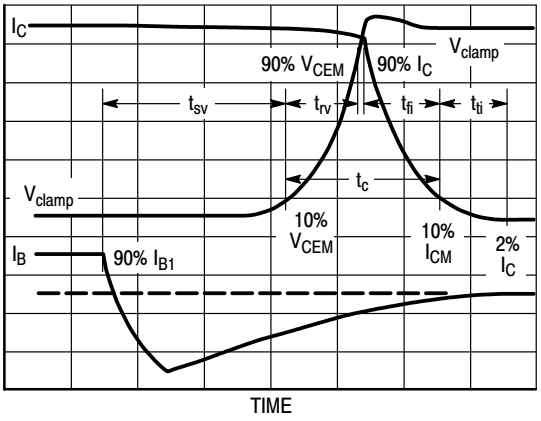


Figure 13. Inductive Switching Measurements

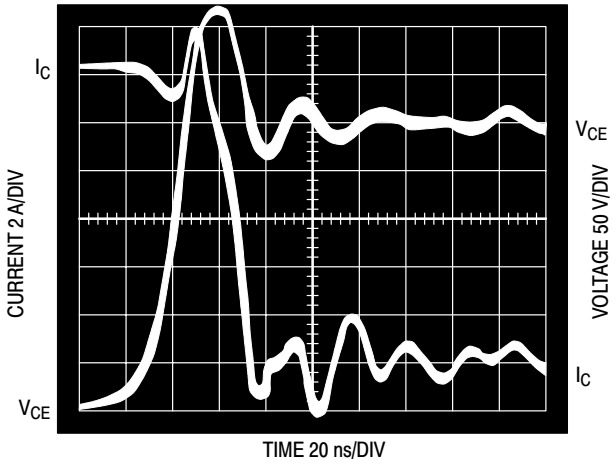


Figure 14. Typical Inductive Switching Waveforms (at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

Table 2. Applications Examples of Switching Circuits

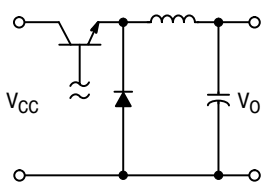
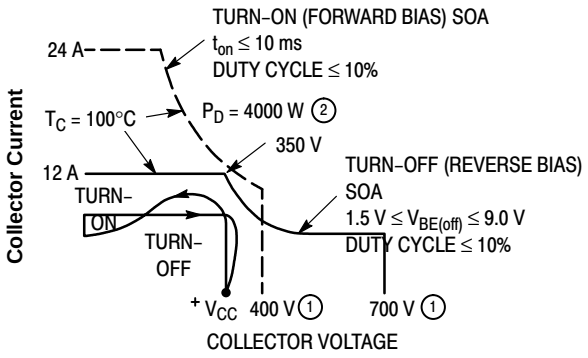
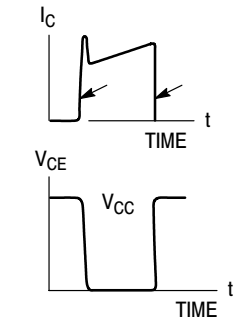
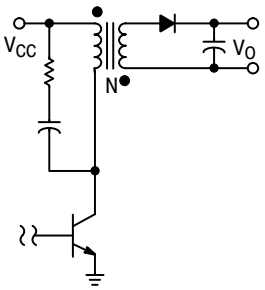
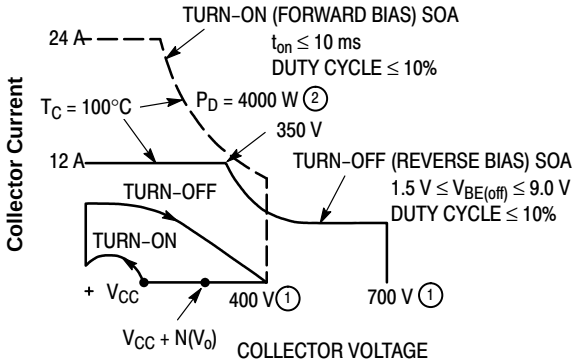
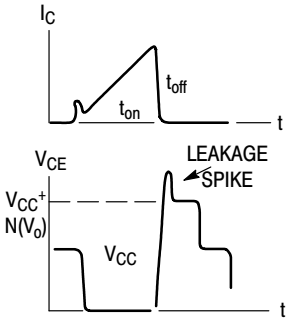
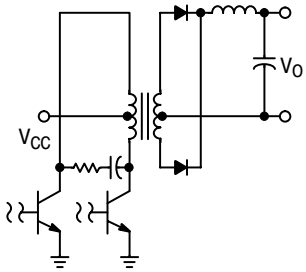
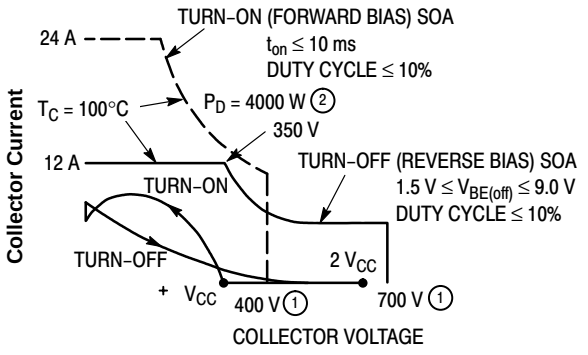
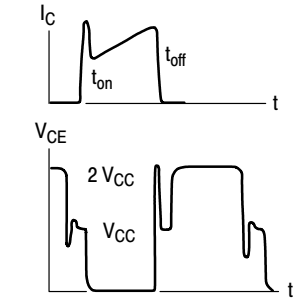
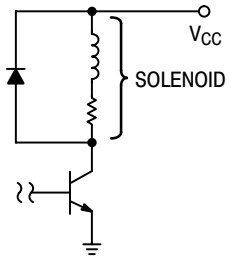
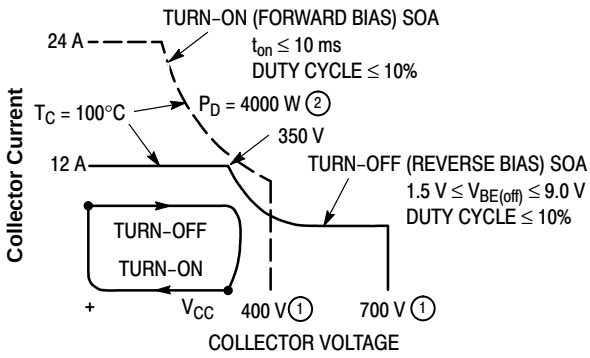
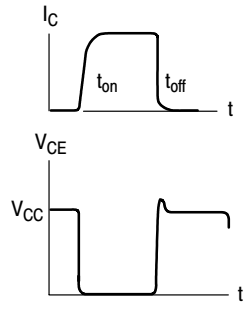
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH−PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

Table 3. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25 100	770 1000	100 230	150 160	200 200	240 320
5	25 100	630 820	72 100	26 55	10 30	100 180
8	25 100	720 920	55 70	27 50	2 8	77 120
12	25 100	640 800	20 32	17 24	2 4	41 54

NOTE: All Data recorded In the Inductive Switching Circuit In Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn–off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

Complementary Silicon Plastic Power Transistors

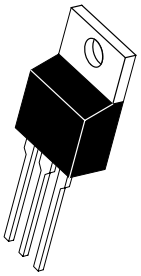
. . . designed for use as high–frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40 (Min) @ I_C = 3.0 Adc
  = 20 (Min) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — MJE15028, MJE15029
  = 150 Vdc (Min) — MJE15030, MJE15031
- High Current Gain — Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO–220AB Compact Package

NPN
MJE15028*
MJE15030*
PNP
MJE15029*
MJE15031*

*ON Semiconductor Preferred Device

8 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
120–150 VOLTS
50 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector–Emitter Voltage	V_{CEO}	120	150	Vdc
Collector–Base Voltage	V_{CB}	120	150	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak	I_C	8.0 16		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

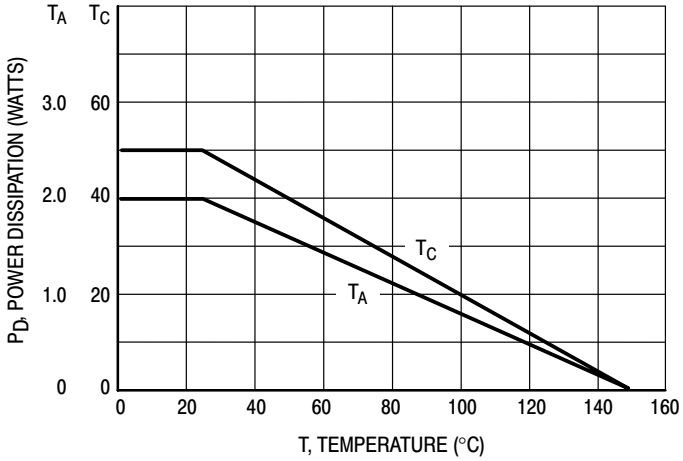


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 2
Publication Order Number:
MJE15028/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029		120	—	
	MJE15030, MJE15031		150	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 120 Vdc, I_B = 0)	MJE15028, MJE15029		—	0.1	
(V_{CE} = 150 Vdc, I_B = 0)	MJE15030, MJE15031		—	0.1	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 120 Vdc, I_E = 0)	MJE15028, MJE15029		—	10	
(V_{CB} = 150 Vdc, I_E = 0)	MJE15030, MJE15031		—	10	
Emitter Cutoff Current		I_{EBO}	—	10	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)			40	—	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)			40	—	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			40	—	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	—	
DC Current Gain Linearity		h_{FE}	**Typ**		
(V_{CE} From 2.0 V to 20 V, I_C From 0.1 A to 3 A)			2		
(NPN TO PNP)			3		
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	0.5	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	1.0	Vdc
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2)		f_T	30	—	MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

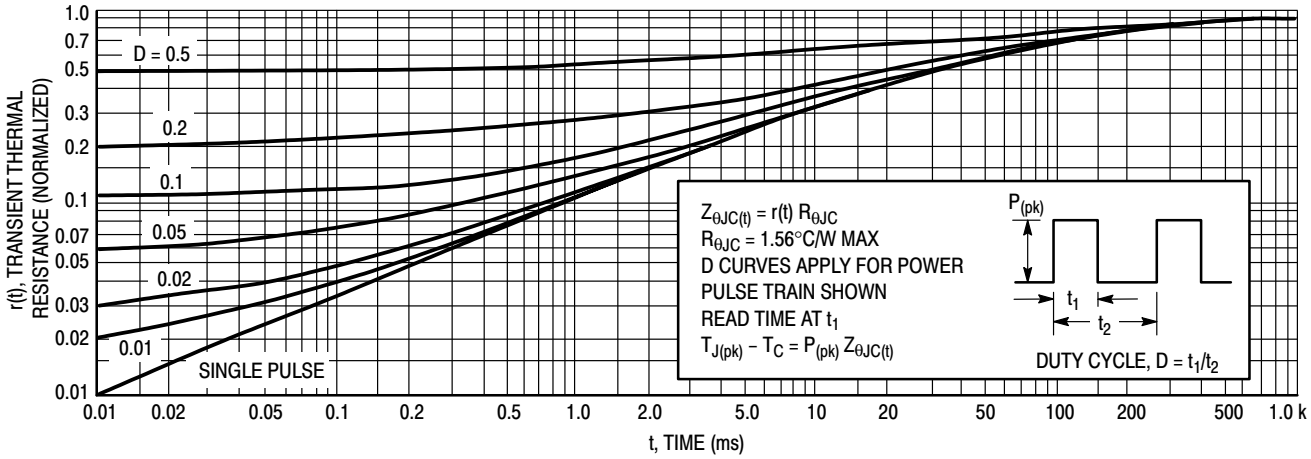


Figure 2. Thermal Response

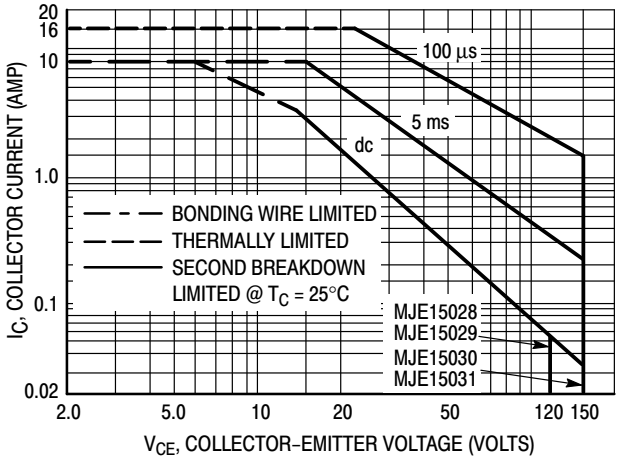


Figure 3. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

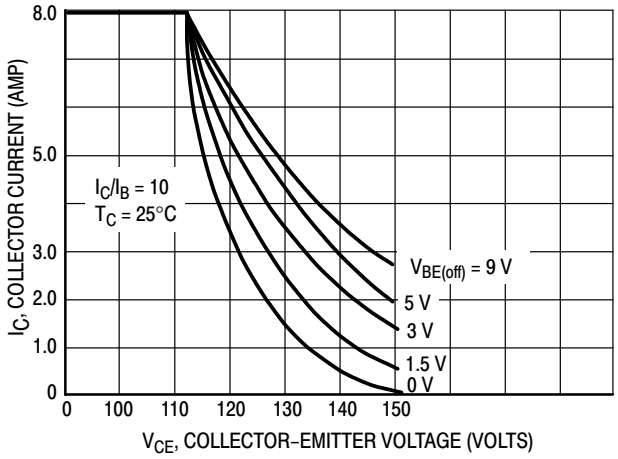


Figure 4. Reverse−Bias Switching Safe Operating Area

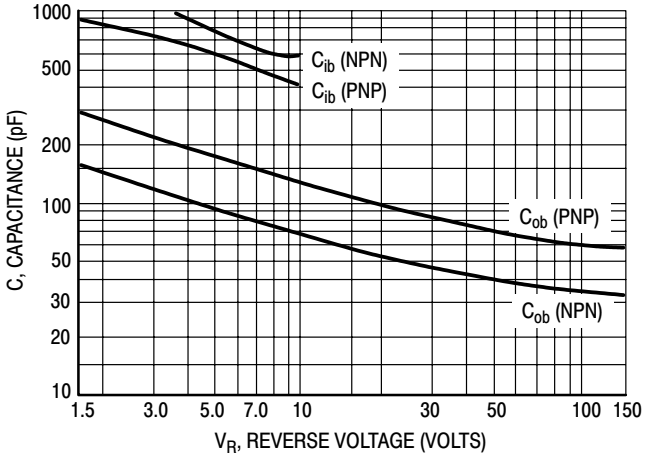


Figure 5. Capacitances

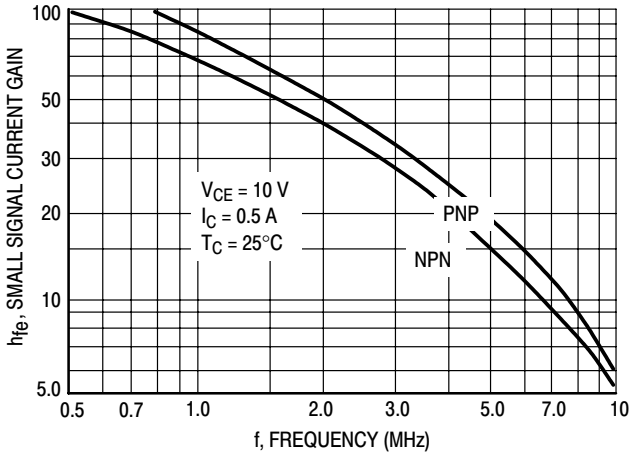


Figure 6. Small−Signal Current Gain

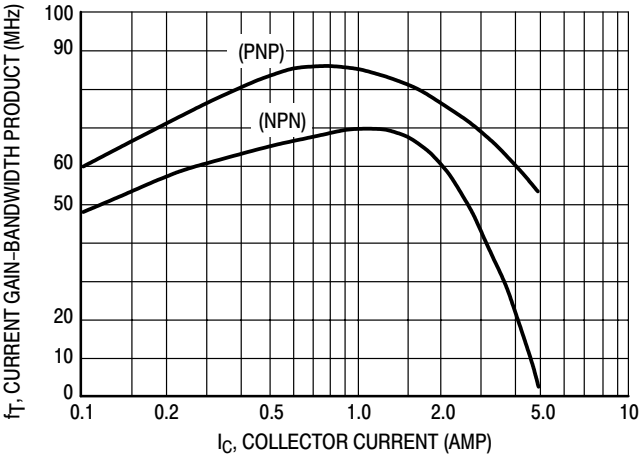
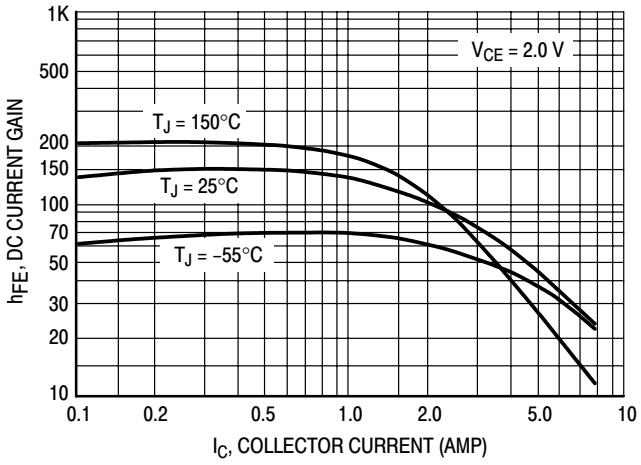


Figure 7. Current Gain−Bandwidth Product

NPN — MJE15028 MJE15030



PNP — MJE15029 MJE15031

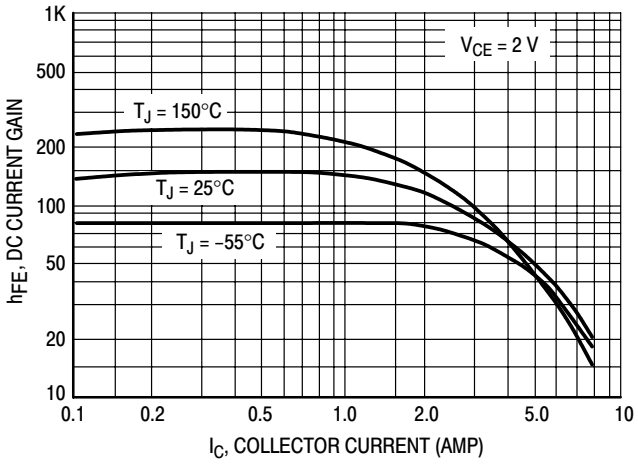
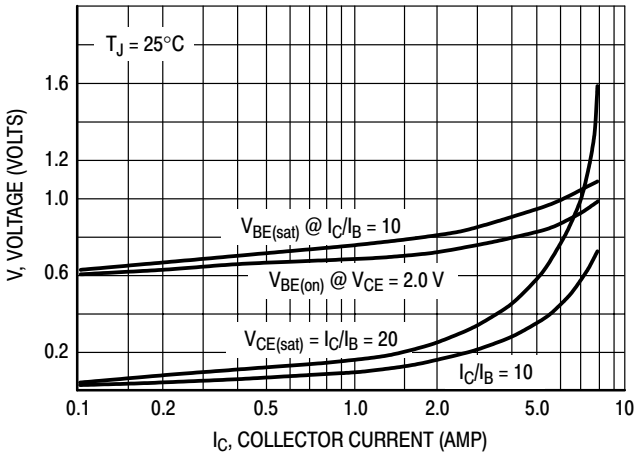


Figure 8. DC Current Gain

NPN



PNP

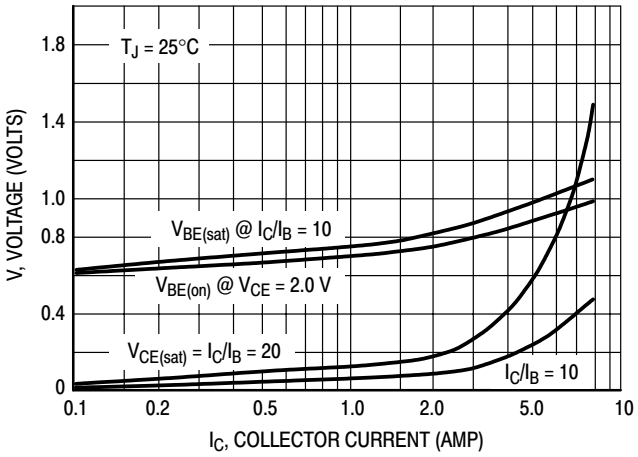


Figure 9. “On” Voltage

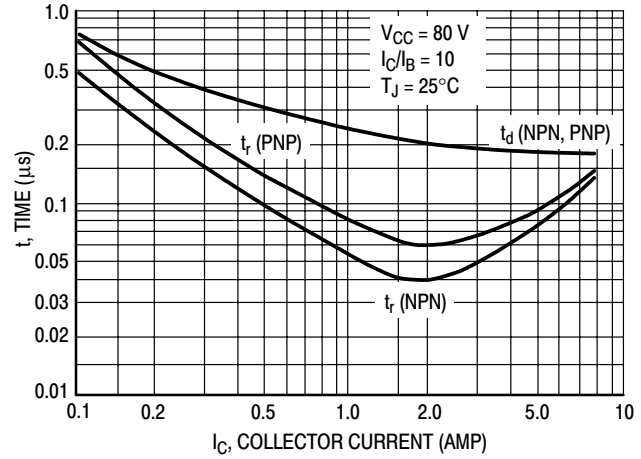


Figure 10. Turn–On Times

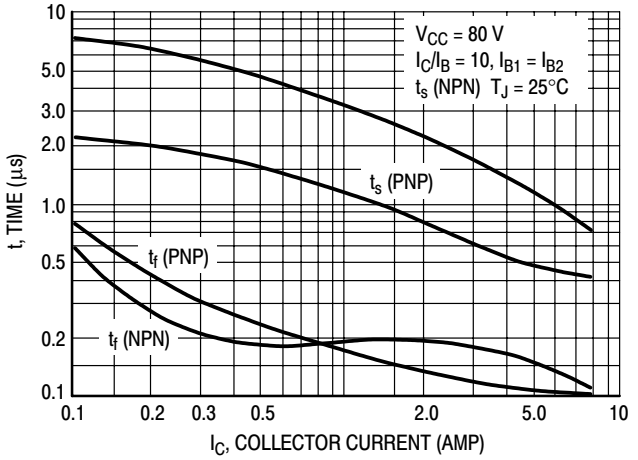


Figure 11. Turn–Off Times

Complementary Silicon Plastic Power Transistors

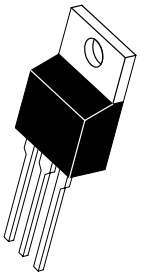
. . . designed for use as high–frequency drivers in audio amplifiers.

- DC Current Gain Specified to 5.0 Amperes
  h_{FE} = 50 (Min) @ I_C = 0.5 Adc
  = 10 (Min) @ I_C = 2.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) — MJE15032, MJE15033
- High Current Gain — Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO–220AB Compact Package

NPN
MJE15032*
PNP
MJE15033*

***ON Semiconductor Preferred Device**

8.0 AMPERES
POWER TRANSISTORS
COMPLEMENTARY
SILICON
250 VOLTS
50 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE15032 MJE15033	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CB}	250	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	8.0 16	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

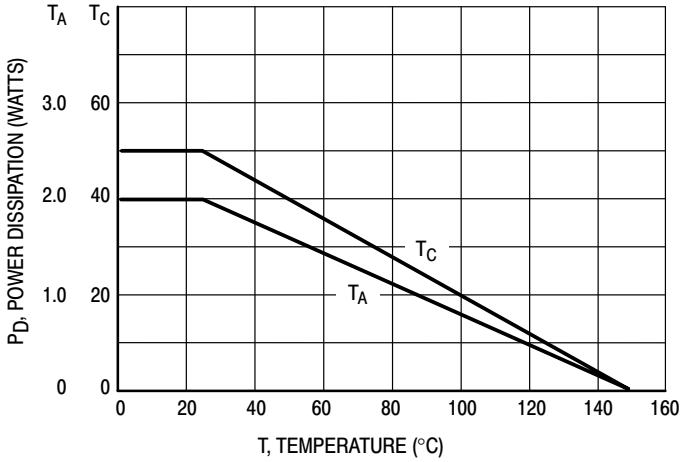


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 1
Publication Order Number:
MJE15032/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) MJE15032, MJE15033	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0) MJE15032, MJE15033	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 50 50 10	 — — —	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	30	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

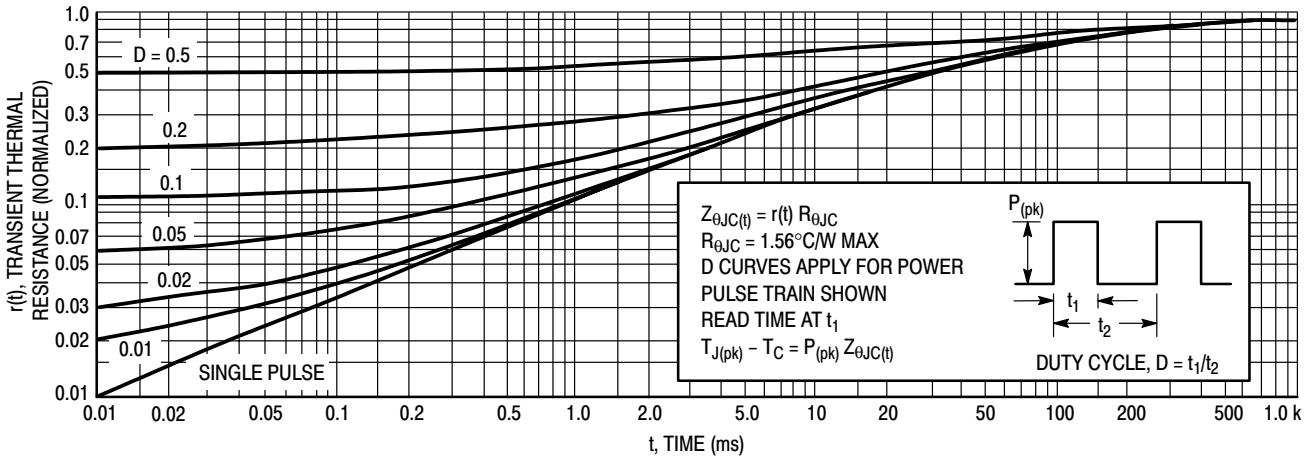


Figure 2. Thermal Response

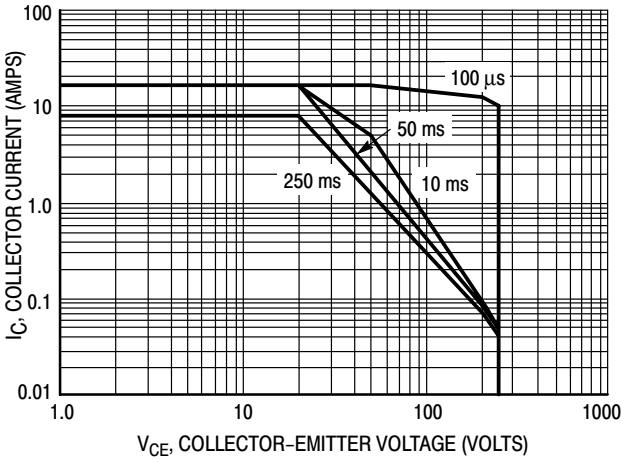


Figure 3. MJE15032 & MJE15033 Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN — MJE15032

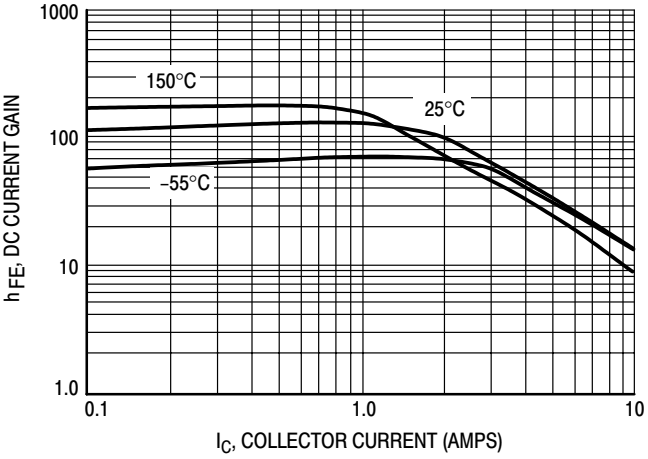


Figure 4. NPN — MJE15032 V_{CE} = 5 V DC Current Gain

PNP — MJE15033

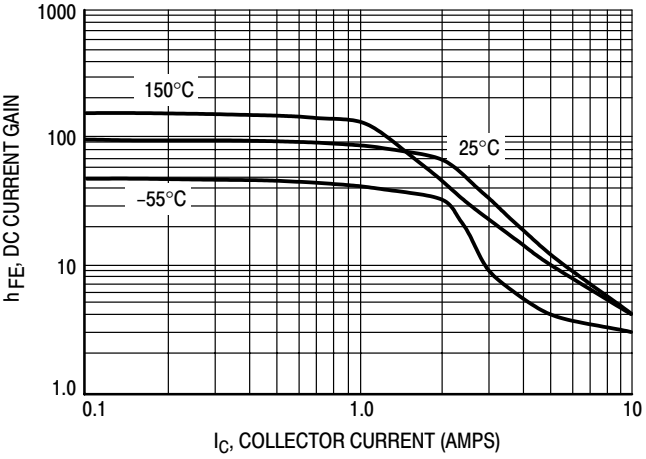


Figure 5. PNP — MJE15033 V_{CE} = 5 V DC Current Gain

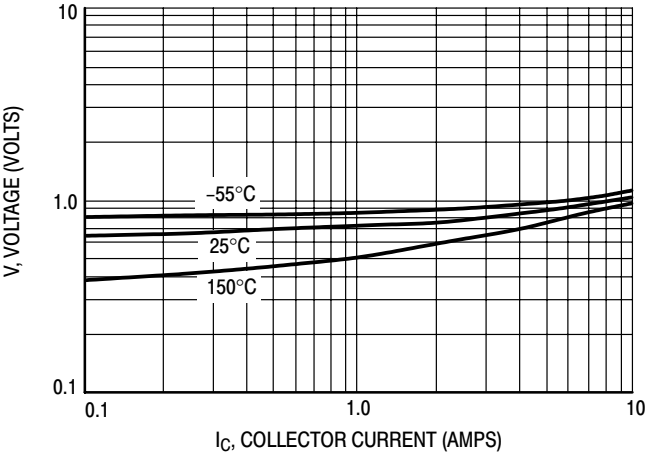


Figure 6. NPN — MJE15032 V_{CE} = 5 V $V_{BE(on)}$ Curve

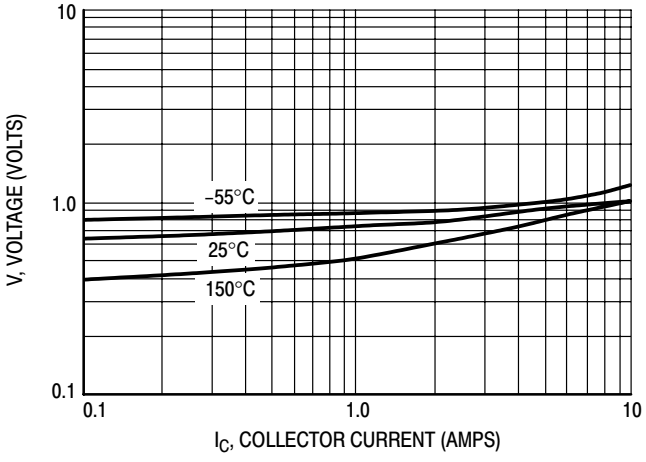


Figure 7. PNP — MJE15033 V_{CE} = 5 V $V_{BE(on)}$ Curve

NPN — MJE15032

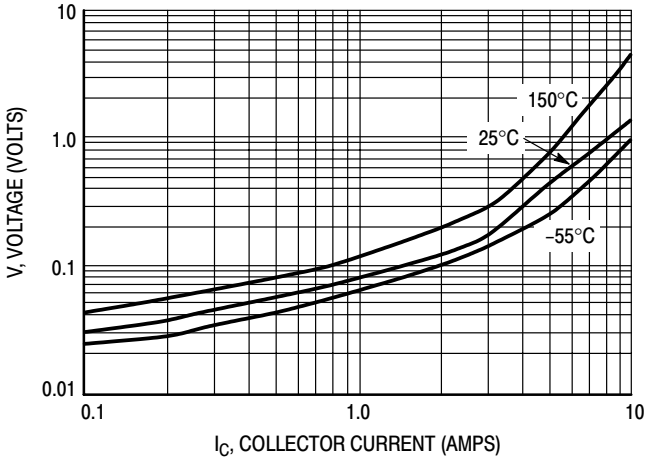


Figure 8. NPN — MJE15032
$V_{CE(sat)}$ I_C/I_B = 10

PNP — MJE15033

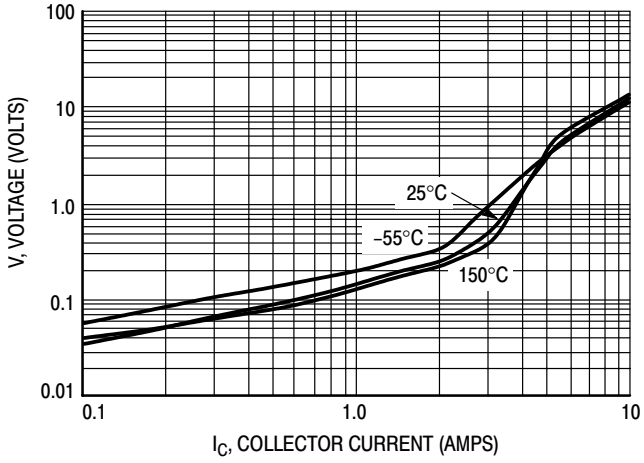


Figure 9. PNP — MJE15033
$V_{CE(sat)}$ I_C/I_B = 10

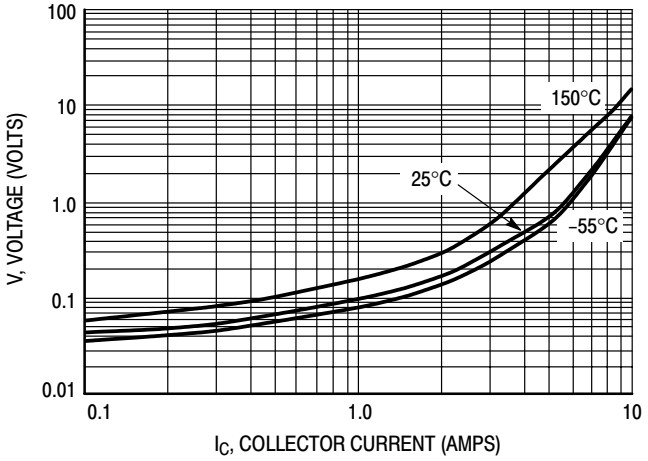


Figure 10. NPN — MJE15032
$V_{CE(sat)}$ I_C/I_B = 20

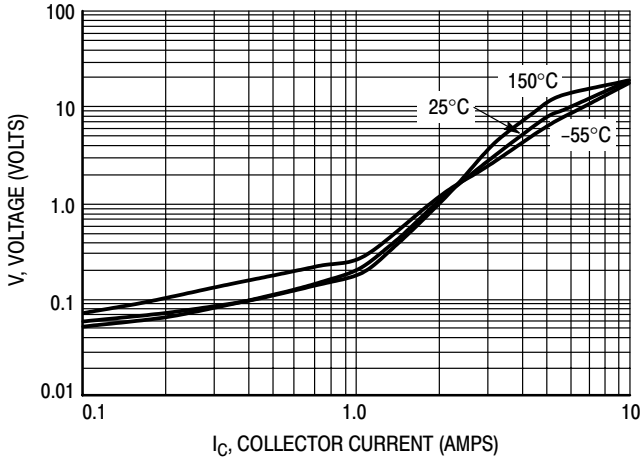


Figure 11. PNP — MJE15033
$V_{CE(sat)}$ I_C/I_B = 20

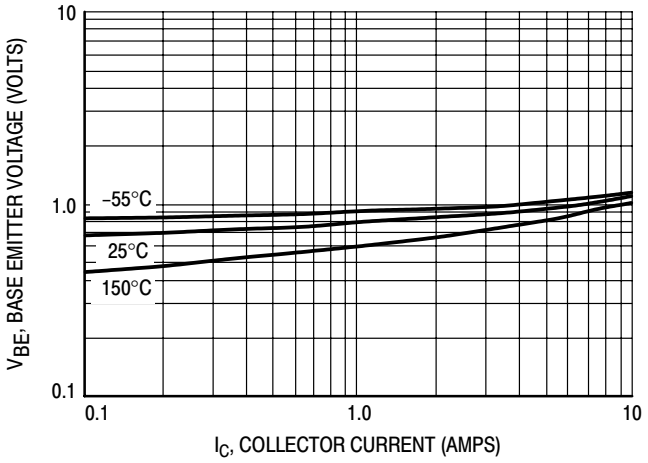


Figure 12. NPN — MJE15032
$V_{BE(sat)}$ I_C/I_B = 10

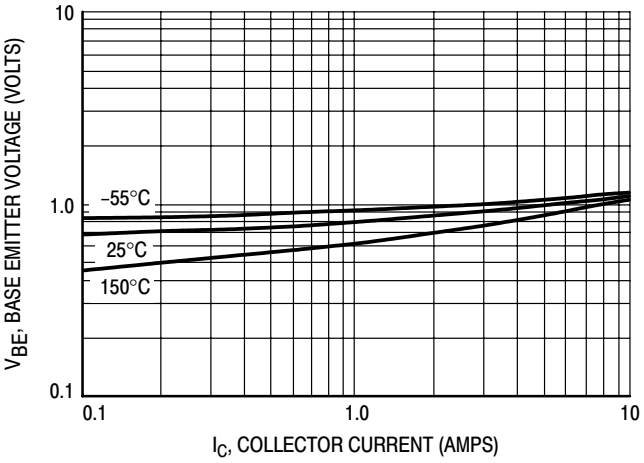


Figure 13. PNP — MJE15033
$V_{BE(sat)}$ I_C/I_B = 10

Complementary Plastic Silicon Power Transistors

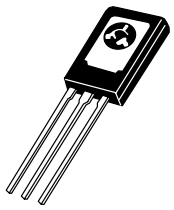
. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc — MJE171, MJE181
  = 80 Vdc — MJE172, MJE182
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current–Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C
  = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

PNP
MJE171*
MJE172*
NPN
MJE181*
MJE182*

*ON Semiconductor Preferred Device

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80 VOLTS
12.5 WATTS



CASE 77–09
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	MJE171 MJE181	MJE172 MJE182	Unit
Collector–Base Voltage	V_{CB}	80	100	Vdc
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	3.0 6.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 4
Publication Order Number:
MJE171/D

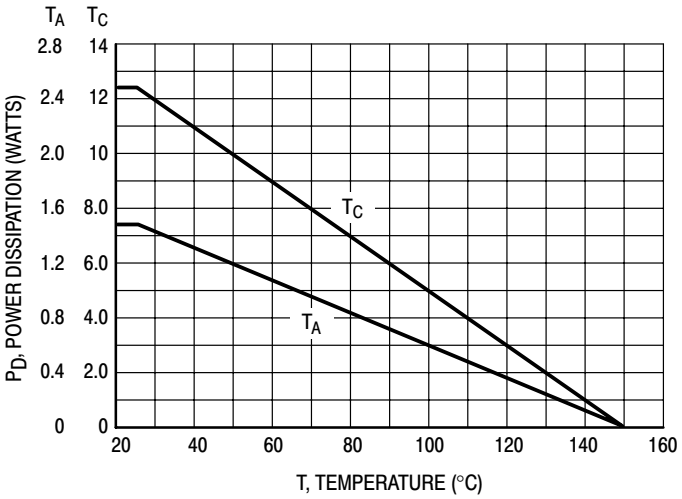


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE171, MJE181	$V_{CEO(sus)}$	60	—	Vdc
	MJE172, MJE182		80	—	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		—	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		—	0.1	
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		—	0.1	mAdc
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		—	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	—	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			—	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			—	1.7	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			—	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			—	2.0	
Base–Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	—	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE171/MJE172		—	60	
	MJE181/MJE182		—	40	

(1) $f_T = |h_{fe}| \bullet f_{test}$.

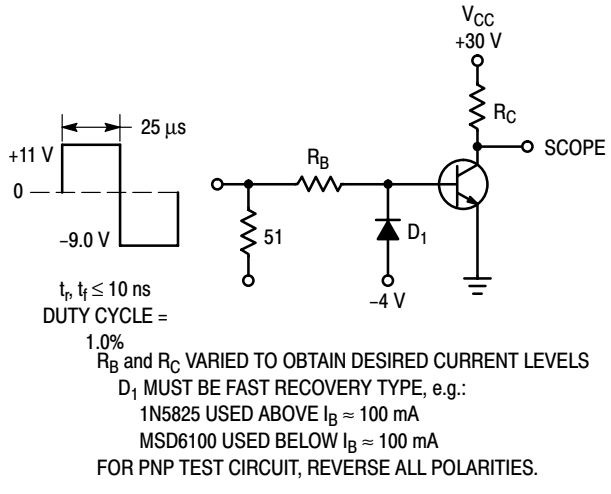


Figure 2. Switching Time Test Circuit

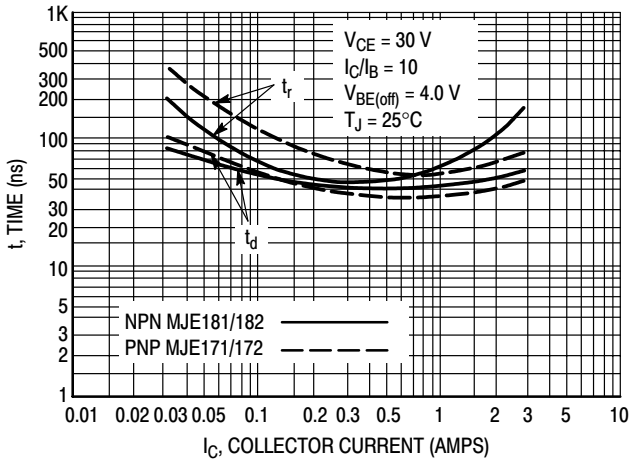


Figure 3. Turn–On Time

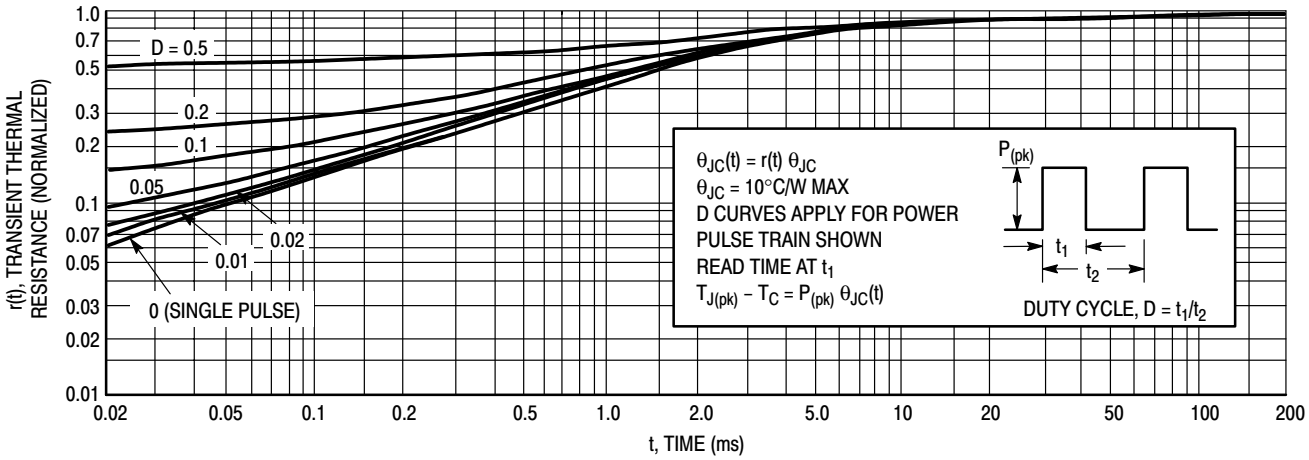


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

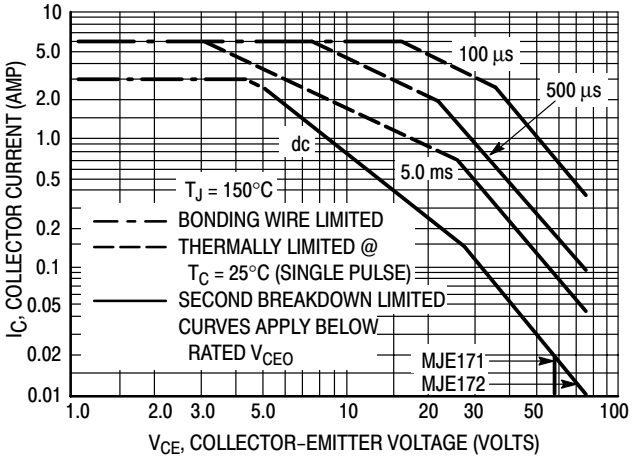


Figure 5. MJE171, MJE172

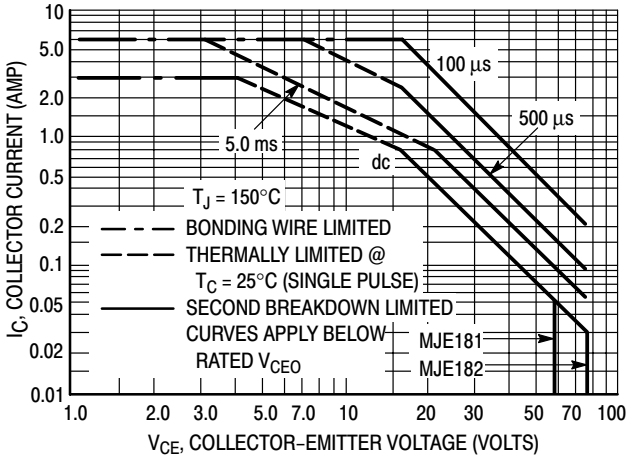


Figure 6. MJE181, MJE182

There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

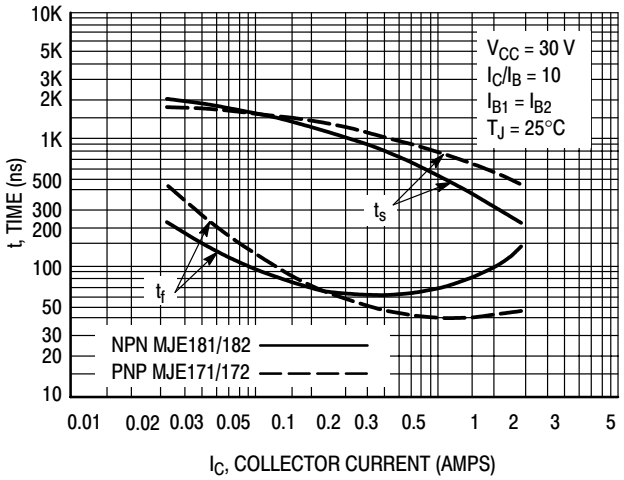


Figure 7. Turn−Off Time

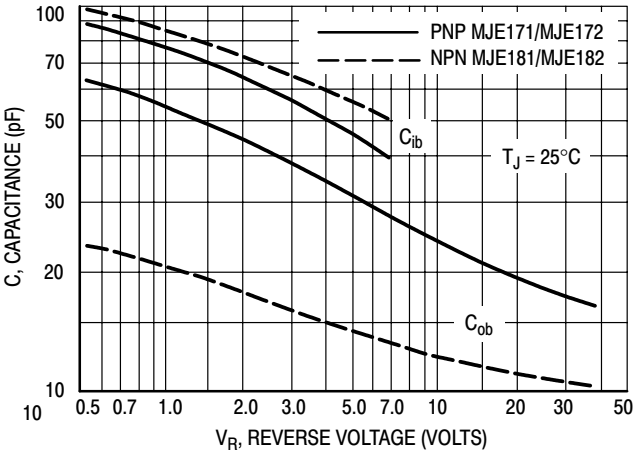


Figure 8. Capacitance

MJE18002*

*ON Semiconductor Preferred Device

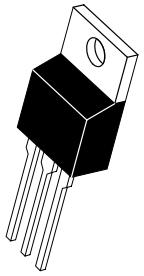
SWITCHMODE™

NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE18002 have an applications specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Standard TO–220

POWER TRANSISTOR
2.0 AMPERES
1000 VOLTS
50 WATTS



CASE 221A–09
TO–220AB
MJE18002

MAXIMUM RATINGS

Rating	Symbol	MJE18002	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	9.0	Vdc
Collector Current – Continuous – Peak(1)	I_C I_{CM}	2.0 5.0	Adc
Base Current – Continuous – Peak(1)	I_B I_{BM}	1.0 2.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18002	Unit
Thermal Resistance – Junction to Case – Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) T_C = 125°C	I_{CES}	–	–	100	μAdc
(V_{CE} = 800 V, V_{EB} = 0) T_C = 125°C		–	–	500	
		–	–	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	–	0.825	1.1	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)		–	0.92	1.25	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)		–	0.2	0.5	
@ T_C = 125°C		–	0.2	0.5	
(I_C = 1.0 Adc, I_B = 0.2 Adc)		–	0.25	0.5	
@ T_C = 125°C		–	0.3	0.6	
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	–	34	–
@ T_C = 125°C		–	27	–	
(I_C = 0.4 Adc, V_{CE} = 1.0 Vdc)		11	17	–	
@ T_C = 125°C		11	20	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		6.0	8.0	–	
@ T_C = 125°C		5.0	8.0	–	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	–	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	–	13	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	35	60	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{ib}	–	400	600	pF
Dynamic Saturation: determined 1.0 μs and 3.0 μs after rising I_{B1} reach 0.9 final I_{B1} (see Figure 18)	$V_{CE(dsat)}$				Vdc
I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V; 1.0 μs; @ T_C = 125°C		–	3.5	–	
		–	8.0	–	
I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V; 3.0 μs; @ T_C = 125°C		–	1.5	–	
		–	3.8	–	
I_C = 1.0 A, I_{B1} = 0.2 A, V_{CC} = 300 V; 1.0 μs; @ T_C = 125°C		–	8.0	–	
		–	14	–	
I_C = 1.0 A, I_{B1} = 0.2 A, V_{CC} = 300 V; 3.0 μs; @ T_C = 125°C		–	2.0	–	
		–	7.0	–	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–On Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 0.2 Adc V_{CC} = 300 V		t_{on}	– –	200 130	300 –	ns
Turn–Off Time		@ T_C = 125°C	t_{off}	– –	1.2 1.5	2.5 –	μs
Turn–On Time	I_C = 1.0 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc V_{CC} = 300 V		t_{on}	– –	85 95	150 –	ns
Turn–Off Time		@ T_C = 125°C	t_{off}	– –	1.7 2.1	2.5 –	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 0.2 Adc		t_{fi}	– –	125 120	200 –	ns
Storage Time		@ T_C = 125°C	t_{si}	– –	0.7 0.8	1.25 –	μs
Crossover Time		@ T_C = 125°C	t_c	– –	110 110	200 –	ns
Fall Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc	@ T_C = 125°C	t_{fi}	– –	110 120	175 –	ns
Storage Time		@ T_C = 125°C	t_{si}	– –	1.7 2.25	2.75 –	μs
Crossover Time		@ T_C = 125°C	t_c	– –	200 250	300 –	ns
Fall Time	I_C = 0.4 Adc, I_{B1} = 50 mAdc, I_{B2} = 50 mAdc	@ T_C = 125°C	t_{fi}	– –	140 185	200 –	ns
Storage Time		@ T_C = 125°C	t_{si}	– –	2.2 2.5	3.0 –	μs
Crossover Time		@ T_C = 125°C	t_c	– –	140 220	250 –	ns

TYPICAL STATIC CHARACTERISTICS

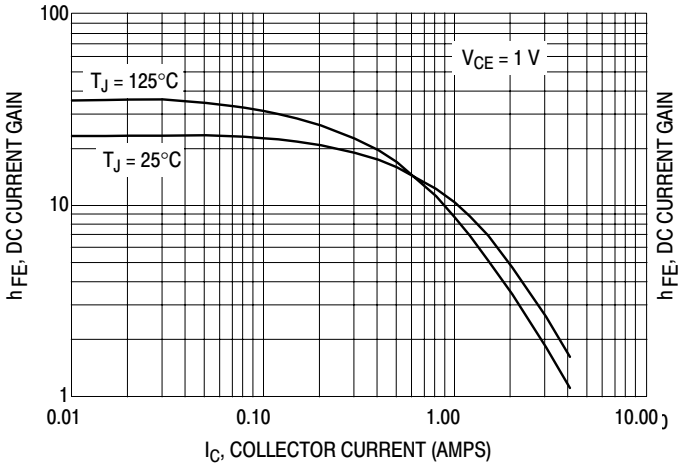


Figure 1. DC Current Gain @ 1 Volt

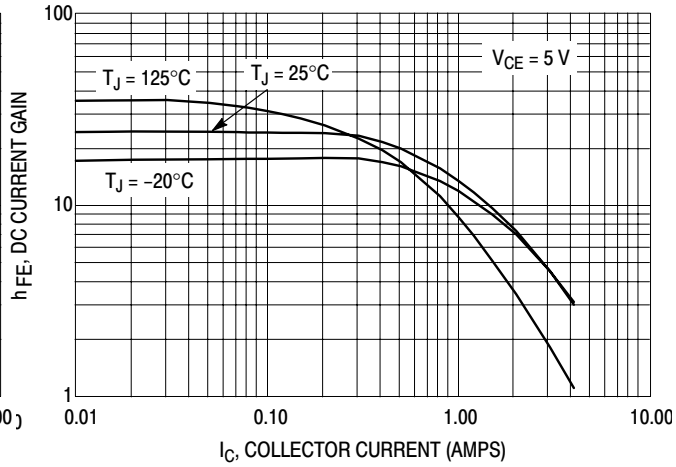


Figure 2. DC Current Gain @ 5 Volts

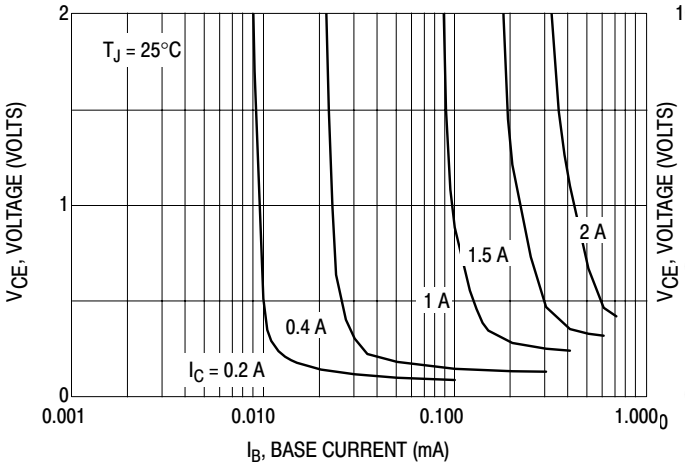


Figure 3. Collector Saturation Region

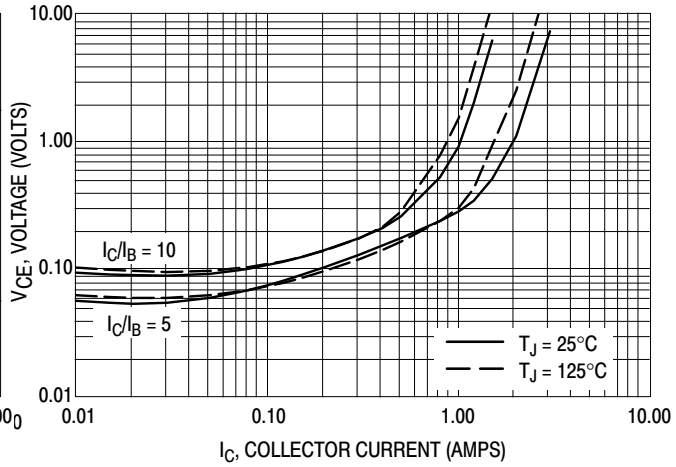


Figure 4. Collector–Emitter Saturation Voltage

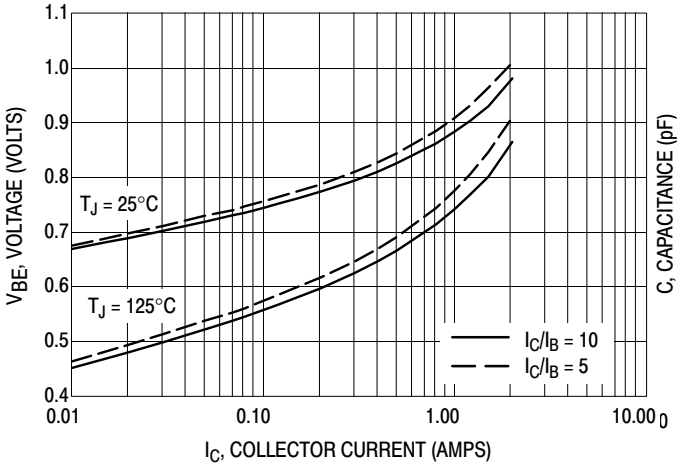


Figure 5. Base–Emitter Saturation Region

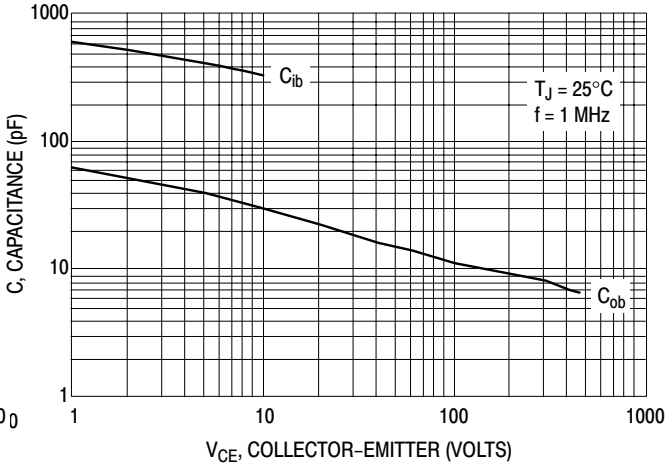


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

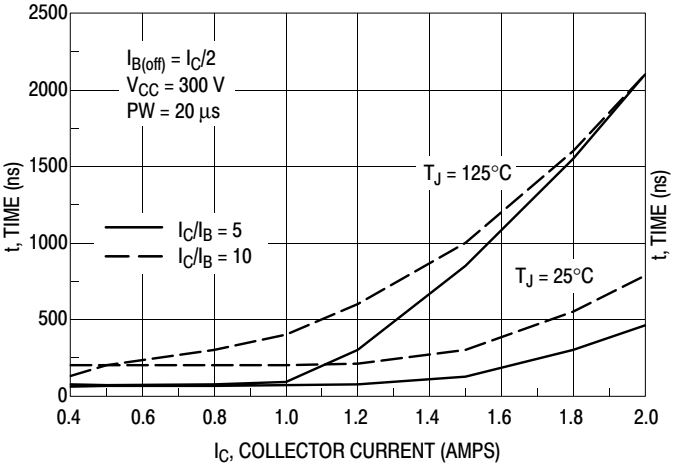


Figure 7. Resistive Switching, t_{on}

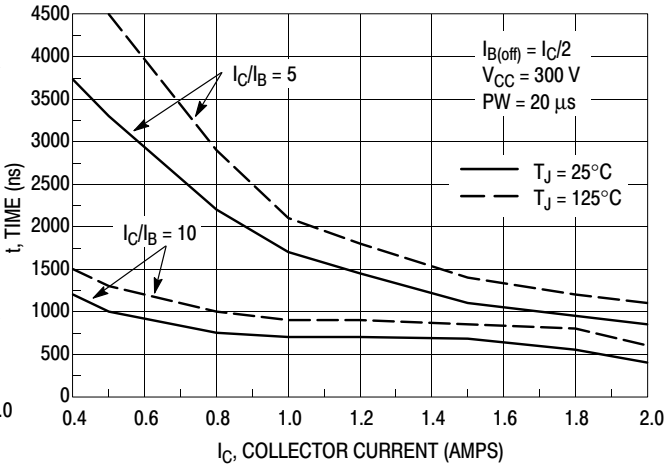


Figure 8. Resistive Switching, t_{off}

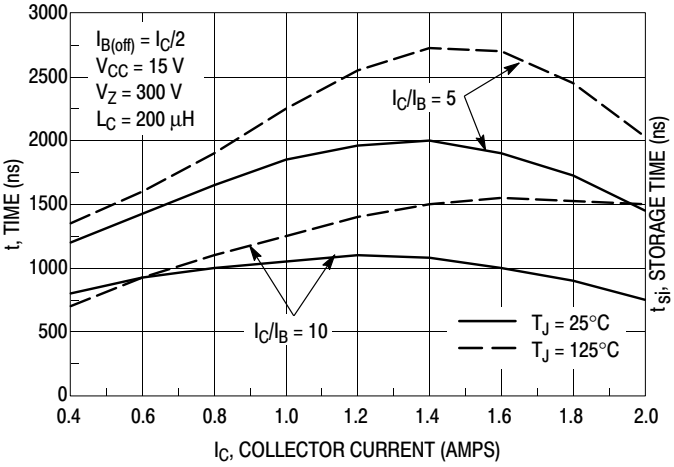


Figure 9. Inductive Storage Time, t_{si}

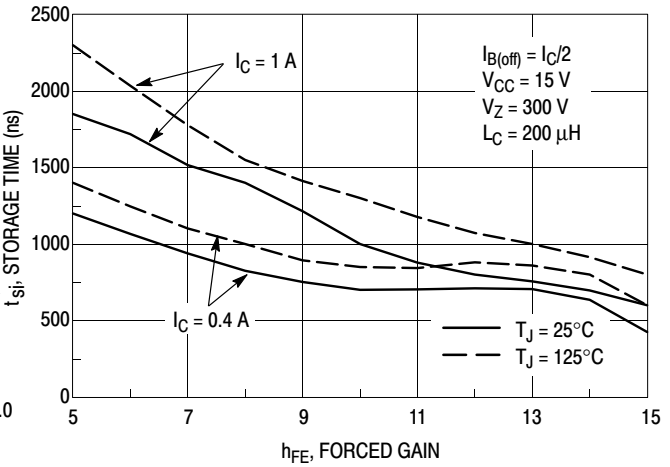


Figure 10. Inductive Storage Time

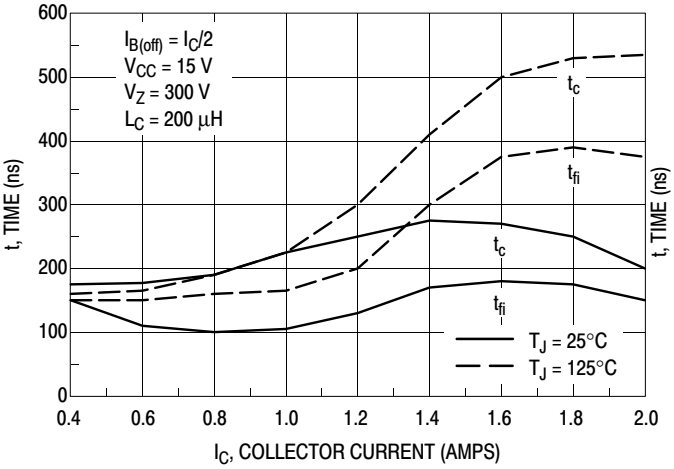


Figure 11. Inductive Switching, t_c and t_{fi}, I_C/I_B = 5

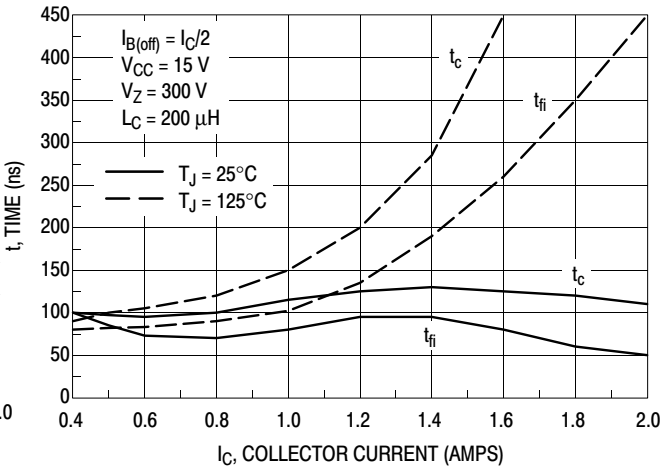


Figure 12. Inductive Switching, t_c and t_{fi}, I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

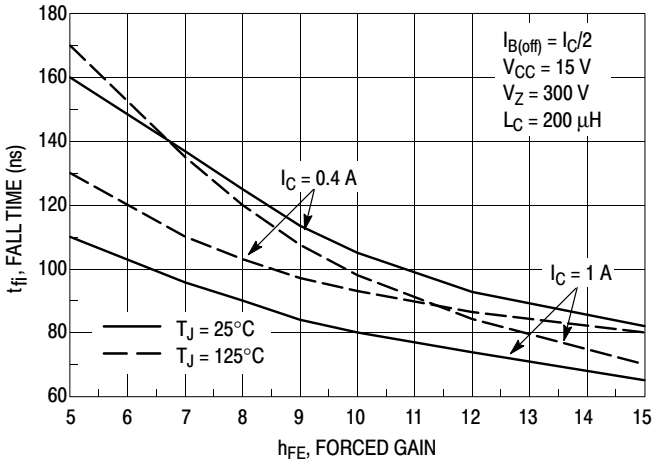


Figure 13. Inductive Fall Time

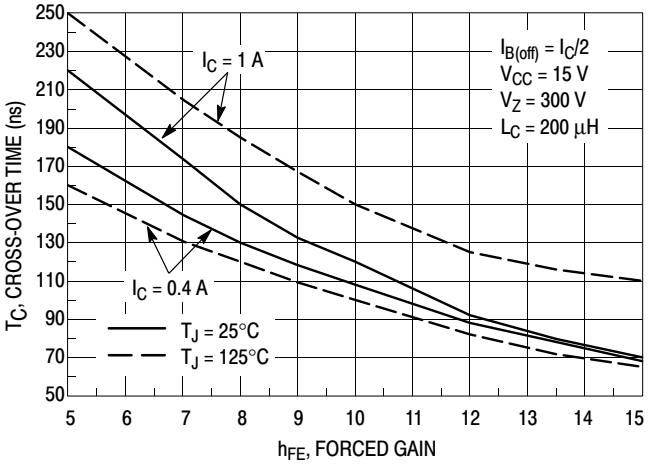


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

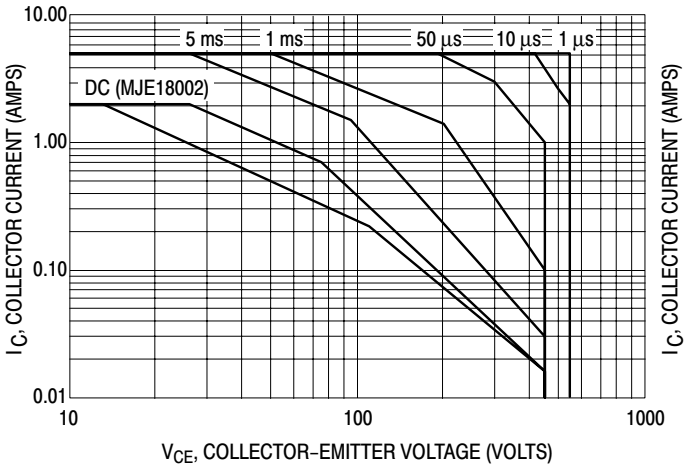


Figure 15. Forward Bias Safe Operating Area

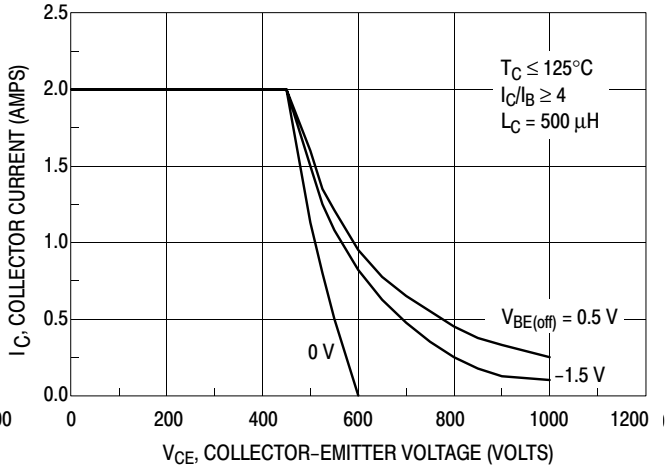


Figure 16. Reverse Bias Switching Safe Operating Area

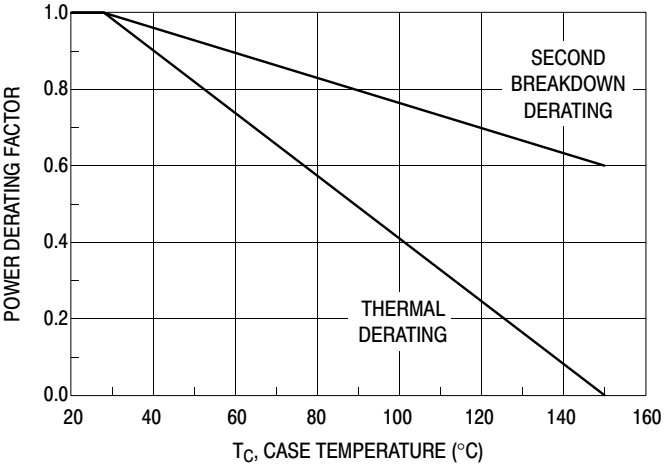


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. T_J(pk) may be calculated from the data in Figures 20 and NO TAG. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

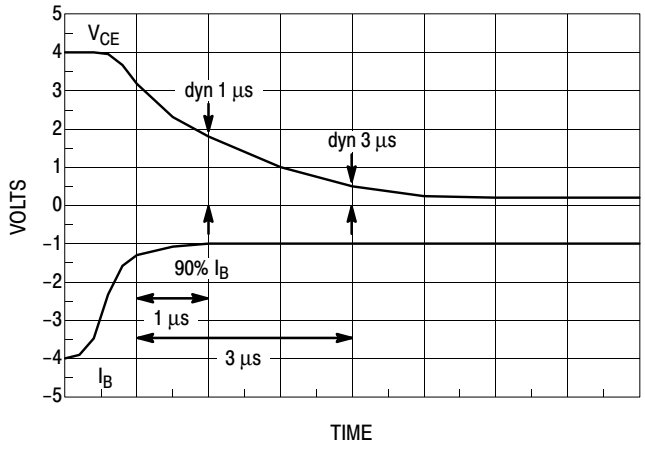


Figure 18. Dynamic Saturation Voltage Measurements

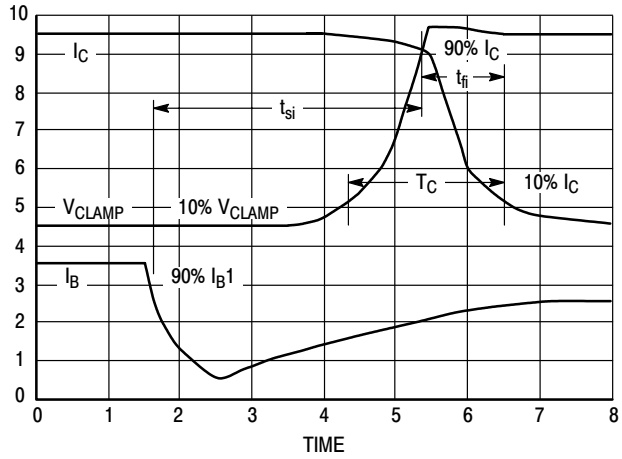
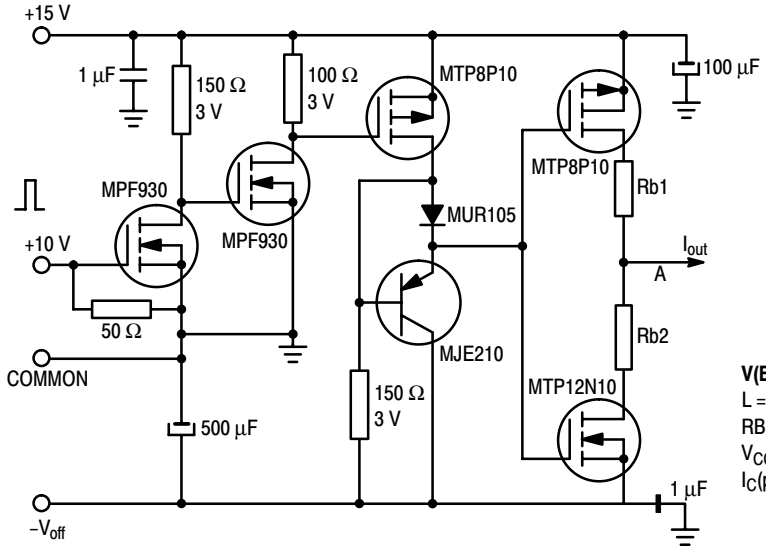
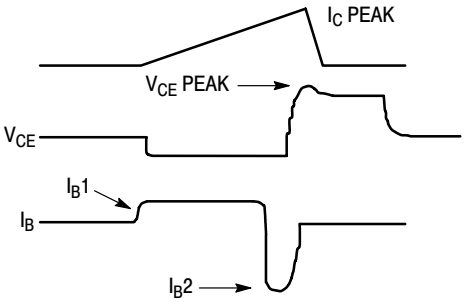


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 μH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

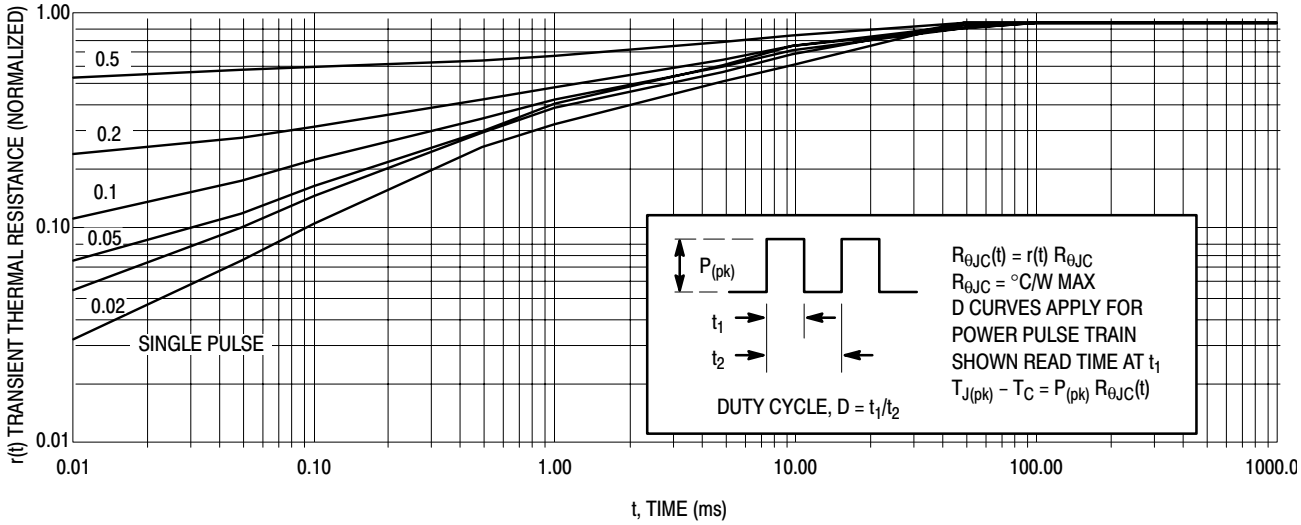
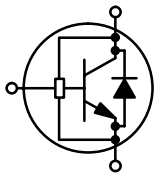


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18002

MJE18004D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
5 AMPERES
1000 VOLTS
75 WATTS

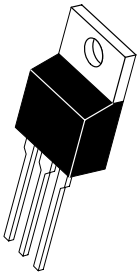


The MJE18004D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)f

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	547		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	1000	1100		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.9 0.8	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.45 0.75	0.75 1	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.9 1.6	1.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.25 0.28	0.5 0.6	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 10	28 14		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	8 6		
(I_C = 1 Adc, V_{CE} = 2.5 Vdc)	@ T_C = 25°C @ T_C = 125°C		18 14	28 20		
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc I_{B1} = 100 mA V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	9 16	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		3.1 9	
	I_C = 2 Adc I_{B1} = 0.4 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		11 18	
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		1.4 8	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 1 Adc)		@ T_C = 25°C @ T_C = 125°C	V_{EC}		0.96 0.72	1.5	V
(I_{EC} = 2 Adc)		@ T_C = 25°C @ T_C = 125°C			1.15 0.8	1.7	
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/μs)		@ T_C = 25°C	t_{fr}		440		ns
(I_F = 1 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
(I_F = 2 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		60	100	pF
Input Capacitance (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			C_{ib}		450	750	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 1 Adc V_{CC} = 250 Vdc	@ T_C = 25°C	t_{on}		500	750	ns
Turn–off Time		@ T_C = 25°C	t_{off}	1.1		1.4	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		100 150	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.6	1.3	μs
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		120 500	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	1.85	 2.6	2.15	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 2.5 Adc I_{B1} = 500 mAdc I_{B2} = 500 mAdc V_Z = 350 V L_C = 300 μH	@ T_C = 25°C @ T_C = 125°C	t_f		130 300	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.12 2.6	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		355 750	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 400 mAdc I_{B2} = 400 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		95 230	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 2.9	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		300 700	450	ns
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		70 100	90	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.7 1.05	0.9	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		75 160	120	ns

TYPICAL STATIC CHARACTERISTICS

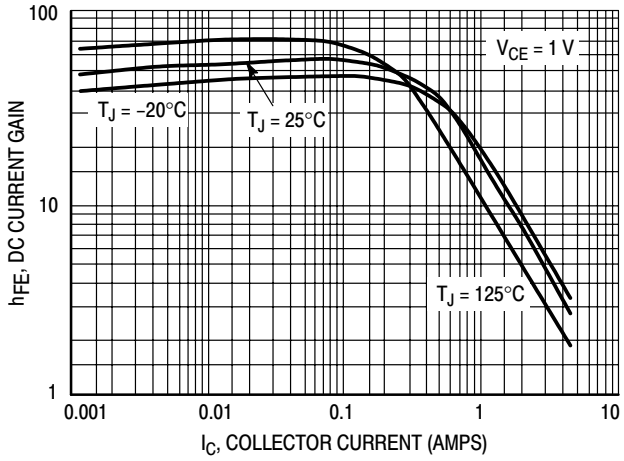


Figure 1. DC Current Gain @ 1 Volt

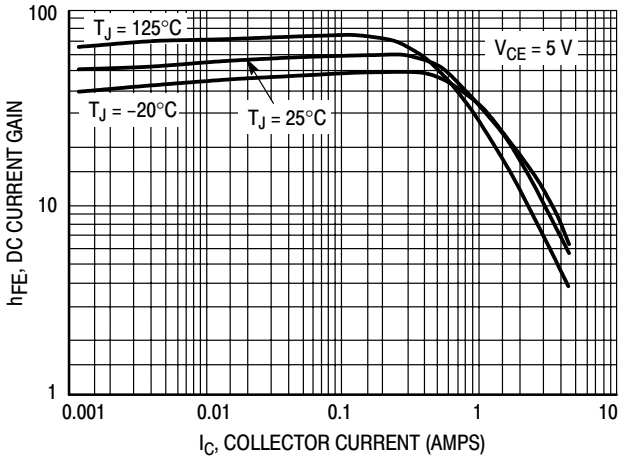


Figure 2. DC Current Gain @ 5 Volt

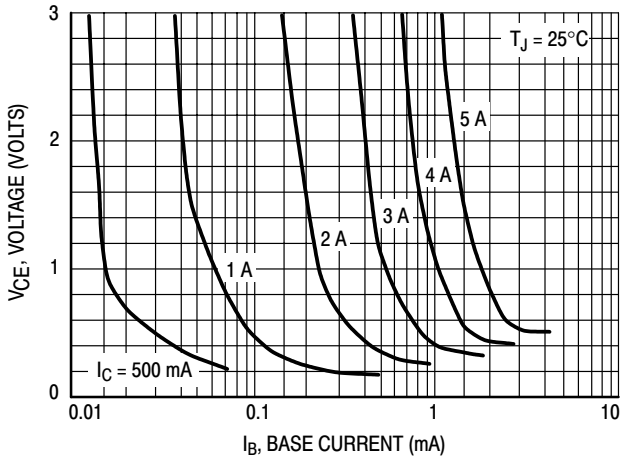


Figure 3. Collector Saturation Region

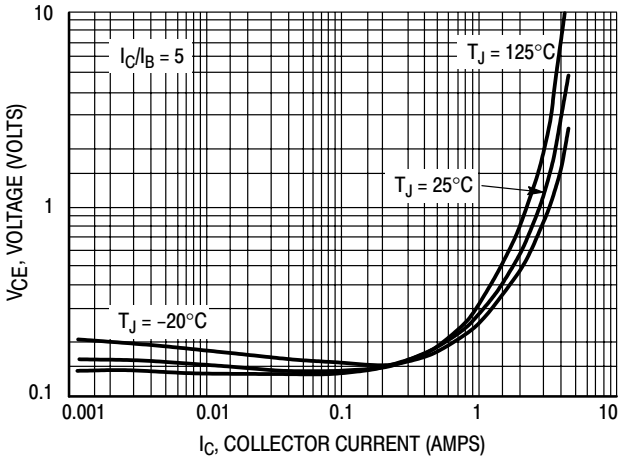


Figure 4. Collector–Emitter Saturation Voltage

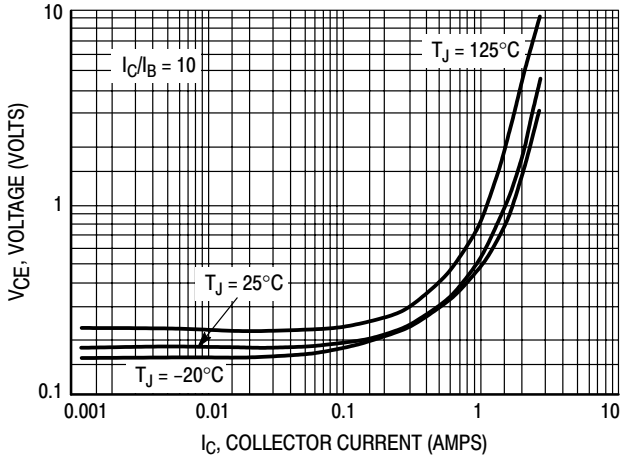


Figure 5. Collector–Emitter Saturation Voltage

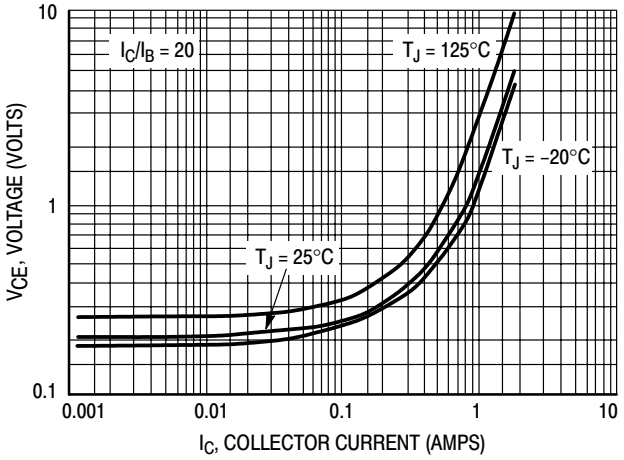


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

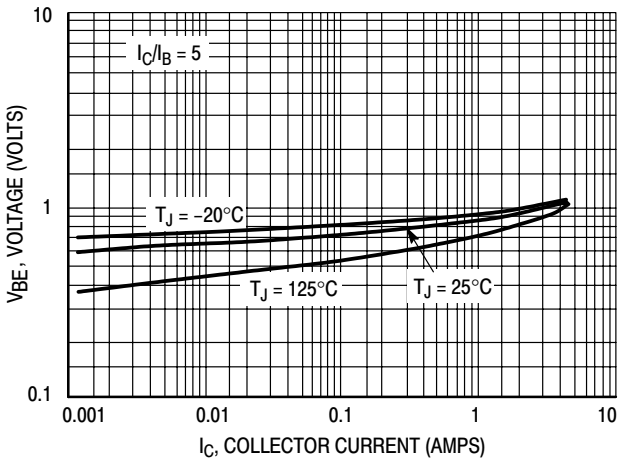


Figure 7. Base–Emitter Saturation Region

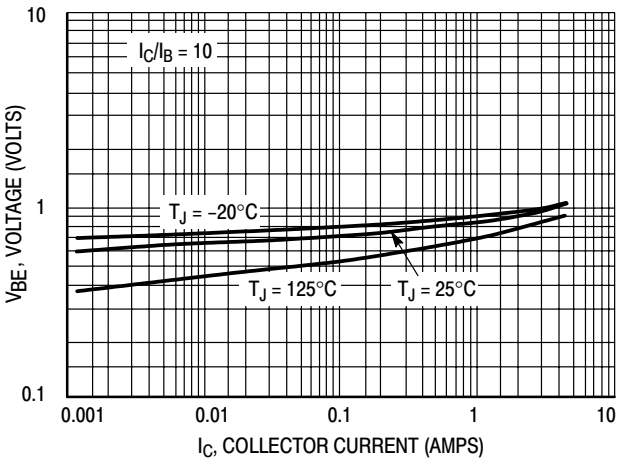


Figure 8. Base–Emitter Saturation Region

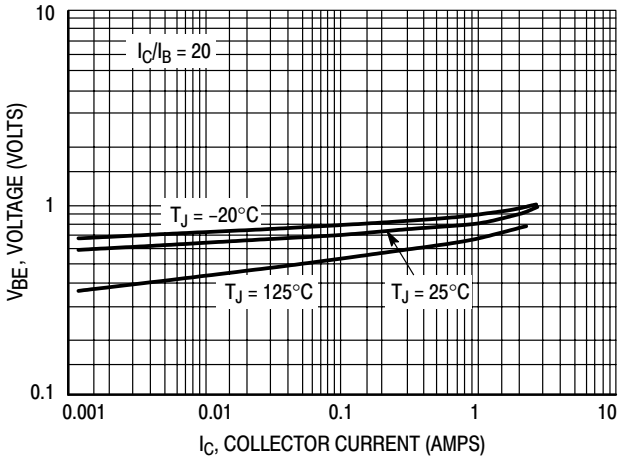


Figure 9. Base–Emitter Saturation Region

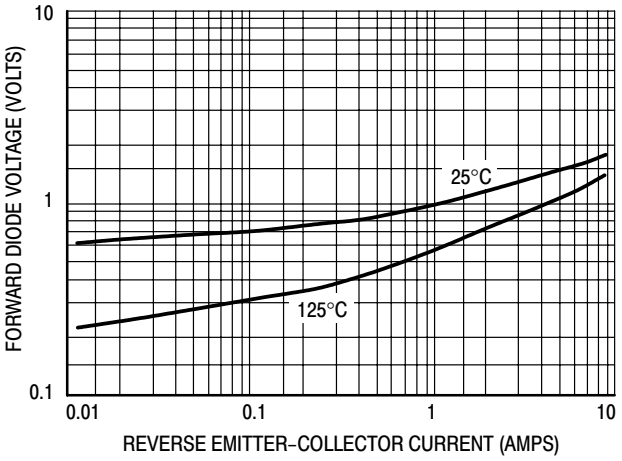


Figure 10. Forward Diode Voltage

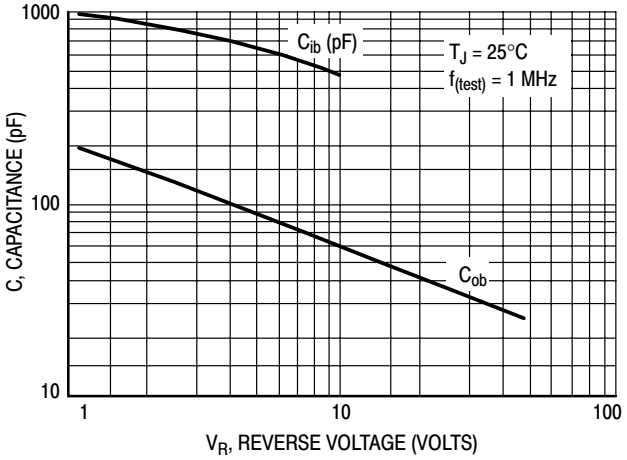


Figure 11. Capacitance

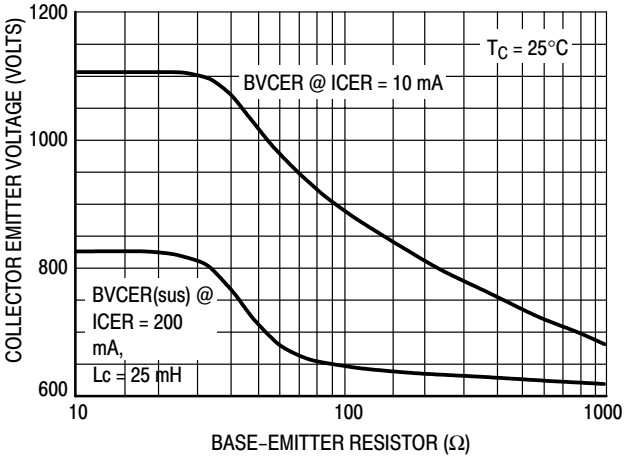


Figure 12. BVCER = f(R_{BE})

TYPICAL SWITCHING CHARACTERISTICS

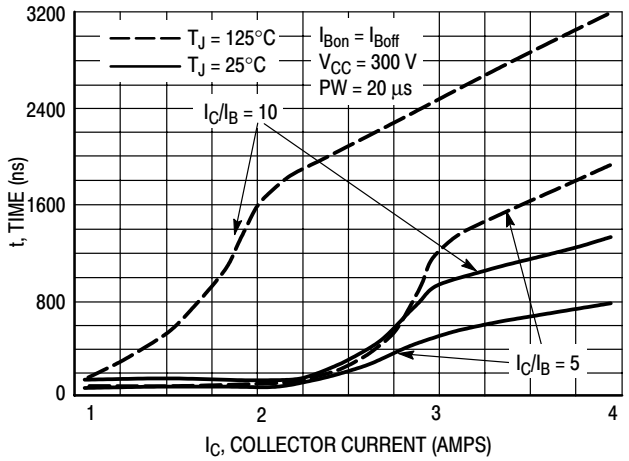


Figure 13. Resistive Switch Time, t_{on}

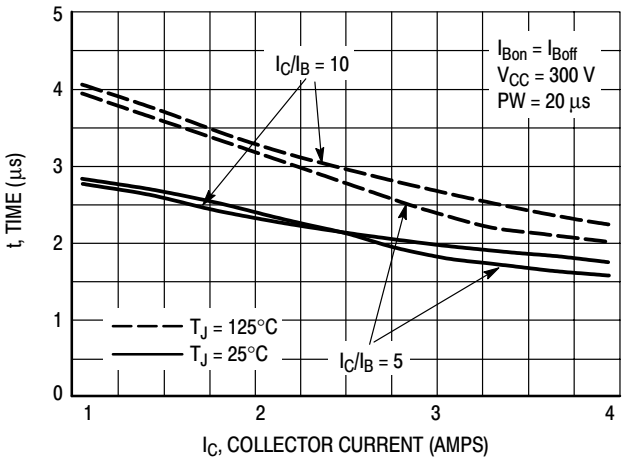


Figure 14. Resistive Switch Time, t_{off}

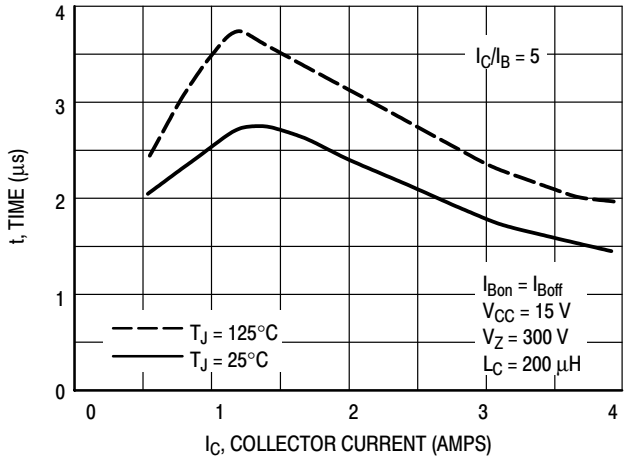


Figure 15. Inductive Storage Time, t_{si} @ I_C/I_B = 5

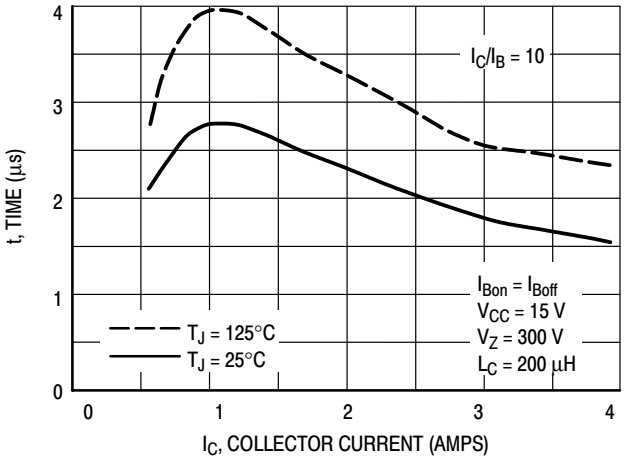


Figure 16. Inductive Storage Time, t_{si} @ I_C/I_B = 10

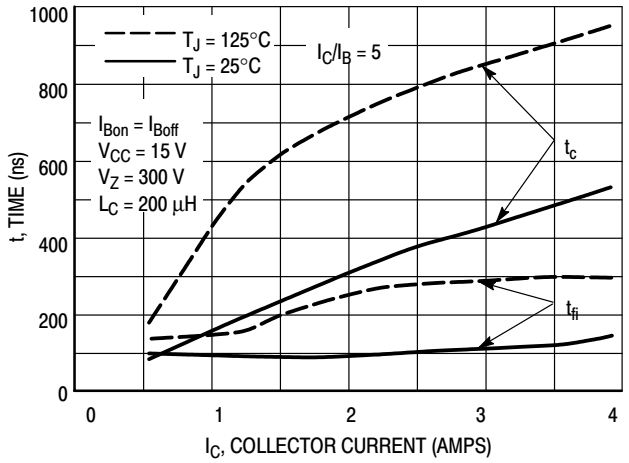


Figure 17. Inductive Switching Time, t_c and t_{fi} @ I_C/I_B = 5

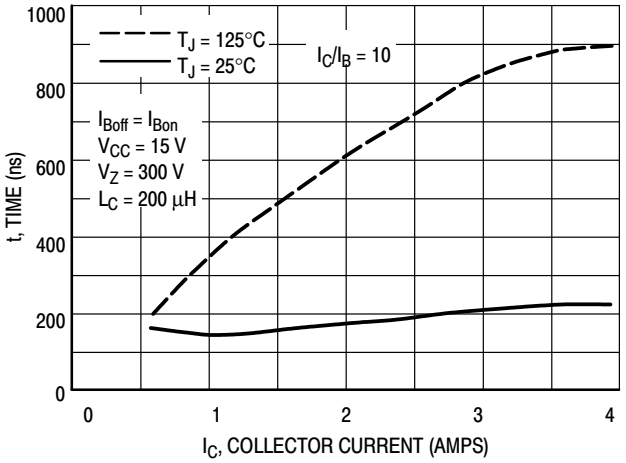


Figure 18. Inductive Switching Time, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

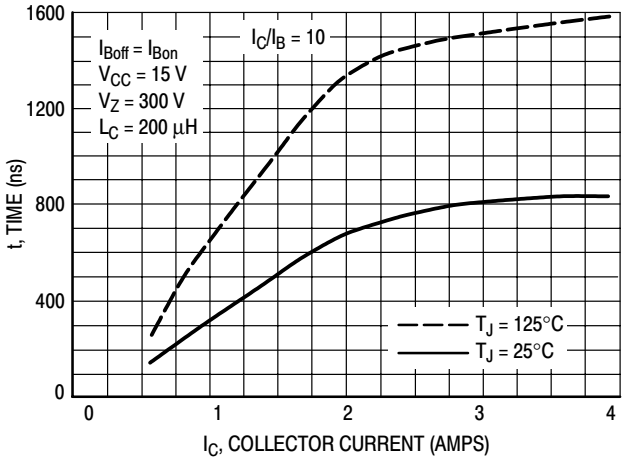


Figure 19. Inductive Switching, t_c @ I_C/I_B = 10

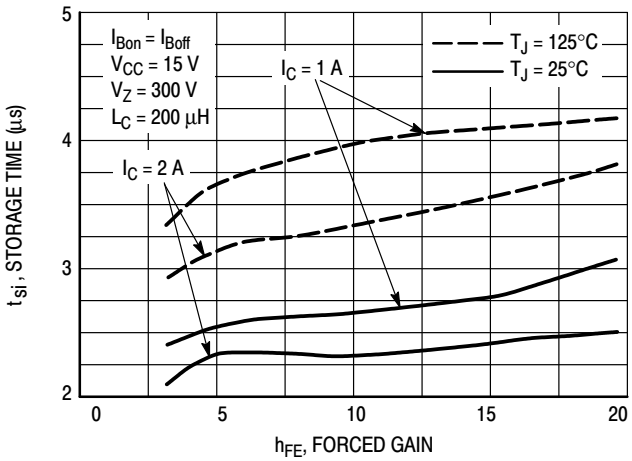


Figure 20. Inductive Storage Time

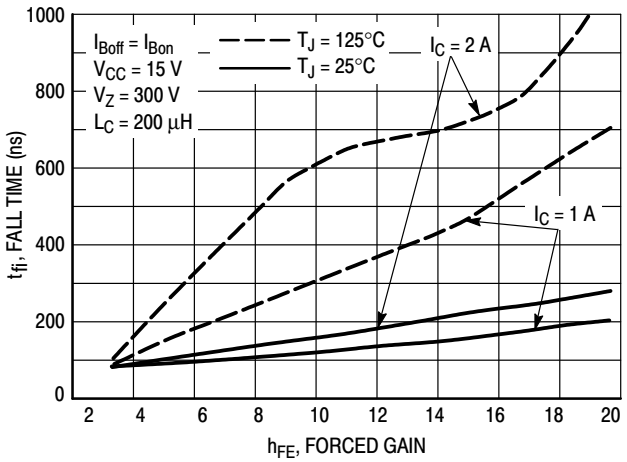


Figure 21. Inductive Fall Time

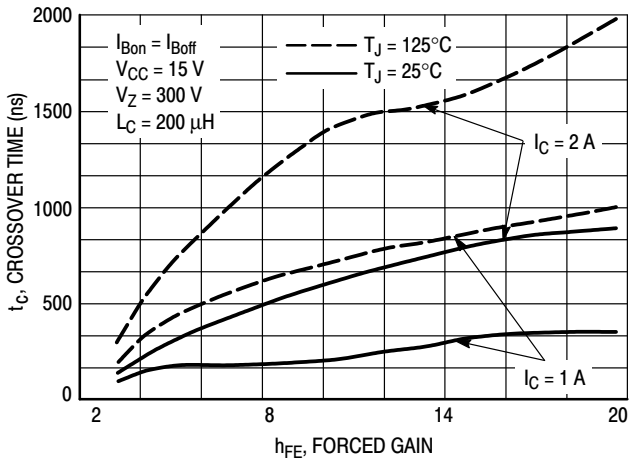


Figure 22. Inductive Crossover Time

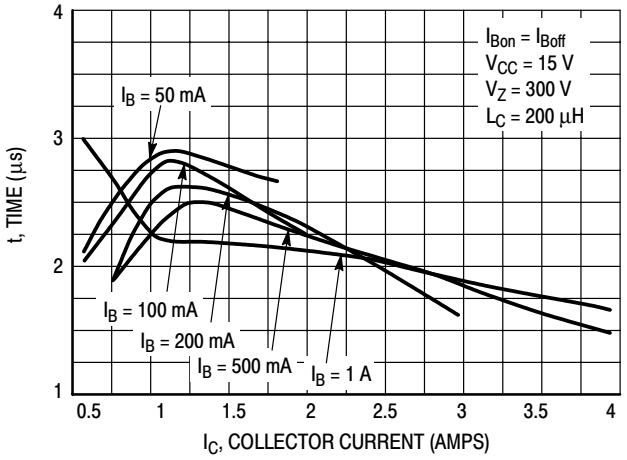


Figure 23. Inductive Storage Time, t_{si}

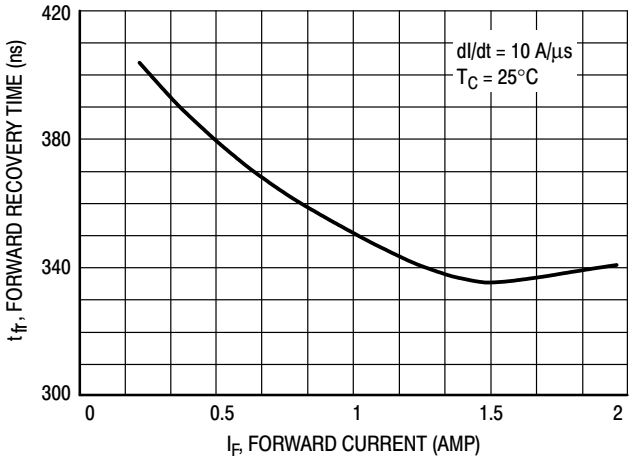


Figure 24. Forward Recovery Time, T_{FR}

TYPICAL SWITCHING CHARACTERISTICS

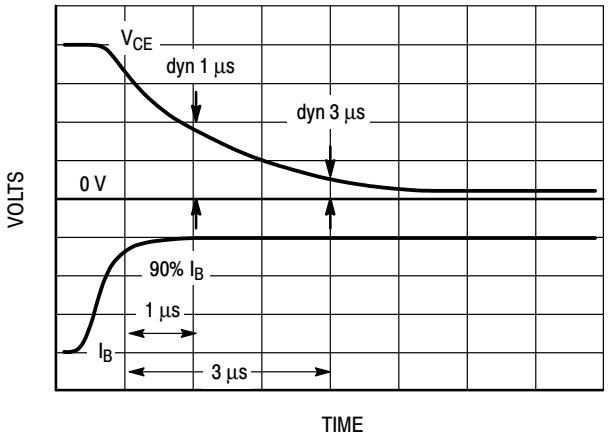


Figure 25. Dynamic Saturation Voltage Measurements

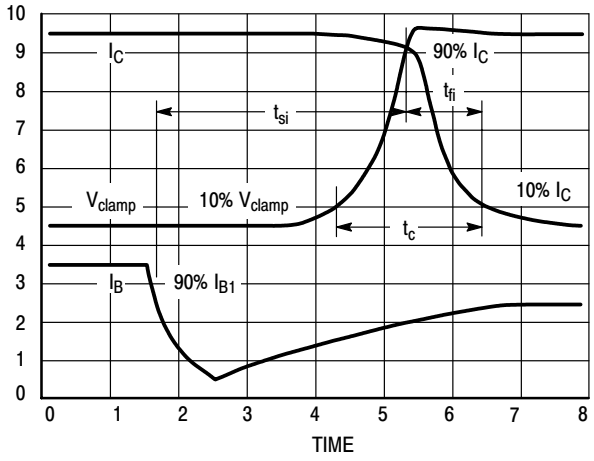


Figure 26. Inductive Switching Measurements

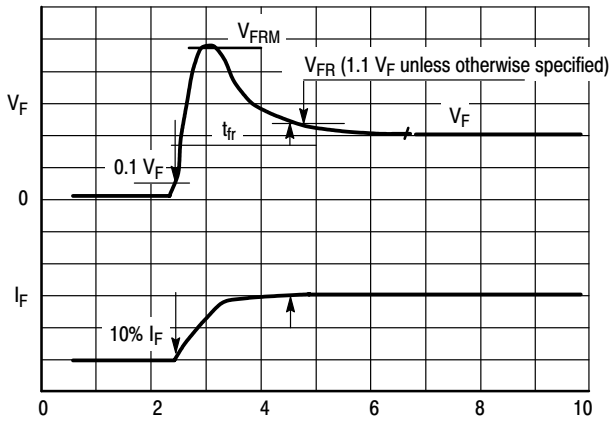
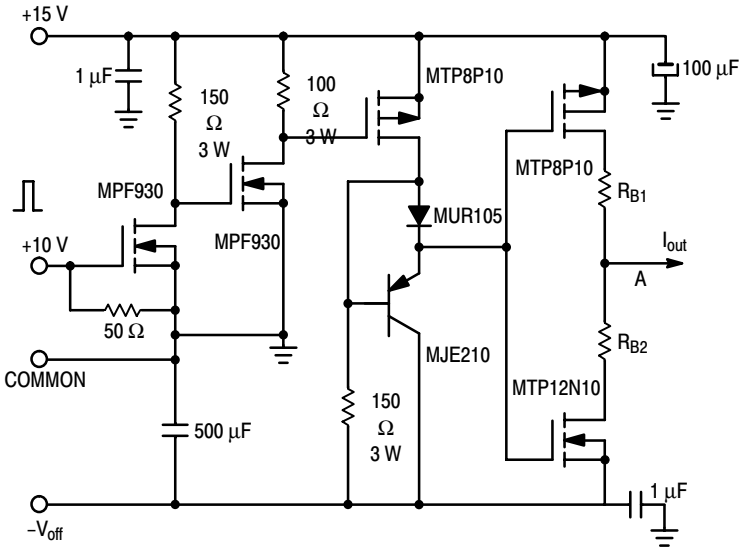
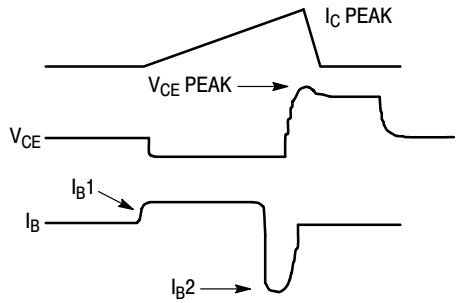


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	RB1 selected for desired Ib1	RB1 selected for desired Ib1

TYPICAL CHARACTERISTICS

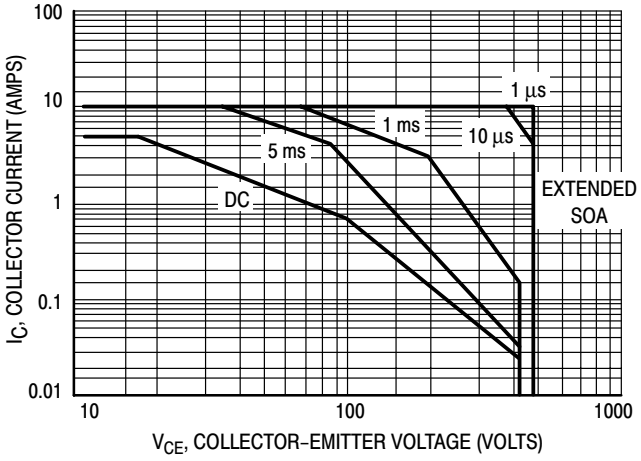


Figure 28. Forward Bias Safe Operating Area

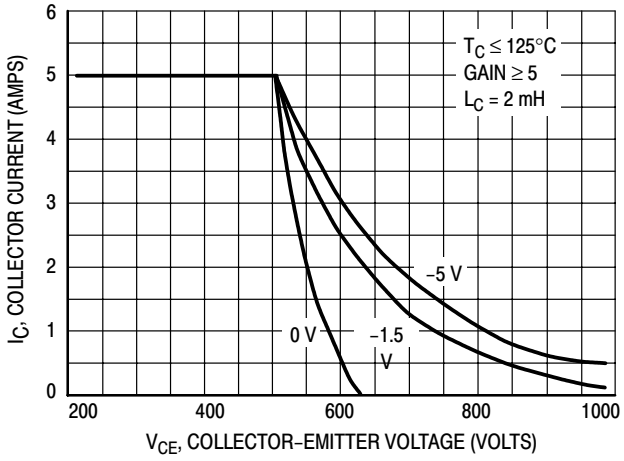


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

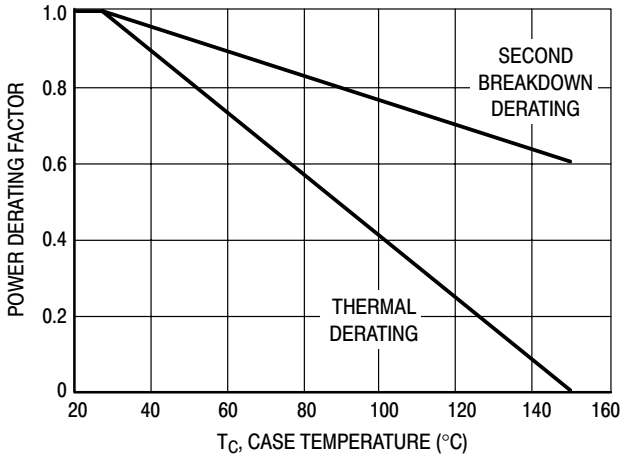


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

T_J(pk) may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

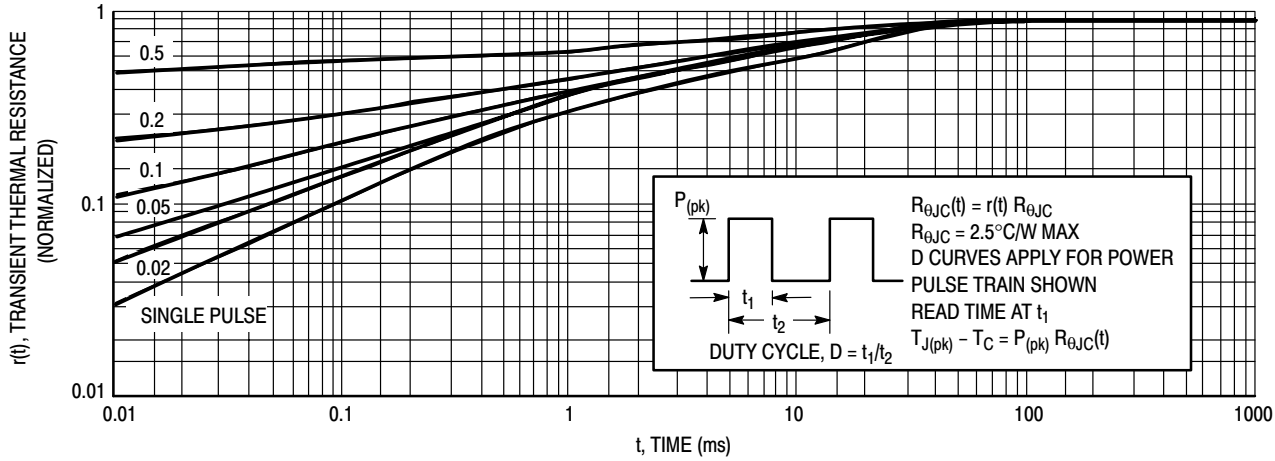


Figure 31. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004D2

MJE18004 *
MJF18004 *

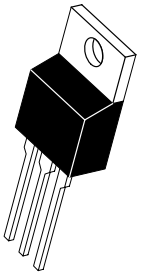
*ON Semiconductor Preferred Device

POWER TRANSISTOR
5.0 AMPERES
1000 VOLTS
35 and 75 WATTS

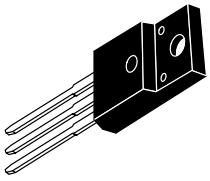
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE/MJF18004 have an applications specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. This high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF18004, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A–09
TO–220AB
MJE18004



CASE 221D–02
ISOLATED TO–220 TYPE
MJF18004

MAXIMUM RATINGS

Rating	Symbol	MJE18004	MJF18004	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	2.0 4.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. Test No. 2 Per Fig. 22b < 30%, T_A = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	35 0.28	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18004	MJF18004	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)				$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)				I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	(T_C = 25°C)			I_{CES}	—	—	100	μAdc
	(T_C = 125°C)				—	—	500	
(V_{CE} = 800 V, V_{EB} = 0)	(T_C = 125°C)				—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)				I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)				$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)					—	0.92	1.25	
Collector–Emitter Saturation Voltage				$V_{CE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)					—	0.25	0.5	
	(T_C = 125°C)				—	0.29	0.6	
(I_C = 2.0 Adc, I_B = 0.4 Adc)					—	0.3	0.45	
	(T_C = 125°C)				—	0.36	0.8	
(I_C = 2.5 Adc, I_B = 0.5 Adc)					—	0.5	0.75	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 2.5 Vdc)				h_{FE}	12	21	—	—
	(T_C = 125°C)				—	20	—	
(I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)					14	—	34	
	(T_C = 125°C)				—	32	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)					6.0	11	—	
	(T_C = 125°C)				—	7.5	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)					10	22	—	
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	50	65	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	800	1000	pF
Dynamic Saturation Voltage:	(I_C = 1.0 Adc	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	—	6.8	—	Vdc
Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	I_{B1} = 100 mAdc V_{CC} = 300 V)				—	14	—	
		3.0 μs	(T_C = 125°C)		—	2.4	—	
					—	5.6	—	
	(I_C = 2.0 Adc	1.0 μs	(T_C = 125°C)		—	11.3	—	
	I_{B1} = 400 mAdc V_{CC} = 300 V)				—	15.5	—	
		3.0 μs	(T_C = 125°C)		—	1.3	—	
					—	6.1	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(2) Proper strike and creepage distance must be provided.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)						
Turn–On Time	(I_C = 1.0 Adc, I_{B1} = 0.1 Adc, I_{B2} = 0.5 Adc, V_{CC} = 300 V)	t_{on}	— —	210 180	300 —	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	— —	1.0 1.3	1.7 —	μs
Turn–On Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc, I_{B1} = 1.0 Adc, V_{CC} = 300 V)	t_{on}	— —	75 90	110 —	ns
Turn–Off Time	(T_C = 125°C)	t_{off}	— —	1.5 1.8	2.5 —	μs
Turn–On Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, I_{B2} = 0.5 Adc, V_{CC} = 250 V)	t_{on}	— —	450 900	800 1400	ns
Storage Time	(T_C = 125°C)	t_s	— —	2.0 2.2	3.0 3.5	μs
Fall Time	(T_C = 125°C)	t_f	— —	275 500	400 800	ns
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)						
Fall Time	(I_C = 1.0 Adc, I_{B1} = 0.1 Adc, I_{B2} = 0.5 Adc)	t_{fi}	— —	100 100	150 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.1 1.4	1.7 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	180 160	250 —	ns
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc, I_{B2} = 1.0 Adc)	t_{fi}	— —	90 150	175 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.7 2.2	2.5 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	180 250	300 —	ns
Fall Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, I_{B2} = 0.5 Adc, $V_{BE(off)}$ = –5.0 Vdc)	t_{fi}	— —	70 100	130 175	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	0.75 1.0	1.0 1.3	μs
Crossover Time	(T_C = 125°C)	t_c	— —	250 250	350 500	ns

TYPICAL STATIC CHARACTERISTICS

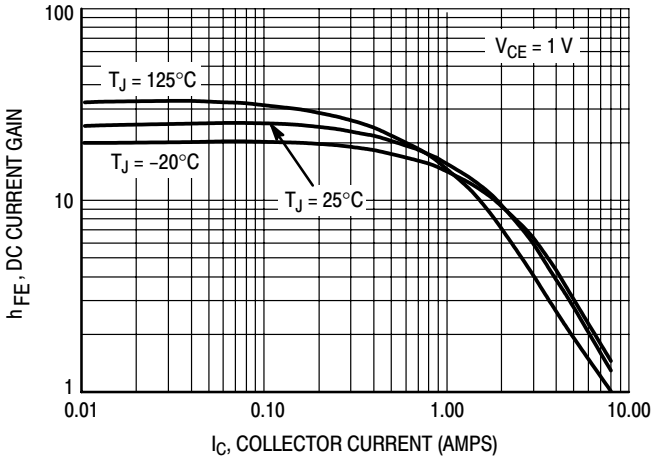


Figure 1. DC Current Gain @ 1 Volt

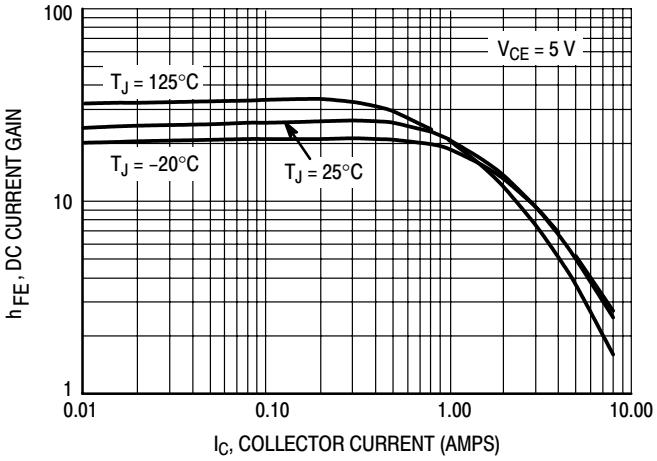


Figure 2. DC Current Gain @ 5 Volts

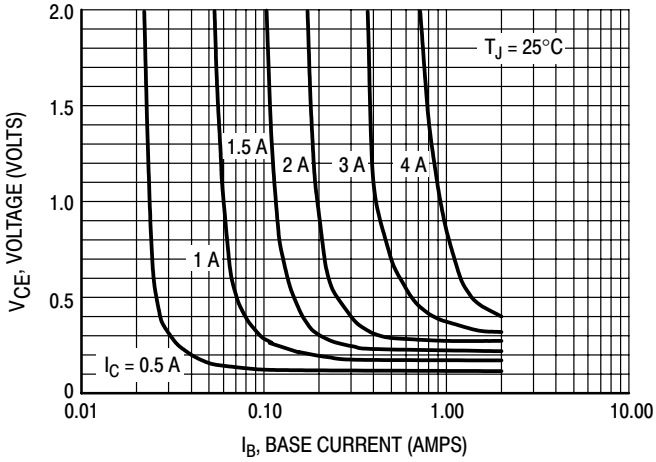


Figure 3. Collector Saturation Region

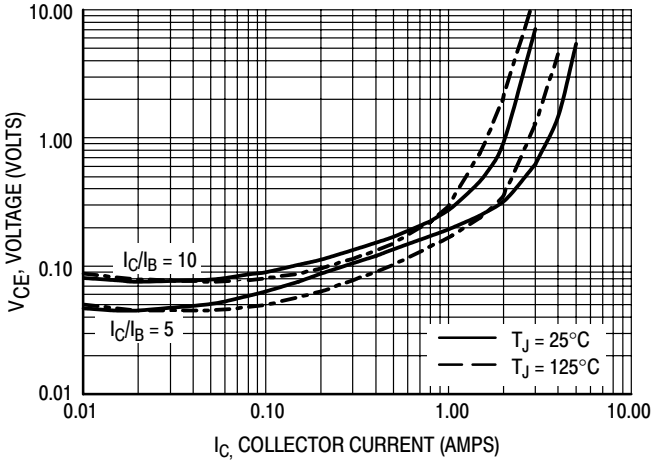


Figure 4. Collector–Emitter Saturation Voltage

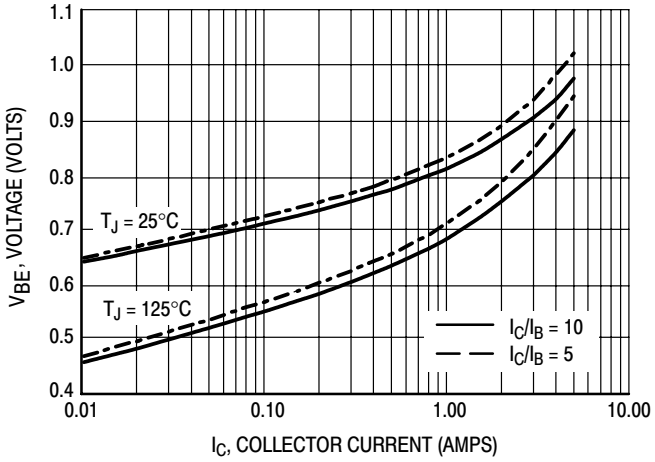


Figure 5. Base–Emitter Saturation Region

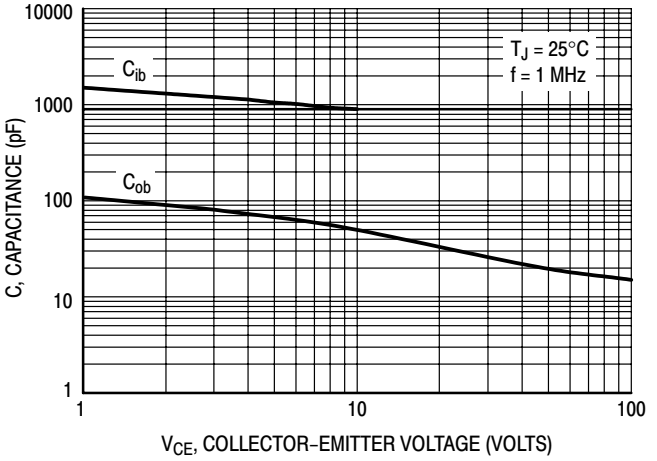


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

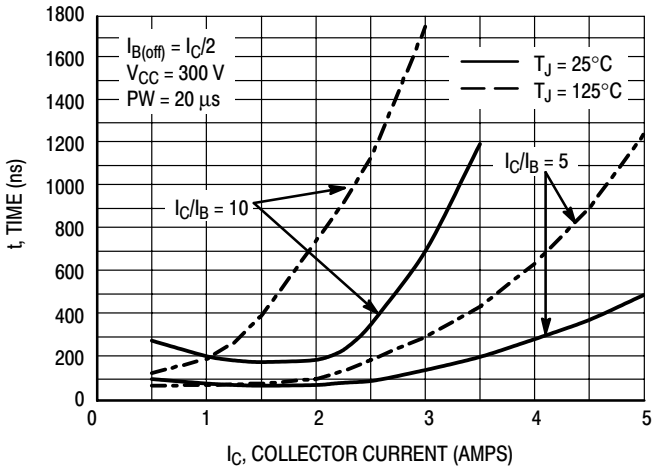


Figure 7. Resistive Switching, t_{on}

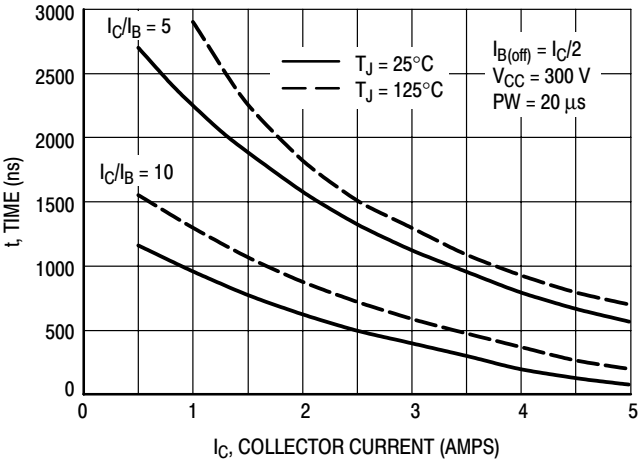


Figure 8. Resistive Switching, t_{off}

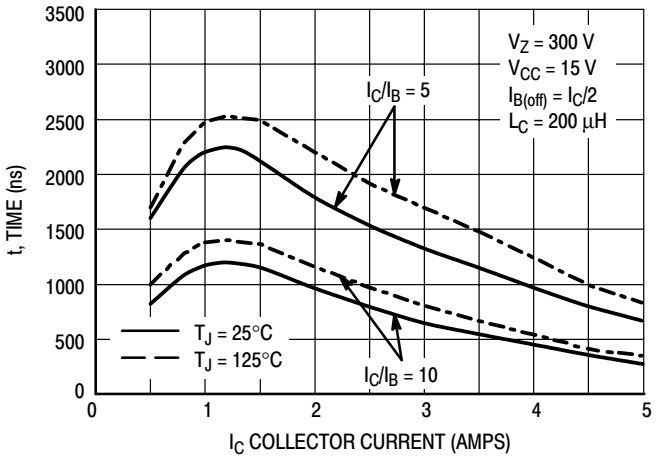


Figure 9. Inductive Storage Time, t_{si}

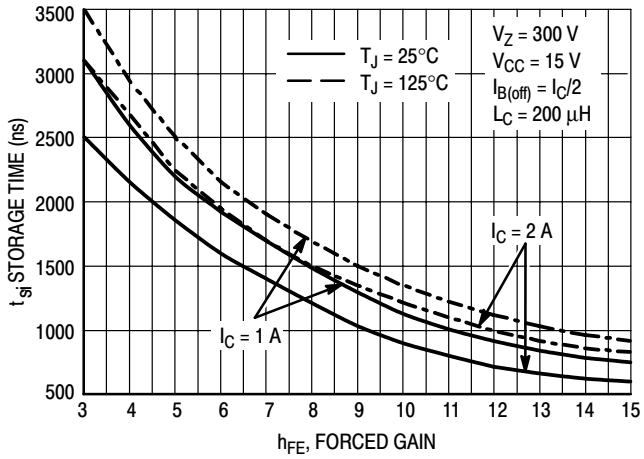


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

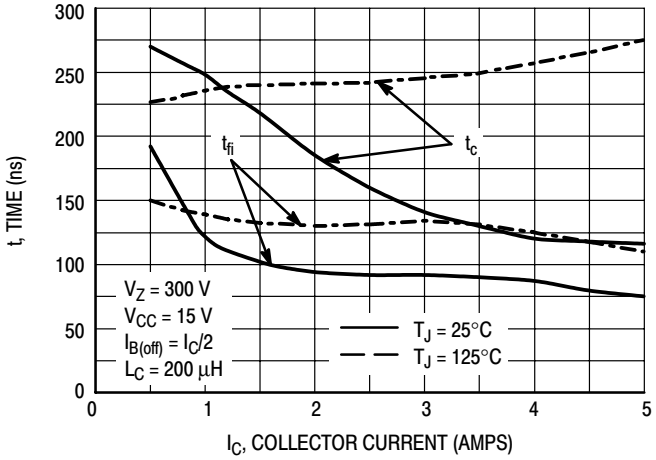


Figure 11. Inductive Switching, t_c and t_{fi}, I_C/I_B = 5

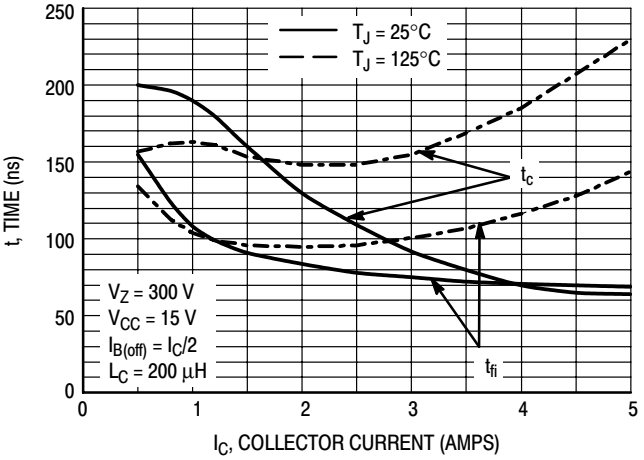


Figure 12. Inductive Switching, t_c and t_{fi}, I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

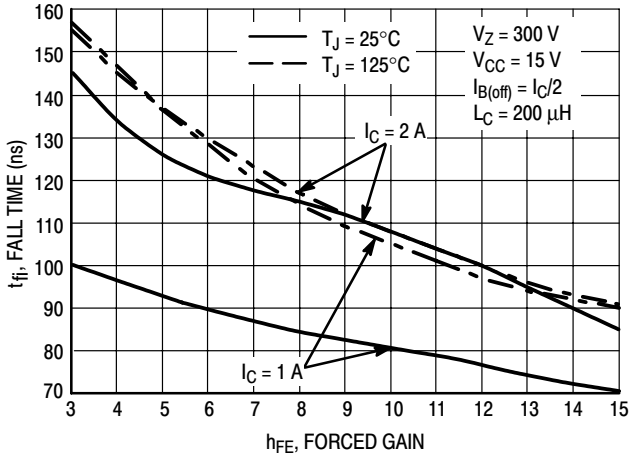


Figure 13. Inductive Fall Time

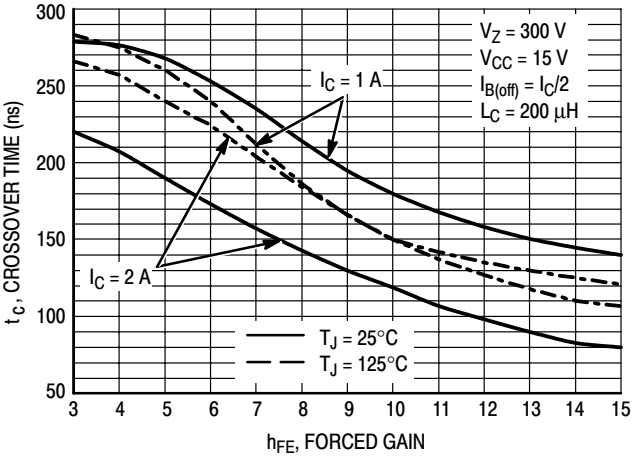


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

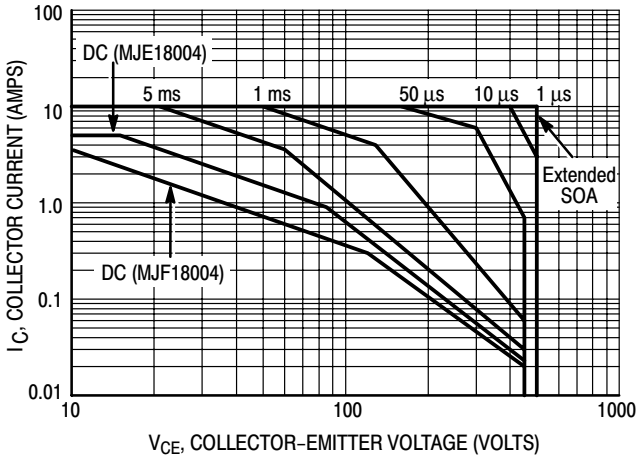


Figure 15. Forward Bias Safe Operating Area

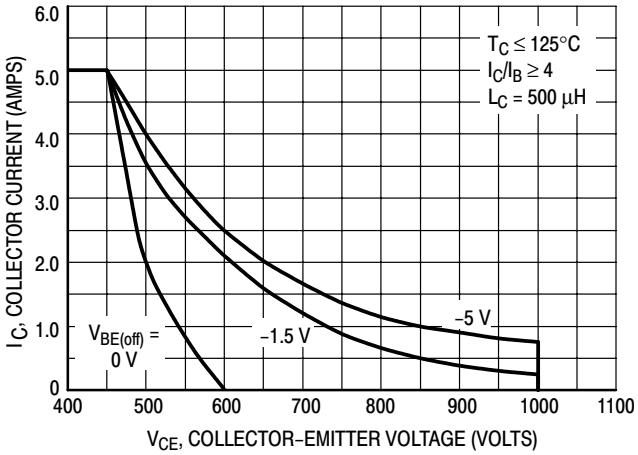


Figure 16. Reverse Bias Safe Operating Area

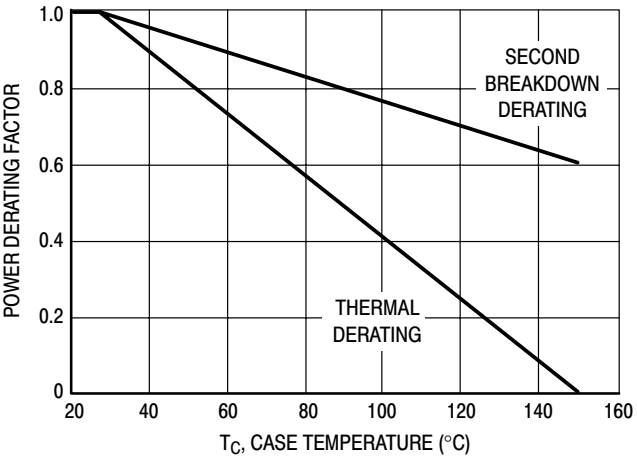


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. T_J(pk) may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

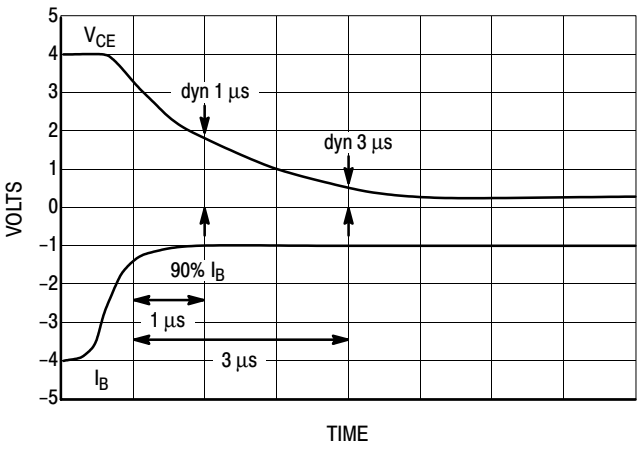


Figure 18. Dynamic Saturation Voltage Measurements

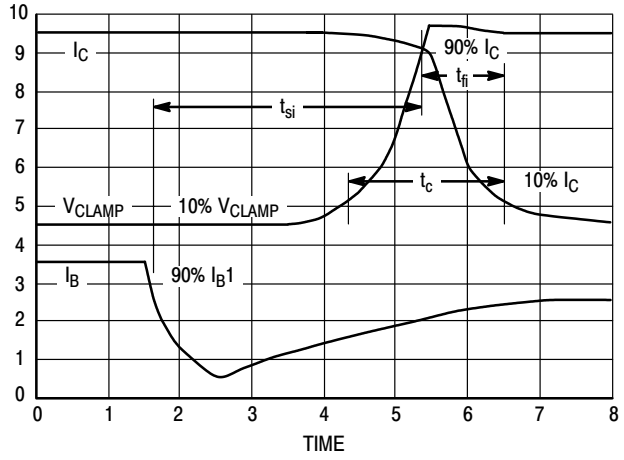
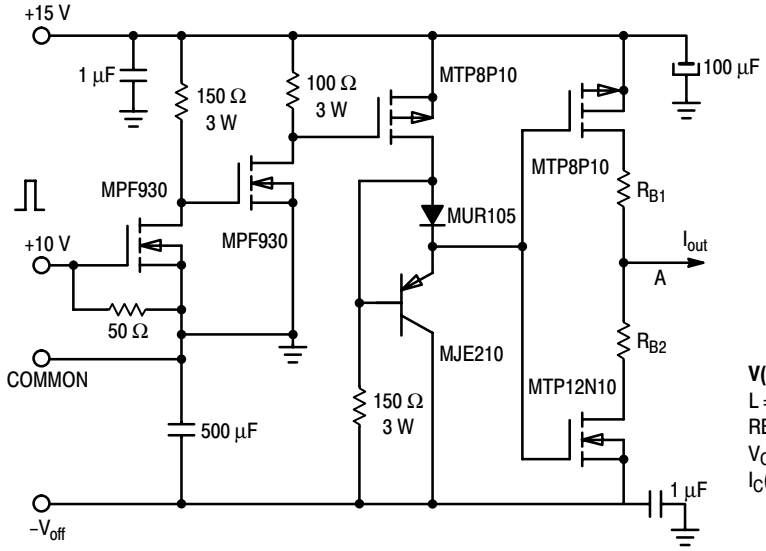
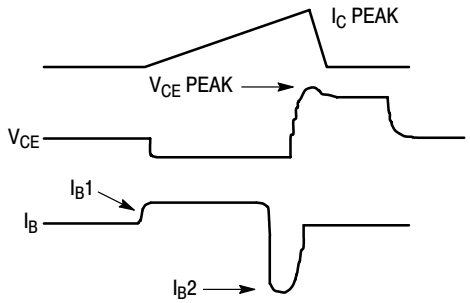


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

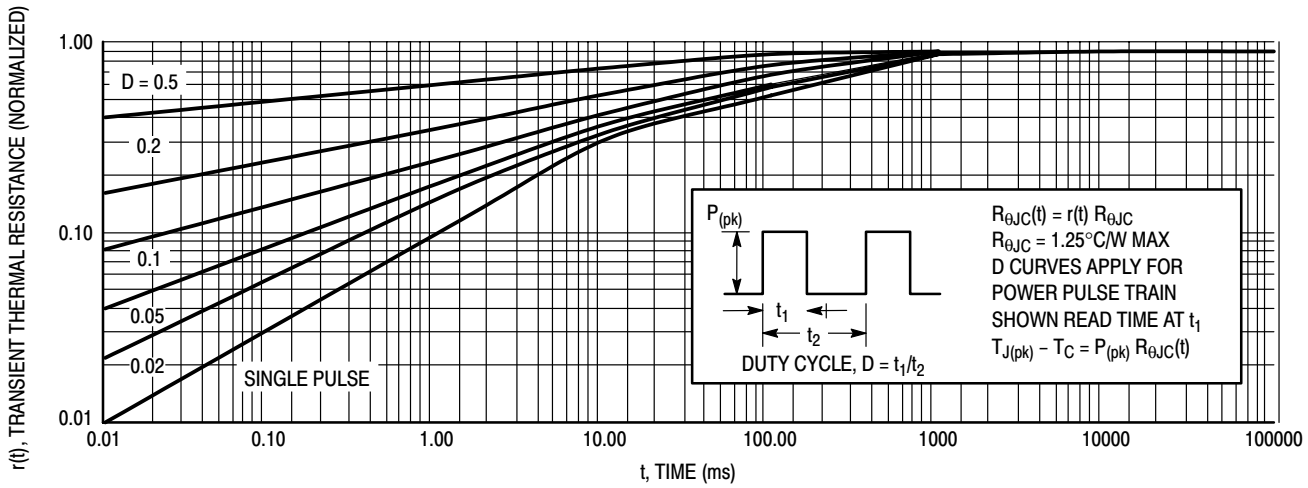


Figure 20. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004

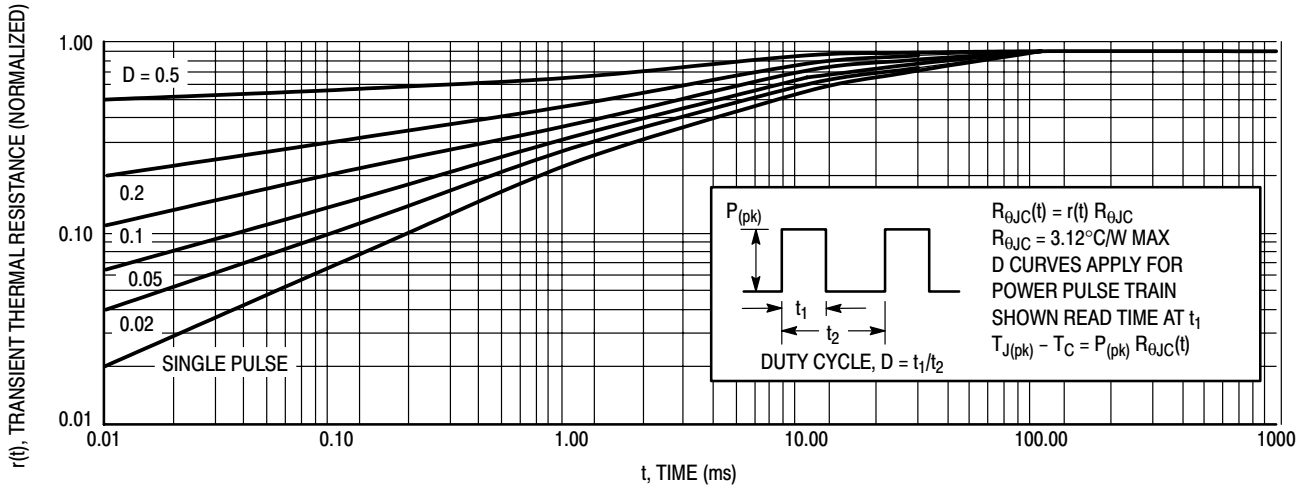


Figure 21. Typical Thermal Response for MJF18004

TEST CONDITIONS FOR ISOLATION TESTS*

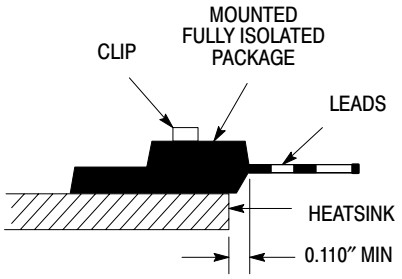


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

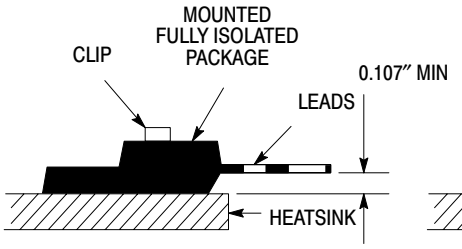


Figure 22b. Clip Mounting Position for Isolation Test Number 2

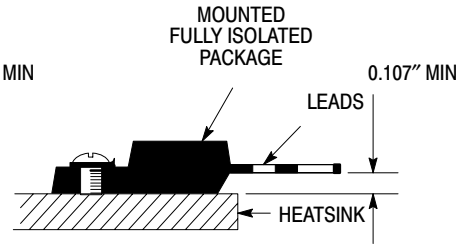


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

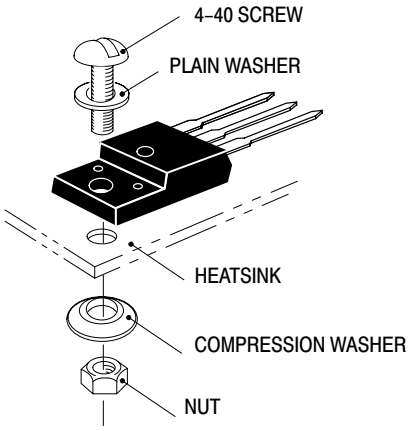


Figure 23a. Screw–Mounted

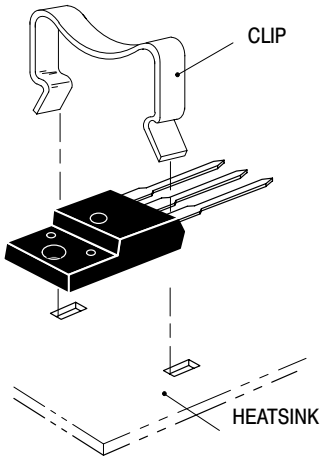


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE18006 *

*ON Semiconductor Preferred Device

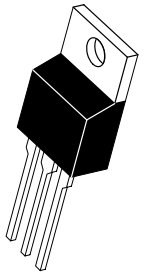
SWITCHMODE™

NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE18006 has an applications specific state–of–the–art die designed for use in 220 V line–operated SWITCHMODE Power supplies and electronic light ballasts. This high voltage/high speed transistor offers the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Standard TO–220

POWER TRANSISTOR
6.0 AMPERES
1000 VOLTS
100 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE18006	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	6.0 15	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18006	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)				$V_{BE(sat)}$	— —	0.83 0.94	1.2 1.3	Vdc
Collector–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)			(T_C = 125°C) (T_C = 125°C)	$V_{CE(sat)}$	— — — —	0.25 0.27 0.35 0.4	0.6 0.65 0.7 0.8	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.3 Adc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)			(T_C = 125°C) (T_C = 125°C) (T_C = 25 to 125°C)	h_{FE}	14 — 6.0 5.0 11 10	— 32 10 8.0 17 22	34 — — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	75	120	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.3 Adc I_{B1} = 130 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	5.5 12	— —	Volts
		3.0 μs	(T_C = 125°C)		— —	3.0 7.0	— —	
	(I_C = 3.0 Adc I_{B1} = 0.6 Adc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	9.5 14.5	— —	
		3.0 μs	(T_C = 125°C)		— —	2.0 7.5	— —	

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

			Symbol	Min	Typ	Max	Unit
Turn–On Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc, V_{CC} = 300 V)	(T_C = 125°C)	t_{on}	— —	90 100	180 —	ns
Turn–Off Time		(T_C = 125°C)	t_{off}	— —	1.7 2.1	2.5 —	μs
Turn–On Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc, V_{CC} = 300 V)	(T_C = 125°C)	t_{on}	— —	200 130	300 —	ns
Turn–Off Time		(T_C = 125°C)	t_{off}	— —	1.2 1.5	2.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

			Symbol	Min	Typ	Max	Unit
Fall Time	(I_C = 1.5 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc)	(T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time		(T_C = 125°C)	t_{si}	— —	1.5 1.9	2.5 —	μs
Crossover Time		(T_C = 125°C)	t_c	— —	220 230	350 —	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)	(T_C = 125°C)	t_{fi}	— —	85 120	150 —	ns
Storage Time		(T_C = 125°C)	t_{si}	— —	2.15 2.75	3.2 —	μs
Crossover Time		(T_C = 125°C)	t_c	— —	200 310	300 —	ns

TYPICAL STATIC CHARACTERISTICS

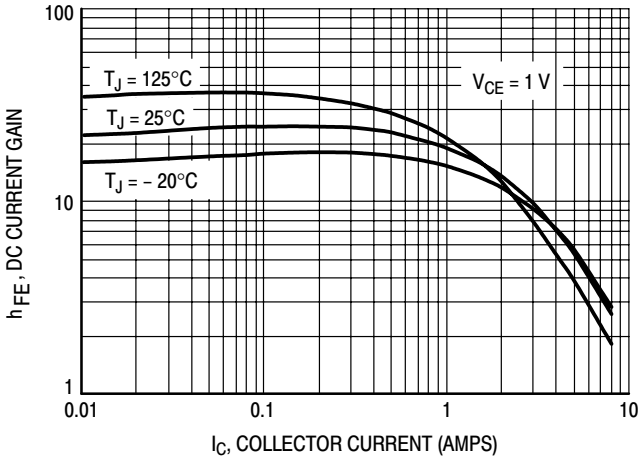


Figure 1. DC Current Gain @ 1 Volt

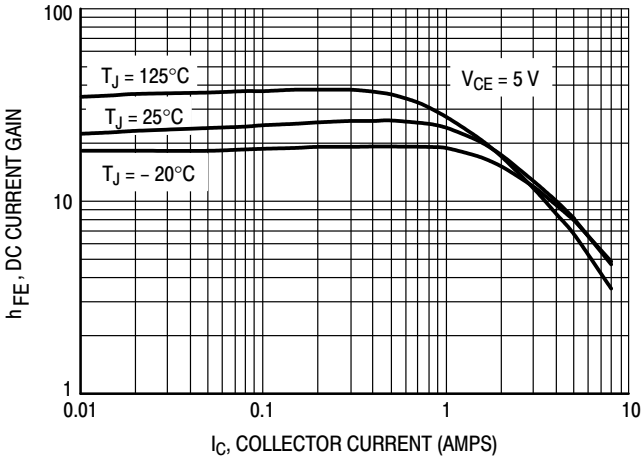


Figure 2. DC Current Gain @ 5 Volts

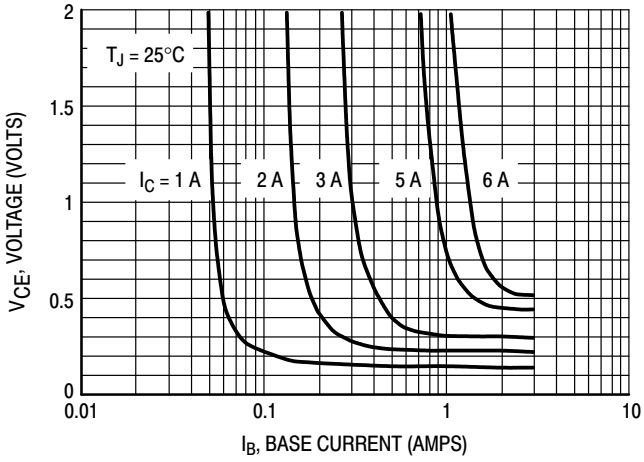


Figure 3. Collector Saturation Region

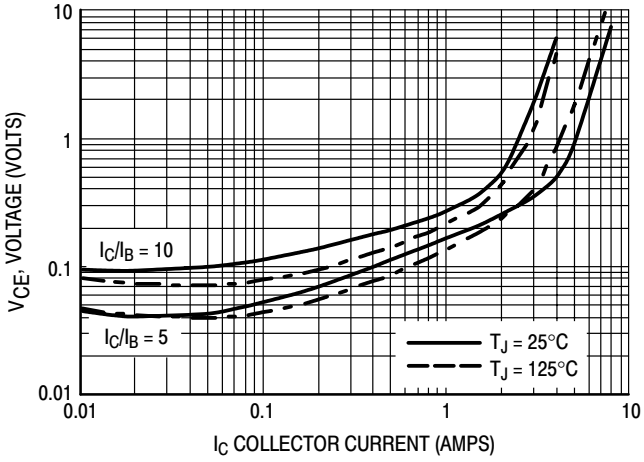


Figure 4. Collector–Emitter Saturation Voltage

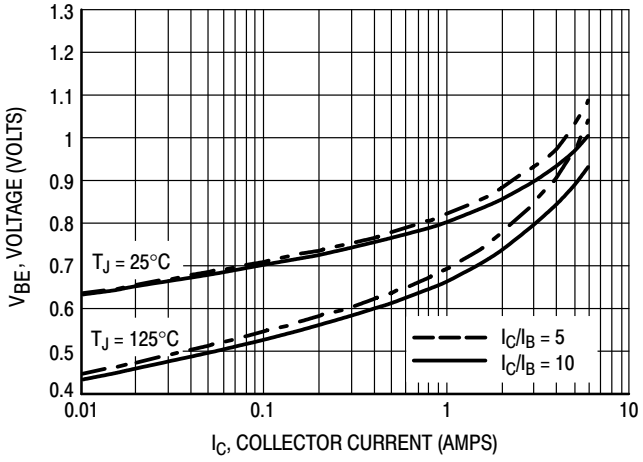


Figure 5. Base–Emitter Saturation Region

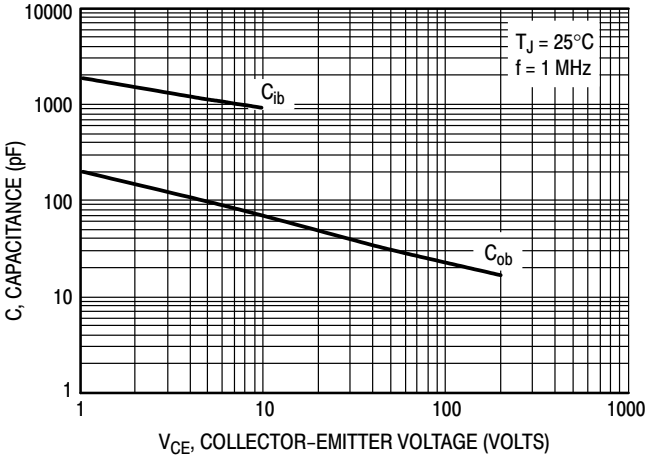


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

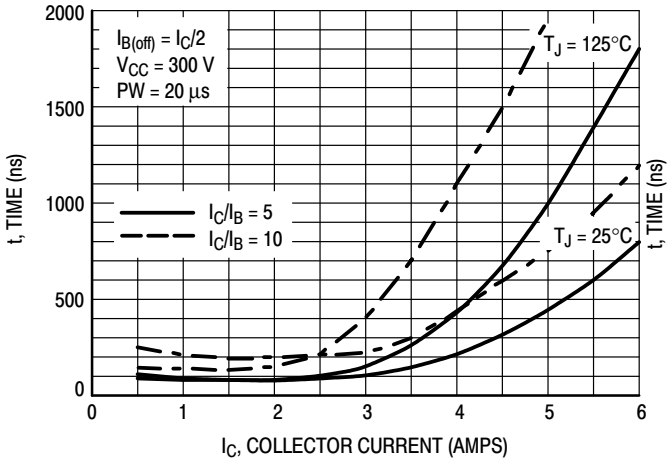


Figure 7. Resistive Switching, t_{on}

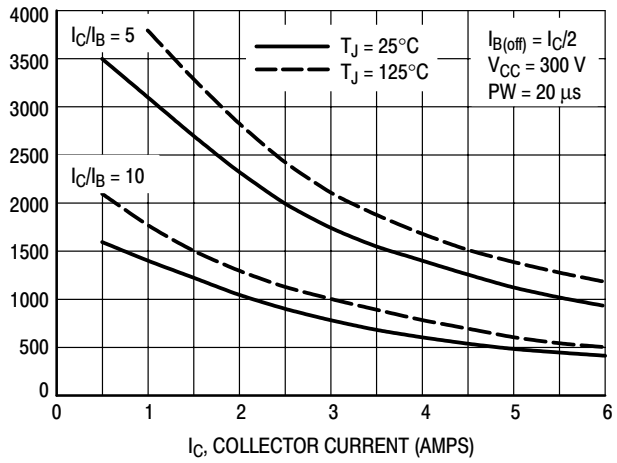


Figure 8. Resistive Switching, t_{off}

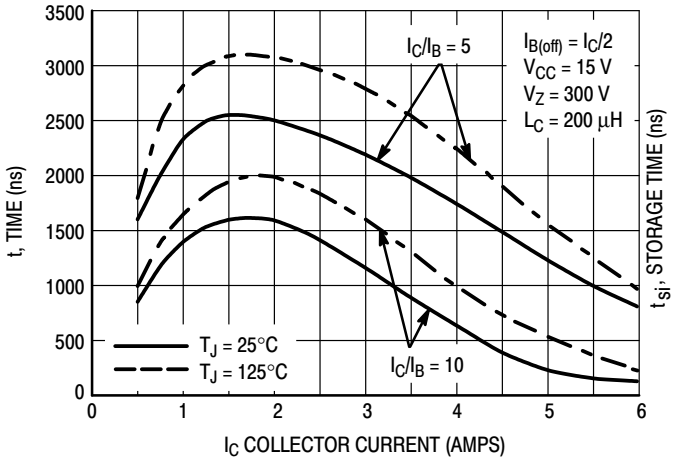


Figure 9. Inductive Storage Time, t_{si}

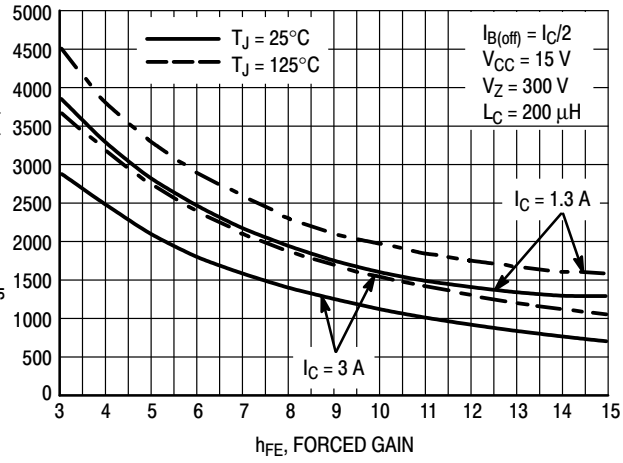


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

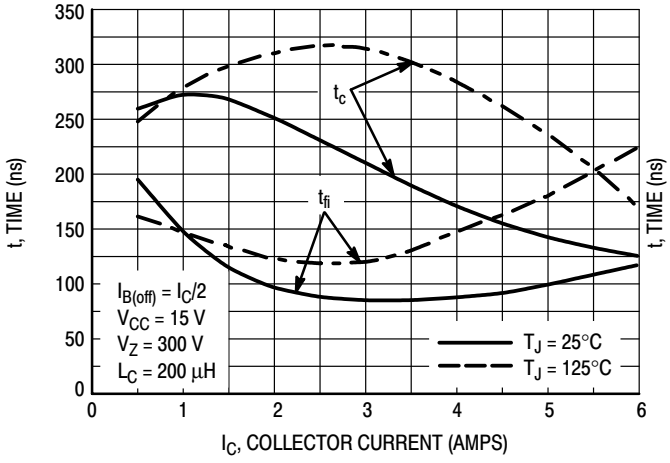


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

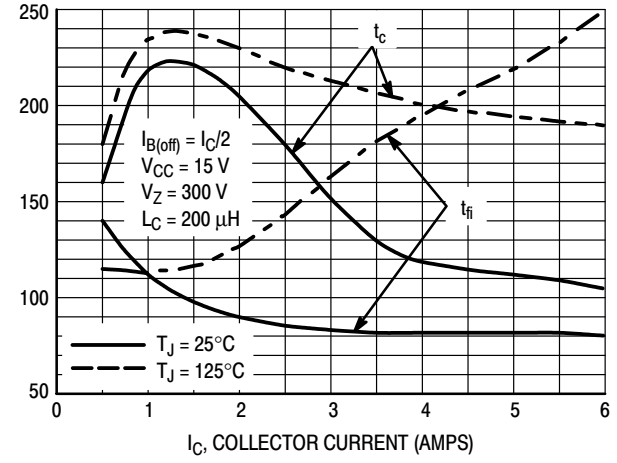


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

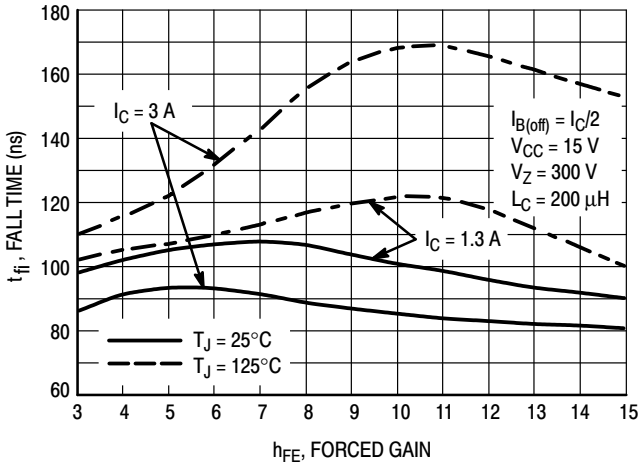


Figure 13. Inductive Fall Time

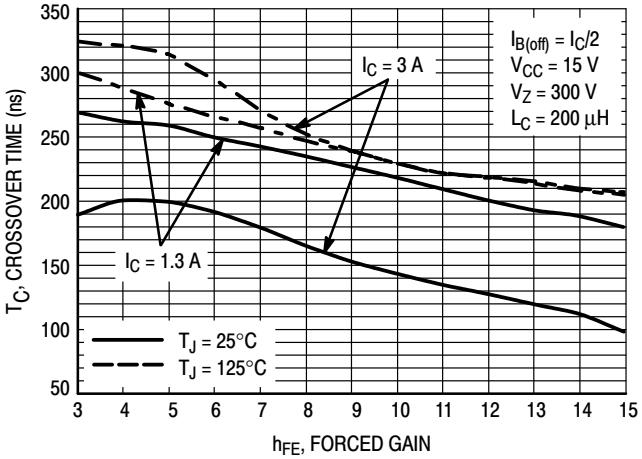


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

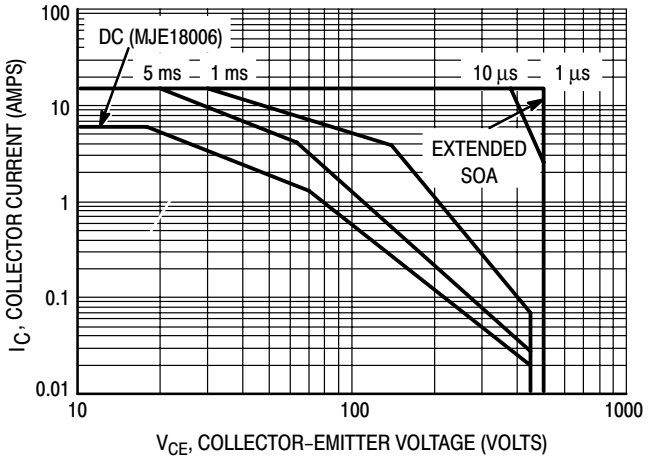


Figure 15. Forward Bias Safe Operating Area

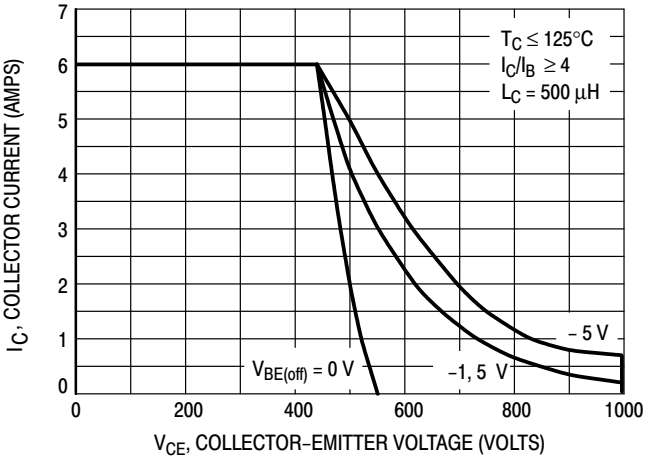


Figure 16. Reverse Bias Switching Safe Operating Area

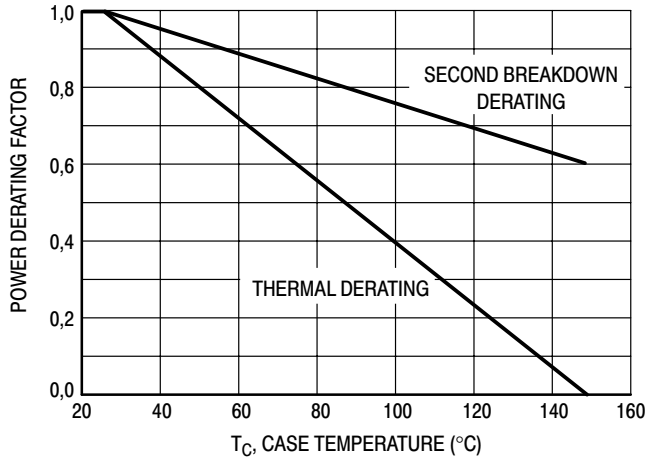


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

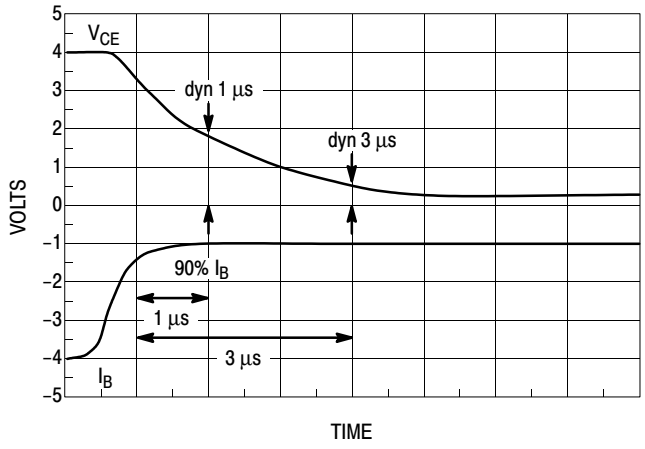


Figure 18. Dynamic Saturation Voltage Measurements

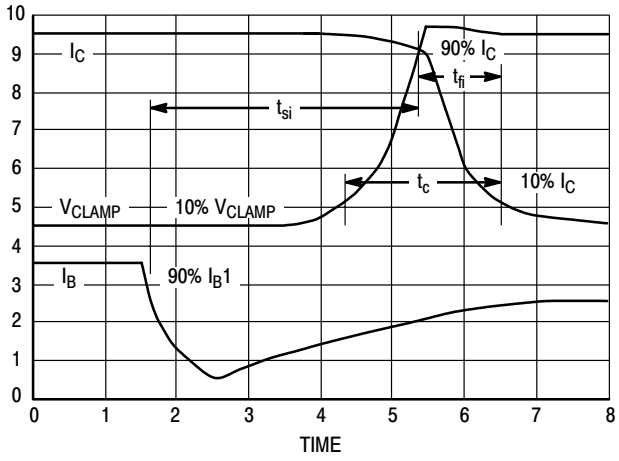
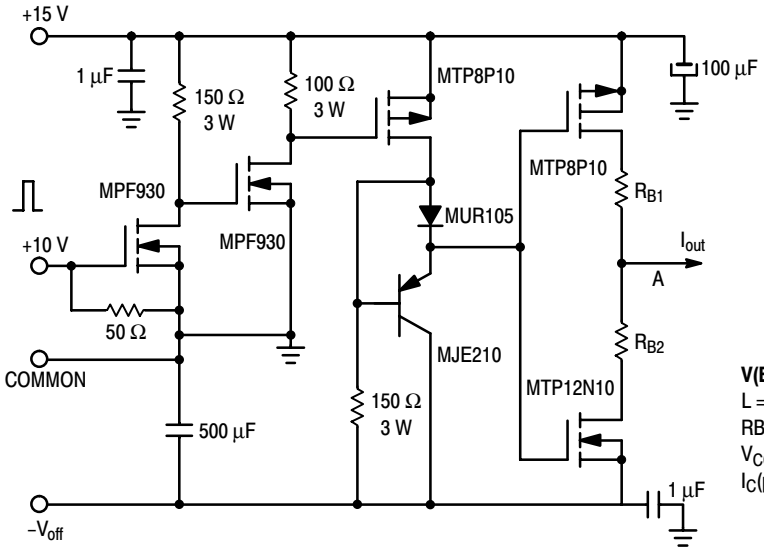
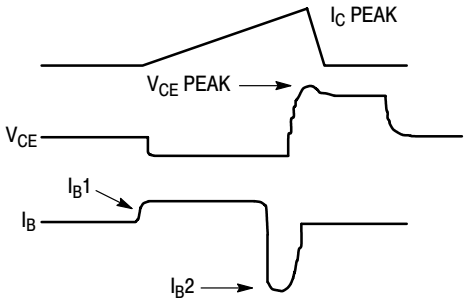


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

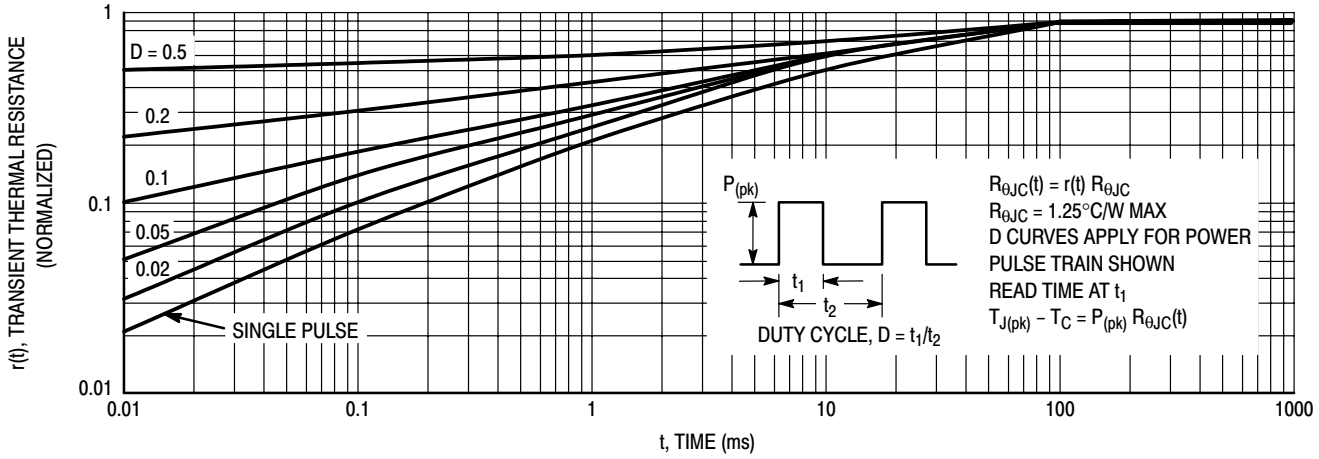


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18006

MJE18008 *
MJF18008 *

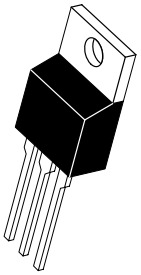
*ON Semiconductor Preferred Device

POWER TRANSISTOR
8.0 AMPERES
1000 VOLTS
45 and 125 WATTS

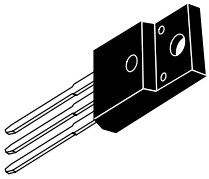
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE/MJF18008 have an applications specific state–of–the–art die designed for use in 220 V line–operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF18008, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A–09
TO–220AB
MJE18008



CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED
MJF18008

MAXIMUM RATINGS

Rating	Symbol	MJE18008	MJF18008	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec,] R.H. < 30%, Test No. 1 Per Fig. 22b T_C = 25°C) Test No. 1 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T^C = 25°C) Derate above 25°C	P_D	125 1.0	45 0.36	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18008	MJF18008	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	2.78 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
MJE18008/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.92	1.25	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		—	0.3	0.6	
(T_C = 125°C)		—	0.3	0.65	
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.35	0.7	
(T_C = 125°C)		—	0.4	0.8	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	—	34	—
(T_C = 125°C)		—	28	—	
(I_C = 4.5 Adc, V_{CE} = 1.0 Vdc)		6.0	9.0	—	
(T_C = 125°C)		5.0	8.0	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		11	15	—	
(T_C = 125°C)		11	16	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(2) Proper strike and creepage distance must be provided.

(continued)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	100	150	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 2.0 Adc I_{B1} = 200 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	5.5 11.5	— —	Vdc
		3.0 μs	(T_C = 125°C)		— —	3.5 6.5	— —	
	(I_C = 5.0 Adc I_{B1} = 1.0 Adc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	11.5 14.5	— —	
		3.0 μs	(T_C = 125°C)		— —	2.4 9.0	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)								
Turn–On Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	200 190	300 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	1.2 1.5	2.5 —	μs
Turn–On Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	100 250	180 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	1.6 2.0	2.5 —	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc)		(T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.5 1.9	2.75 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	250 230	350 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc)		(T_C = 125°C)	t_{fi}	— —	85 135	150 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	2.0 2.6	3.2 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	210 250	300 —	ns

TYPICAL STATIC CHARACTERISTICS

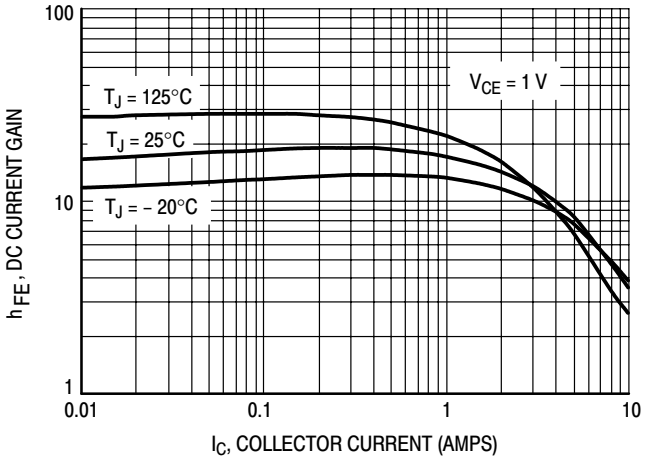


Figure 21. DC Current Gain @ 1 Volt

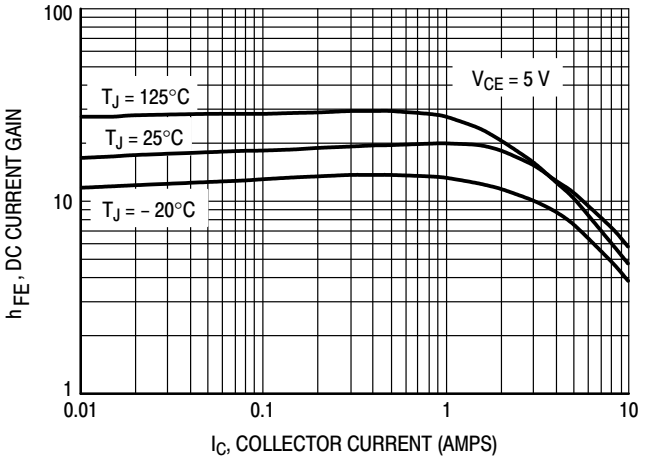


Figure 22. DC Current Gain @ 5 Volts

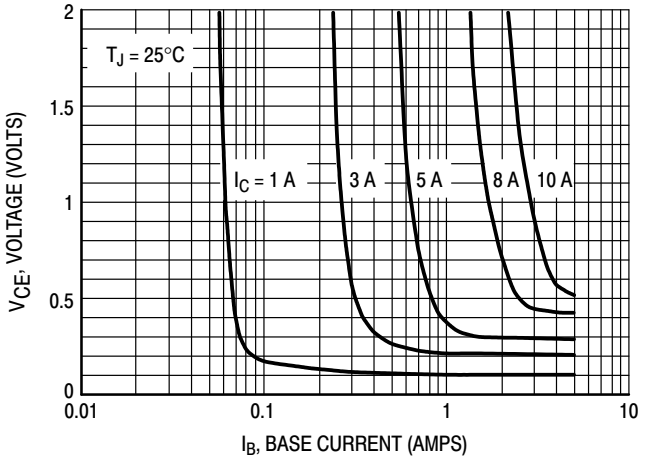


Figure 23. Collector Saturation Region

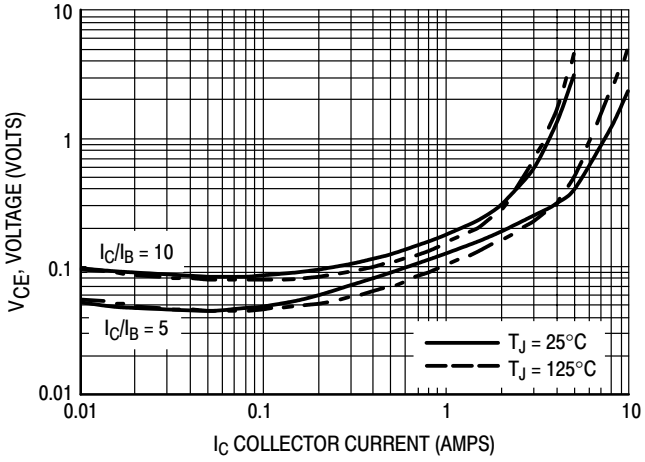


Figure 24. Collector–Emitter Saturation Voltage

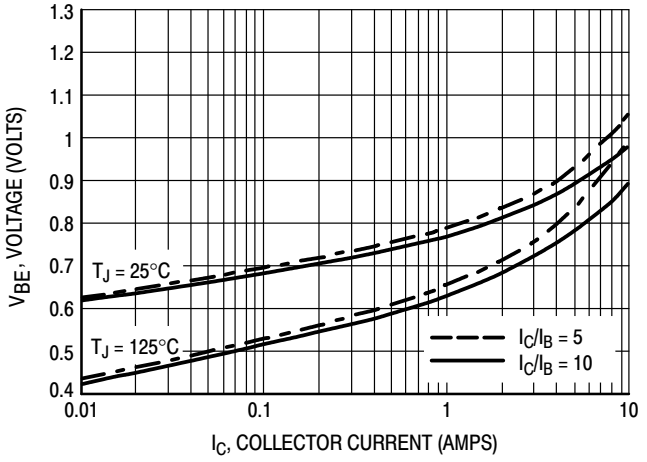


Figure 25. Base–Emitter Saturation Region

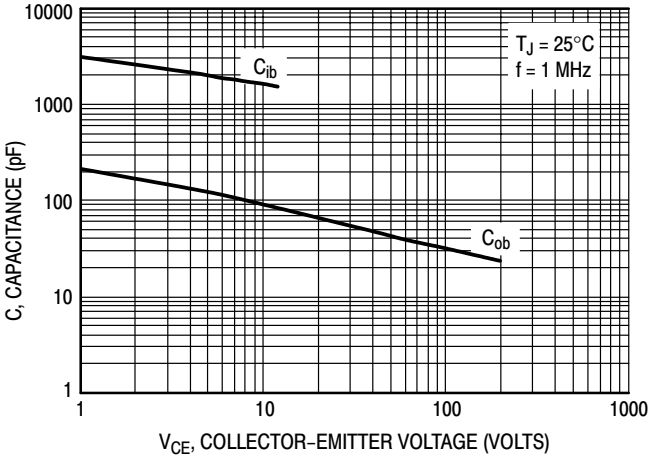


Figure 26. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

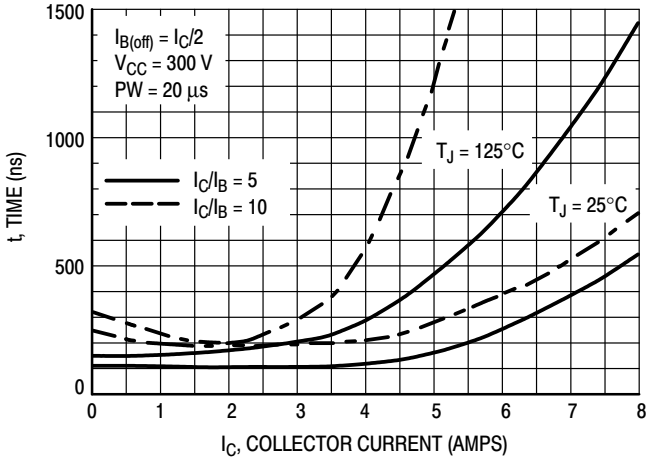


Figure 27. Resistive Switching, t_{on}

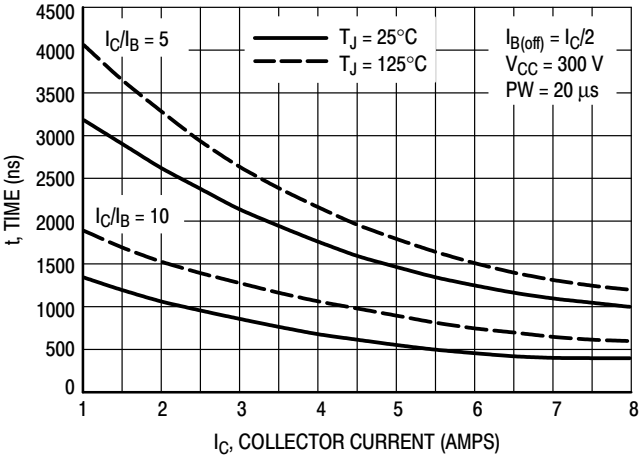


Figure 28. Resistive Switching, t_{off}

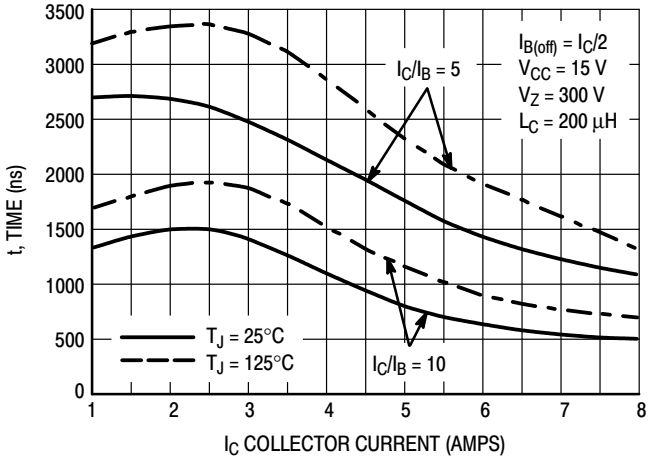


Figure 29. Inductive Storage Time, t_{si}

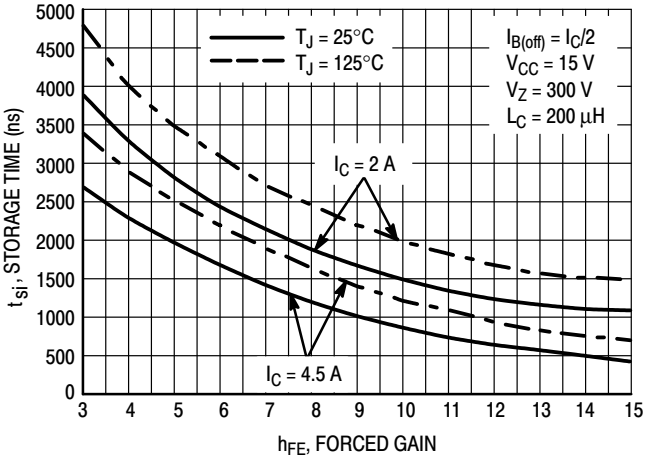


Figure 30. Inductive Storage Time, $t_{si}(h_{FE})$

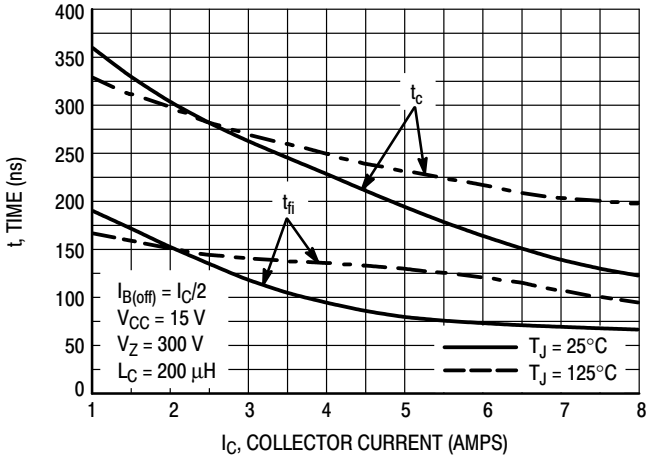


Figure 31. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

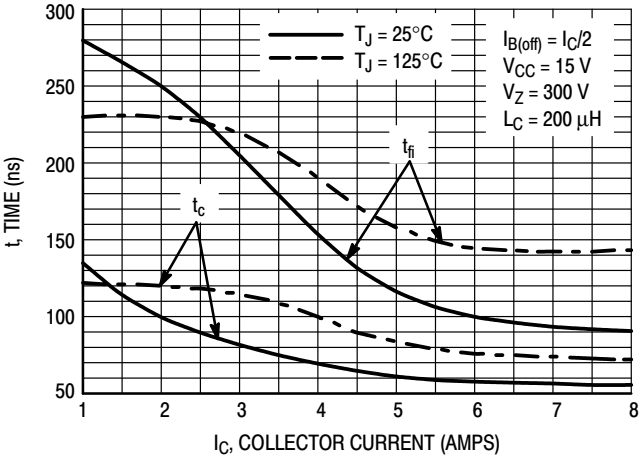


Figure 32. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

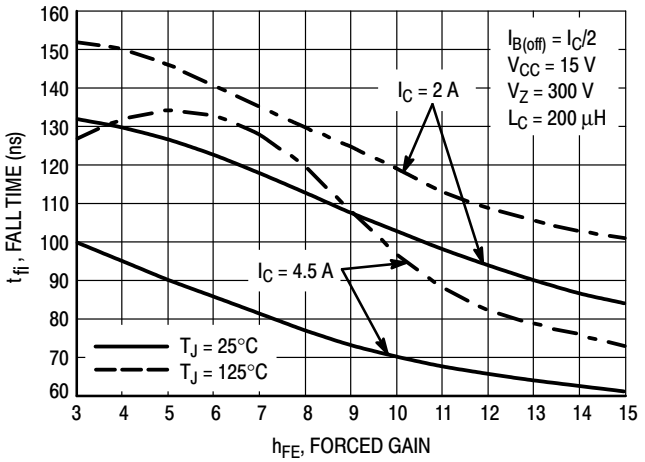


Figure 33. Inductive Fall Time

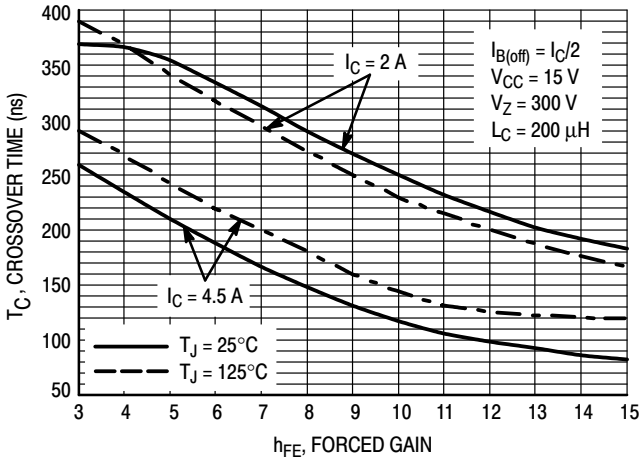


Figure 34. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

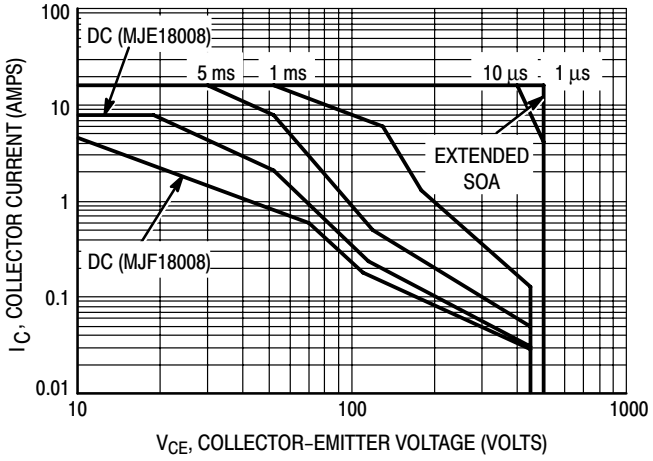


Figure 35. Forward Bias Safe Operating Area

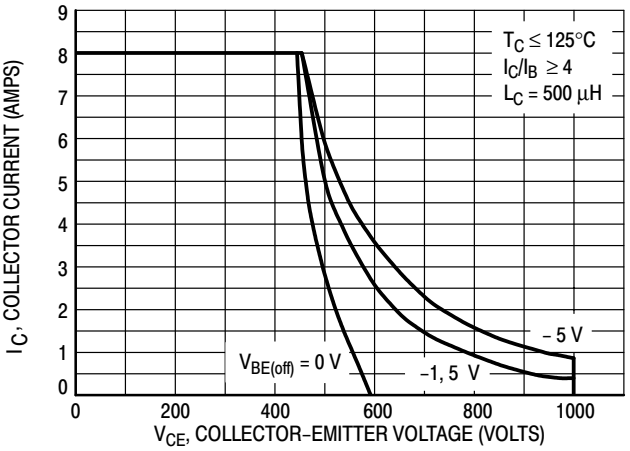


Figure 36. Reverse Bias Switching Safe Operating Area

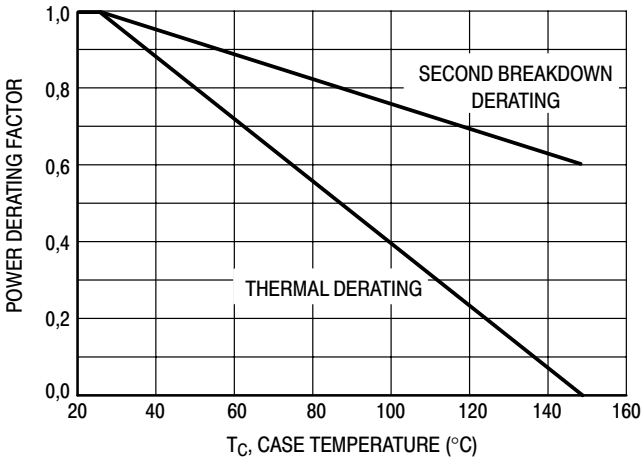


Figure 37. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 35 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 35 may be found at any case temperature by using the appropriate curve on Figure 37. $T_{J(pk)}$ may be calculated from the data in Figure 40 and 41. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 36). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

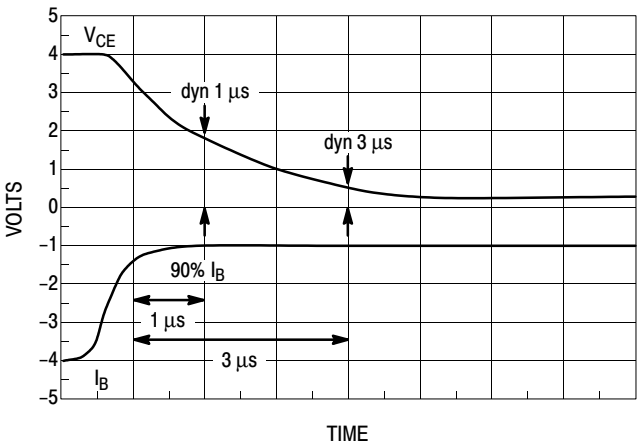


Figure 38. Dynamic Saturation Voltage Measurements

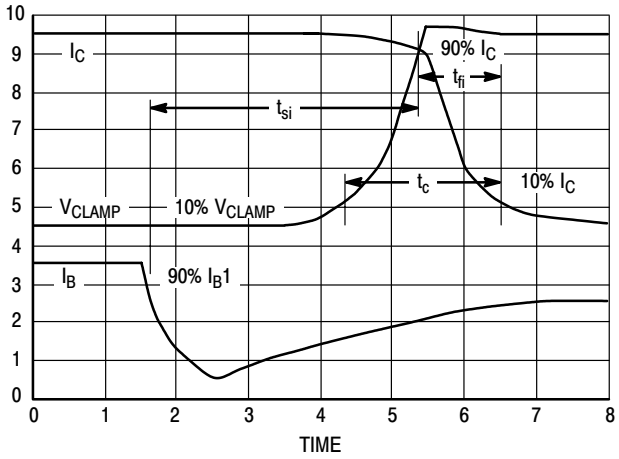
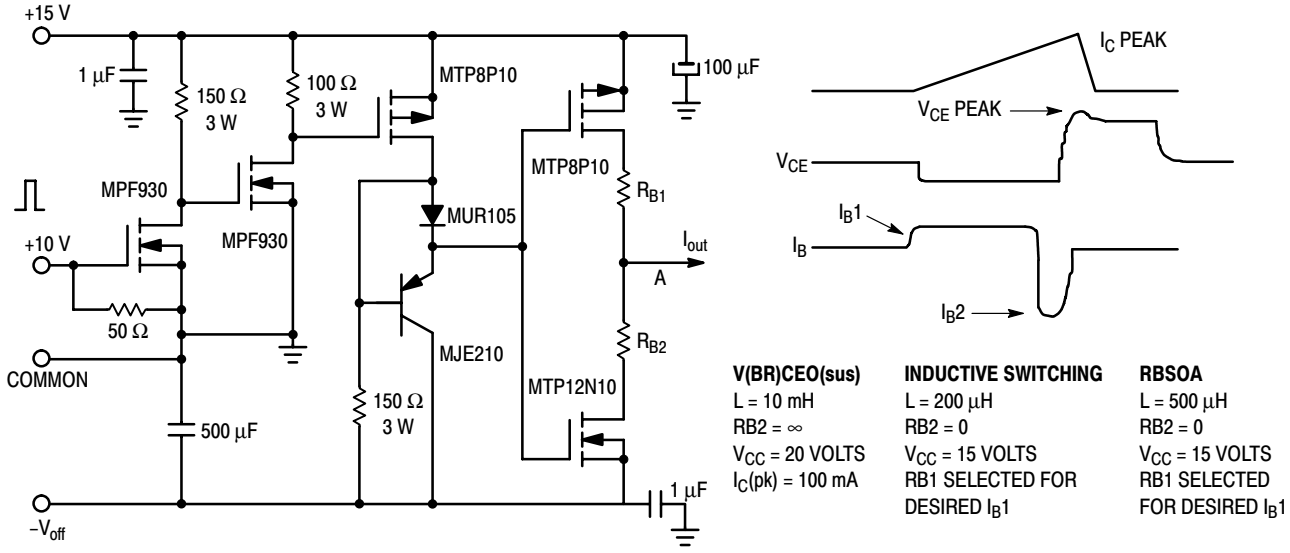


Figure 39. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

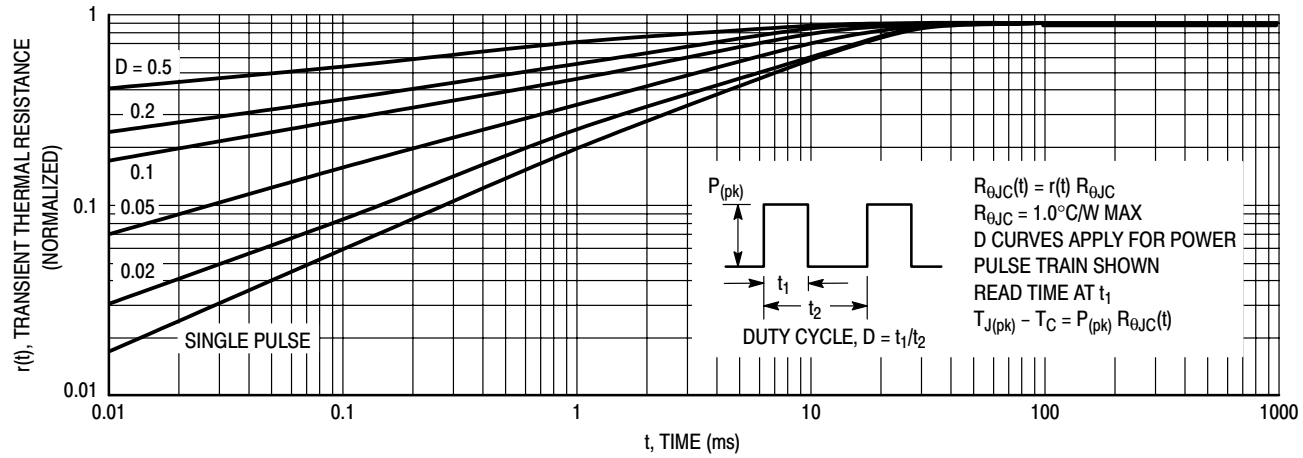


Figure 40. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18008

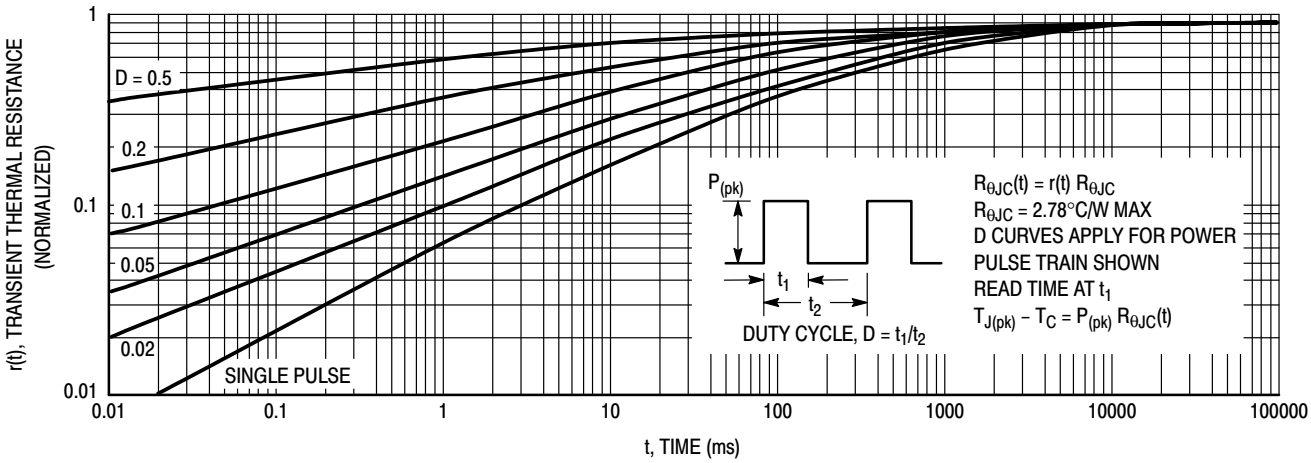


Figure 41. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18008

TEST CONDITIONS FOR ISOLATION TESTS*

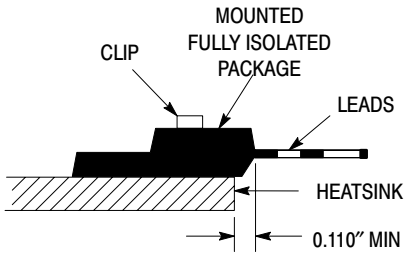


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

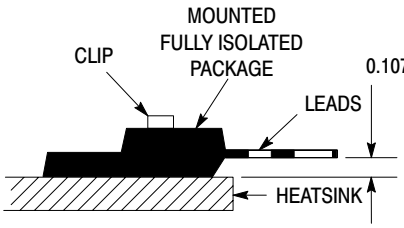


Figure 22b. Clip Mounting Position for Isolation Test Number 2

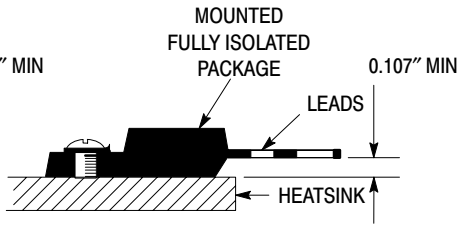


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

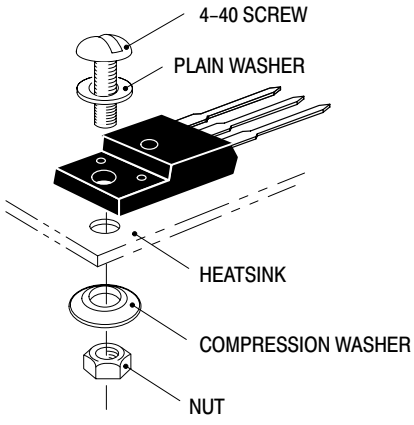


Figure 23a. Screw–Mounted

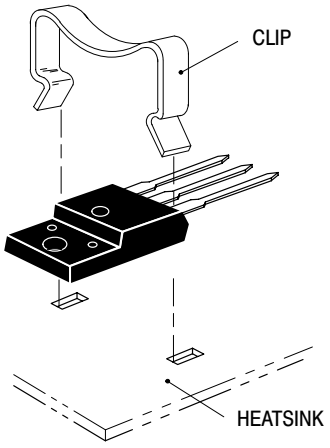


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Silicon Power Plastic Transistors

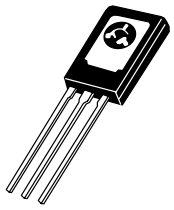
. . . designed for low voltage, low–power, high–gain audio amplifier applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current–Gain — Bandwidth Product —
  f_T = 65 MHz (Min) @ I_C
  = 100 mAdc
- Annular Construction for Low Leakage —
  I_{CBO} = 100 nAdc @ Rated V_{CB}

NPN
MJE200*
PNP
MJE210*

*ON Semiconductor Preferred Device

5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
25 VOLTS
15 WATTS



CASE 77–09
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	40	Vdc
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Emitter–Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 9
Publication Order Number:
MJE200/D

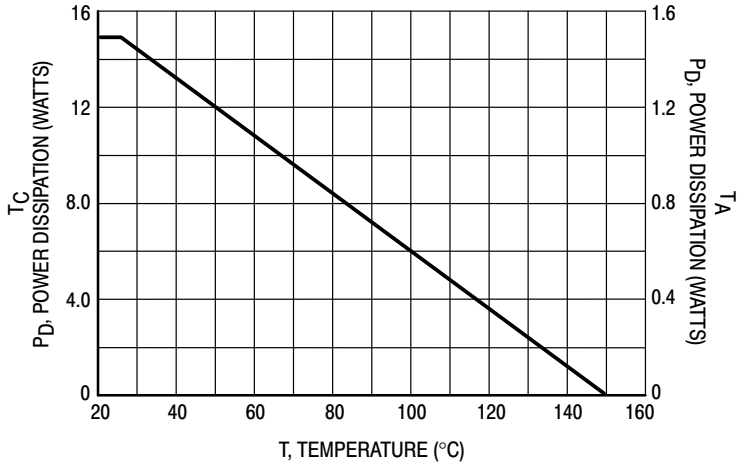


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 — —	 100 100	 nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}	 —	 100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 70 45 10	 — 180 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	 — — —	 0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200 MJE210	C_{ob}	 — —	 80 120	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

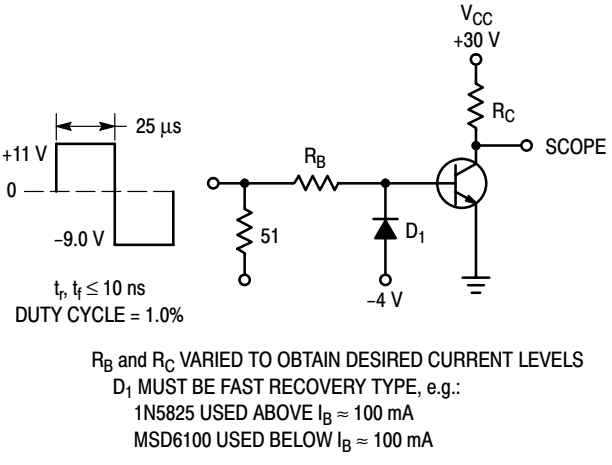


Figure 2. Switching Time Test Circuit

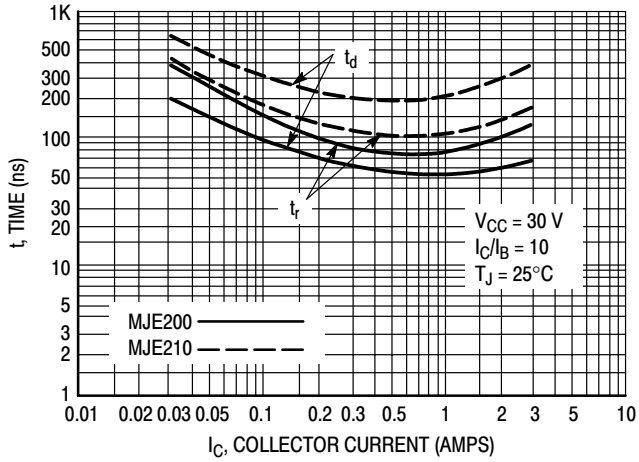


Figure 3. Turn−On Time

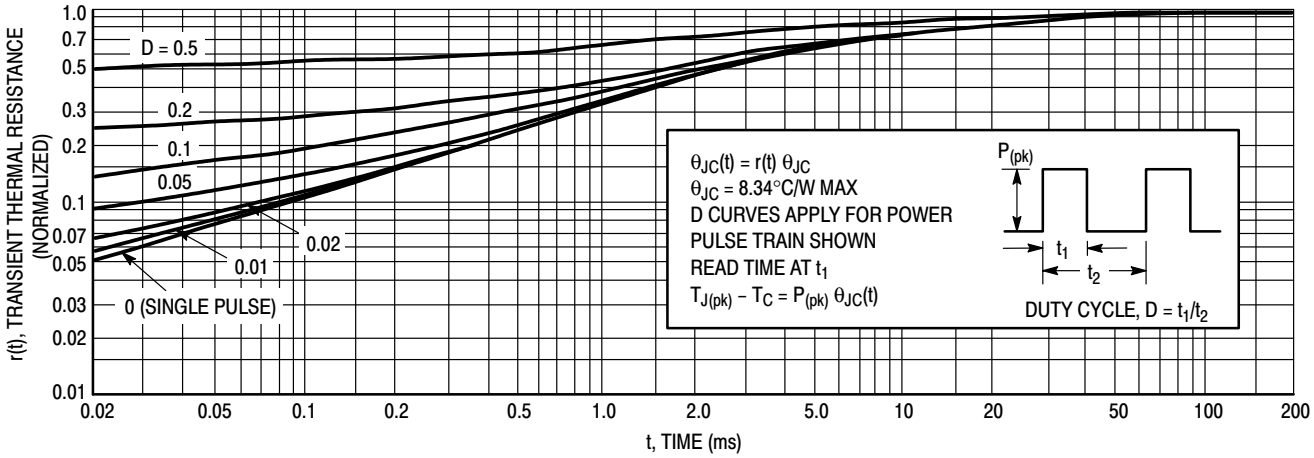


Figure 4. Thermal Response

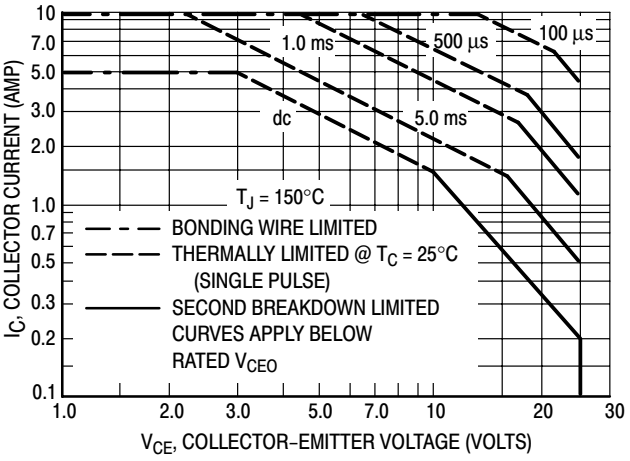


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

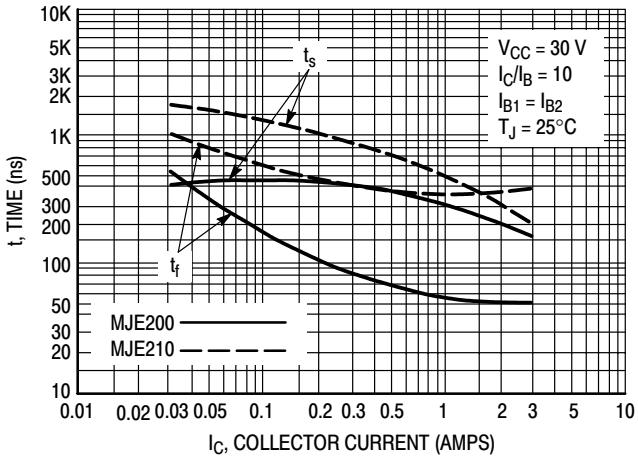


Figure 6. Turn–Off Time

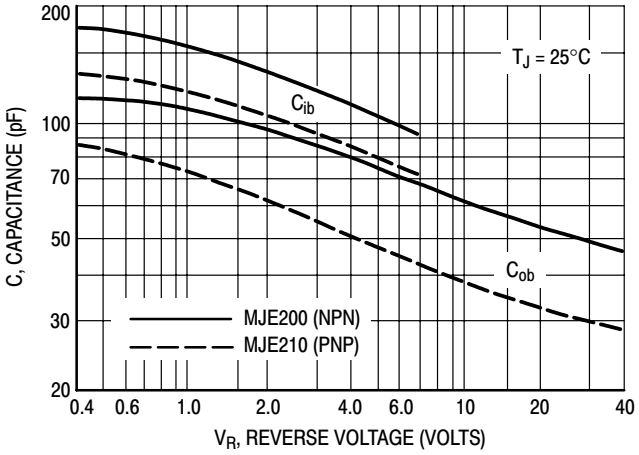
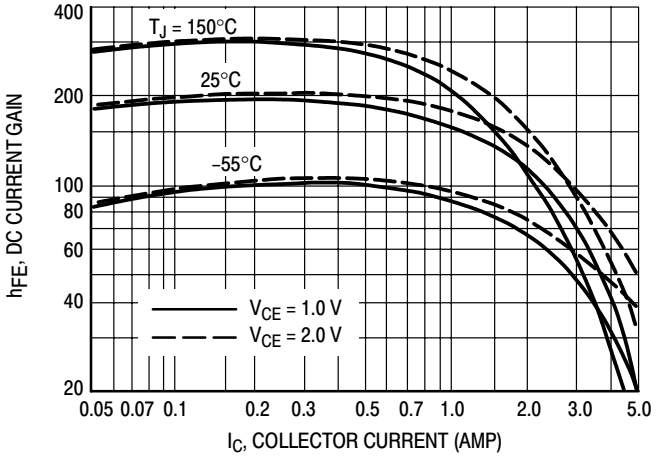


Figure 7. Capacitance

NPN
MJE200



PNP
MJE210

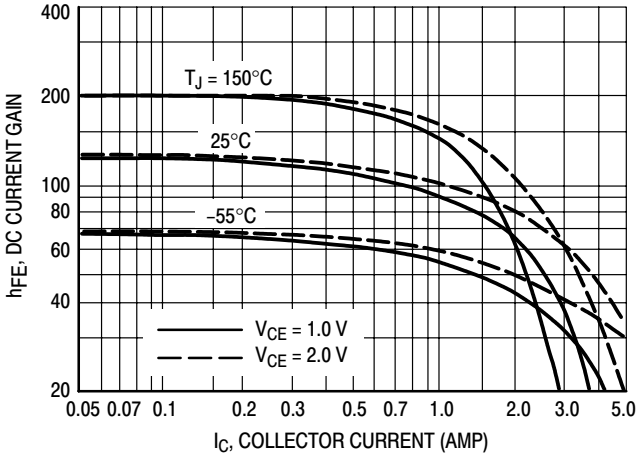
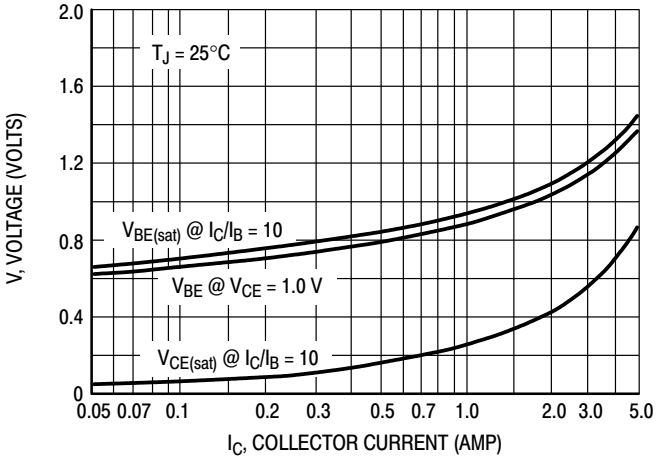


Figure 8. DC Current Gain



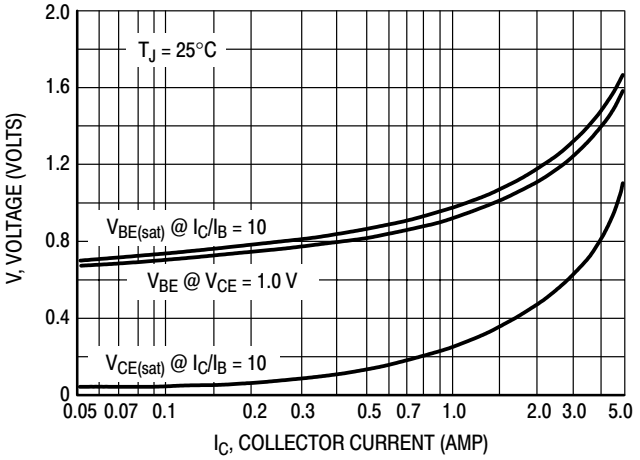
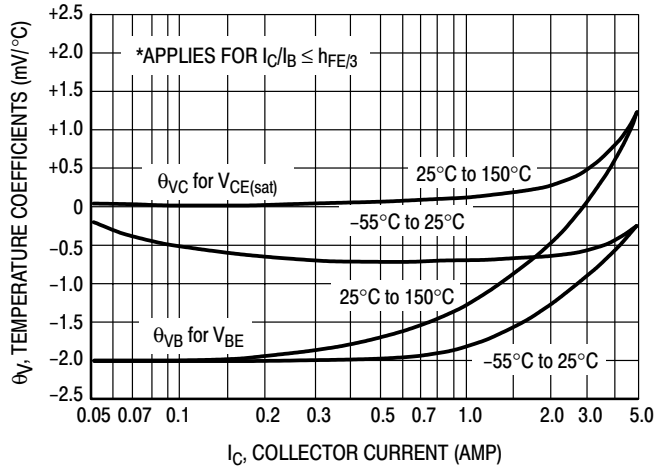


Figure 9. “On” Voltage



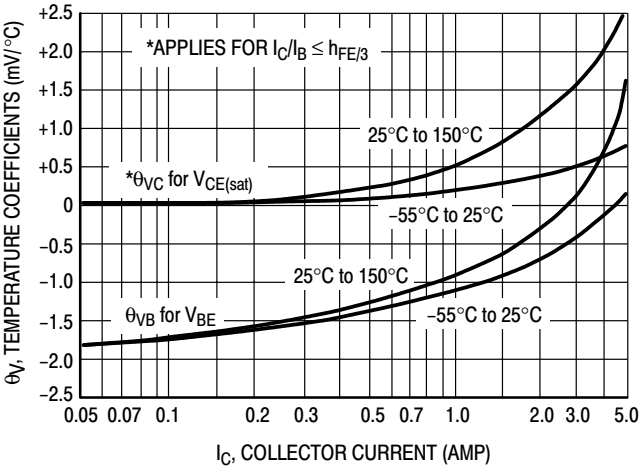


Figure 10. Temperature Coefficients

Complementary Silicon Power Plastic Transistors

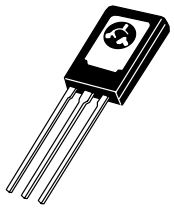
. . . designed for low power audio amplifier and low–current, high–speed switching applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — MJE243, MJE253
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40–200
  = 40–120 — MJE243, MJE253
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages
  I_{CBO} = 100 nAdc (Max) @ Rated V_{CB}

NPN
MJE243*
PNP
MJE253*

*ON Semiconductor Preferred Device

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
100 VOLTS
15 WATTS



CASE 77–09
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0	Adc
Base Current	I_B	10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/ac
Total Power Dissipation @ T_A = 25°C Derate @ 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 9
Publication Order Number:
MJE243/D

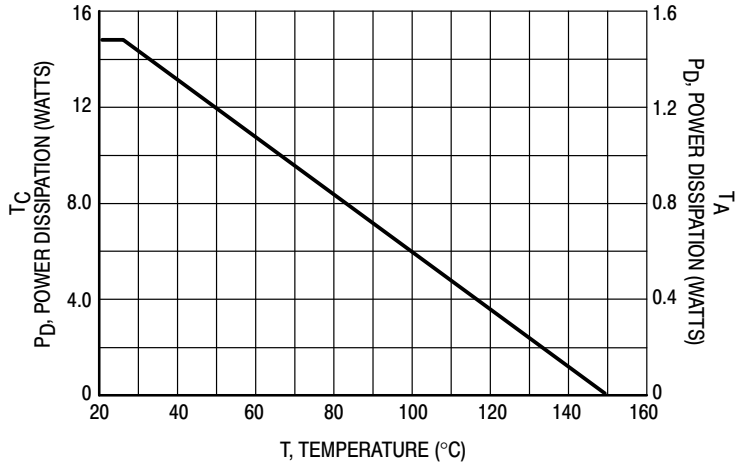
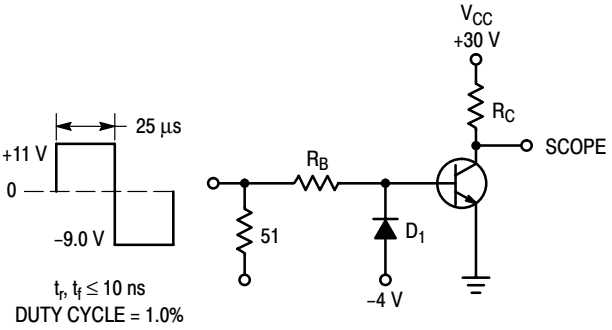


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CE} = 100 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}	 — —	 0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 40 15	 180 —	—
Collector–Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	 — —	 0.3 0.6	Vdc
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	50	pF



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 2. Switching Time Test Circuit

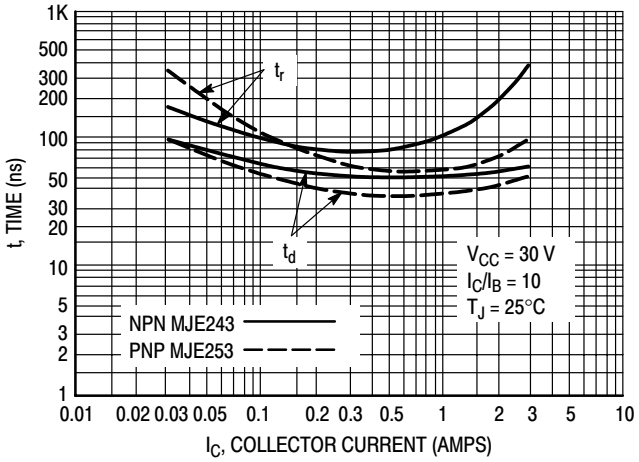


Figure 3. Turn−On Time

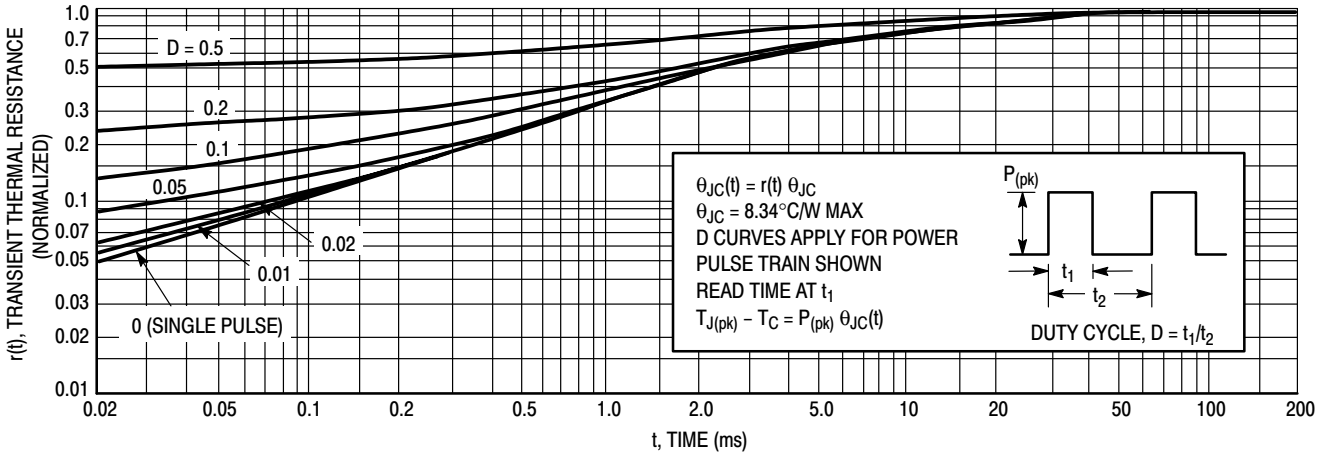


Figure 4. Thermal Response

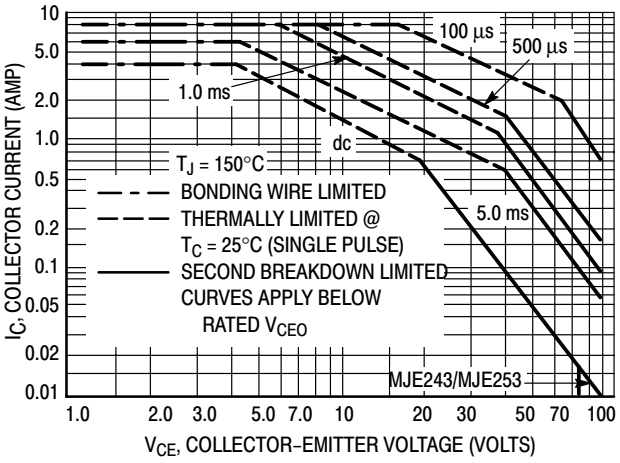


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

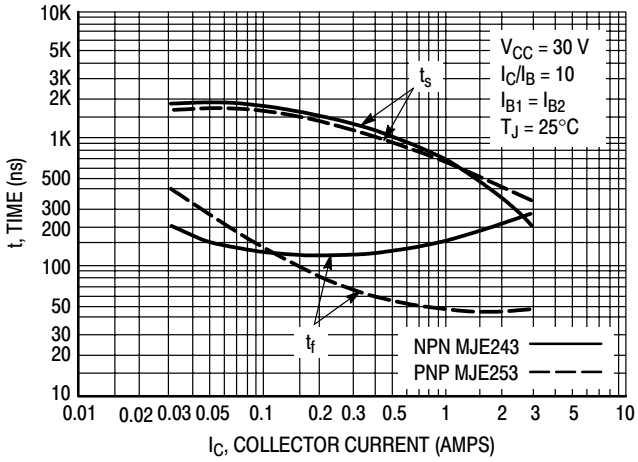


Figure 6. Turn–Off Time

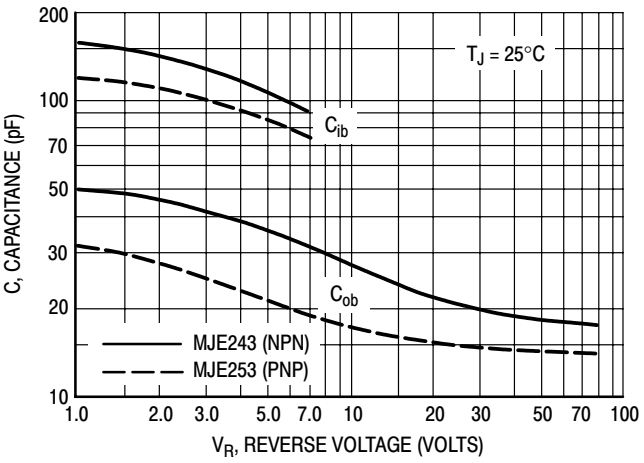
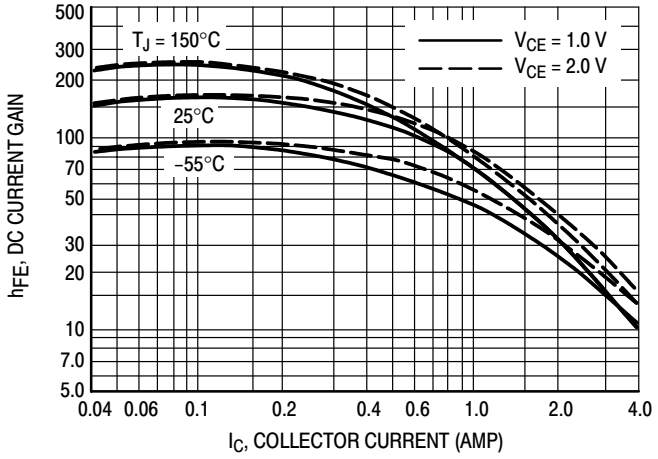


Figure 7. Capacitance

NPN
MJE243



PNP
MJE253

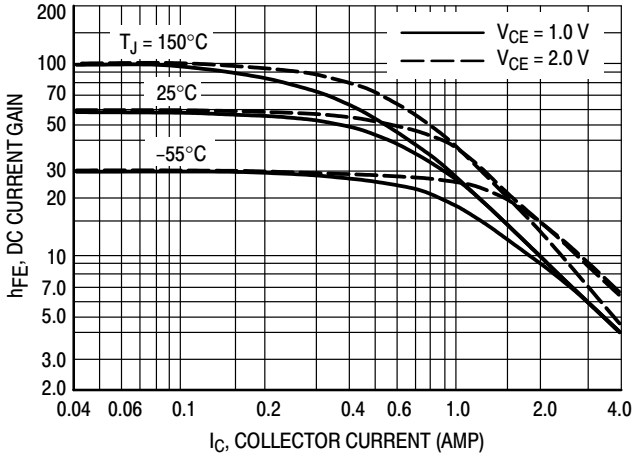
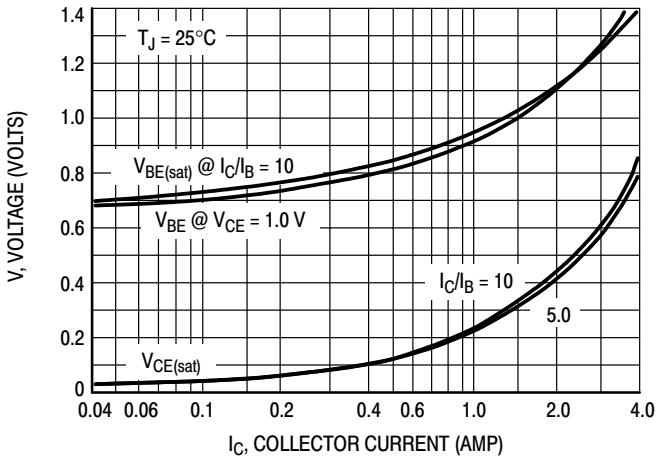


Figure 8. DC Current Gain



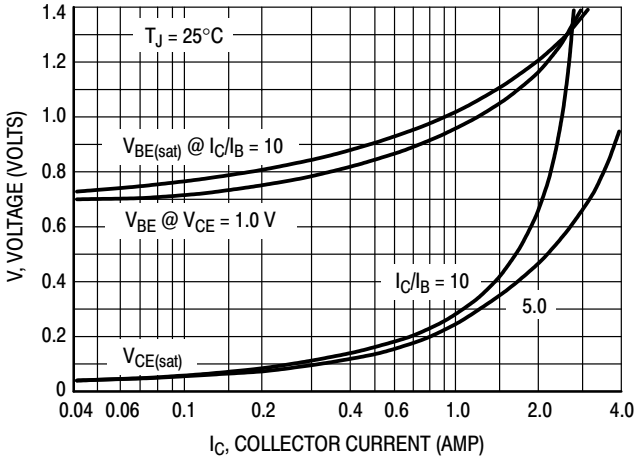
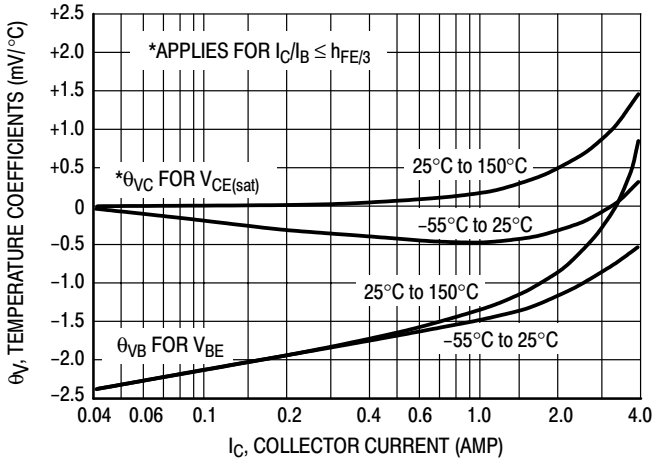


Figure 9. “On” Voltages



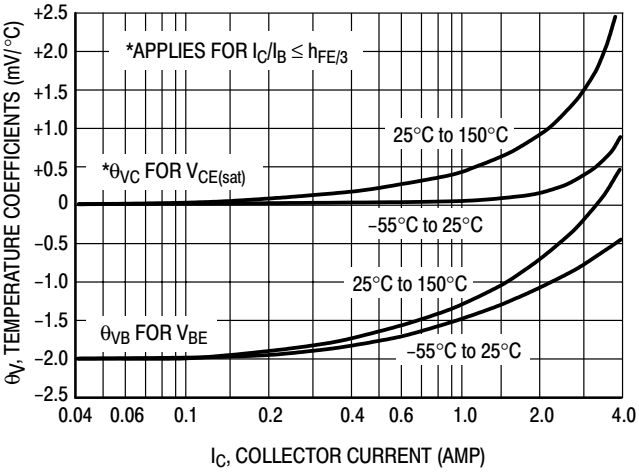


Figure 10. Temperature Coefficients

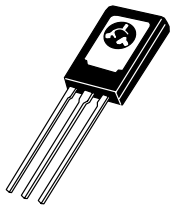
Complementary Silicon Power Transistors

. . . designed specifically for use with the MC3419 Solid–State Subscriber Loop Interface Circuit (SLIC).

- High Safe Operating Area
  $I_{S/B}$ @ 40 V, 1.0 s = 0.375 A — TO–126
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- High DC Current Gain
  h_{FE} @ 120 mA, 10 V = 1500 (Min)

NPN
MJE270
PNP
MJE271

2.0 AMPERE
COMPLEMENTARY
POWER DARLINGTON
TRANSISTORS
100 VOLTS
15 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	2.0 4.0	Adc
Base Current	I_B	0.1	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.3	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, non–repetitive)	$I_{S/b}$	375	—	Adc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 20 mAdc, V_{CE} = 3.0 Vdc) (I_C = 120 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 500 1500	 — —	—
Collector–Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 0.2 mAdc) (I_C = 120 mAdc, I_B = 1.2 mAdc)	$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 120 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 0.05 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	—	MHz

NOTES:
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

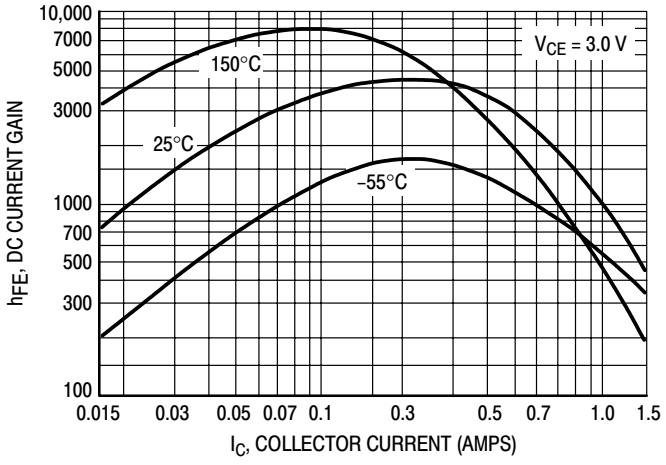


Figure 1. DC Current Gain

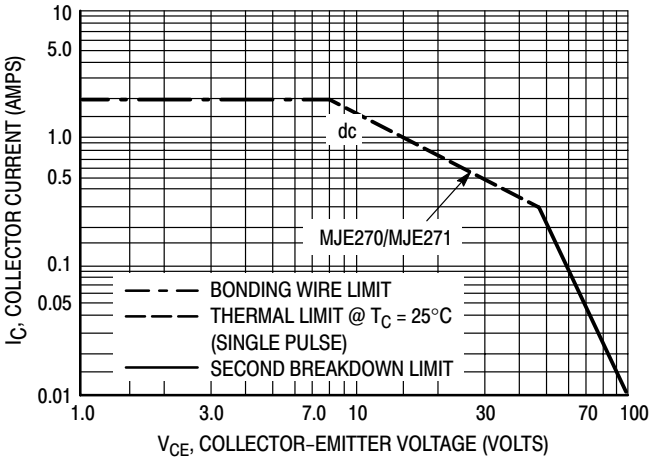


Figure 2. Safe Operating Area

Complementary Silicon Plastic Power Transistors

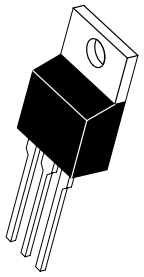
. . . designed for use in general–purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product —
  f_T = 2.0 MHz (Min) @ I_C
  = 500 mAdc

PNP
MJE2955T*
NPN
MJE3055T*

*ON Semiconductor Preferred Device

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 VOLTS
75 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CB}	70	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C MJE3055T, MJE2955T	P_D†	75 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

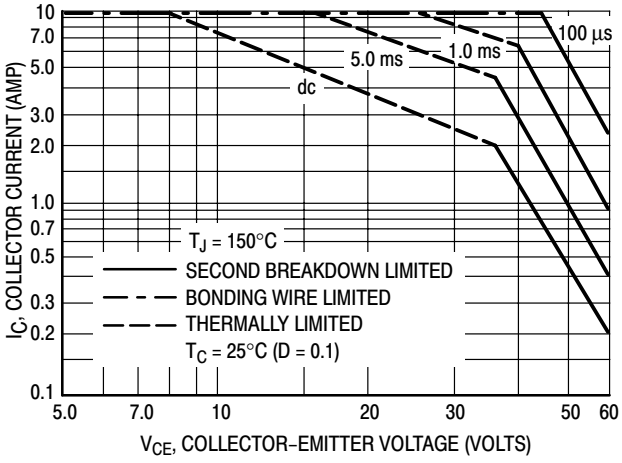


Figure 1. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4 0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 100 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 8.0	Vdc
Base–Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 20%.

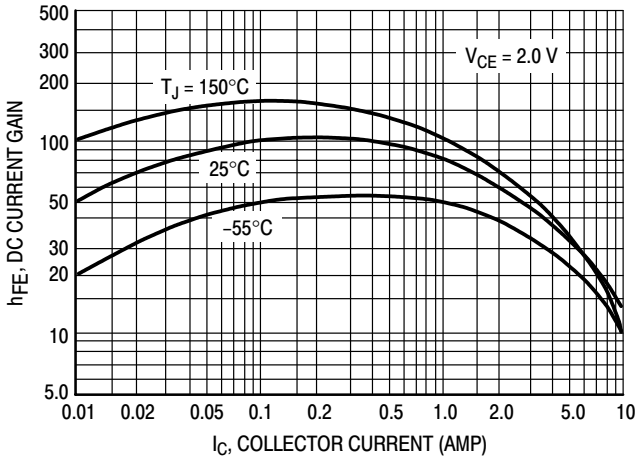


Figure 2. DC Current Gain

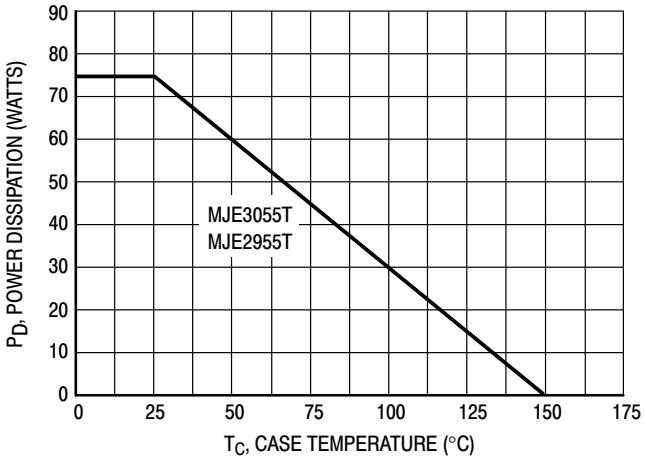
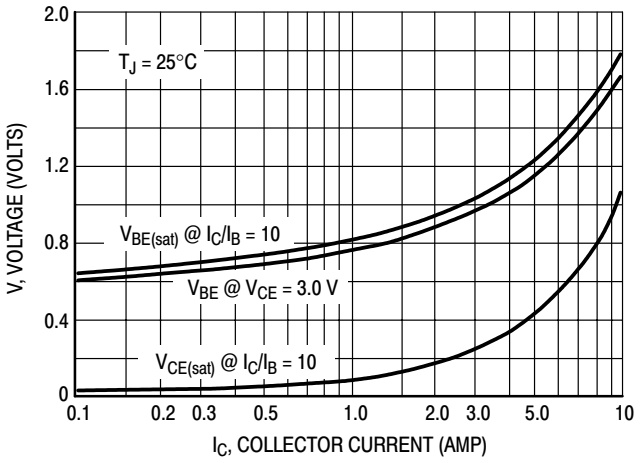


Figure 3. Power Derating

MJE2955T



MJE3055T

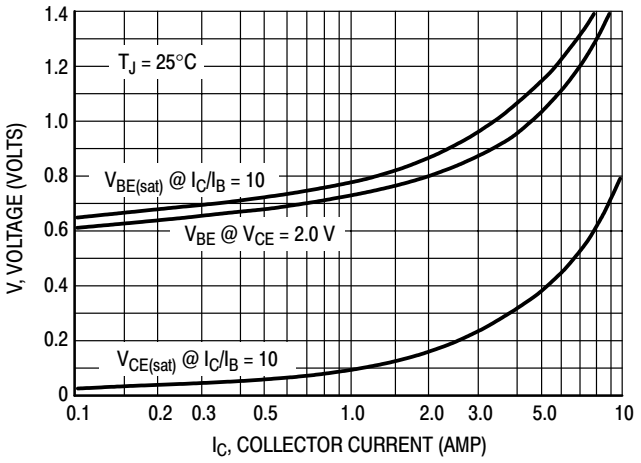


Figure 4. “On” Voltages

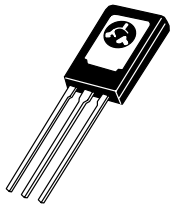
MJE340

Plastic Medium Power NPN Silicon Transistor

. . . useful for high–voltage general purpose applications.

- Suitable for Transformerless, Line–Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
300 VOLTS
20 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Emitter–Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

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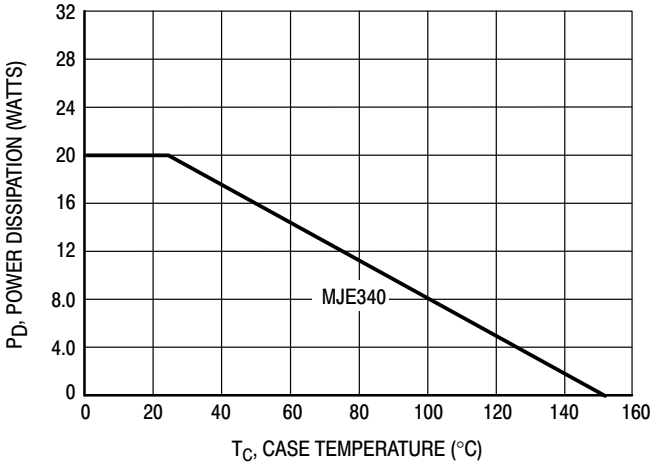


Figure 5. Power Temperature Derating

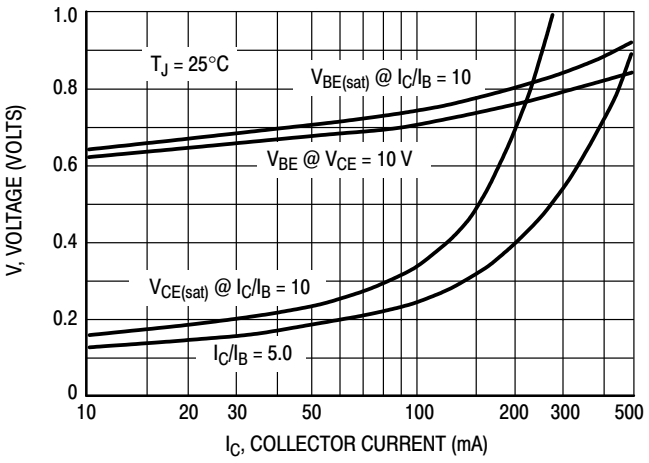


Figure 6. "On" Voltages

ACTIVE–REGION SAFE OPERATING AREA

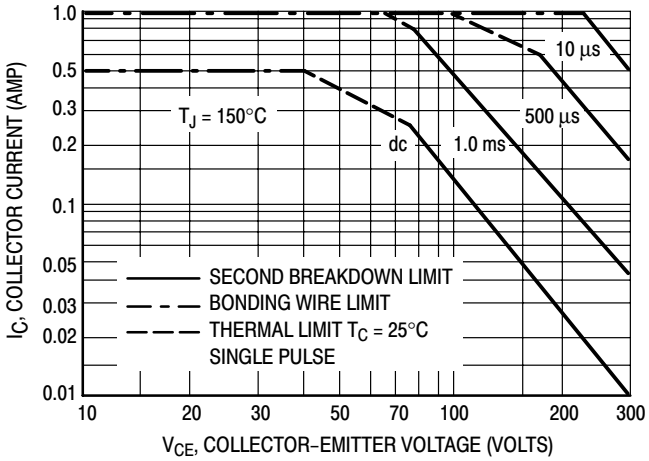


Figure 7. MJE340

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

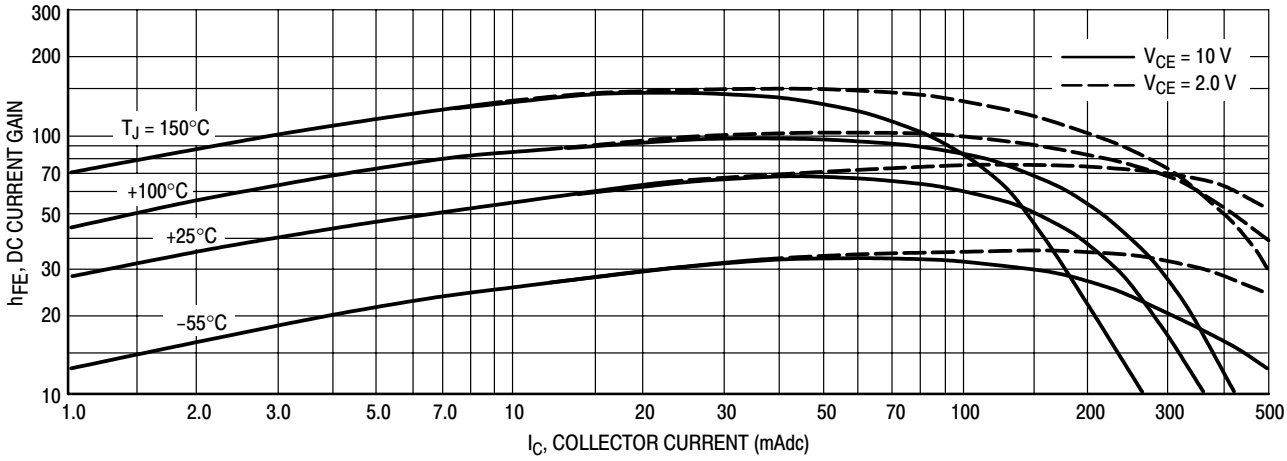


Figure 8. DC Current Gain

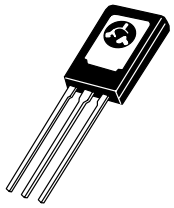
MJE3439

NPN Silicon High-Voltage Power Transistors

0.3 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
15 WATTS

. . . designed for use in line–operated equipment requiring high f_T.

- High DC Current Gain
  h_{FE} = 40–160 @ I_C
  = 20 mAdc
- Current Gain Bandwidth Product —
  f_T = 15 MHz (Min) @ I_C
  = 10 mAdc
- Low Output Capacitance
  C_{ob} = 10 pF (Max) @ f
  = 1.0 MHz



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	350	Vdc
Collector–Base Voltage	V_{CB}	450	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	0.3	Adc
Base Current	I_B	150	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	°C/W

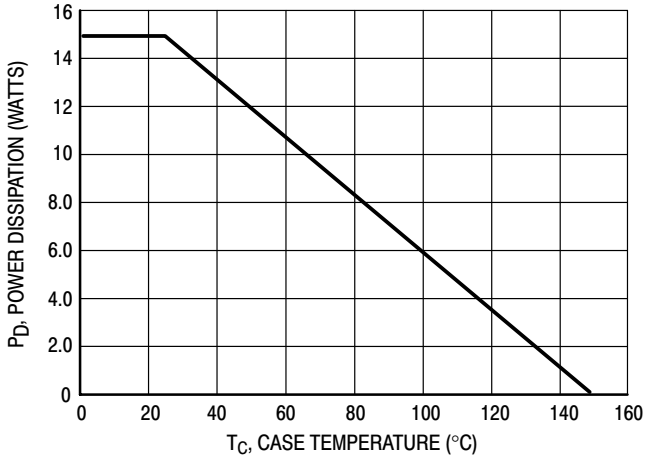


Figure 1. Power–Temperature Derating Curve

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MJE3439/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	350	—	Vdc
Collector Cutoff Current (V_{CE} = 300 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	—	500	μAdc
Collector Cutoff Current (V_{CB} = 350 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	20	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc) (I_C = 20 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 30 15	 — 200	—
Collector–Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)	$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	0.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)	f_T	15	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	10	pF
Small–Signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	—	—

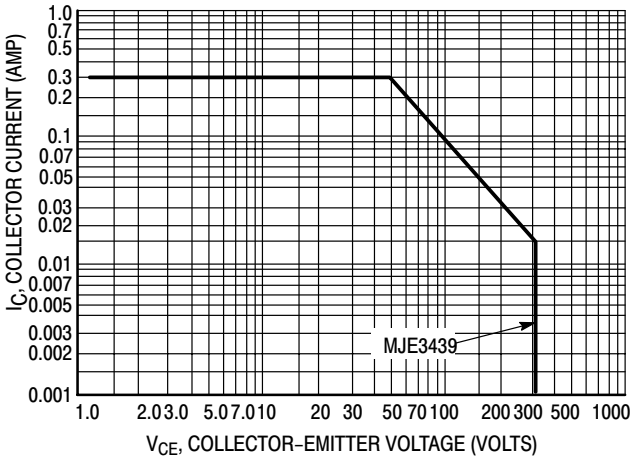


Figure 2. Active–Region Safe Operating Area

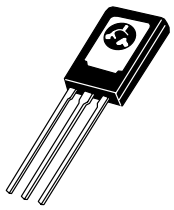
The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

MJE344

Plastic NPN Silicon Medium-Power Transistor

. . . useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
150–200 VOLTS
20 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	MJE344	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CB}	200	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Base Current	I_B	250	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

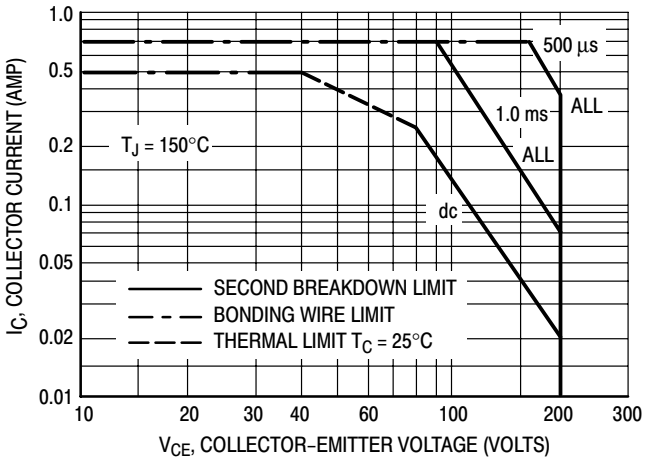


Figure 1. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less then the limitations imposed by second breakdown.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	300	—
Collector–Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 10 MHz)	f_T	15	—	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	—	15	pF
Small–Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	—	—

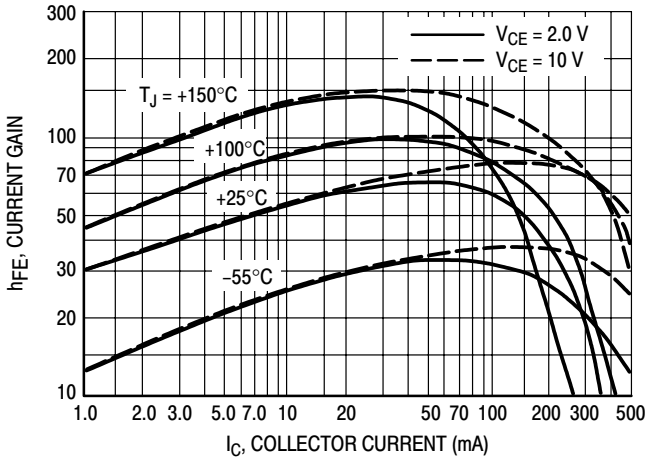


Figure 2. DC Current Gain

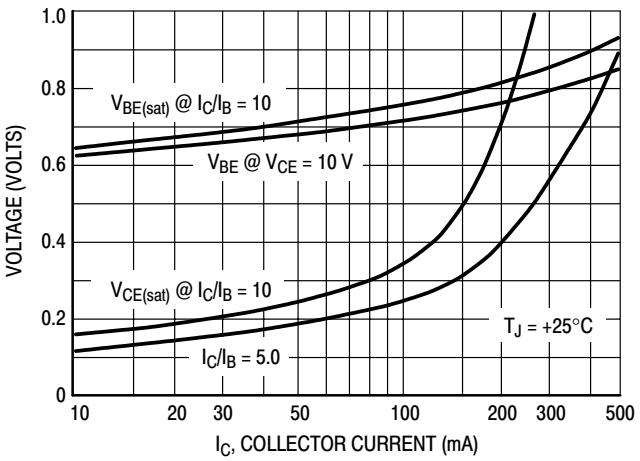


Figure 3. “On” Voltages

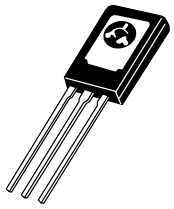
MJE350

Plastic Medium Power PNP Silicon Transistor

. . . designed for use in line–operated applications such as low power, line–operated series pass and switching regulators requiring PNP capability.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain —
  h_{FE} = 30–240 @ I_C = 50 mAdc
- Plastic Thermopad Package

0.5 AMPERE POWER TRANSISTOR PNP SILICON 300 VOLTS 20 WATTS



CASE 77–09 TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Emitter–Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

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Publication Order Number: MJE350/D

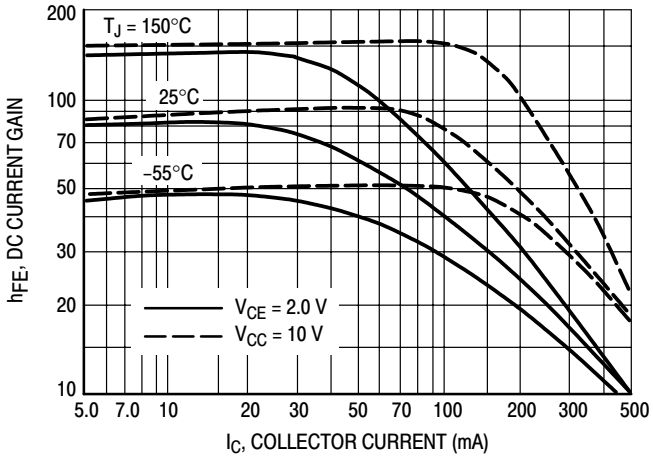


Figure 1. DC Current Gain

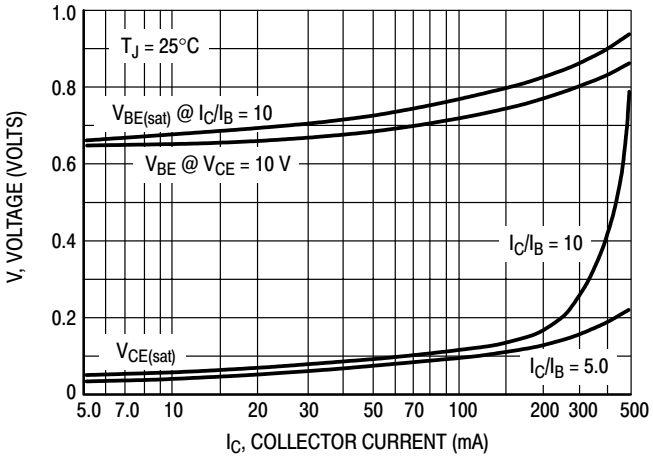


Figure 2. "On" Voltages

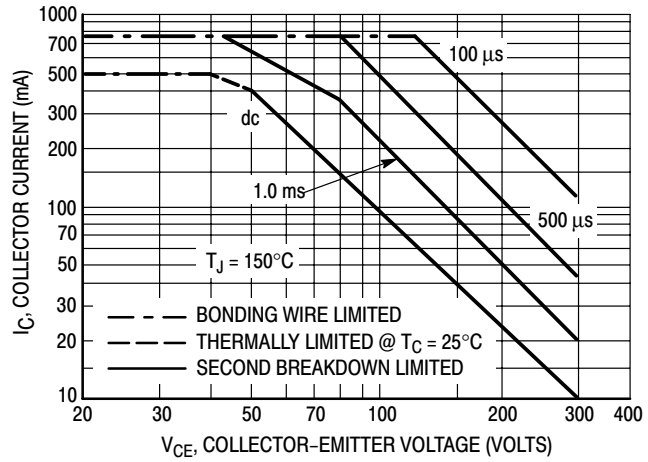


Figure 3. Active−Region Safe Operating Area

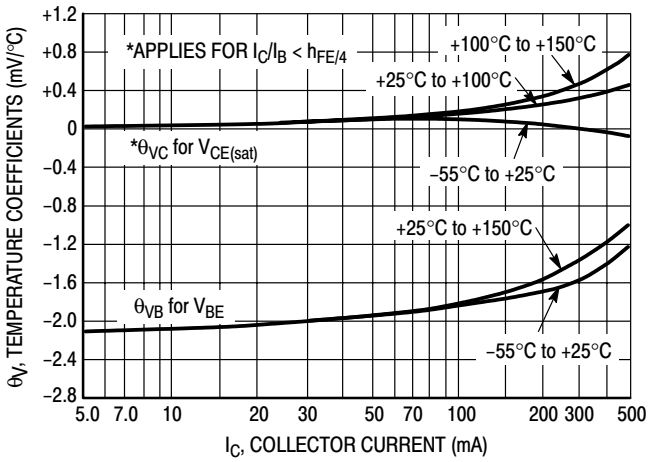


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

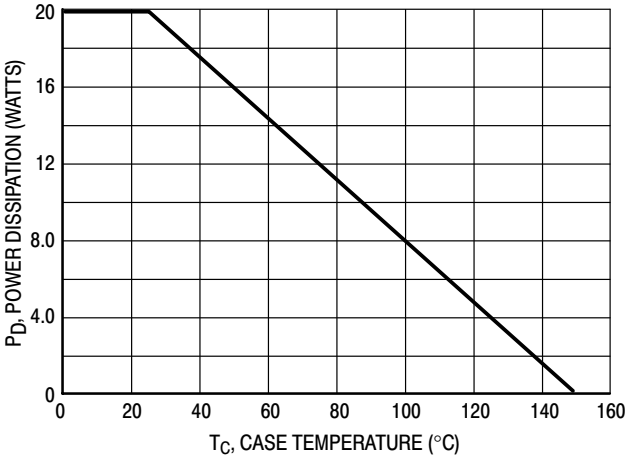


Figure 5. Power Derating

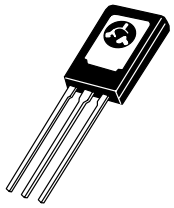
MJE371

Plastic Medium-Power PNP Silicon Transistors

4 AMPERE
POWER TRANSISTOR
PNP SILICON
40 VOLTS
40 WATTS

. . . designed for use in general–purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C
  = 1.0 Adc
- MJE371 is Complementary to NPN MJE521



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CB}	40	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter–Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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Publication Order Number:
MJE371/D

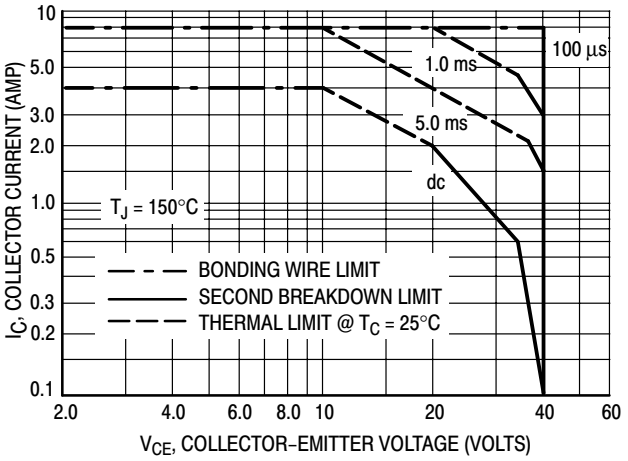


Figure 1. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less then the limitations imposed by second breakdown.

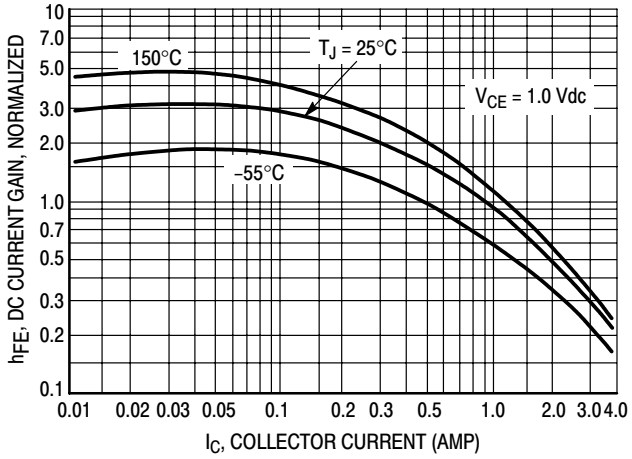


Figure 2. DC Current Gain

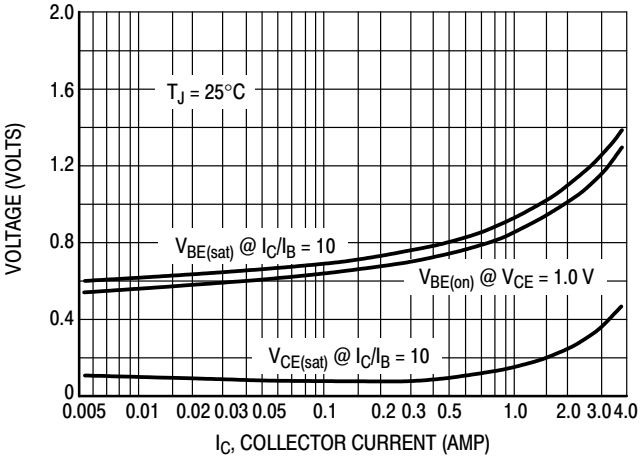


Figure 3. "On" Voltage

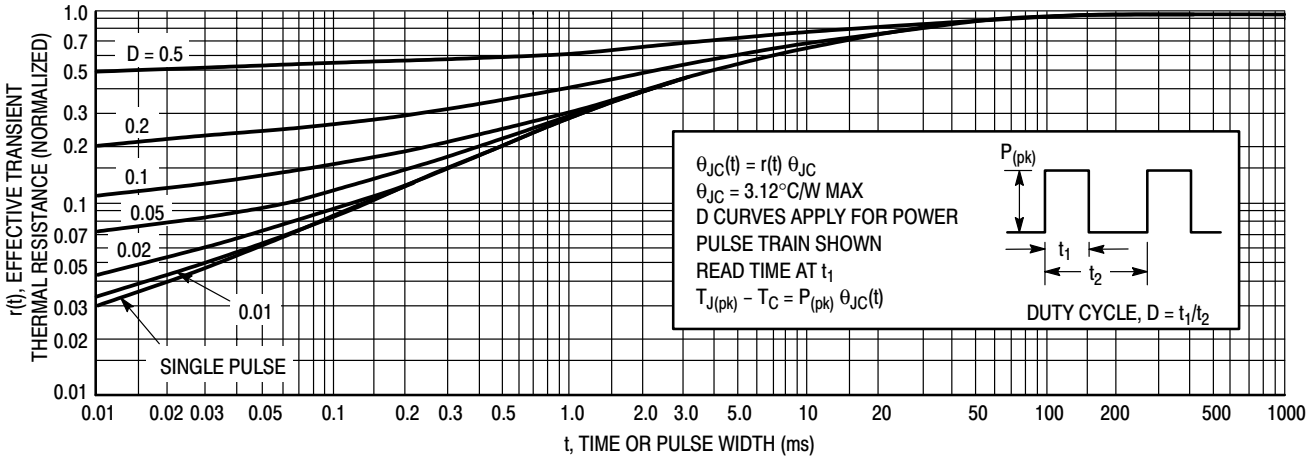


Figure 4. Thermal Response

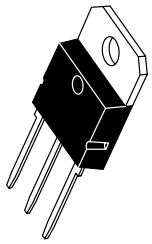
High-Voltage — High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector–Emitter Sustaining Voltage —
  NPN PNP
  $V_{CEO(sus)}$ = 160 Vdc — MJE4343 MJE4353
- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 35 (Typ)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C
  = 8.0 Adc

NPN
MJE4343
PNP
MJE4353

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
160 VOLTS



CASE 340D–02
TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V_{CEO}	160	Vdc
Collector–Base Voltage	V_{CB}	160	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak (1)	I_C	16 20	Adc
Base Current — Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C	P_D	125	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

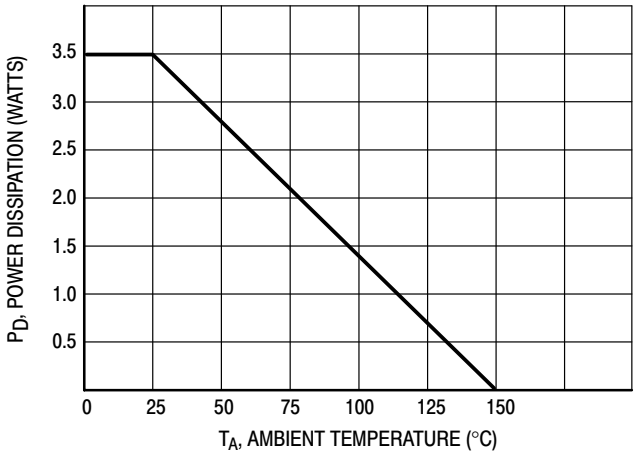


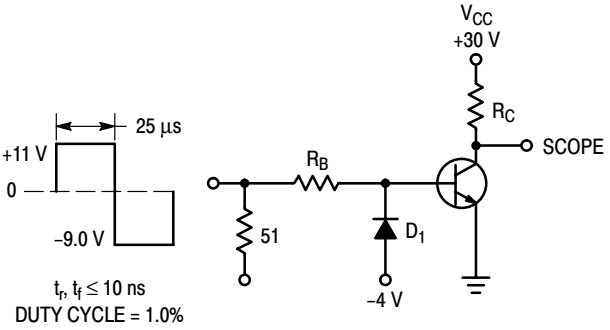
Figure 1. Power Derating
Reference: Ambient Temperature

April, 2001 – Rev. 2
Publication Order Number:
MJE4343/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	 160	 —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CEO}	 —	 750	μAdc
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	1.0 5.0	mAdc
Collector–Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	—	750	μAdc
Emitter–Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 15 8.0	 35 (Typ) 15 (Typ)	—
Collector–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 800 mA) (I_C = 16 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	 — —	 2.0 3.5	Vdc
Base–Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	—	3.9	Vdc
Base–Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	3.9	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\geq$ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Note: Reverse polarities to test PNP devices.

Figure 2. Switching Times Test Circuit

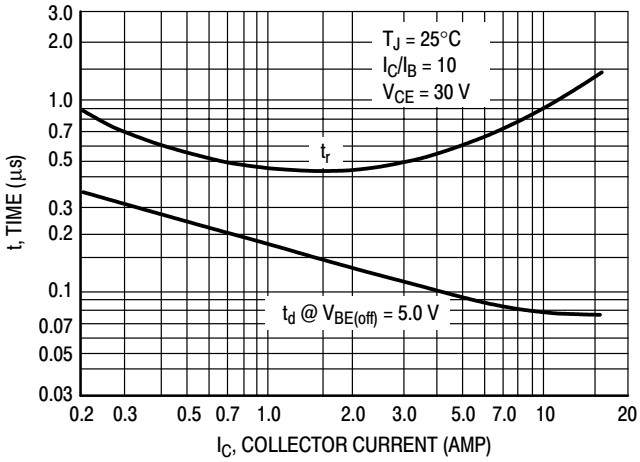


Figure 3. Typical Turn−On Time

TYPICAL CHARACTERISTICS

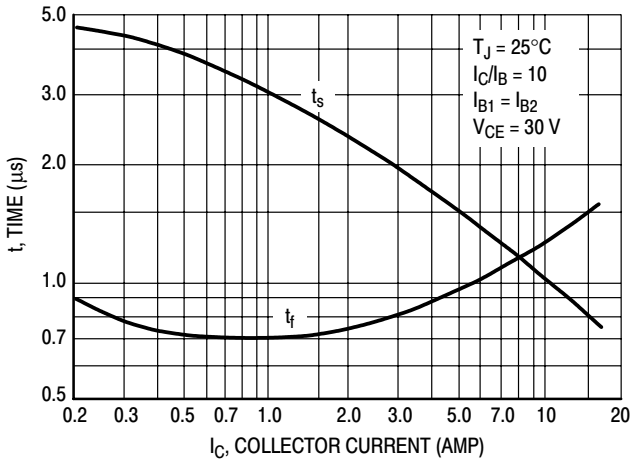


Figure 4. Turn−Off Time

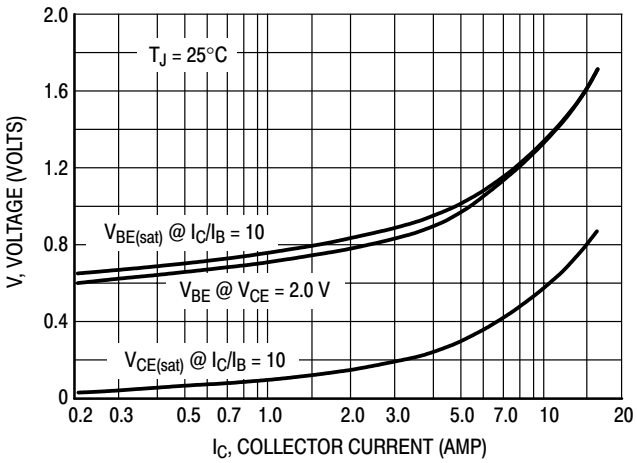


Figure 5. On Voltages

DC CURRENT GAIN

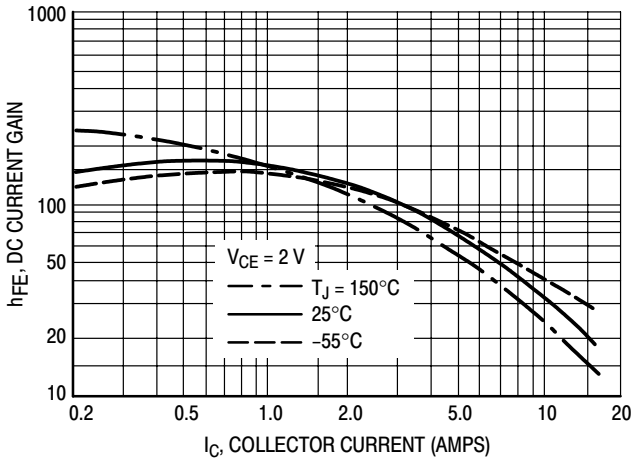


Figure 6. MJE4340 Series (NPN)

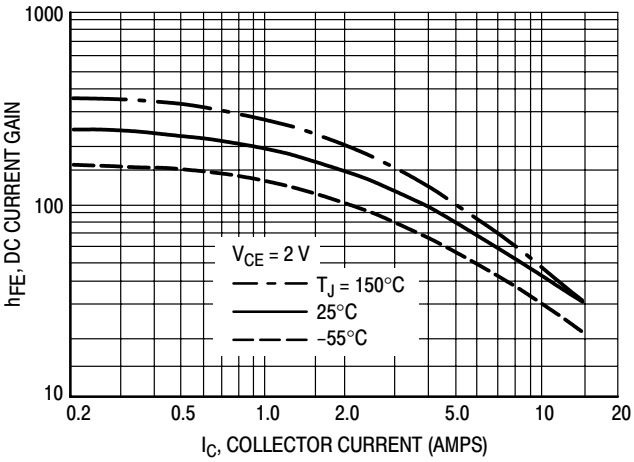


Figure 7. MJE4350 Series (PNP)

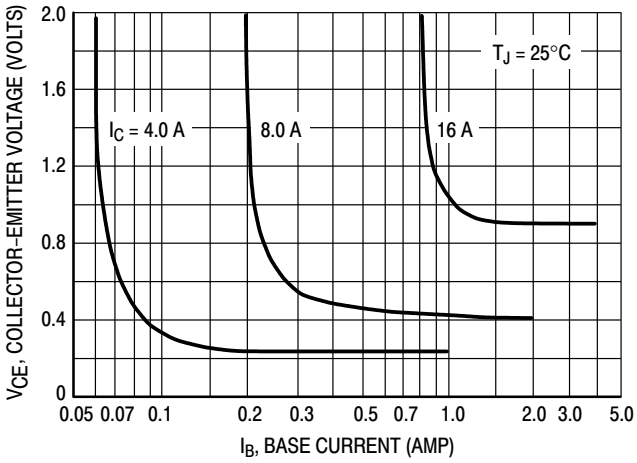


Figure 8. Collector Saturation Region

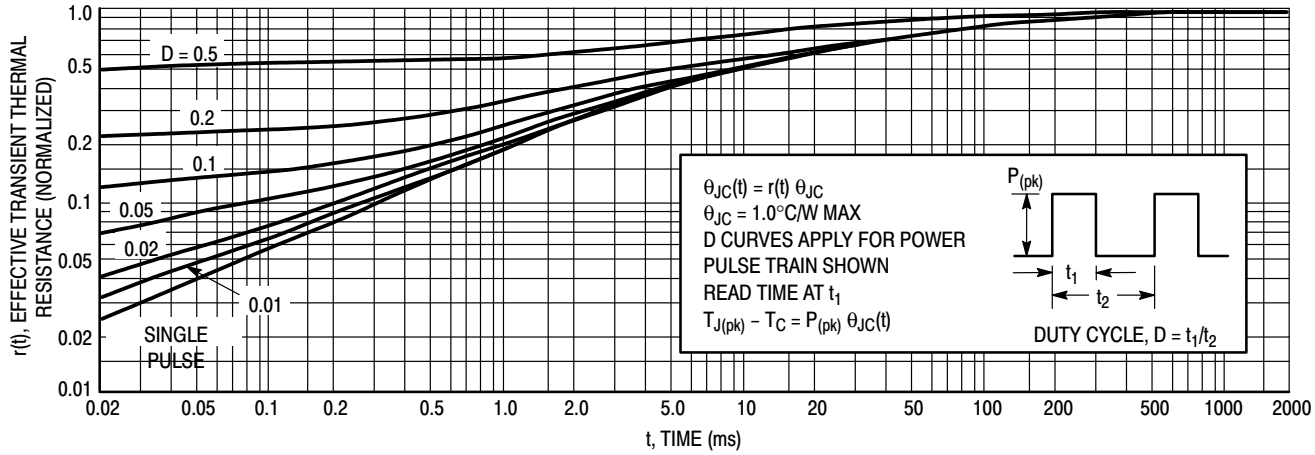


Figure 9. Thermal Response

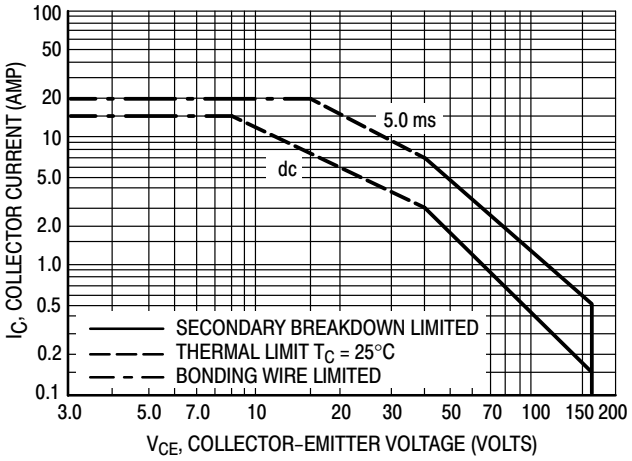


Figure 10. Maximum Forward Bias Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

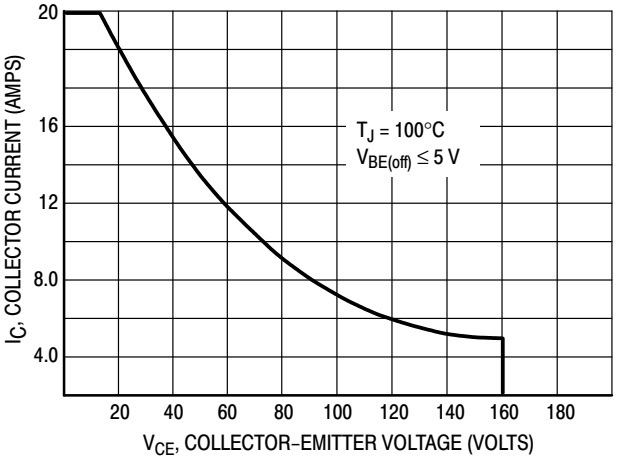


Figure 11. Maximum Reverse Bias Safe Operating Area

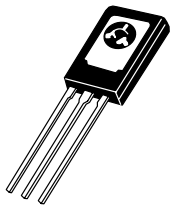
MJE521

Plastic Medium-Power NPN Silicon Transistor

. . . designed for use in general–purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE371

4 AMPERE
POWER TRANSISTOR
NPN SILICON
40 VOLTS
40 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CB}	40	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter–Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

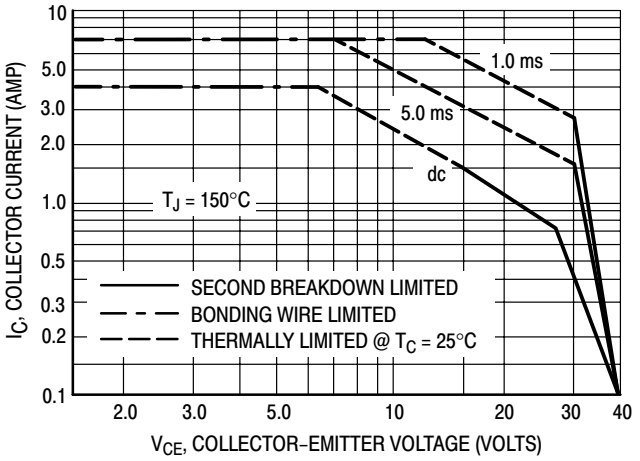


Figure 1. Active–Region Safe Operating Area

The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided (T_{Jpk}) ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

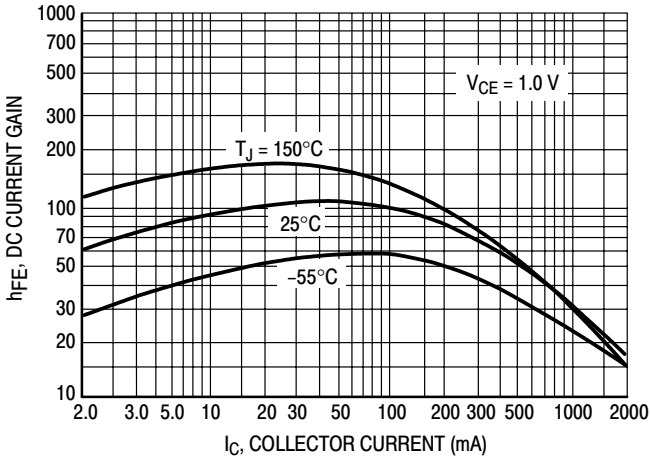


Figure 2. DC Current Gain

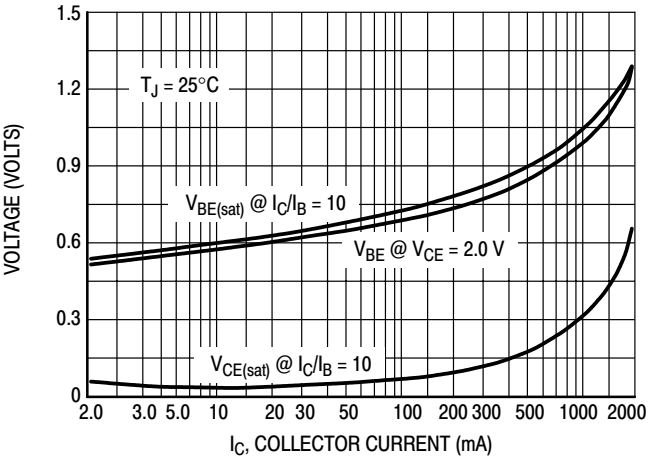


Figure 3. “On” Voltage

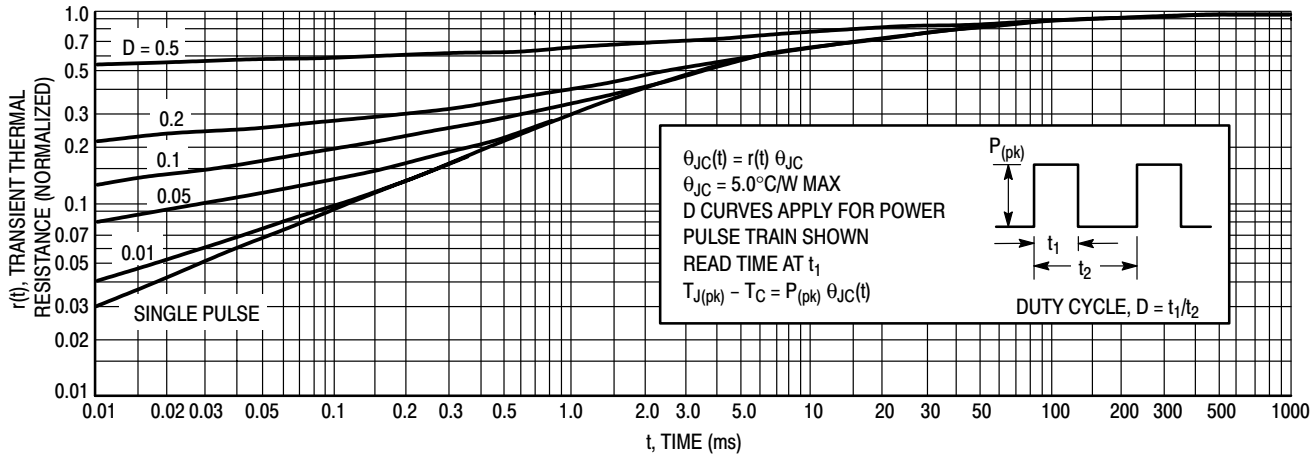


Figure 4. Thermal Response

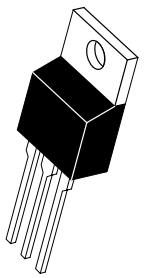
MJE5730
MJE5731
MJE5731A

High Voltage PNP Silicon Power Transistors

. . . designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- 300 V to 400 V (Min) — $V_{CEO(sus)}$
- 1.0 A Rated Collector Current
- Popular TO–220 Plastic Package
- PNP Complements to the TIP47 thru TIP50 Series

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
300–350–400 VOLTS
40 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5730	MJE5731	MJE5731A	Unit
Collector–Emitter Voltage	V_{CEO}	300	350	375	Vdc
Collector–Base Voltage	V_{CB}	300	350	375	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inducting Load Energy (See Figure 10)	E	20			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

April, 2001 – Rev. 3
Publication Order Number:
MJE5730/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	MJE5730		300	—	
	MJE5731		350	—	
	MJE5731A		375	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 200 Vdc, I_B = 0)	MJE5730		—	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	MJE5731		—	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	MJE5731A		—	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 300 Vdc, V_{BE} = 0)	MJE5730		—	1.0	
(V_{CE} = 350 Vdc, V_{BE} = 0)	MJE5731		—	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	MJE5731A		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	—
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	1.0	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	1.5	Vdc
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product		f_T	10	—	MHz
(I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)					
Small–Signal Current Gain		h_{fe}	25	—	—
(I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

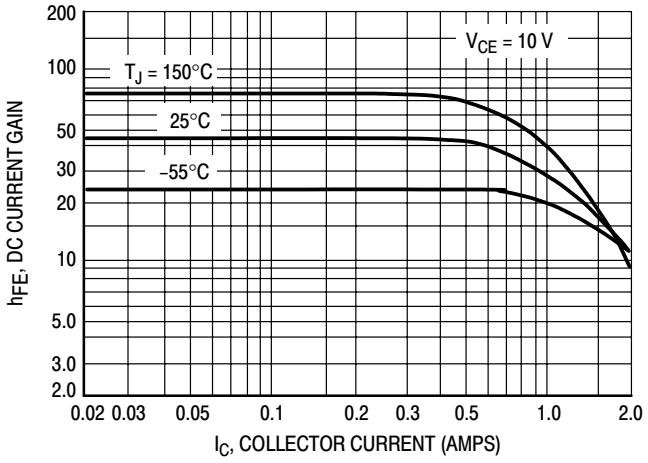


Figure 1. DC Current Gain

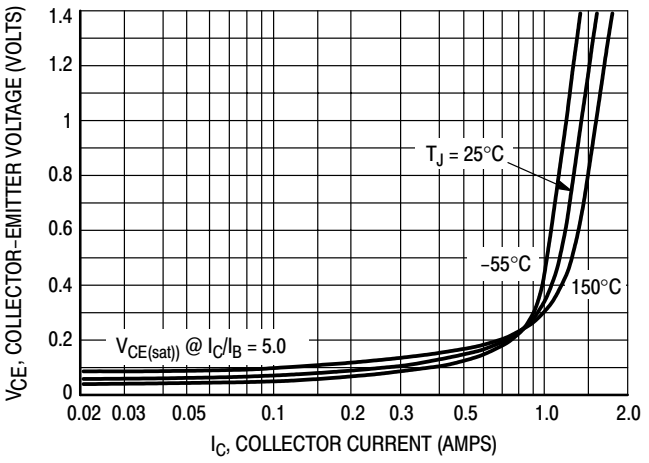


Figure 2. Collector–Emitter Saturation Voltage

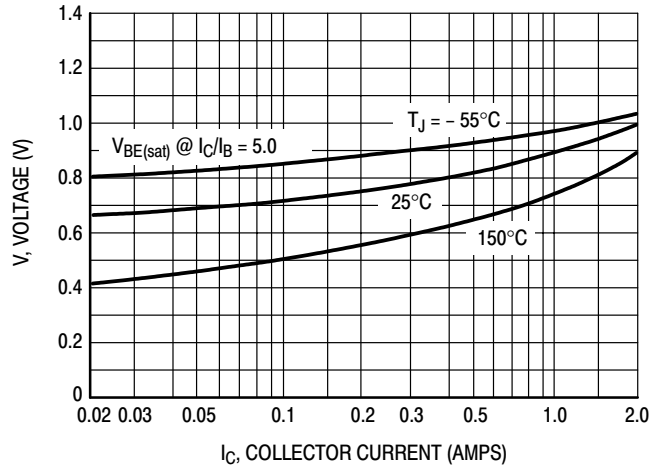


Figure 3. Base–Emitter Voltage

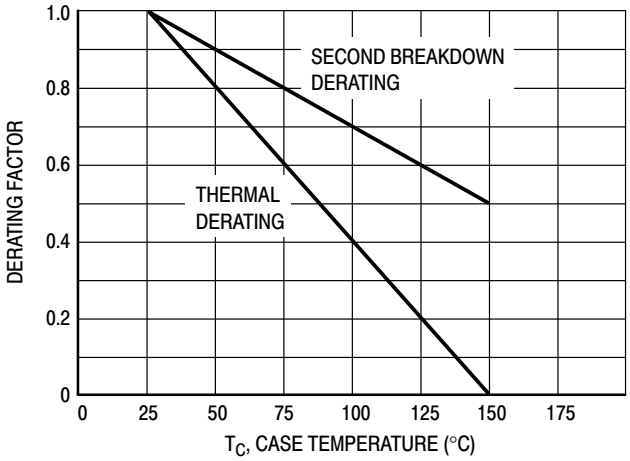


Figure 4. Normalized Power Derating

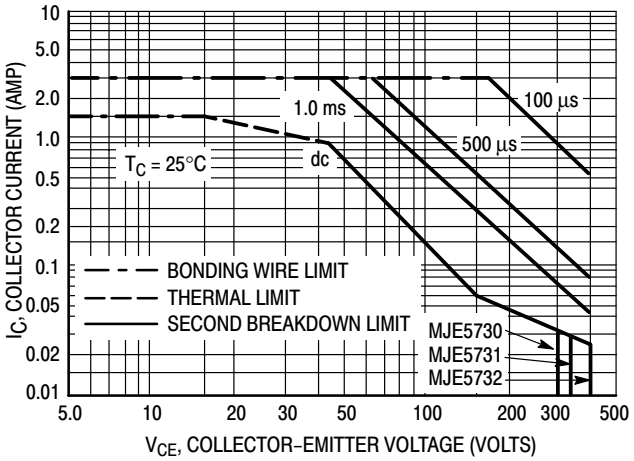


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

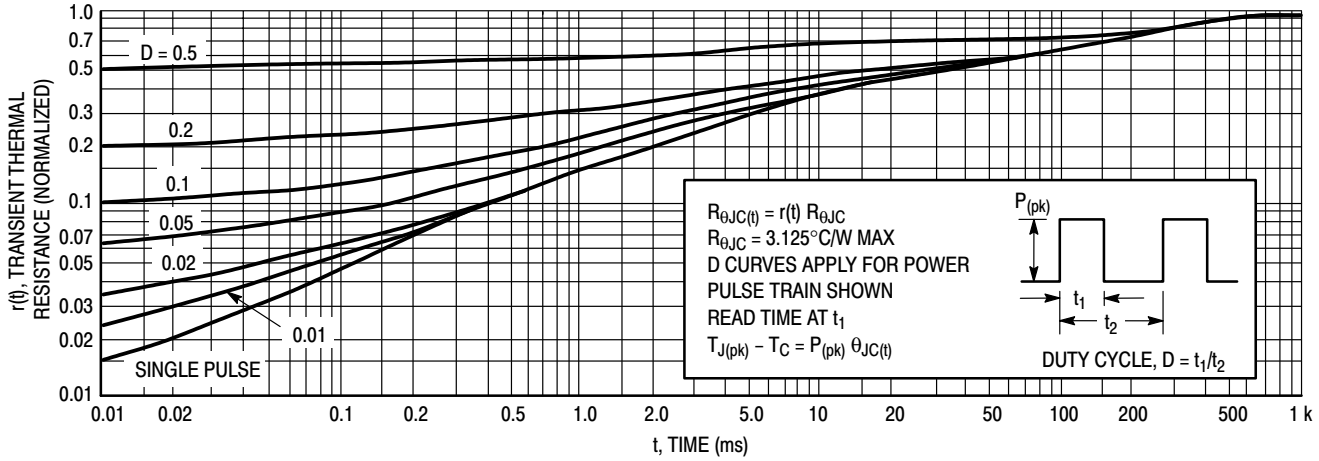


Figure 6. Thermal Response

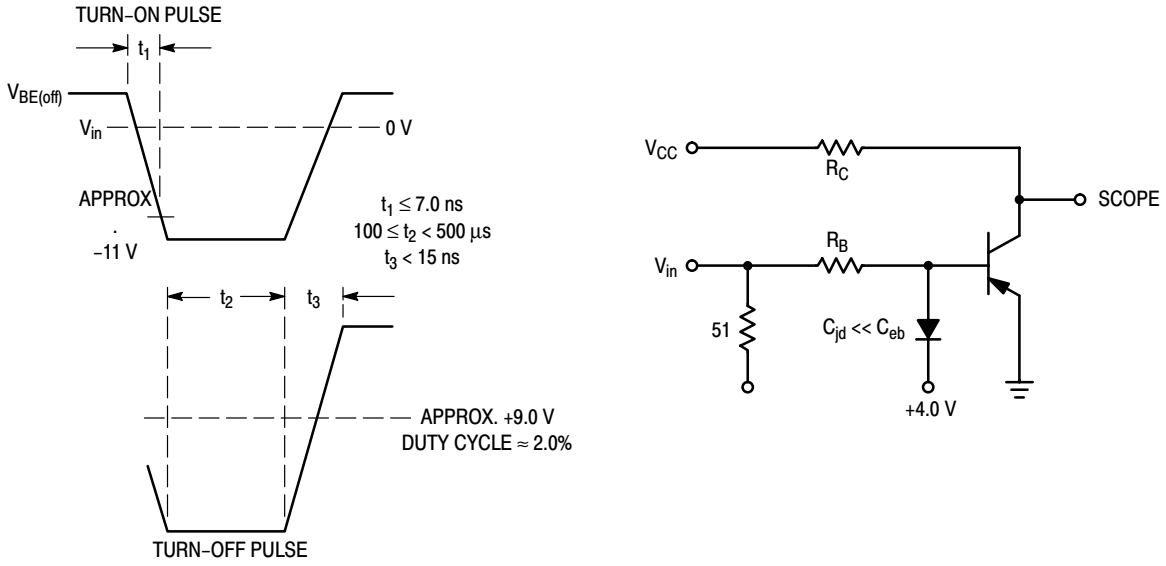


Figure 7. Switching Time Equivalent Circuit

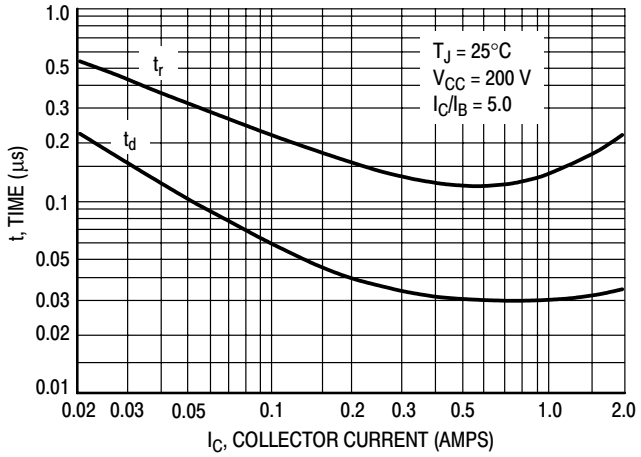


Figure 8. Turn−On Resistive Switching Times

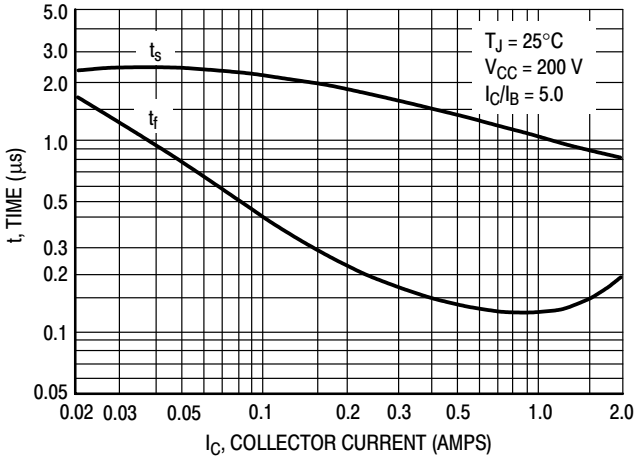
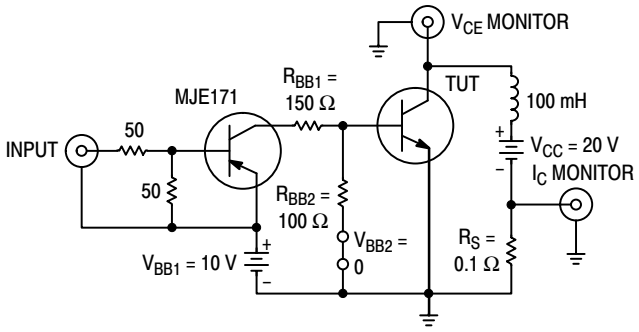


Figure 9. Resistive Turn−Off Switching Times

Test Circuit



Voltage and Current Waveforms

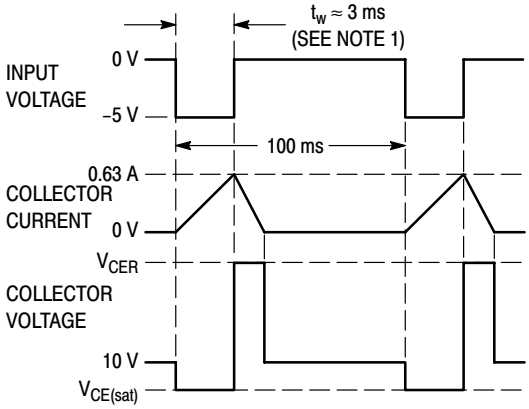


Figure 10. Inductive Load Switching

NPN Silicon Power Darlington Transistors

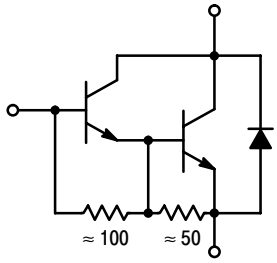
MJE5740
MJE5742*

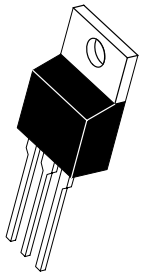
*ON Semiconductor Preferred Device

The MJE5740 and MJE5742 Darlington transistors are designed for high–voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

POWER DARLINGTON TRANSISTORS
8 AMPERES
300, 400 VOLTS
80 WATTS





CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5740	MJE5742	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector–Emitter Voltage	V_{CEV}	600	800	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	8 16		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2 16		 Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 80 640		 Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle = 10%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 4
Publication Order Number:
MJE5740/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector–Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	MJE5740 MJE5742	$V_{CEO(sus)}$	300 400	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	–	–	75	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 7			

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (3)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5 Vdc) (I_C = 4 Adc, V_{CE} = 5 Vdc)		h_{FE}	50 200	100 400	– –	–
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	– – –	2 3 2.2	Vdc
Base–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	– – –	– – –	2.5 3.5 2.4	Vdc
Diode Forward Voltage (4) (I_F = 5 Adc)		V_f	–	–	2.5	Vdc
SWITCHING CHARACTERISTICS						
Typical Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, $I_{C(pk)}$ = 6 A I_{B1} = I_{B2} = 0.25 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.04	–	μs
Rise Time		t_r	–	0.5	–	μs
Storage Time		t_s	–	8	–	μs
Fall Time		t_f	–	2	–	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	($I_{C(pk)}$ = 6 A, $V_{CE(pk)}$ = 250 Vdc I_{B1} = 0.06 A, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	–	4	–	μs
Crossover Time		t_c	–	2	–	μs

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%. (continued)

(3) Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.

(4) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

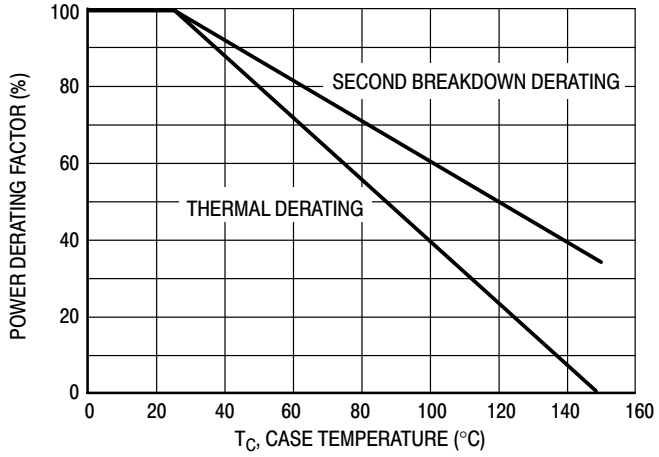


Figure 11. Power Derating

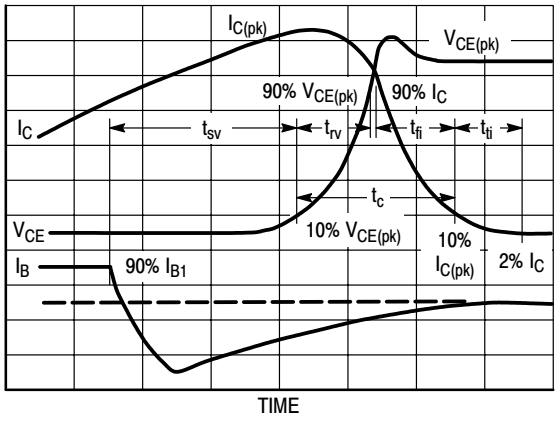


Figure 12. Inductive Switching Measurements

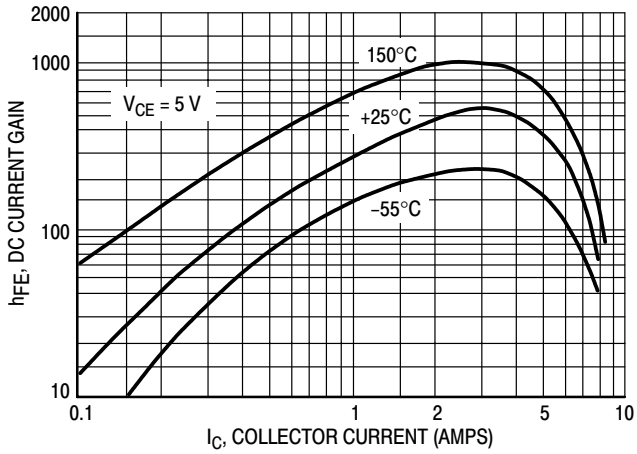


Figure 13. DC Current Gain

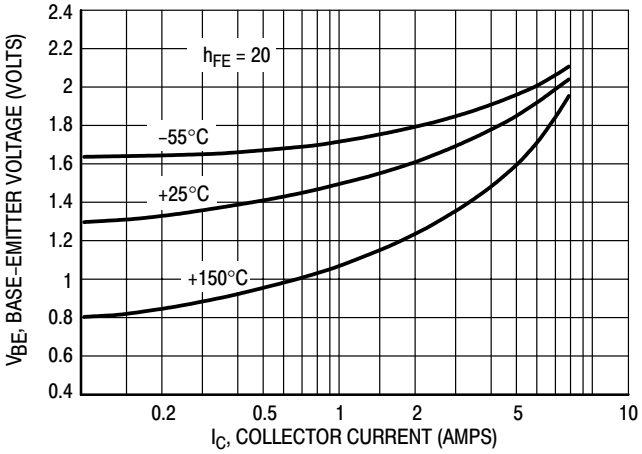
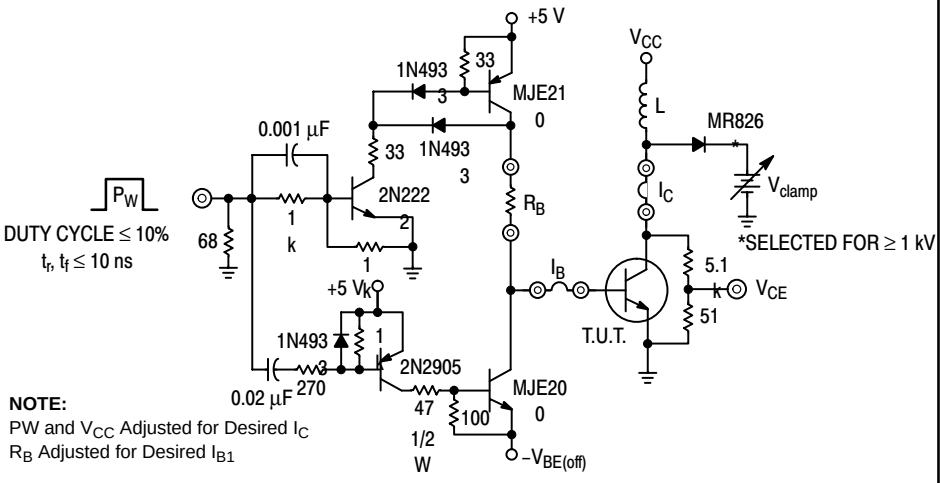
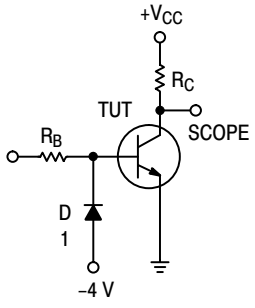
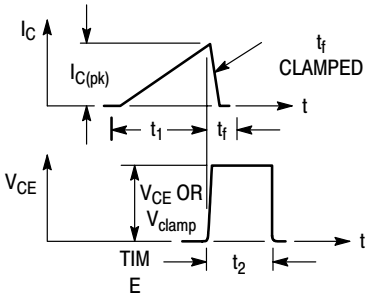
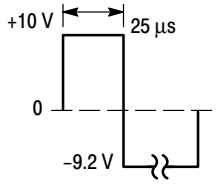


Figure 14. Base−Emitter Voltage

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~16 TURNS) #16 GAP FOR 200 µH/20 A L_{coil} = 200 µH V_{CC} = 30 V $V_{CE(pk)}$ = 250 Vdc $I_{C(pk)}$ = 6 A	V_{CC} = 250 V D1 = 1N5820 OR EQUIV.
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ TEST EQUIPMENT SCOPE−TEKTRONICS 475 OR EQUIVALENT	 t_r, t_f < 10 ns DUTY CYCLE = 1% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

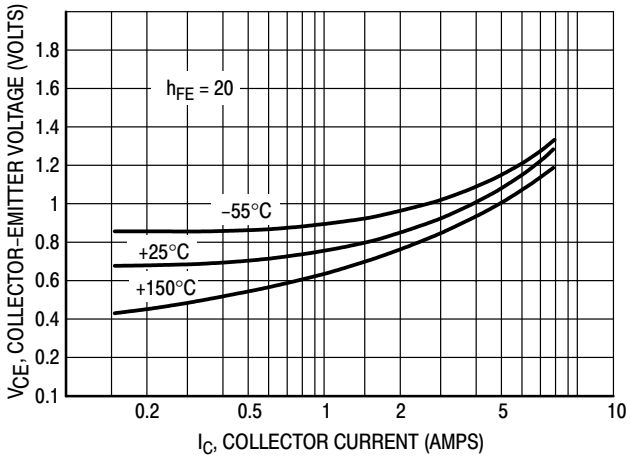


Figure 15. Inductive Switching Measurements

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 11.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

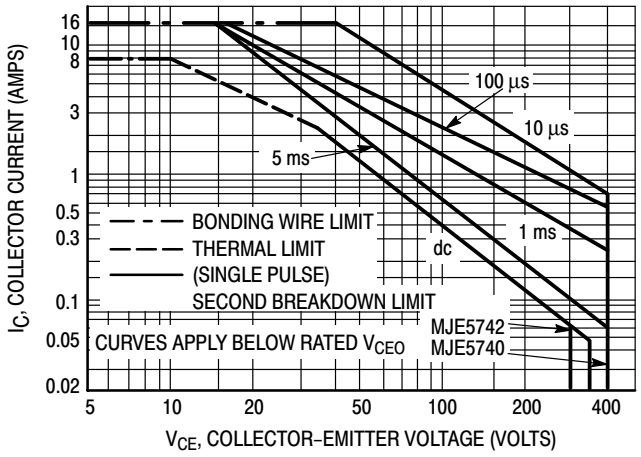


Figure 16. Forward Bias Safe Operating Area

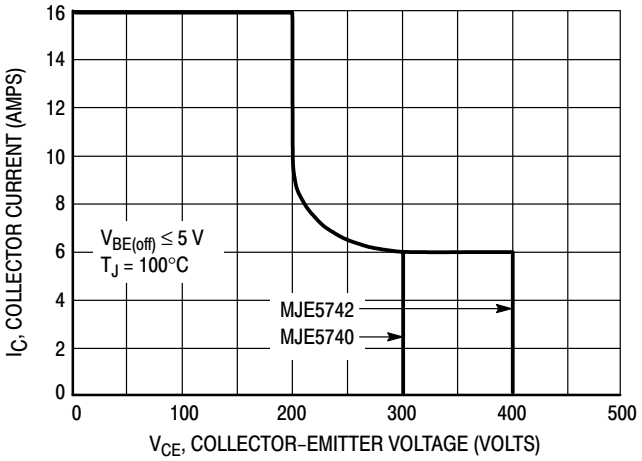


Figure 17. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

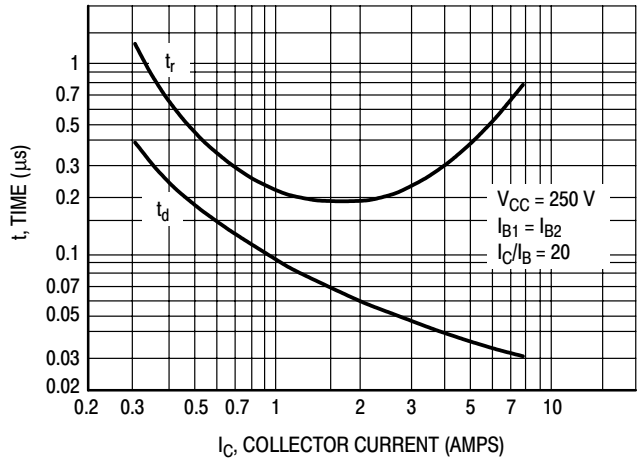


Figure 18. Turn–On Time

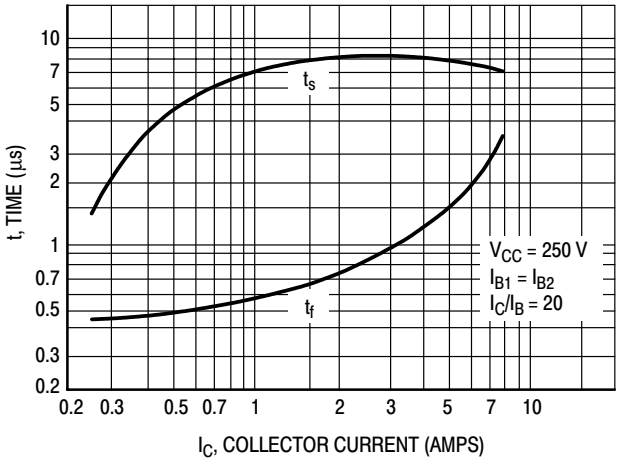


Figure 19. Turn–Off Time

SWITCHMODE™ Series PNP Silicon Power Transistors

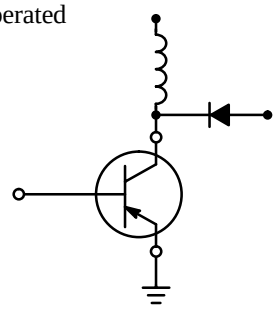
MJE5850
MJE5851*
MJE5852*

*ON Semiconductor Preferred Device

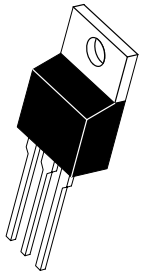
The MJE5850, MJE5851 and the MJE5852 transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated SWITCHMODE applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn–Off Times
100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)
Operating Temperature Range –65 to +150°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



8 AMPERE
PNP SILICON
POWER TRANSISTORS
300, 350, 400 VOLTS
80 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5850	MJE5851	MJE5852	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector–Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 1 6			Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.640			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 2
Publication Order Number:
MJE5850/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE5850 MJE5851 MJE5852	$V_{CEO(sus)}$	300 350 400	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 13			
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc) (I_C = 5.0 Adc, V_{CE} = 5 Vdc)		h_{FE}	 15 5	 — —	 — —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 3.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2.0 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	270	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.100	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	μs
Fall Time		t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	μs
Crossover Time		t_c	—	0.4	1.5	μs
Fall Time		t_{fi}	—	0.1	—	μs
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.125	—	μs
Fall Time		t_{fi}	—	0.1	—	μs

*Pulse Test: PW = 300 μs. Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

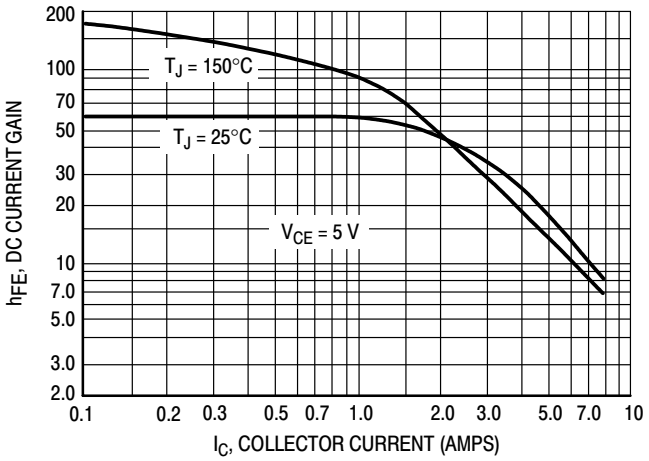


Figure 1. DC Current Gain

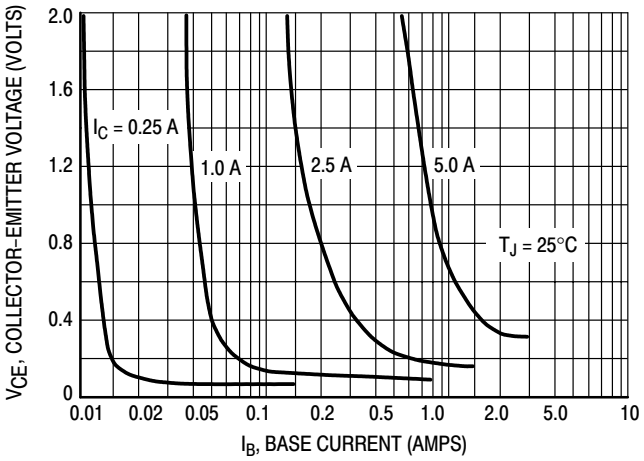


Figure 2. Collector Saturation Region

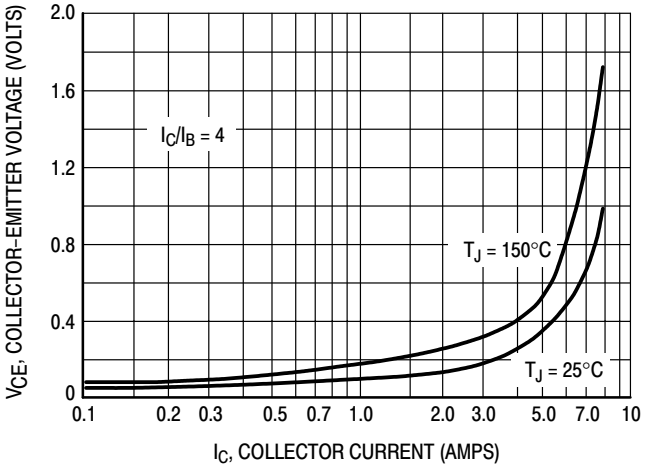


Figure 3. Collector−Emitter Saturation Voltage

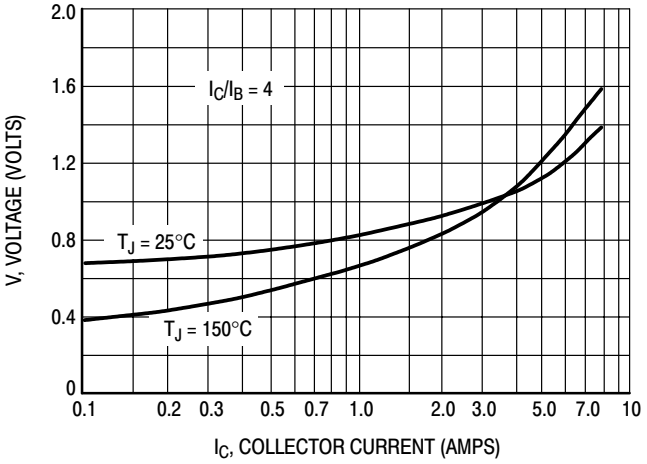


Figure 4. Base−Emitter Voltage

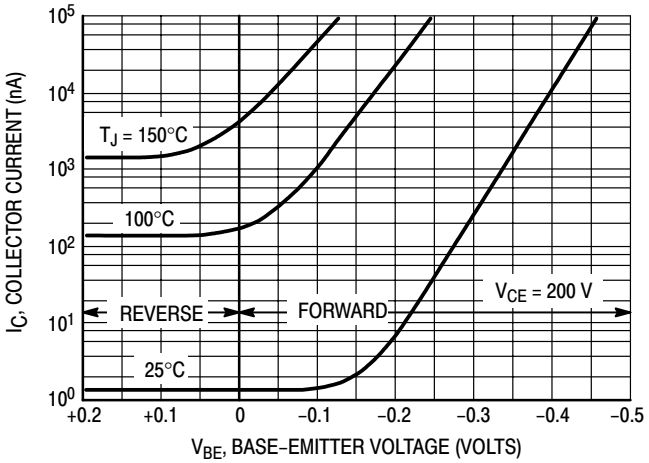


Figure 5. Collector Cutoff Region

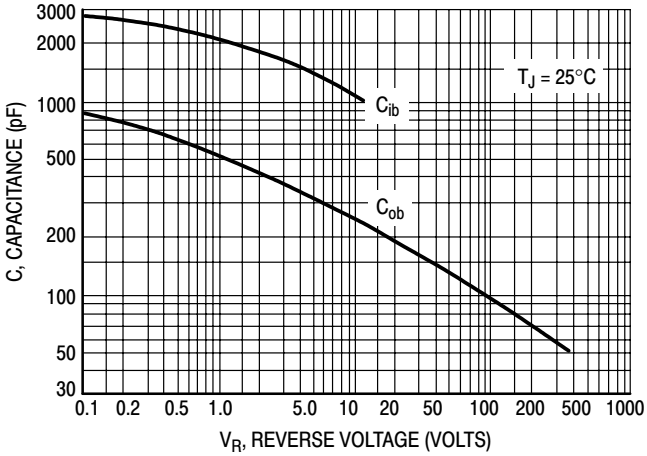
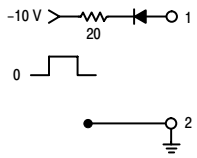
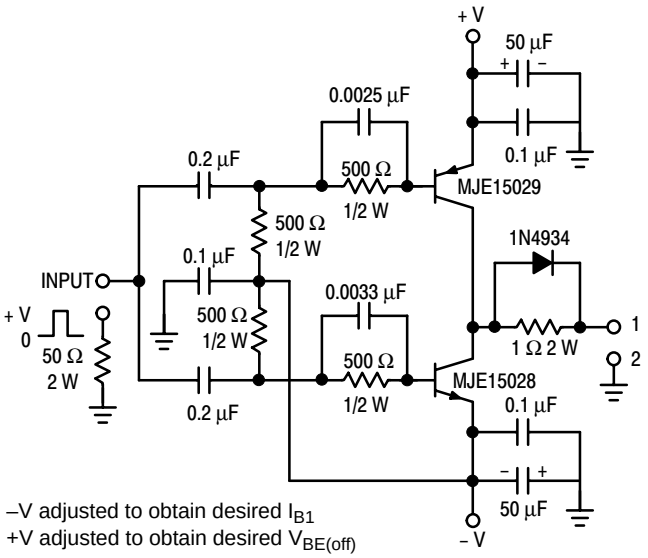
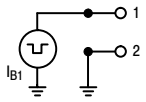
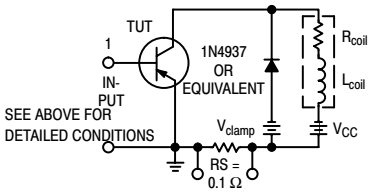
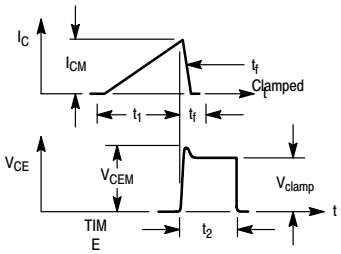
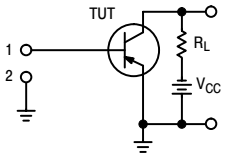


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 –V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$	**TURN–ON TIME**  I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT**  SEE ABOVE FOR DETAILED CONDITIONS **OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** 

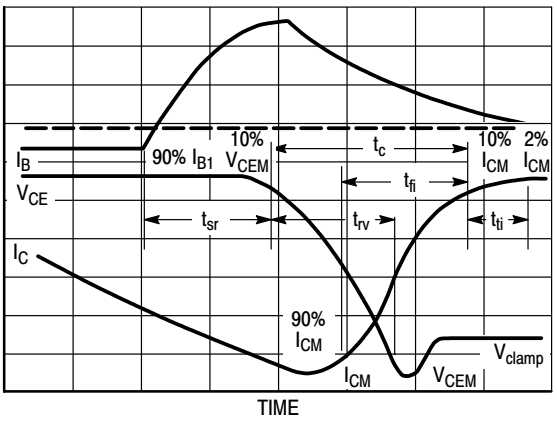


Figure 7. Inductive Switching Measurements

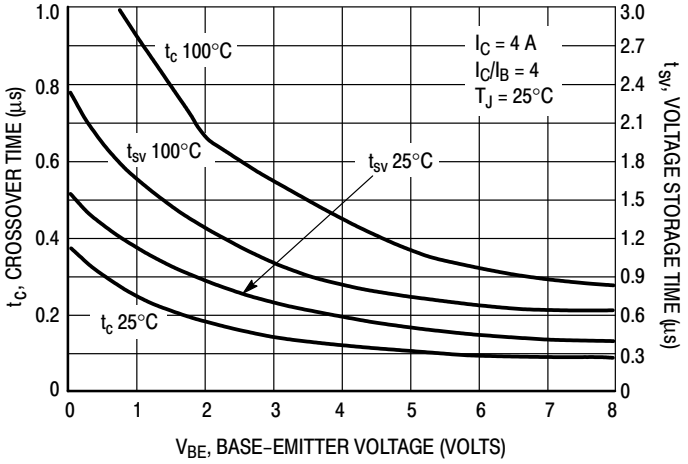


Figure 8. Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time,10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$P_{SWT} = 1/2\ V_{CC} I_C(t_c) f$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

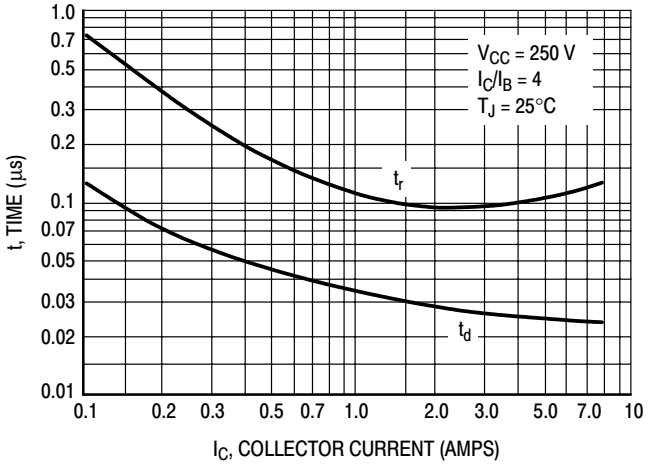


Figure 9. Turn–On Switching Times

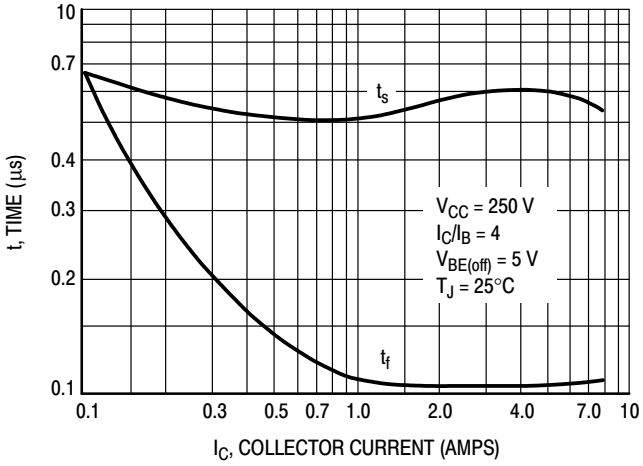


Figure 10. Turn–Off Switching Time

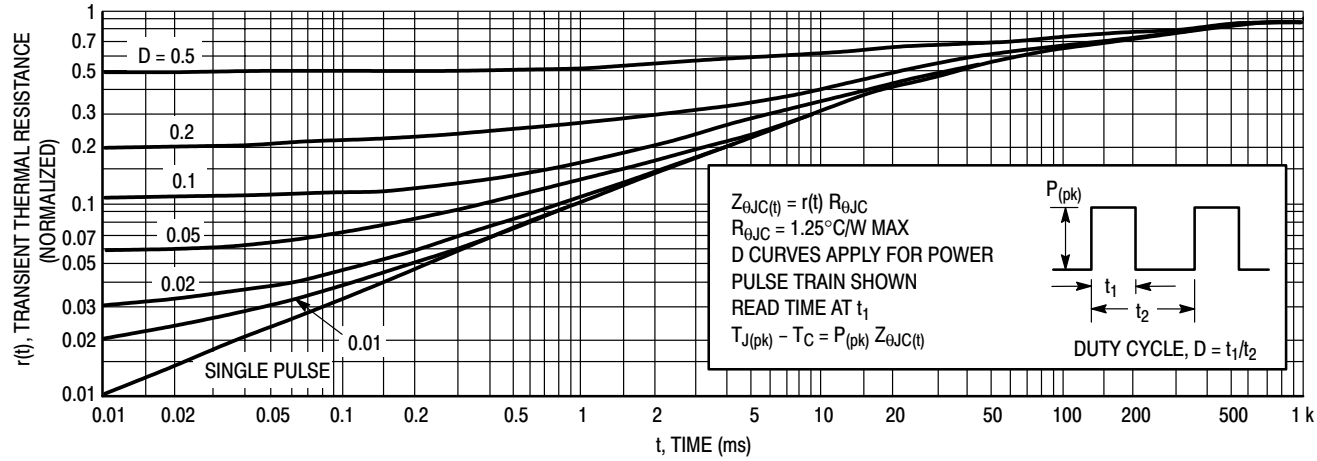


Figure 11. Typical Thermal Response [$Z_{\theta JC}(t)$]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

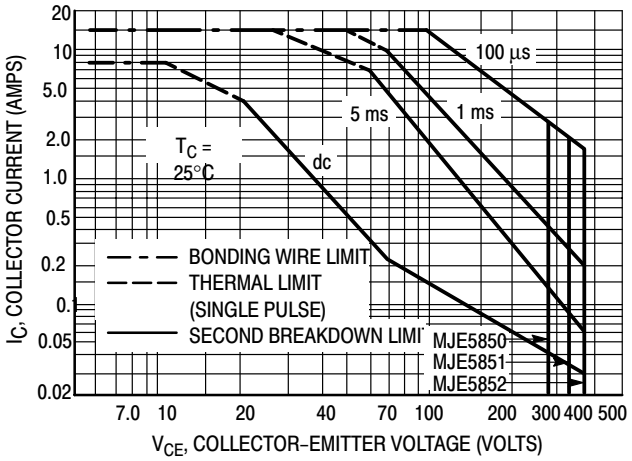


Figure 12. Maximum Forward Bias Safe Operating Area

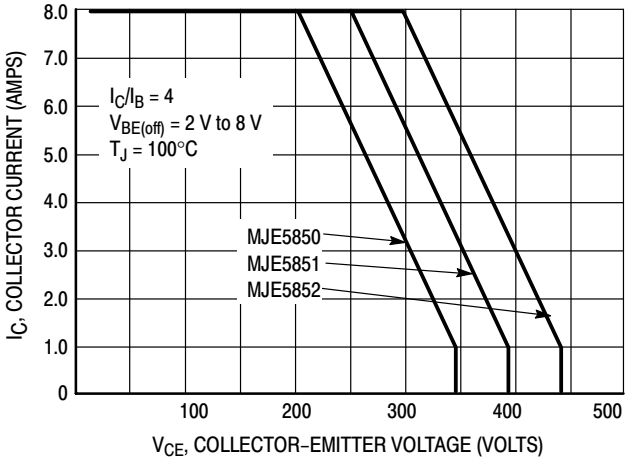


Figure 13. RBSOA, Maximum Reverse Bias Safe Operating Area

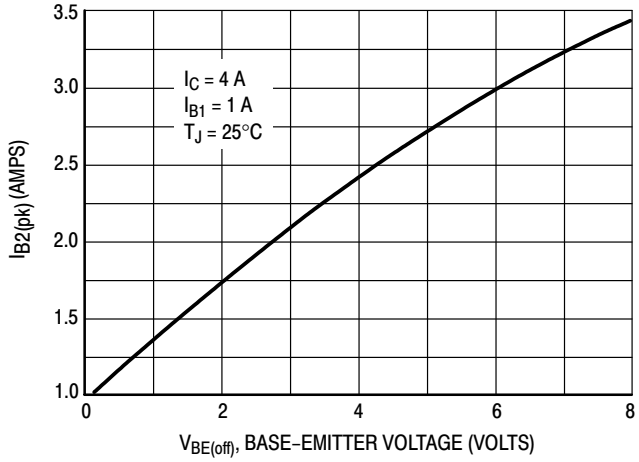


Figure 14. Peak Reverse Base Current

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

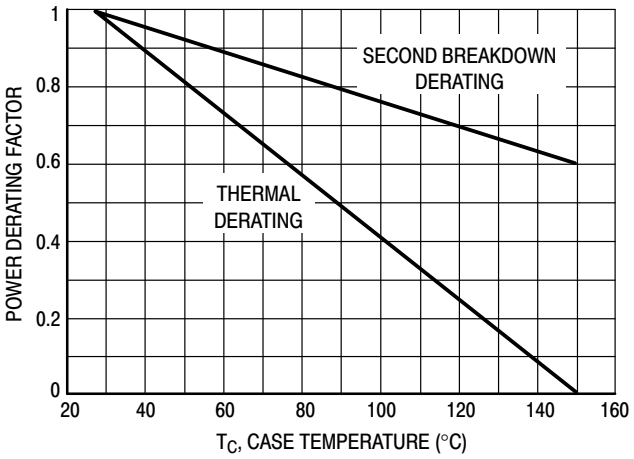


Figure 15. Forward Bias Power Derating

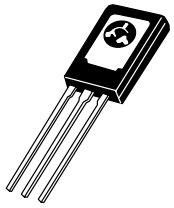
Plastic Darlington Complementary Silicon Power Transistors

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C
  = 2.0 Adc
- Monolithic Construction with Built–in Base–Emitter Resistors to Limit Leakage
  Multiplication
- Choice of Packages —
  MJE700 and MJE800 series

PNP
MJE700
MJE702
MJE703
NPN
MJE800
MJE802
MJE803

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
40 WATT
50 WATT



CASE 77–08
TO–225AA TYPE
MJE700–703
MJE800–803

MAXIMUM RATINGS

Rating	Symbol	MJE700 MJE800	MJE702 MJE703 MJE802 MJE803	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
		CASE 77		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case CASE 77 TO–220	$R_{\theta JC}$	 3.13 2.50	°C/W

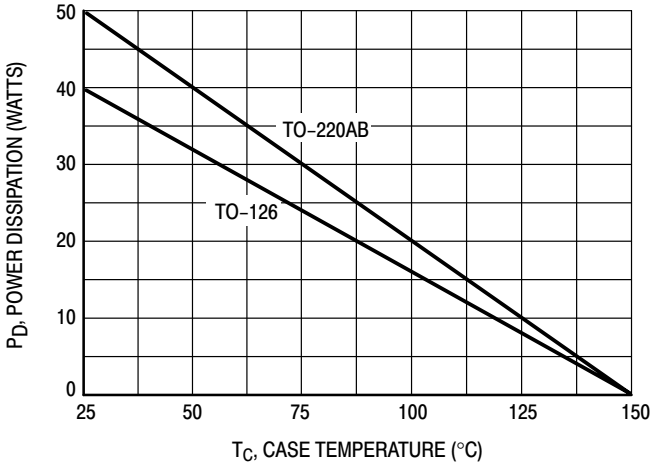


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (1)	MJE700, MJE800	$V_{(BR)CEO}$	60	—	Vdc
(I_C = 50 mAdc, I_B = 0)	MJE702, MJE703, MJE802, MJE803		80	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 60 Vdc, I_B = 0)	MJE700, MJE800		—	100	
(V_{CE} = 80 Vdc, I_B = 0)	MJE702, MJE703, MJE802, MJE803		—	100	
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0)		I_{CBO}	—	100	μAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)			—	500	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700, MJE702, MJE800, MJE802		750	—	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE703, MJE803		750	—	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		100	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 30 mAdc)	MJE700, MJE702, MJE800, MJE802		—	2.5	
(I_C = 2.0 Adc, I_B = 40 mAdc)	MJE703, MJE803		—	2.8	
(I_C = 4.0 Adc, I_B = 40 mAdc)	All devices		—	3.0	
Base–Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700, MJE702, MJE800, MJE802		—	2.5	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE703, MJE803		—	2.5	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		—	3.0	
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

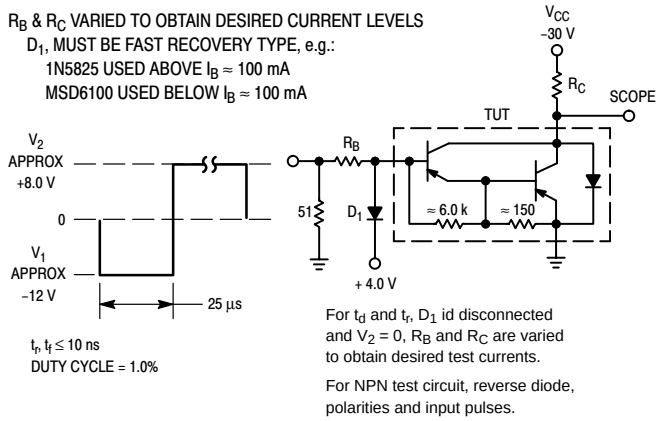


Figure 2. Switching Times Test Circuit

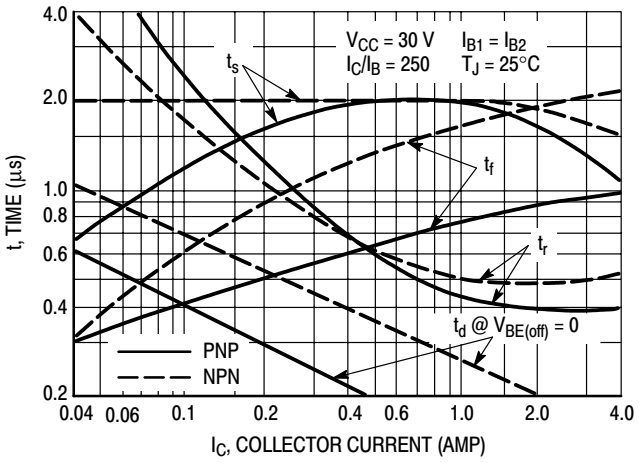


Figure 3. Switching Times

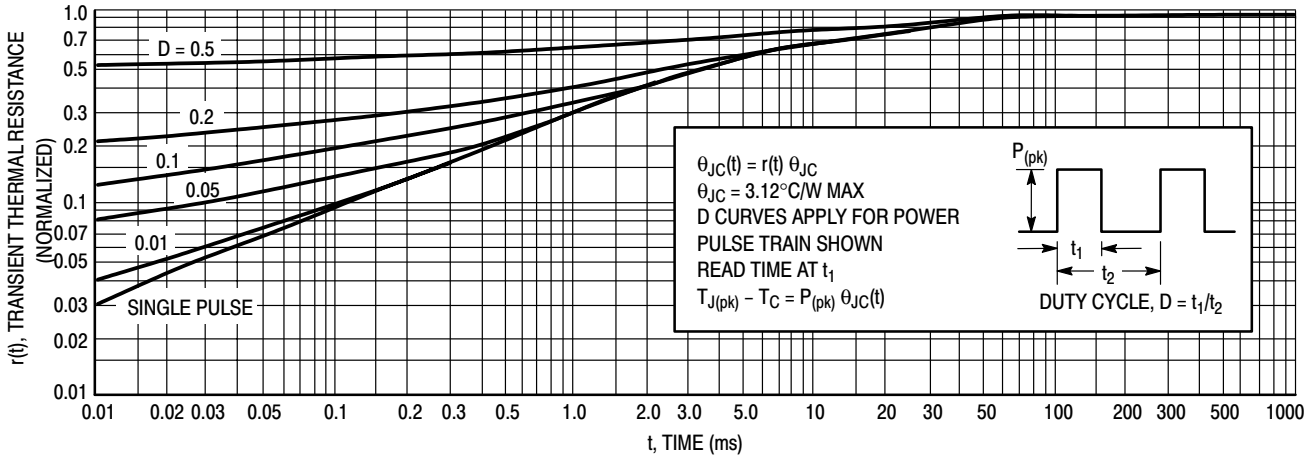


Figure 4. Thermal Response (MJE700, 800 Series)

ACTIVE−REGION SAFE−OPERATING AREA

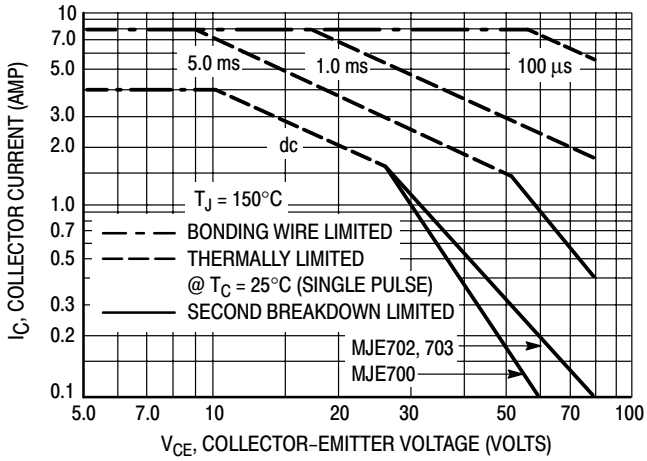


Figure 5. MJE700 Series

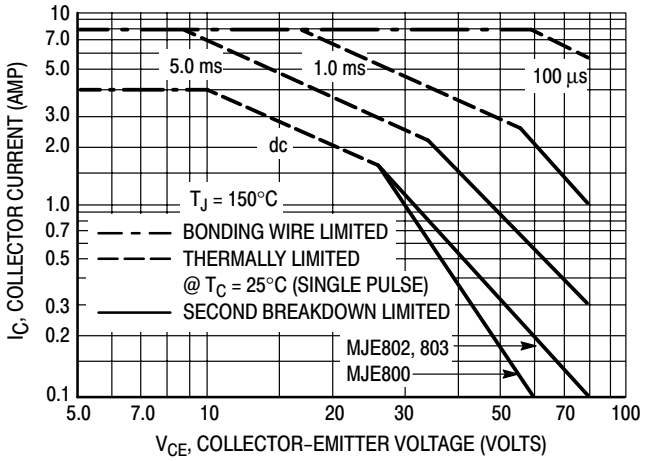
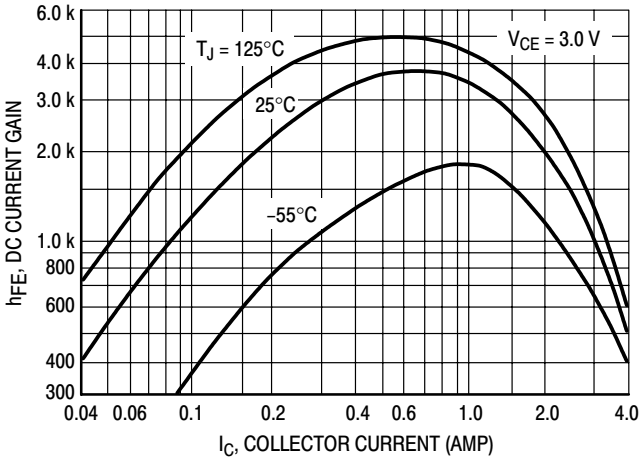


Figure 6. MJE800 Series

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 are based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PNP
MJE700 Series



NPN
MJE800 Series

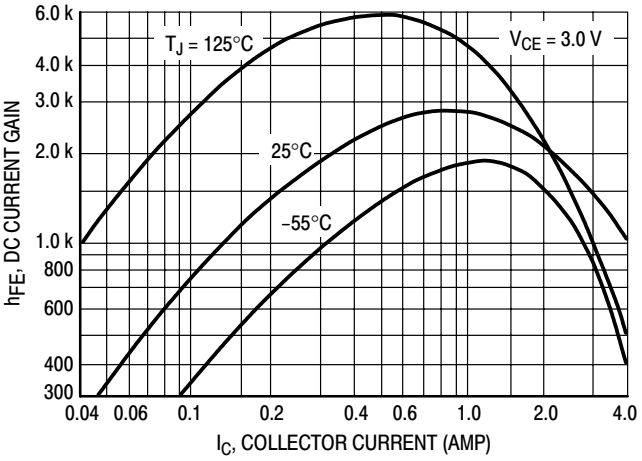
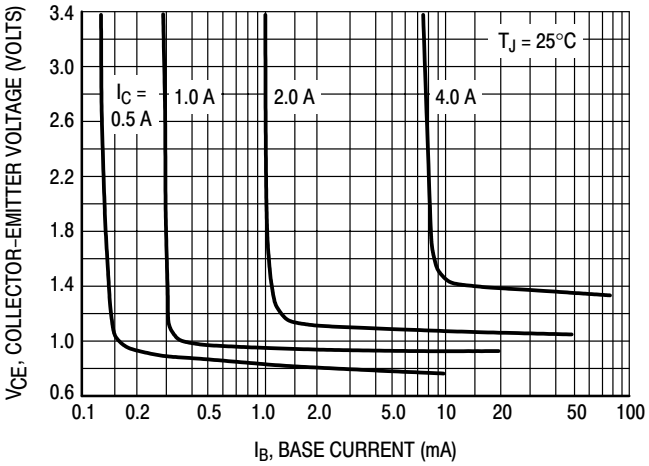


Figure 7. DC Current Gain



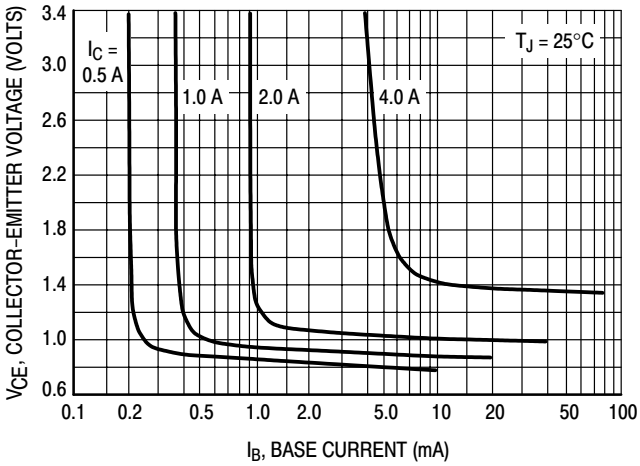
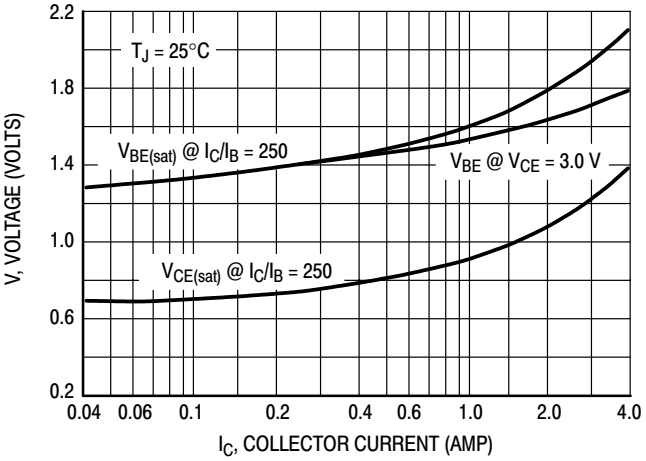


Figure 8. Collector Saturation Region



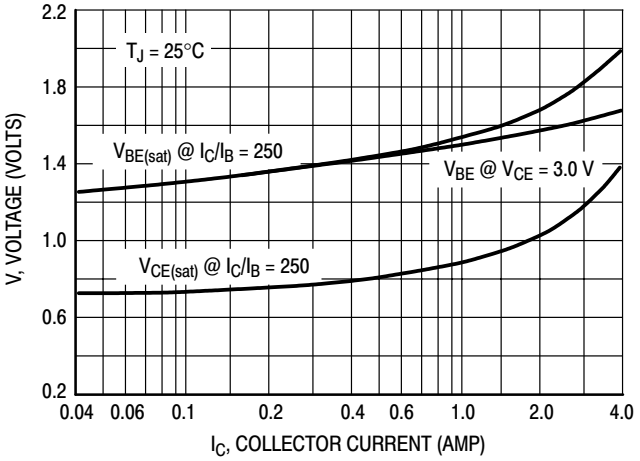


Figure 9. “On” Voltages

Complementary Power Darlingtons

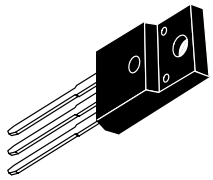
For Isolated Package Applications

NPN
MJF122
PNP
MJF127

COMPLEMENTARY SILICON POWER DARLINGTONS 5 AMPERES 100 VOLTS 30 WATTS

Designed for general–purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP122 and TIP127
- 100 $V_{CEO(sus)}$
- 5 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 2000 (Min) @ I_C = 3 Adc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (1) Test No. 1 Per Fig. 14 (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 15 T_A = 25°C) Test No. 3 Per Fig. 16	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous Peak	I_C	5 8	Adc
Base Current	I_B	0.12	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C	P_D	30 0.24	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.1	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

April, 2001 – Rev. 2
Publication Order Number:
MJF122/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)		I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 3 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 2000	— —	—
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 12 mAdc) (I_C = 5 Adc, I_B = 20 mAdc)		$V_{CE(sat)}$	— —	2 3.5	Vdc
Base–Emitter On Voltage (I_C = 3 Adc, V_{CE} = 3 Vdc)		$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)		h_{fe}	4	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJF127 MJF122	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

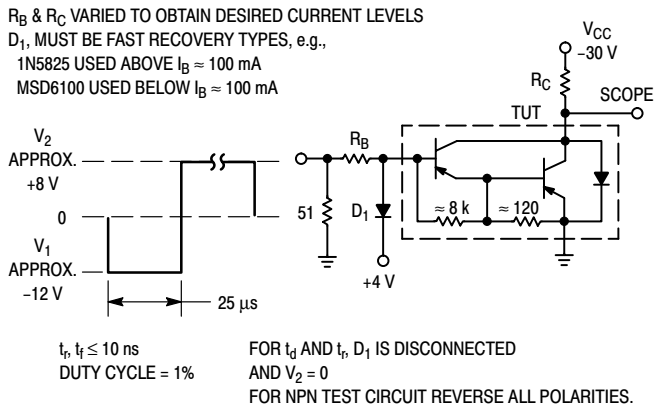


Figure 10. Switching Times Test Circuit

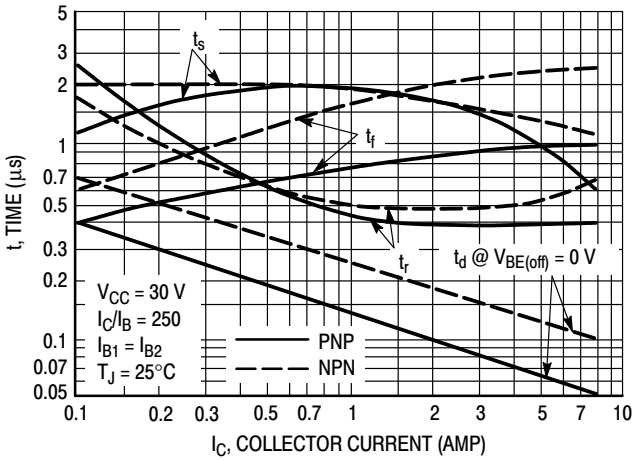


Figure 11. Typical Switching Times

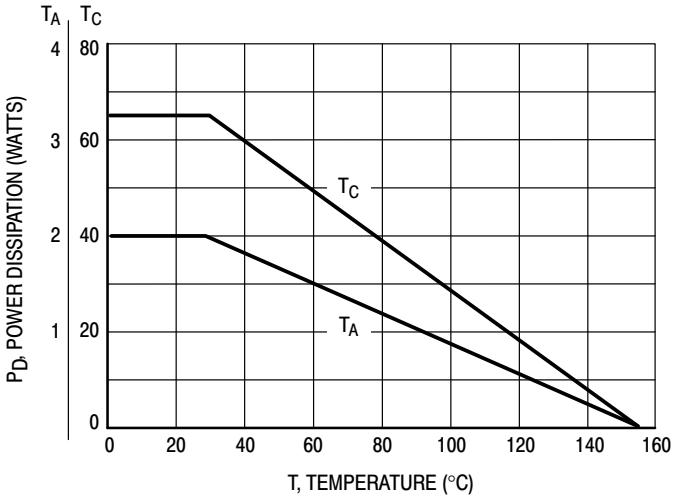


Figure 12. Maximum Power Derating

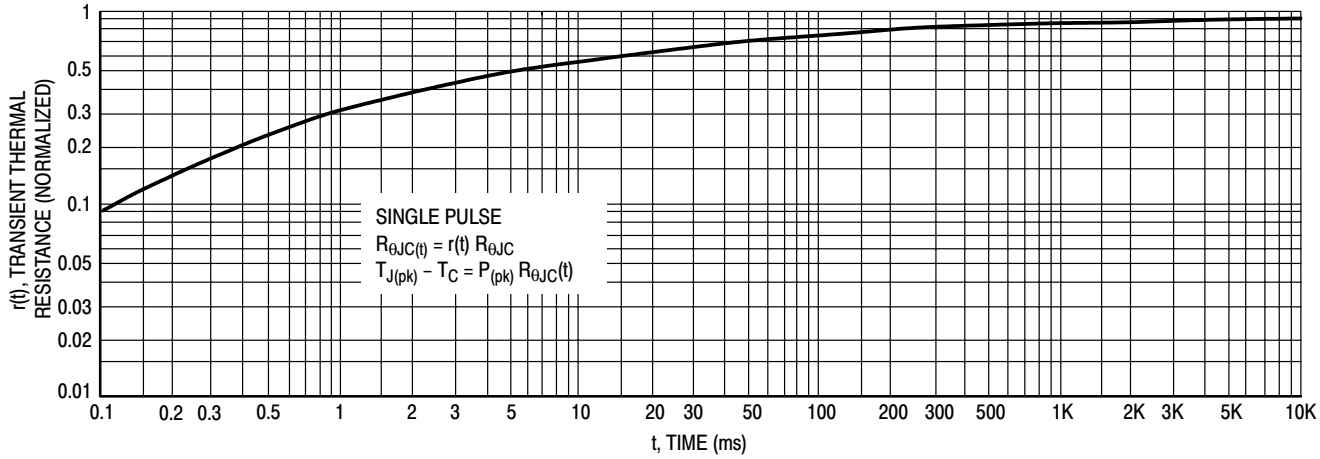


Figure 13. Thermal Response

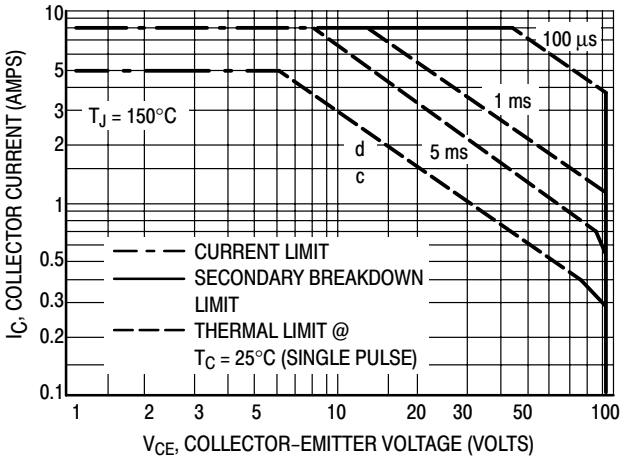


Figure 14. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

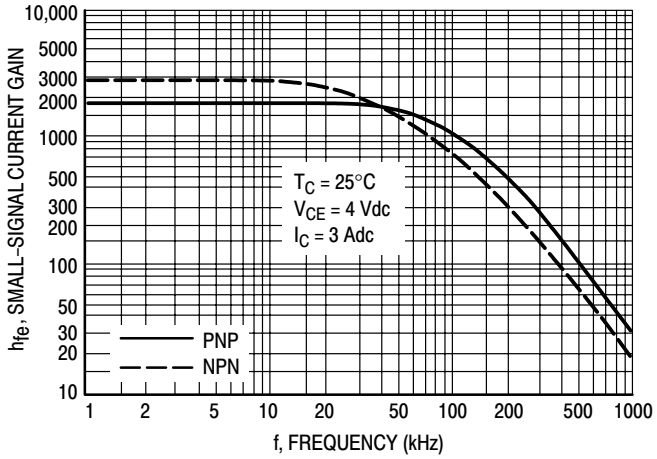


Figure 15. Typical Small−Signal Current Gain

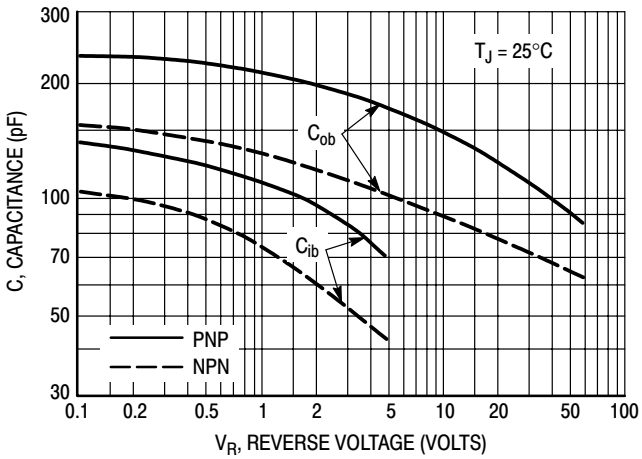
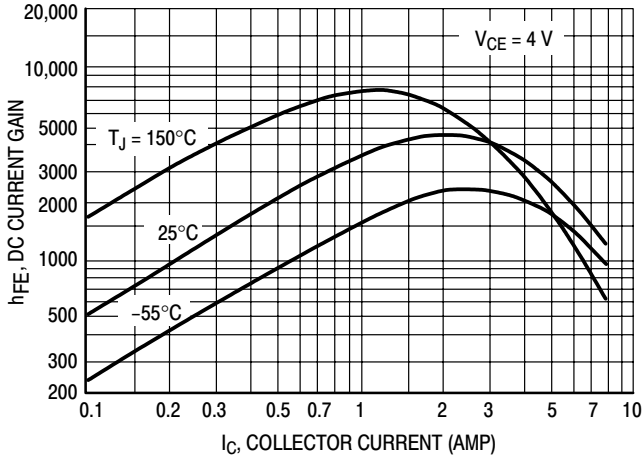


Figure 16. Typical Capacitance

NPN
MJF122



PNP
MJF127

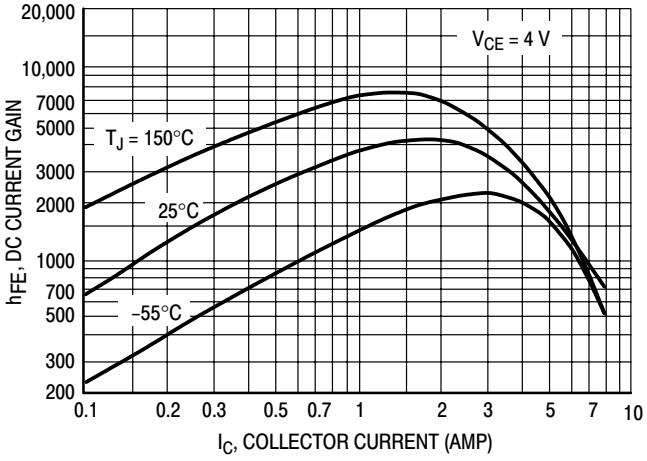
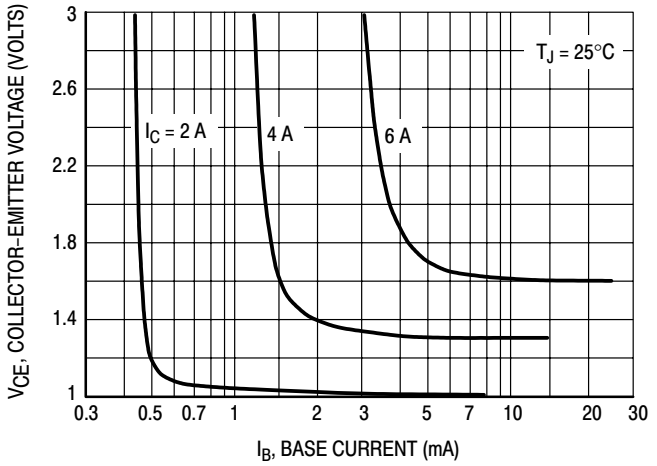


Figure 17. Typical DC Current Gain



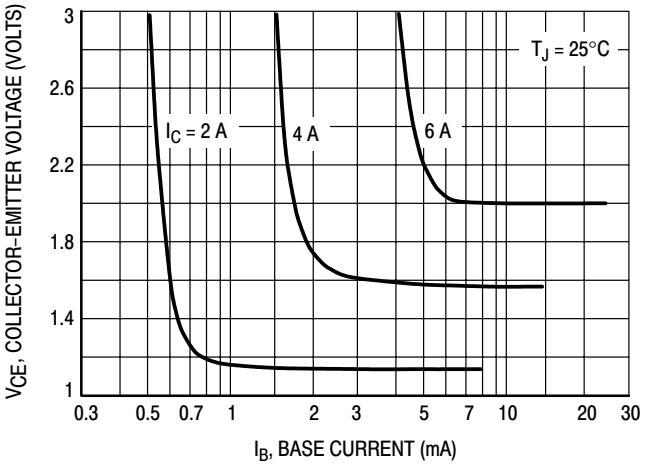
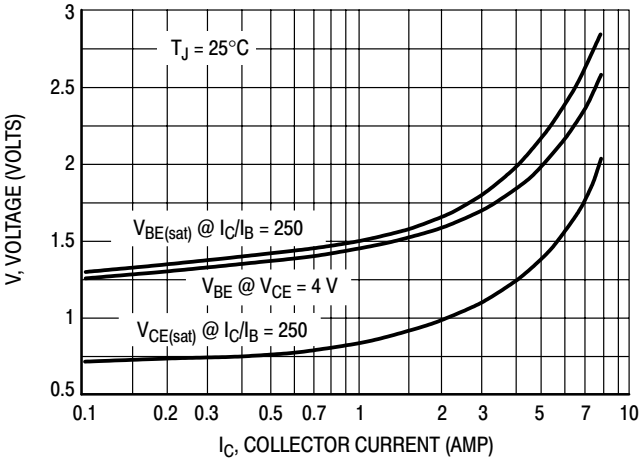


Figure 18. Typical Collector Saturation Region

NPN
MJF122



PNP
MJF127

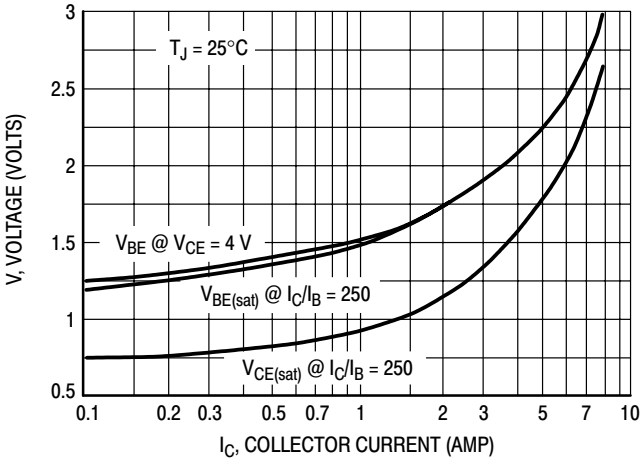
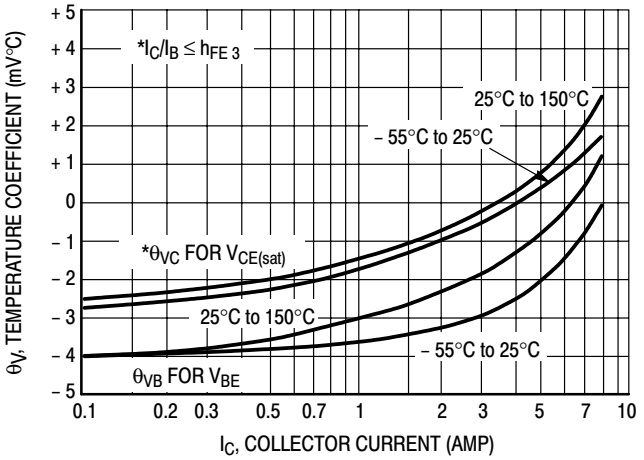


Figure 19. Typical “On” Voltages



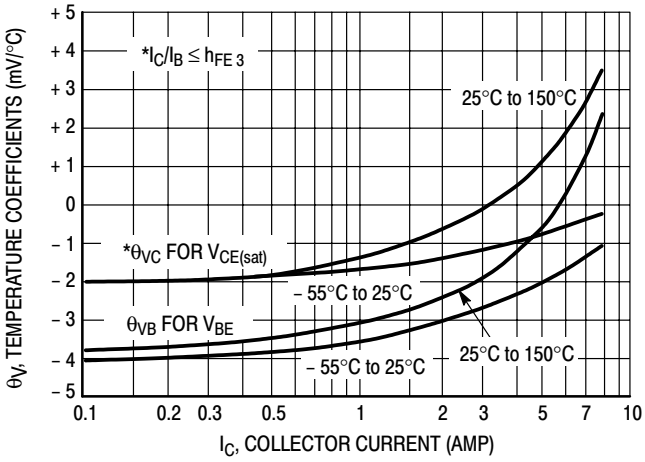
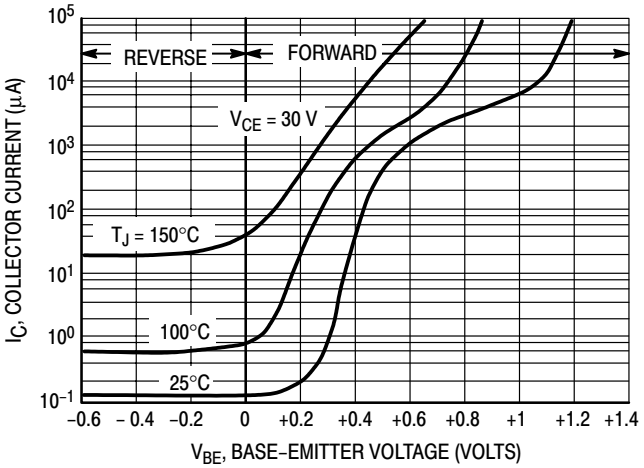


Figure 20. Typical Temperature Coefficients



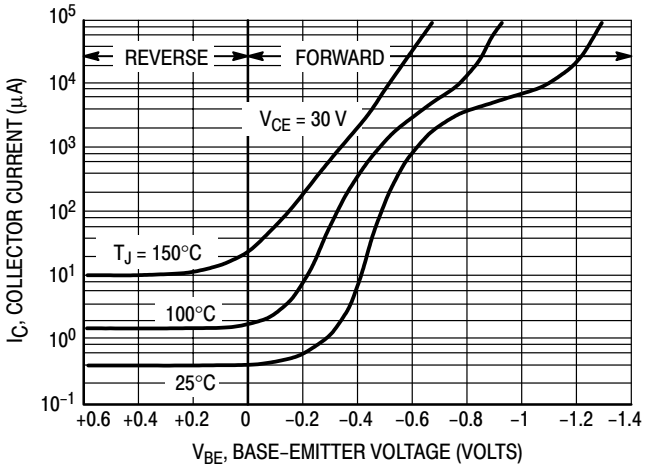
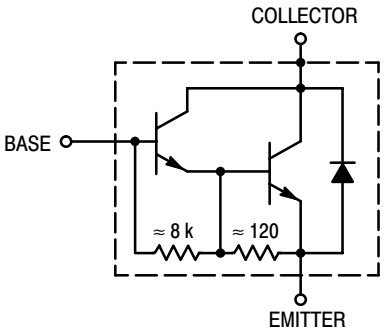


Figure 21. Typical Collector Cut–Off Region

NPN
MJF122



PNP
MJF127

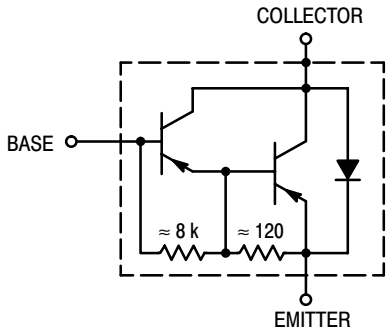


Figure 22. Darlington Schematic

TEST CONDITIONS FOR ISOLATION TESTS*

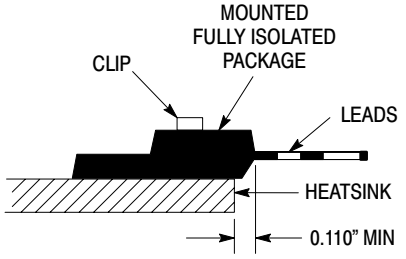


Figure 23. Clip Mounting Position for Isolation Test Number 1

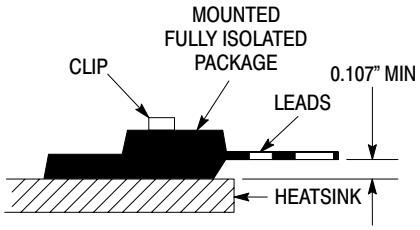


Figure 24. Clip Mounting Position for Isolation Test Number 2

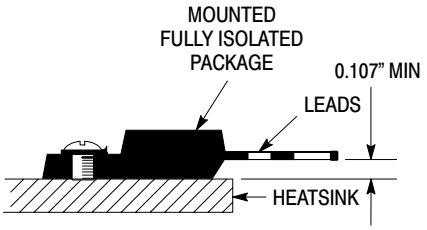


Figure 25. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

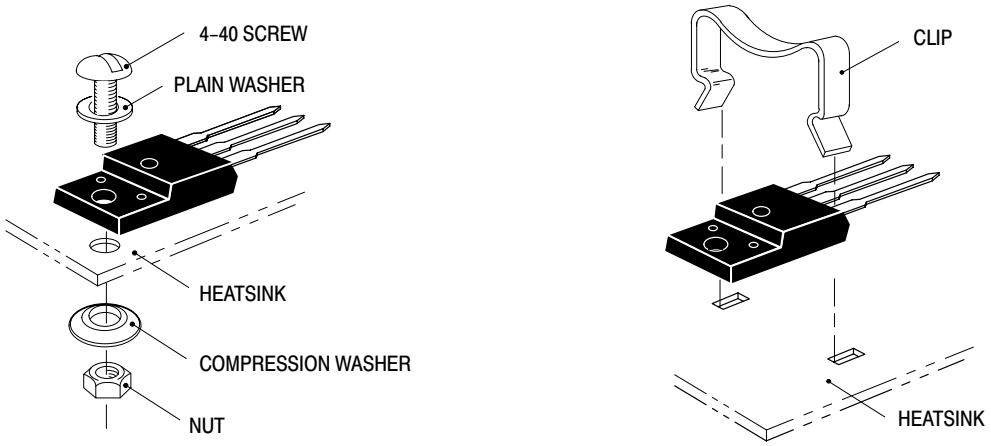


Figure 26. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

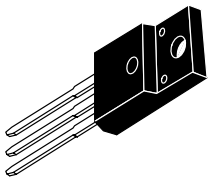
** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Transistors

For Isolated Package Applications

NPN
MJF15030
PNP
MJF15031

COMPLEMENTARY SILICON POWER TRANSISTORS
8 AMPERES
150 VOLTS
36 WATTS



CASE 221D–02
TO–220 TYPE

Designed for general–purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular MJE15030 and MJE15031
- 150 $V_{CEO(sus)}$
- 8 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain–Bandwidth Product
  f_T = 30 MHz (Min) @ I_C
  = 500 mAdc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

April, 2001 – Rev. 2
Publication Order Number:
MJF15030/D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	150	Vdc
Collector–Base Voltage	V_{CB}	150	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 11 / Test No. 2 Per Fig. 12 / Test No. 3 Per Fig. 13	V_{ISOL}	4500 / 3500 / 1500	V_{RMS}
Collector Current — Continuous / — Peak	I_C	8 / 16	Adc
Base Current	I_B	2	Adc
Total Power Dissipation* @ T_C = 25°C / Derate above 25°C	P_D	36 / 0.29	Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2 / 0.016	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2 Vdc) / (I_C = 2 Adc, V_{CE} = 2 Vdc) / (I_C = 3 Adc, V_{CE} = 2 Vdc) / (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	40 / 40 / 40 / 20	— / — / — / —	—
DC Current Gain Linearity (V_{CE} from 2 V to 20 V, I_C from 0.1 A to 3 A) (NPN to PNP)	h_{FE}	Typ: 2 / 3		
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	1	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain–Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	—	MHz

NOTES:

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

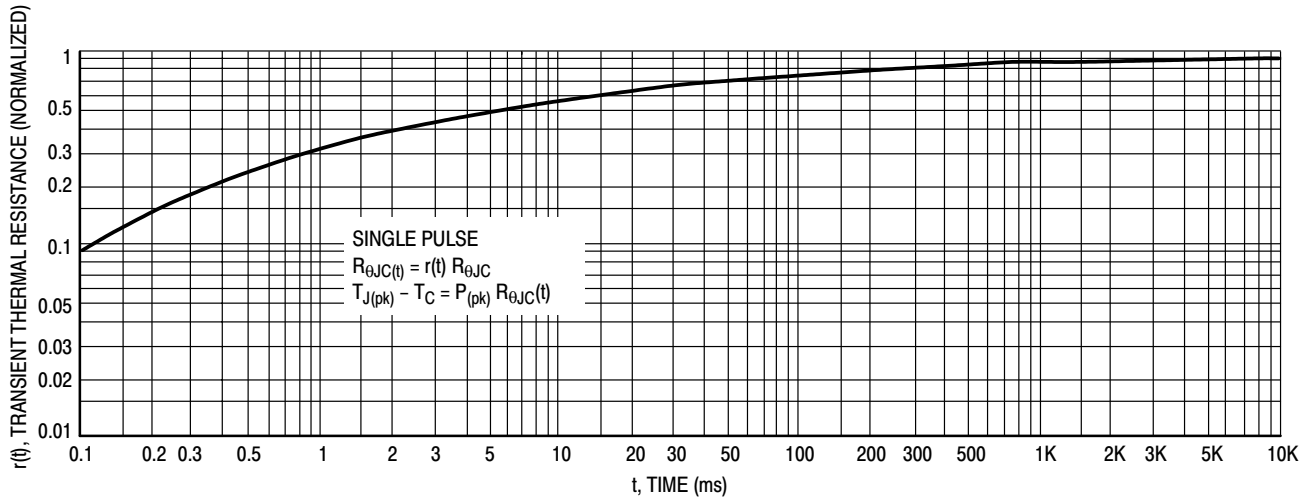


Figure 1. Thermal Response

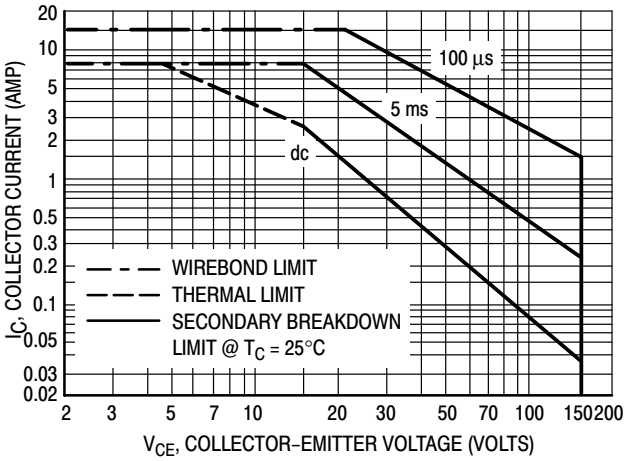


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

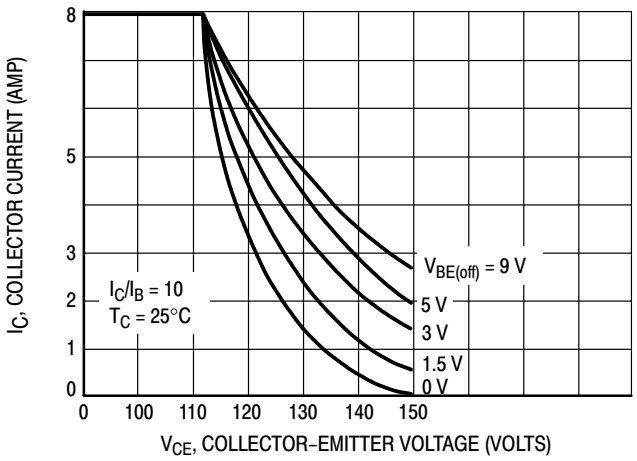


Figure 3. Reverse Bias Switching Safe Operating Area

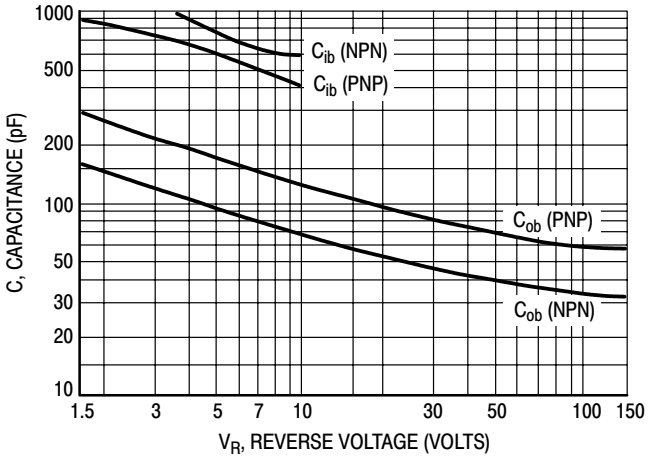


Figure 4. Capacitances

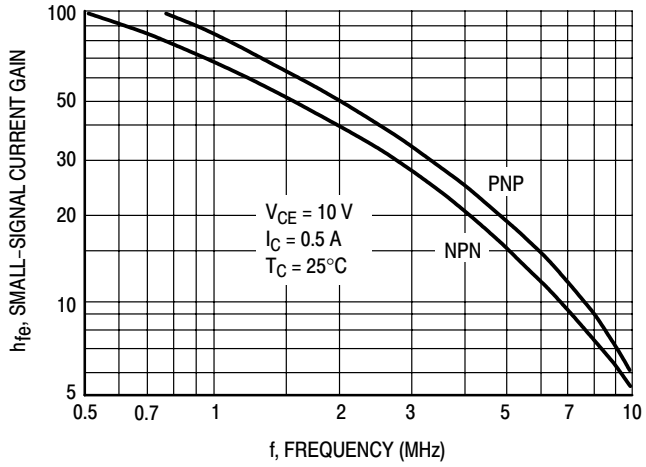


Figure 5. Small–Signal Current Gain

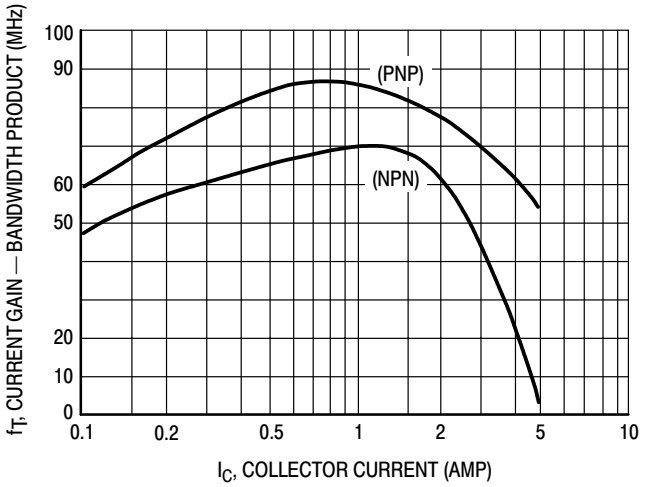


Figure 6. Current Gain — Bandwidth Product

DC CURRENT GAIN

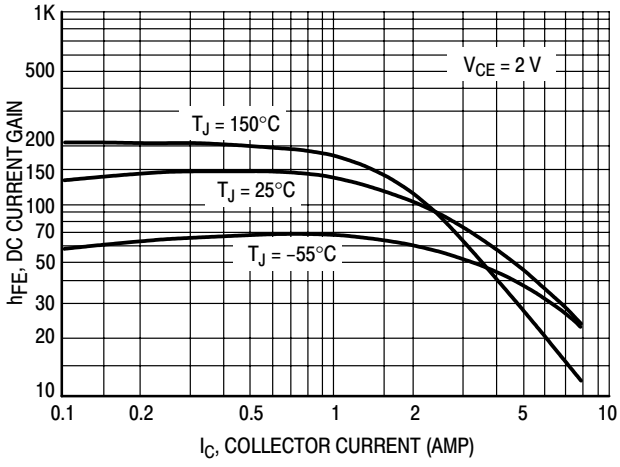


Figure 7a. MJF15030 NPN

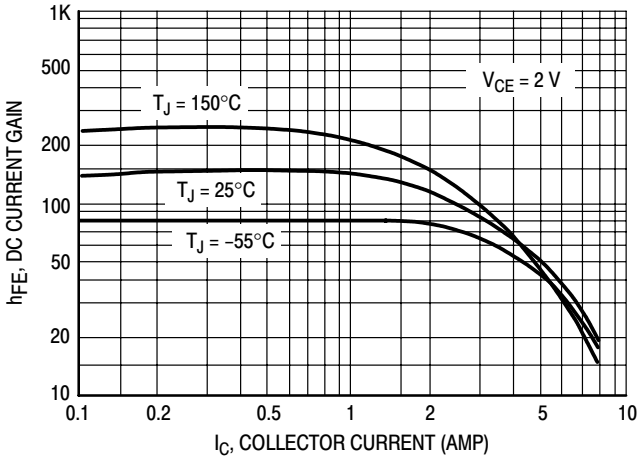


Figure 7b. MJF15031 PNP

“ON” VOLTAGE

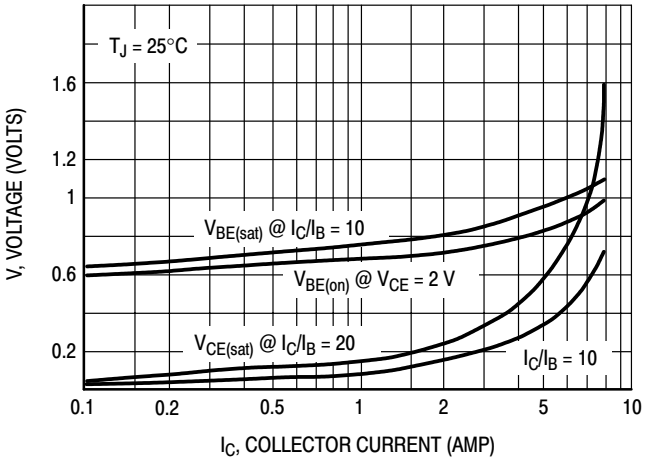


Figure 8a. MJF15030 NPN

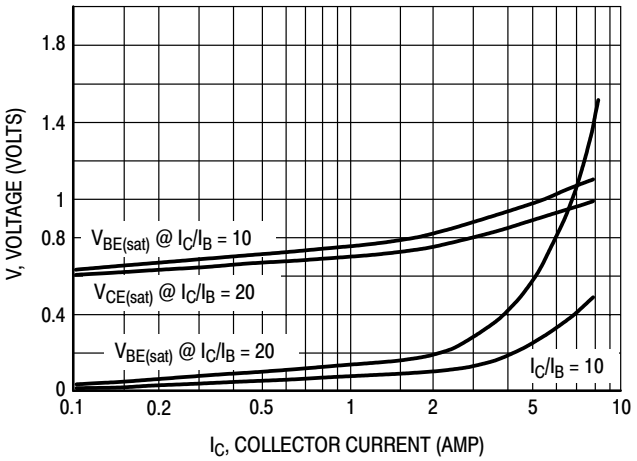


Figure 8b. MJF15031 PNP

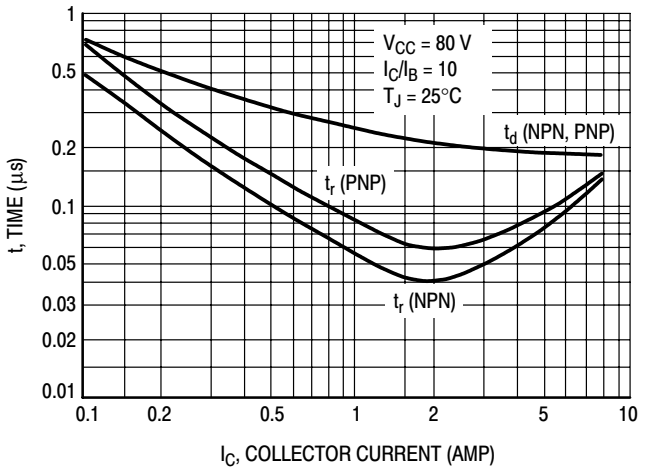


Figure 9. Turn–On Times

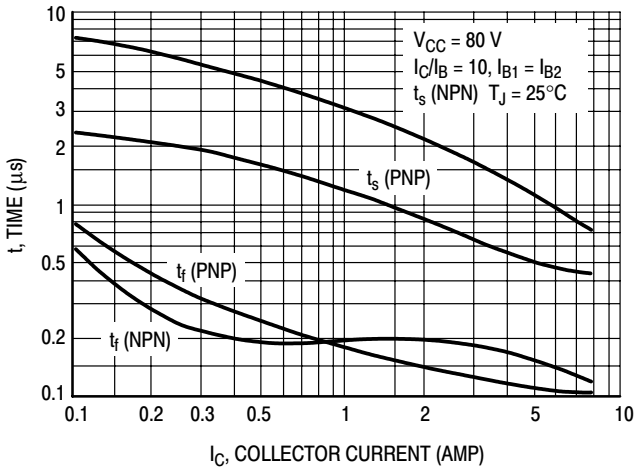


Figure 10. Turn–Off Times

TEST CONDITIONS FOR ISOLATION TESTS*

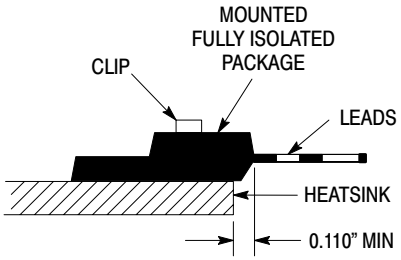


Figure 11. Clip Mounting Position for Isolation Test Number 1

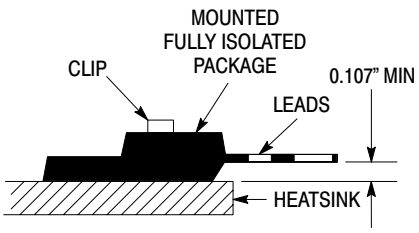


Figure 12. Clip Mounting Position for Isolation Test Number 2

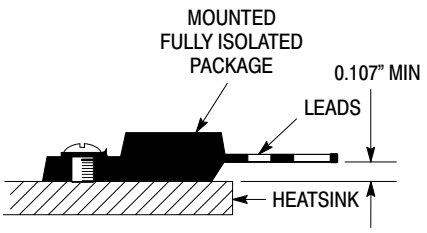


Figure 13. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

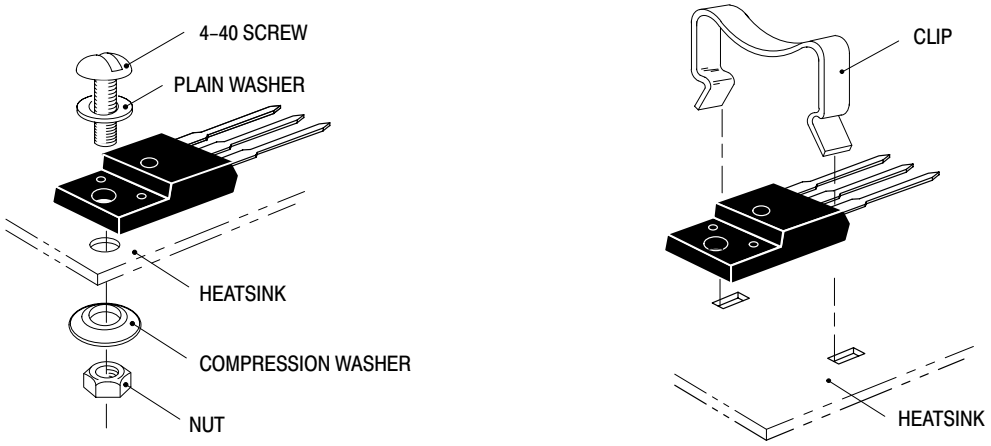


Figure 14. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

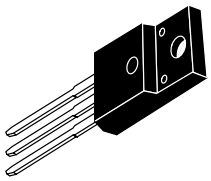
Complementary Silicon Power Transistors

. . . specifically designed for general purpose amplifier and switching applications.

- Isolated Overmold Package (1500 Volts RMS Min)
- Electrically Similar to the Popular MJE3055T and MJE2955T
- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ 90 Volts
- 10 Amperes Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

NPN
MJF3055
PNP
MJF2955

COMPLEMENTARY SILICON POWER TRANSISTORS
10 AMPERES
90 VOLTS
30 WATTS



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	90	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	90	Vdc
Base–Emitter Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	10	Adc
Base Current — Continuous	I_B	6	Adc
RMS Isolation Voltage (3) Test No. 1 Per Fig. 4 (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 5 T_A = 25°C) Test No. 3 Per Fig. 6	V_{ISOL}	4500 3500 1500	V_{RMS}
Total Power Dissipation @ T_C = 25°C (2) Derate above 25°C	P_D	30 0.25	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case (2)	$R_{\theta JC}$	4	°C/W
Thermal Resistance — Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
(3) Proper strike and creepage distance must be provided.

April, 2001 – Rev. 2
Publication Order Number:
MJF3055/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	90	—	Vdc
Collector Cutoff Current (V_{CE} = 90 Vdc, V_{BE} = 0)	I_{CES}	—	1	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, I_E = 0)	I_{CBO}	—	1	μAdc
Emitter–Base Leakage (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_{CE} = 4 Adc, V_{CE} = 4 Vdc) (I_{CE} = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	20 5	100 —	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1 2.5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{BE} = 4 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f_{test} = 500 kHz)	f_T	2	—	MHz

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

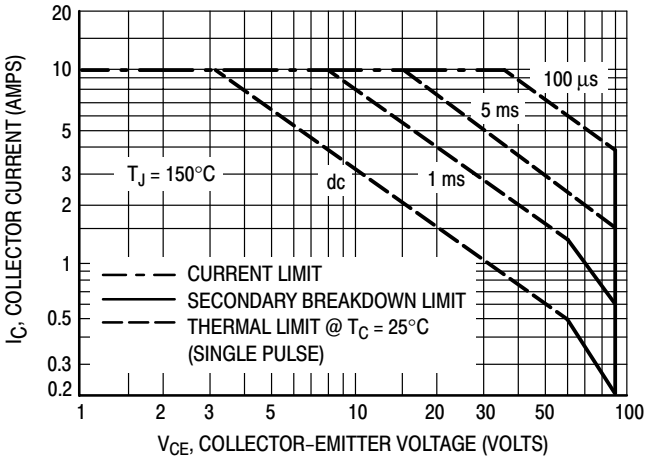


Figure 7. Maximum Forward Bias Safe Operating Area

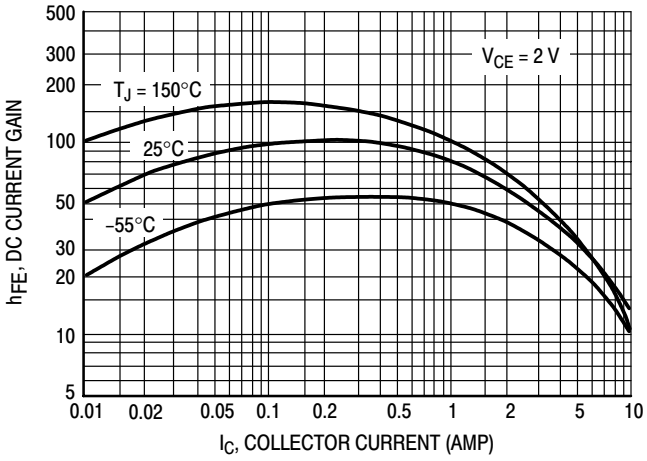


Figure 8. DC Current Gain

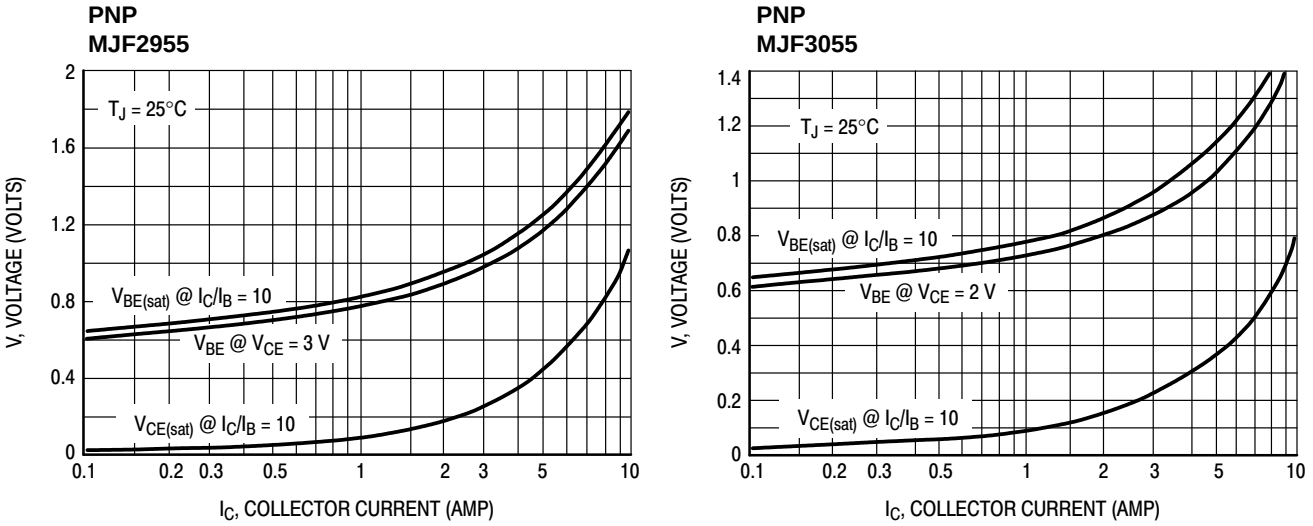


Figure 9. “On” Voltages

TEST CONDITIONS FOR ISOLATION TESTS*

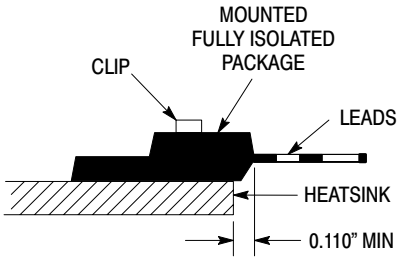


Figure 10. Clip Mounting Position for Isolation Test Number 1

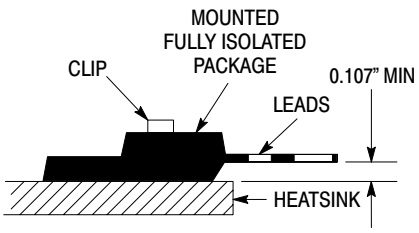


Figure 11. Clip Mounting Position for Isolation Test Number 2

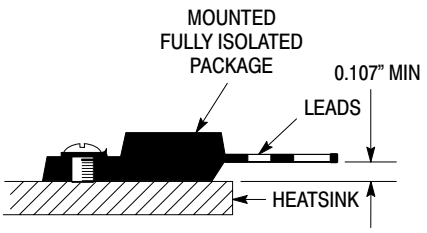


Figure 12. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

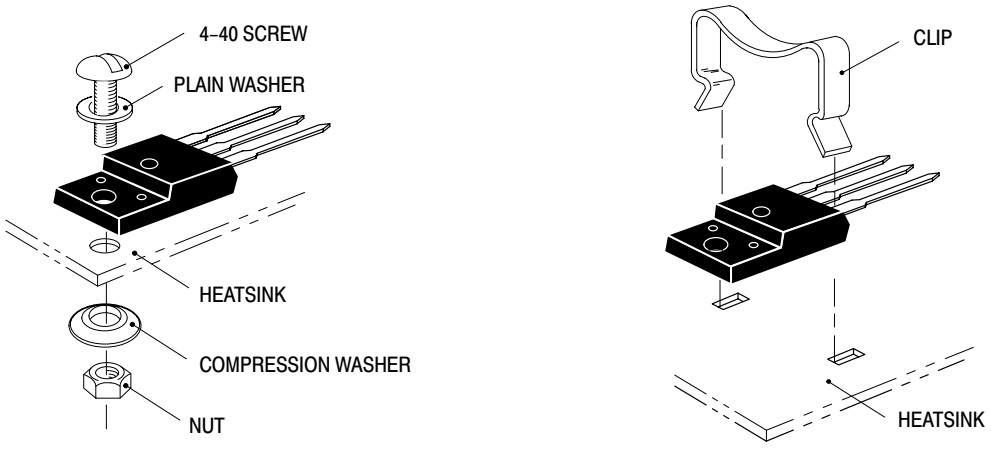


Figure 13. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJF44H11 (NPN), MJF45H11 (PNP)

Preferred Devices

Complementary Power Transistors

For Isolated Package Applications

. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current – Continuous – Peak	I_C	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 50 1.67	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

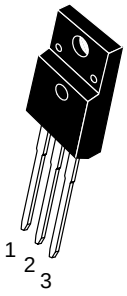
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ON Semiconductor™

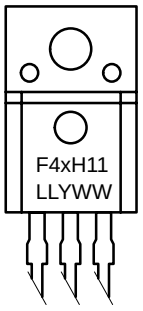
http://onsemi.com

SILICON POWER TRANSISTORS
10 AMPERES
80 VOLTS
50 WATTS



ISOLATED TO–220
CASE 221D
PLASTIC

MARKING DIAGRAM



F4xH11 = Specific Device Code
x = 4 or 5
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF44H11	TO–220	50 Units/Rail
MJF45H11	TO–220	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	–	–	1.0	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	–	–	10	μA
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	–	–	1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	–	–	–
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	–	–	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJF44H11 MJF45H11	C_{cb}	– –	130 230	– –	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJF44H11 MJF45H11	f_T	– –	50 40	– –	MHz
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJF44H11 MJF45H11	$t_d + t_r$	– –	300 135	– –	ns
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJF44H11 MJF45H11	t_s	– –	500 500	– –	ns
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJF44H11 MJF45H11	t_f	– –	140 100	– –	ns

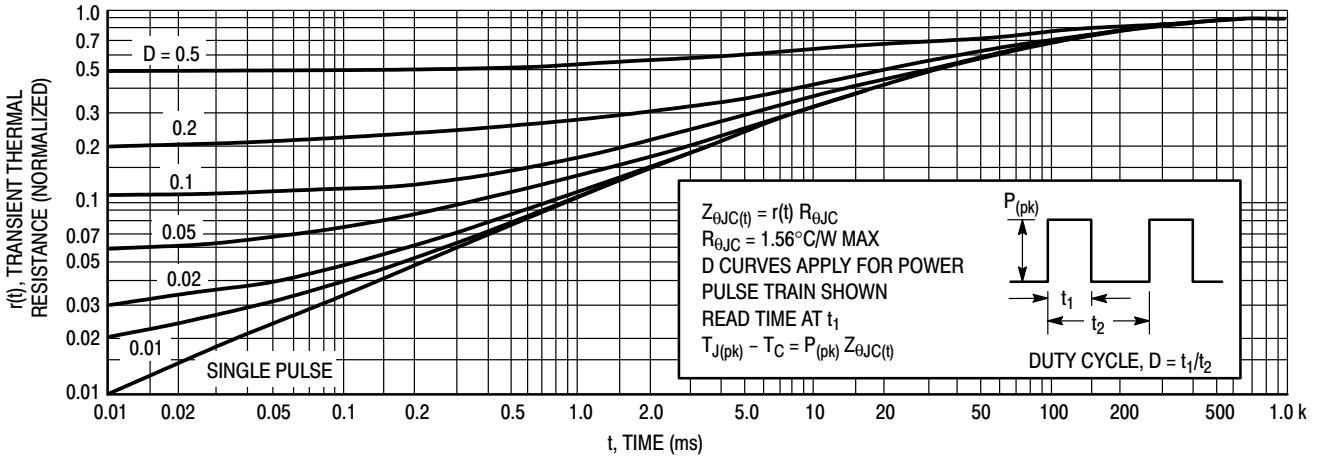


Figure 1. Thermal Response

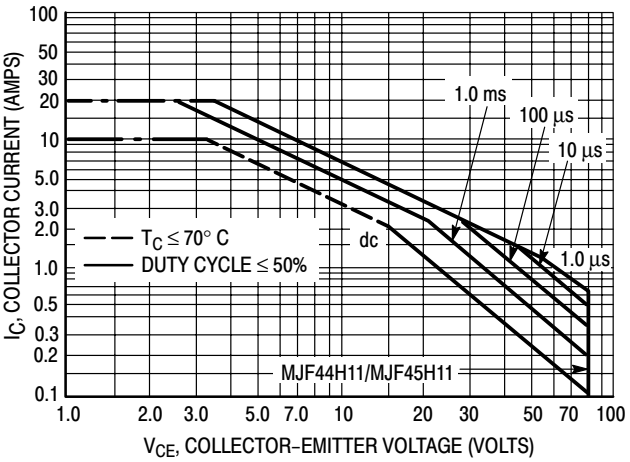


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

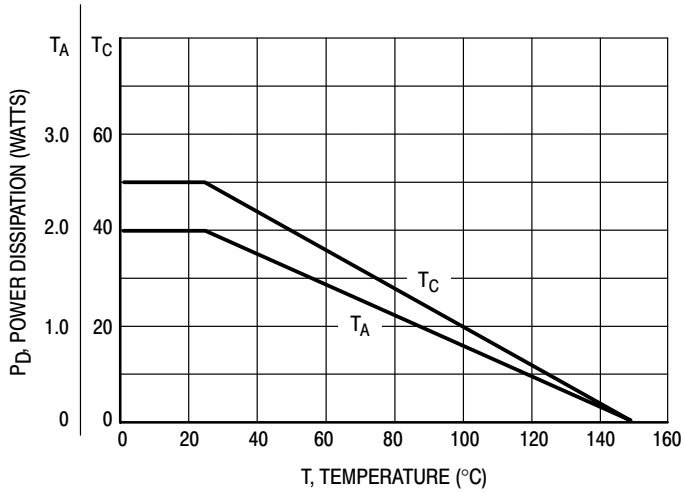


Figure 3. Power Derating

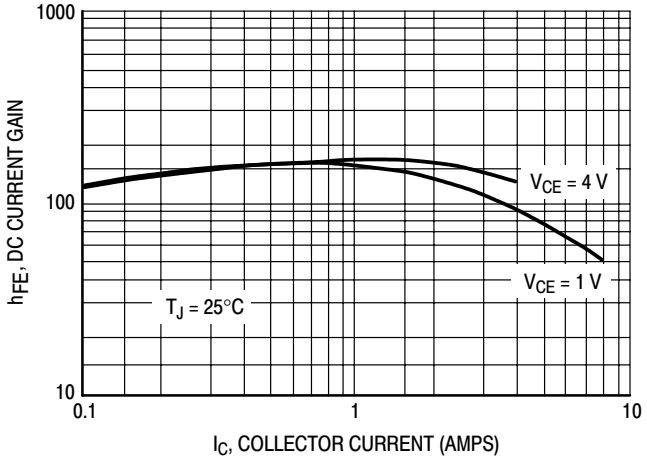


Figure 4. MJF44H11 DC Current Gain

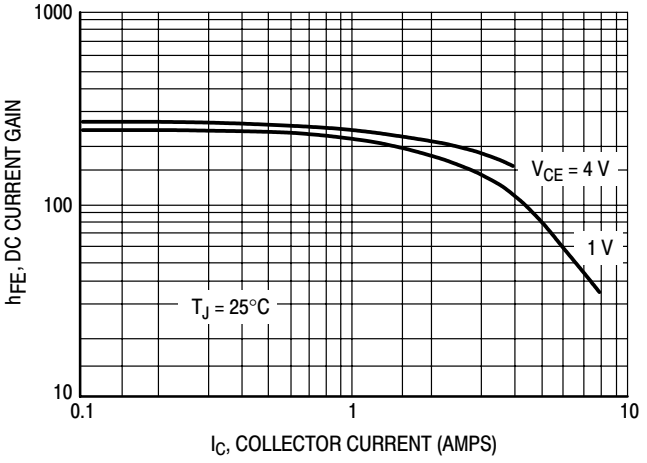


Figure 5. MJF45H11 DC Current Gain

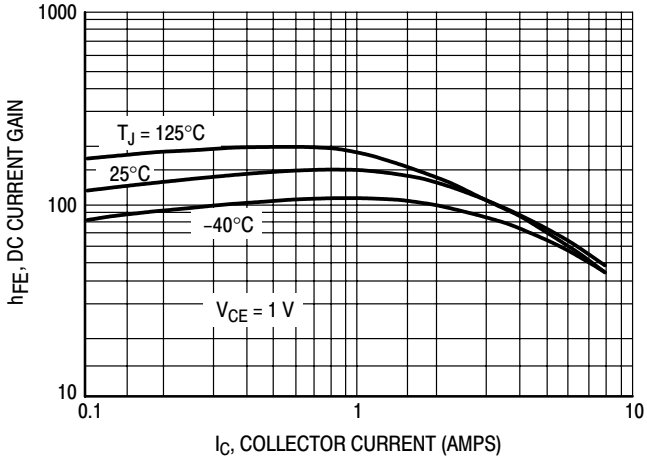


Figure 6. MJF44H11 Current Gain versus Temperature

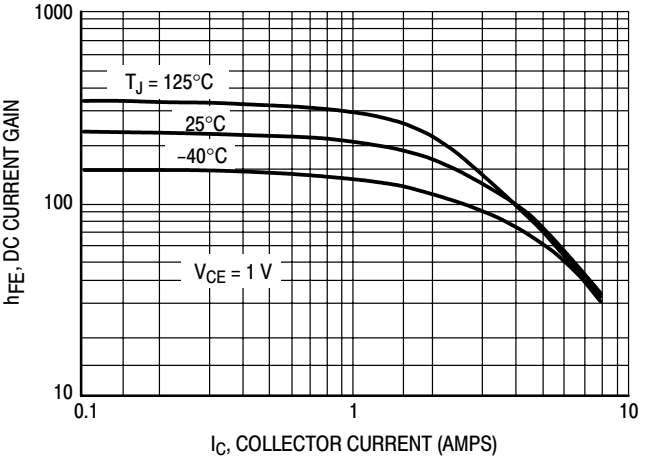


Figure 7. MJF45H11 Current Gain versus Temperature

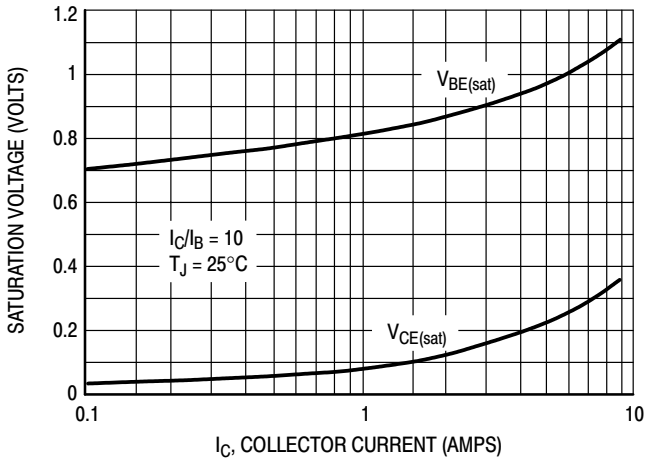


Figure 8. MJF44H11 On–Voltages

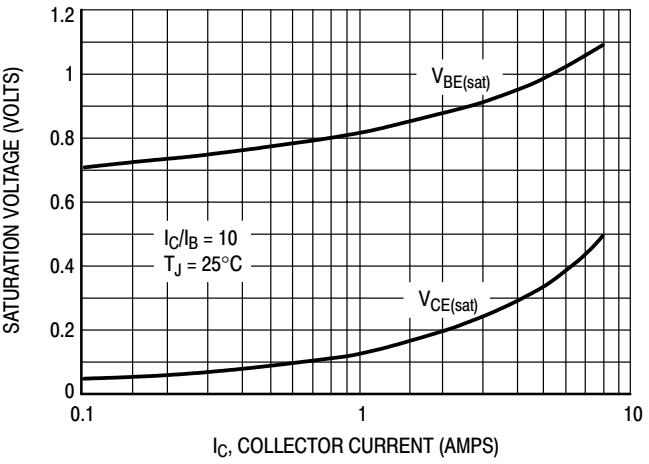


Figure 9. MJF45H11 On–Voltages

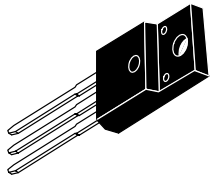
MJF47

High Voltage Power Transistor
Isolated Package Applications

Designed for line operated audio output amplifiers, switching power supply drivers and other switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP47
- 250 $V_{CEO(sus)}$
- 1 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

NPN SILICON
POWER TRANSISTOR
1 AMPERE
250 VOLTS
28 WATTS



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CB}	350	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 10 / Test No. 2 Per Fig. 11 / Test No. 3 Per Fig. 12	V_{ISOL}	4500 / 3500 / 1500	V_{RMS}
Collector Current — Continuous / Peak	I_C	1 / 2	Adc
Base Current	I_B	0.6	Adc
Total Power Dissipation* @ T_C = 25°C / Derate above 25°C	P_D	28 / 0.23	Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2 / 0.016	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.4	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

April, 2001 – Rev. 2
Publication Order Number:
MJF47/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	0.2	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	I_{CES}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	1	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)	h_{FE}	30 10	150 —	—
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} 10 Vdc, f = 2 MHz)	f_T	10	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

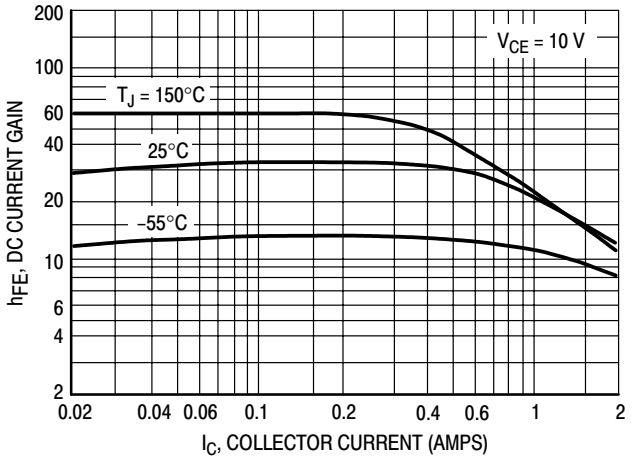


Figure 1. DC Current Gain

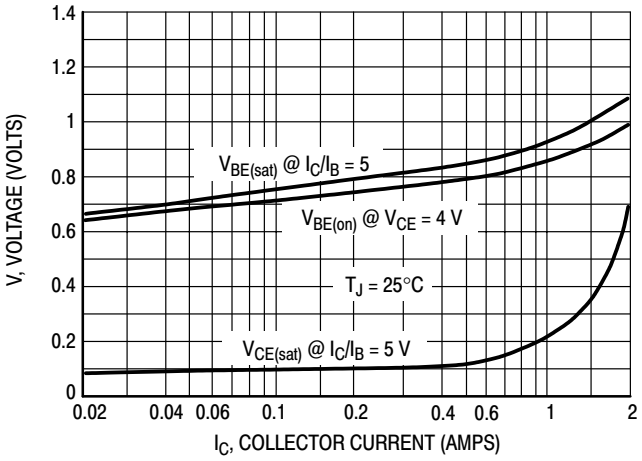


Figure 2. “On” Voltages

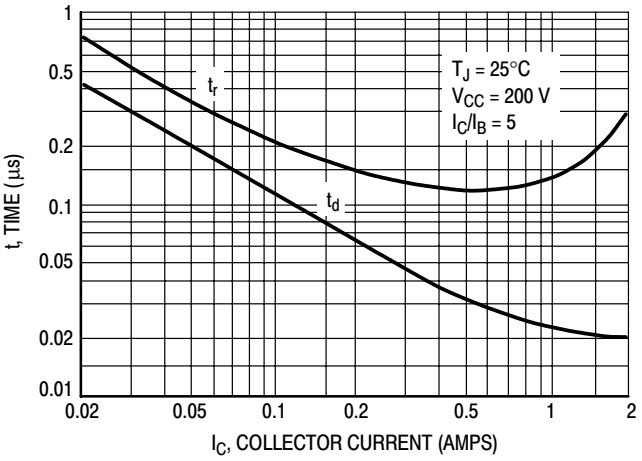


Figure 3. Turn–On Time

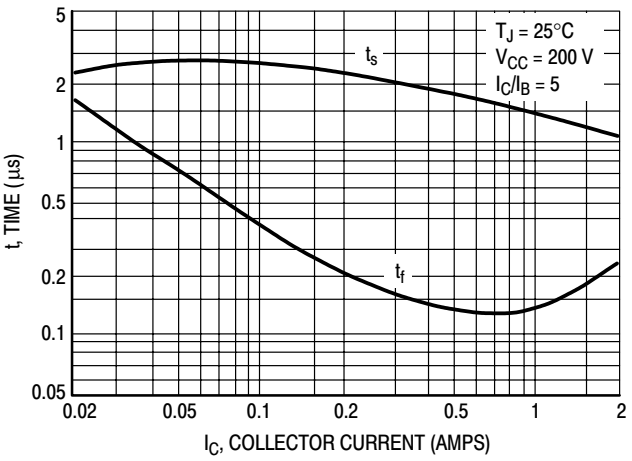


Figure 4. Turn–Off Time

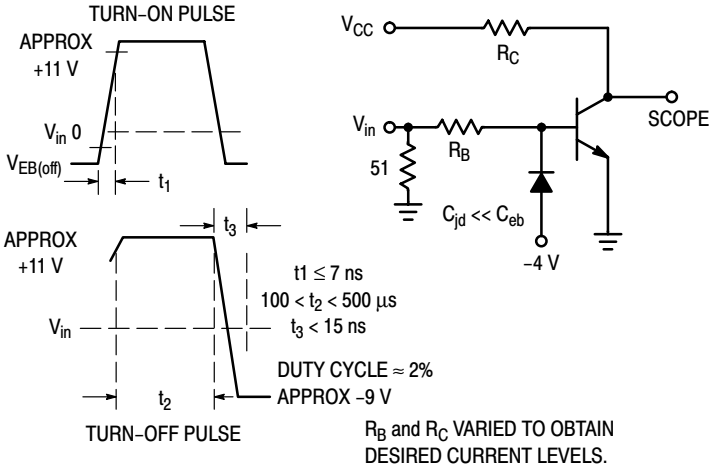


Figure 5. Switching Time Equivalent Circuit

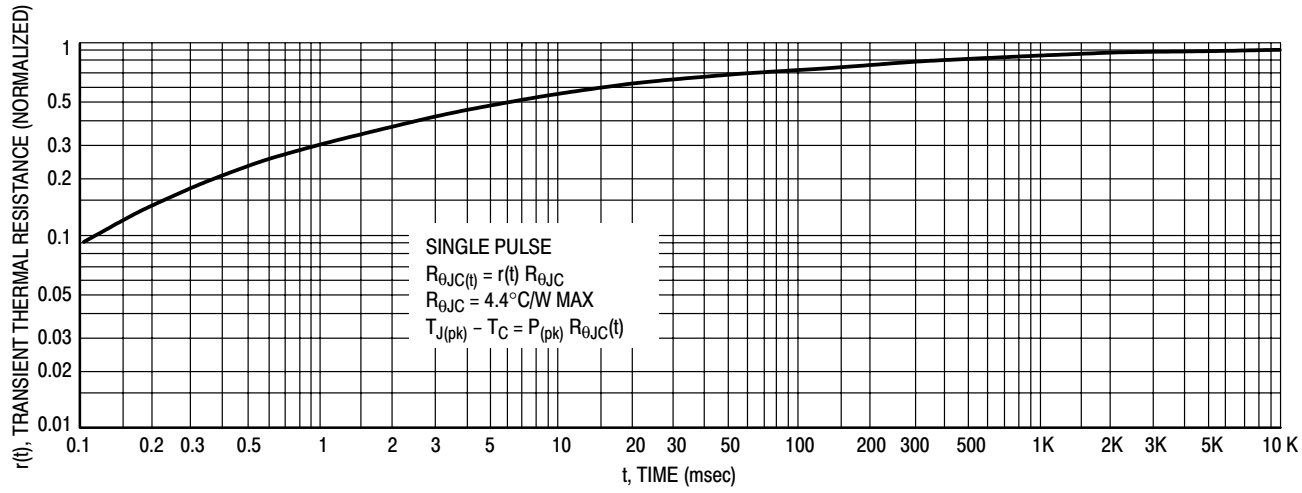


Figure 6. Thermal Response

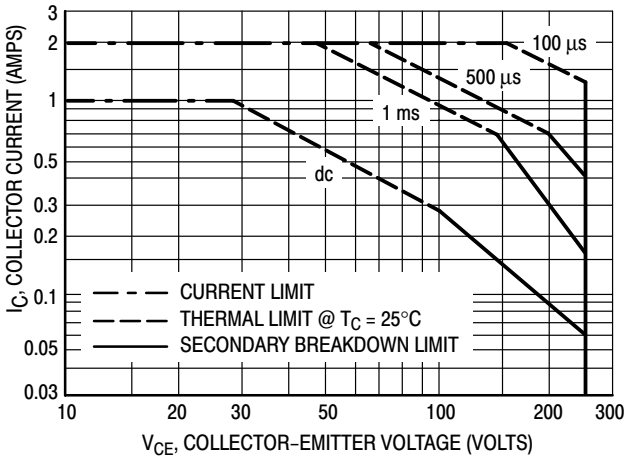


Figure 7. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

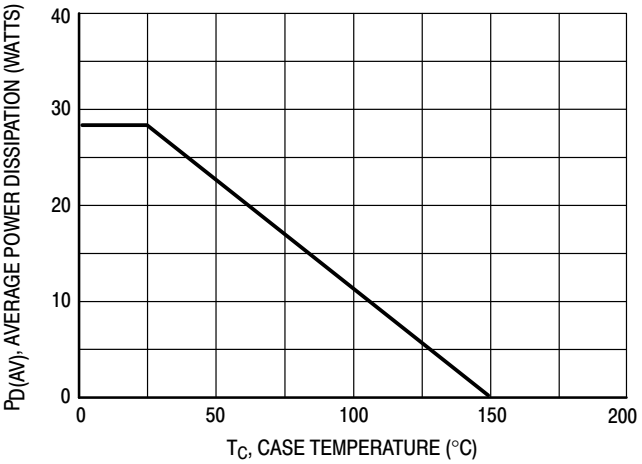


Figure 8. Power Derating

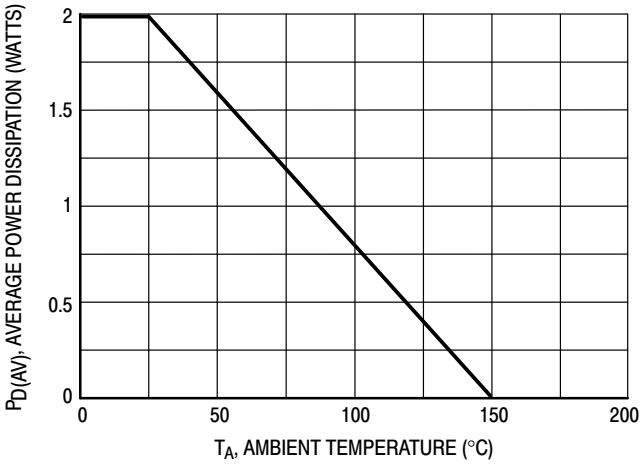


Figure 9. Power Derating

TEST CONDITIONS FOR ISOLATION TESTS*

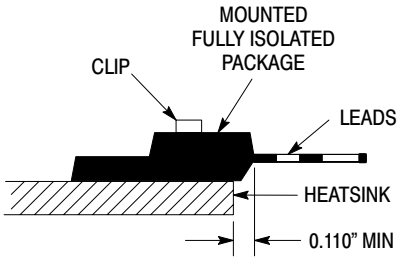


Figure 10. Clip Mounting Position for Isolation Test Number 1

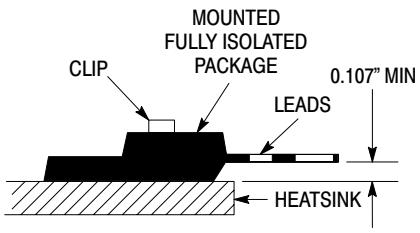


Figure 11. Clip Mounting Position for Isolation Test Number 2

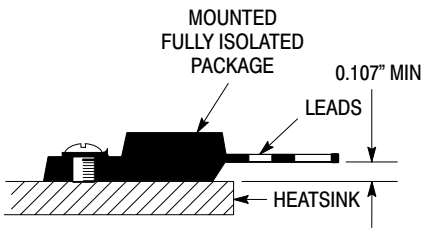


Figure 12. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

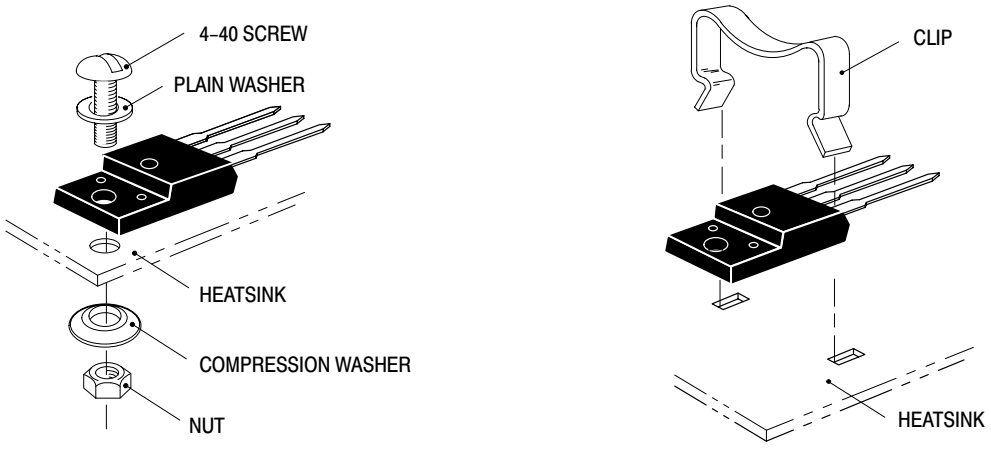


Figure 13. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Darlingtons

For Isolated Package Applications

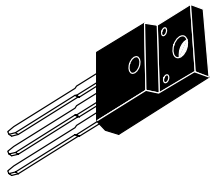
NPN
MJF6388*
PNP
MJF6668*

*ON Semiconductor Preferred Devices

COMPLEMENTARY SILICON POWER DARLINGTONS 10 AMPERES 100 VOLTS 40 WATTS

Designed for general–purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Isolated Overmold Package, TO–220 Type
- Electrically Similar to the Popular 2N6388, 2N6668, TIP102 and TIP107
- 100 $V_{CEO(sus)}$
- 10 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 1000 (Min) @ I_C = 5.0 Adc
- High Isolation Voltage (up to 4500 VRMS)
- Case 221D is UL Recognized at 3500 VRMS: File #E69369



CASE 221D–02
UL RECOGNIZED

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	100	Vdc
Collector–Base Voltage		V_{CB}	100	Vdc
Emitter–Base Voltage		V_{EB}	5.0	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Figure 14 Test No. 2 Per Figure 15 Test No. 3 Per Figure 16	V_{ISOL}	4500 3500 1500	V
Collector Current — Continuous — Peak(2)		I_C	10 15	Adc
Base Current		I_B	1.0	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	40 0.31	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

(1) Proper strike and creepage distance must be provided.
(2) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied and a mounting torque of 6 to 8 in•lbs.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

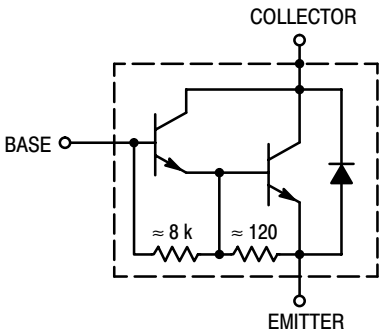
April, 2001 – Rev. 5
Publication Order Number:
MJF6388/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	— —	10 3.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	3000 1000 200 100	15000 — — —	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc) (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 8.0 Adc, I_B = 80 mAdc) (I_C = 10 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	— — — —	2.0 2.0 2.5 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	— —	2.8 4.5	Vdc
Base–Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz) MJF6388 MJF6668	C_{ob}	—	200 300	pF
Insulation Capacitance (Collector–to–External Heatsink)	C_{c-hs}	—	3.0 Typ	pF
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	1000	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

NPN
MJF6388



PNP
MJF6668

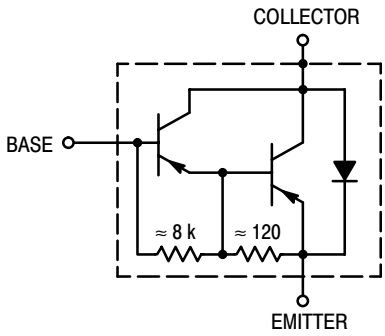


Figure 1. Darlington Schematic

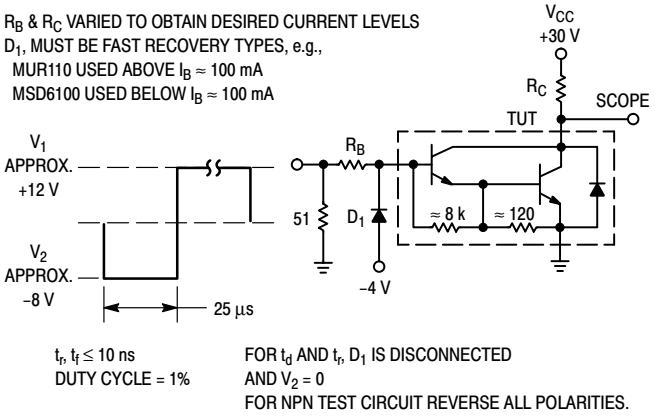
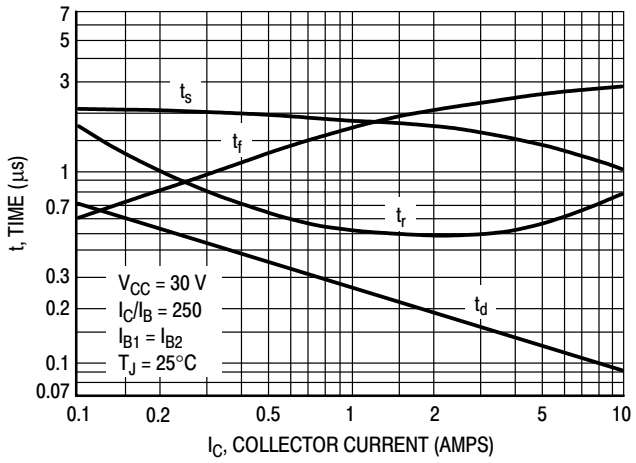


Figure 2. Switching Times Test Circuit

NPN
MJF6388



PNP
MJF6668

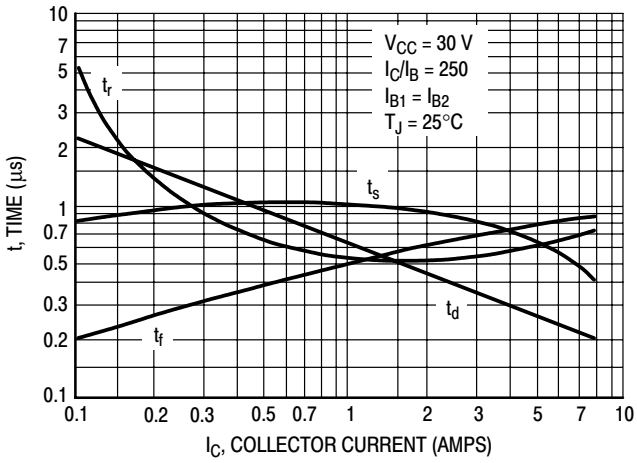


Figure 3. Typical Switching Times

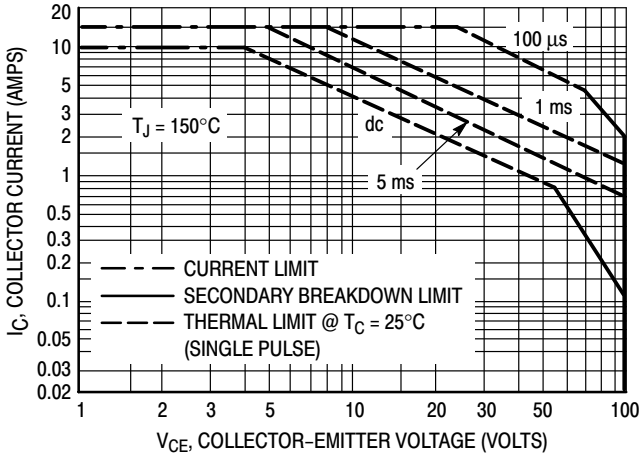


Figure 4. Maximum Forward Bias Safe Operating Area

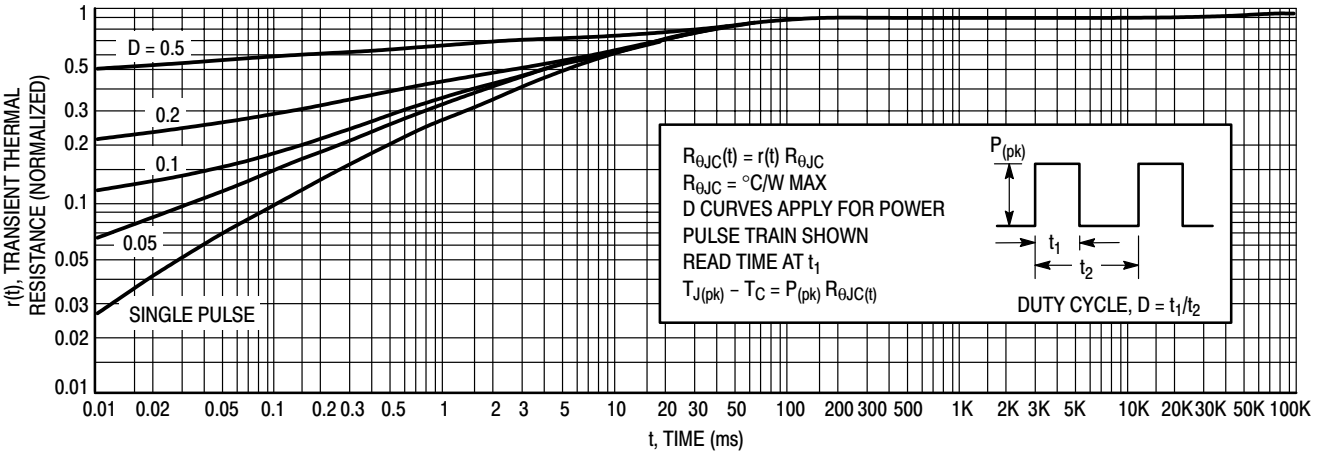


Figure 5. Thermal Response

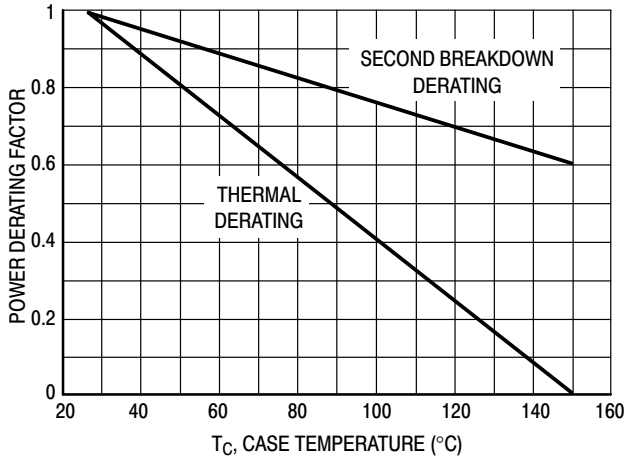


Figure 6. Maximum Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = l50°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

NPN
MJF6388

PNP
MJF6668

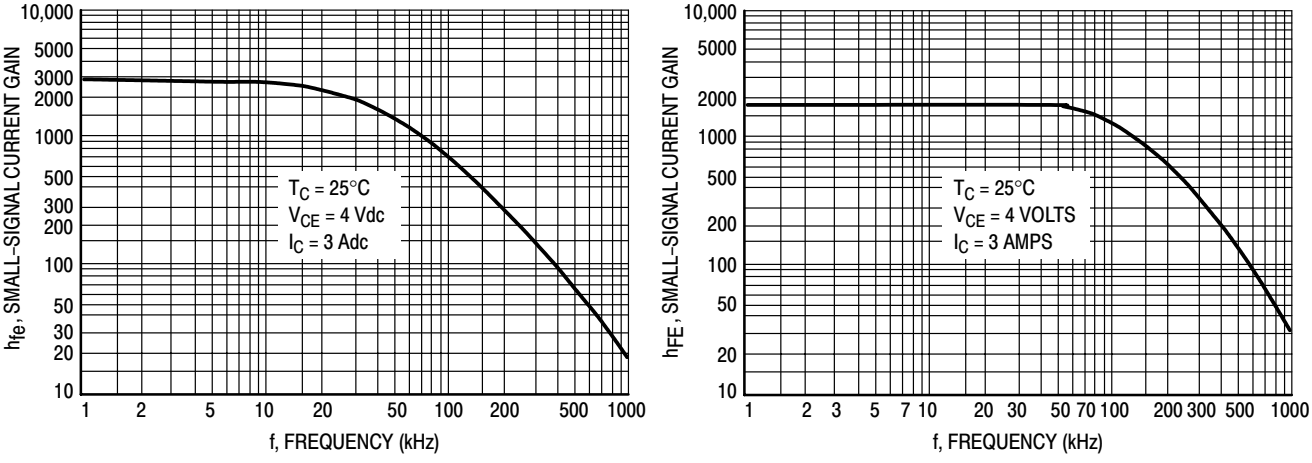
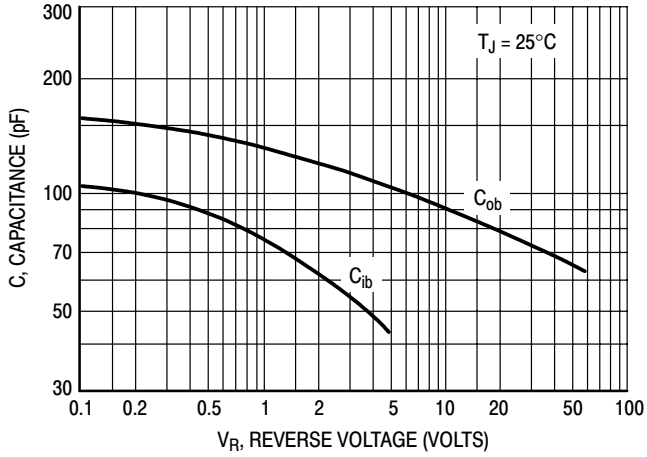


Figure 7. Typical Small–Signal Current Gain

NPN
MJF6388



PNP
MJF6668

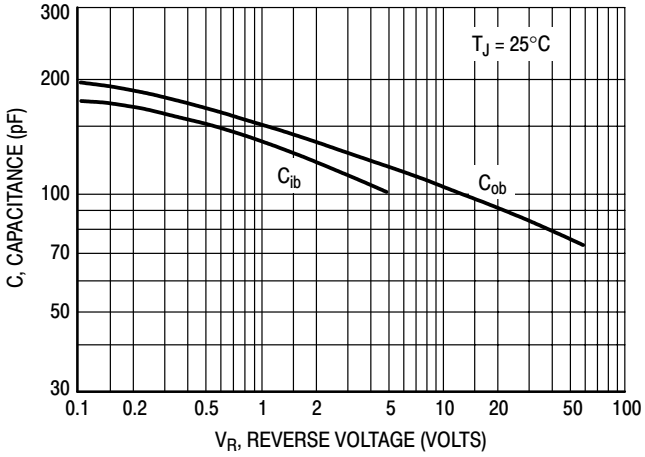
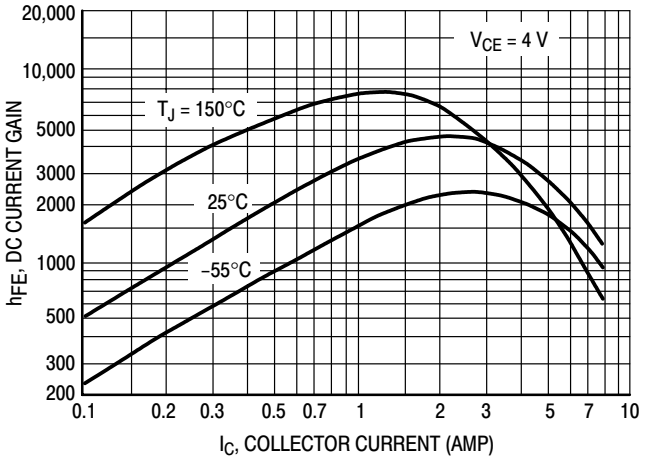


Figure 8. Typical Capacitance



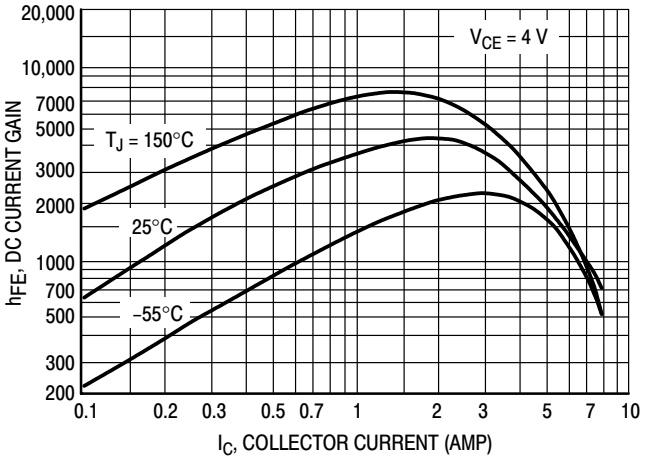
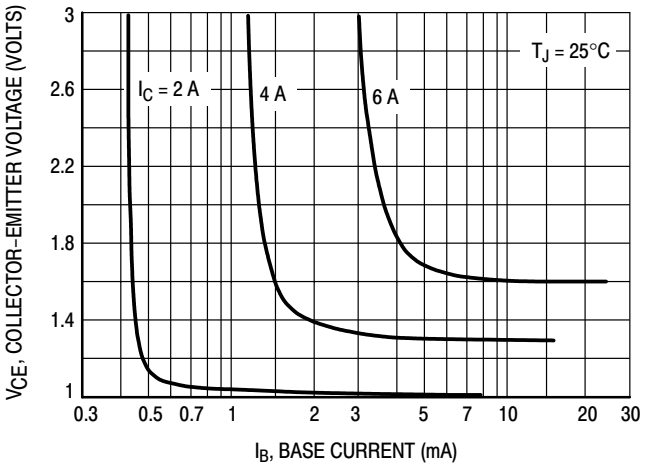


Figure 9. Typical DC Current Gain



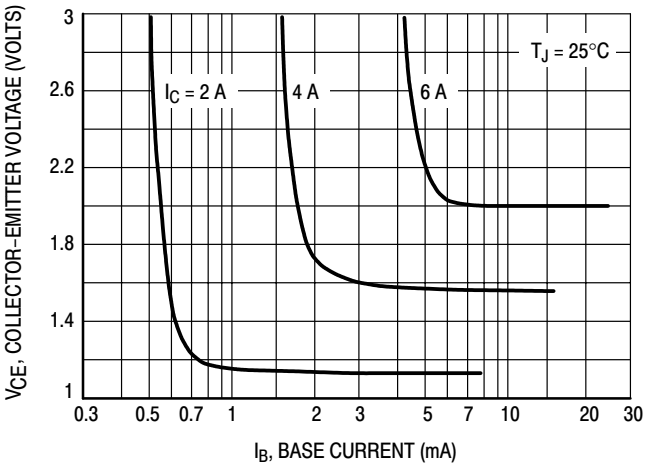
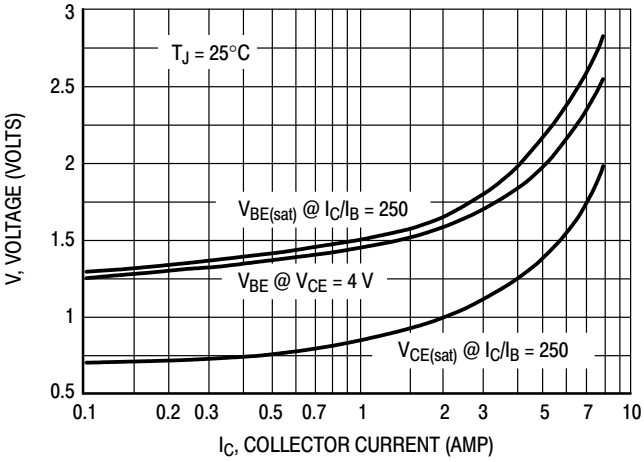


Figure 10. Typical Collector Saturation Region

NPN
MJF6388



PNP
MJF6668

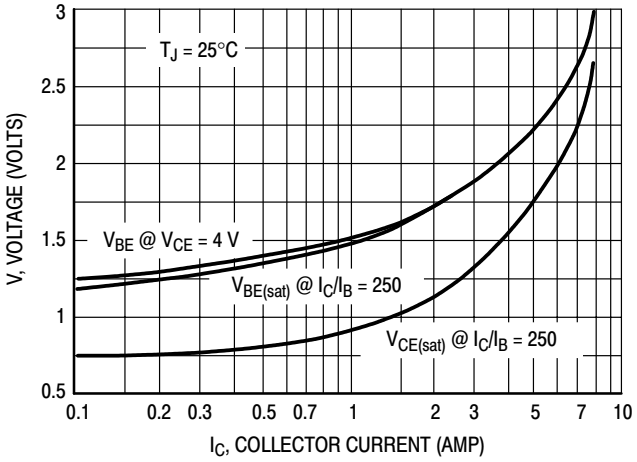
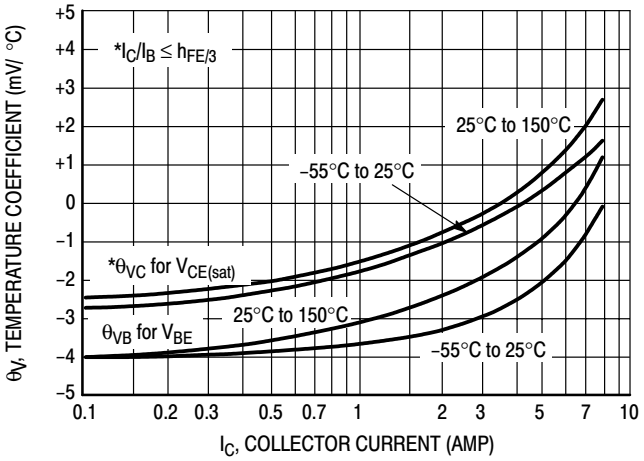


Figure 11. Typical “On” Voltages



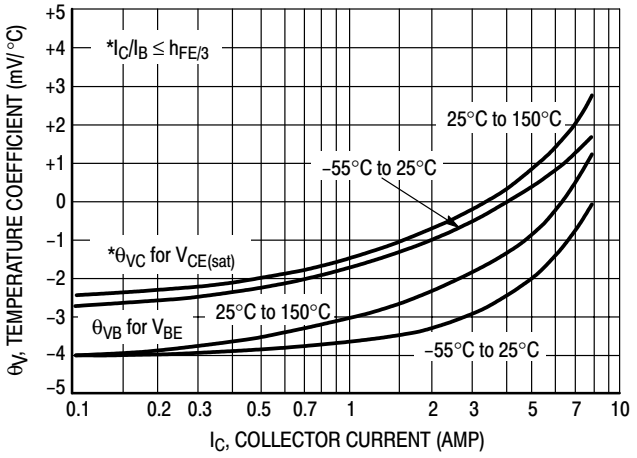
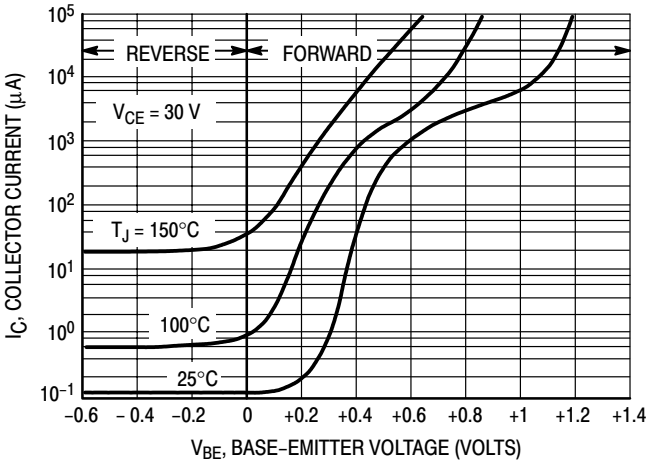


Figure 12. Typical Temperature Coefficients



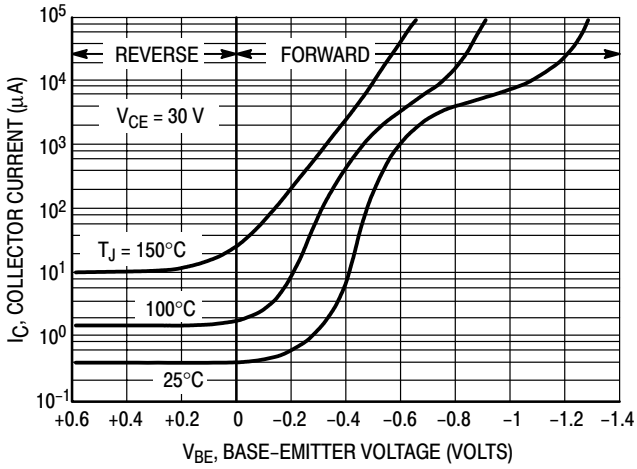


Figure 13. Typical Collector Cut–Off Region

TEST CONDITIONS FOR ISOLATION TESTS*

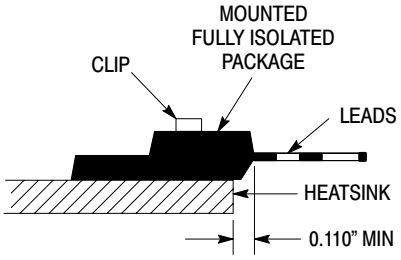


Figure 14. Clip Mounting Position for Isolation Test Number 1

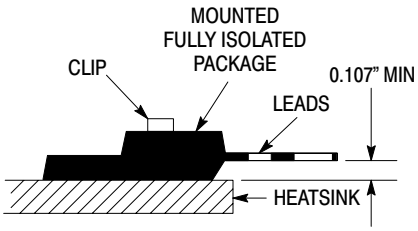


Figure 15. Clip Mounting Position for Isolation Test Number 2

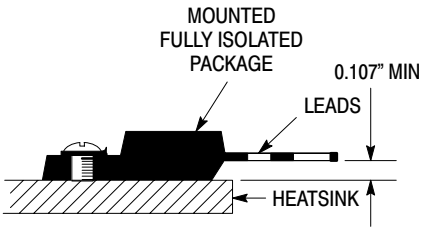


Figure 16. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

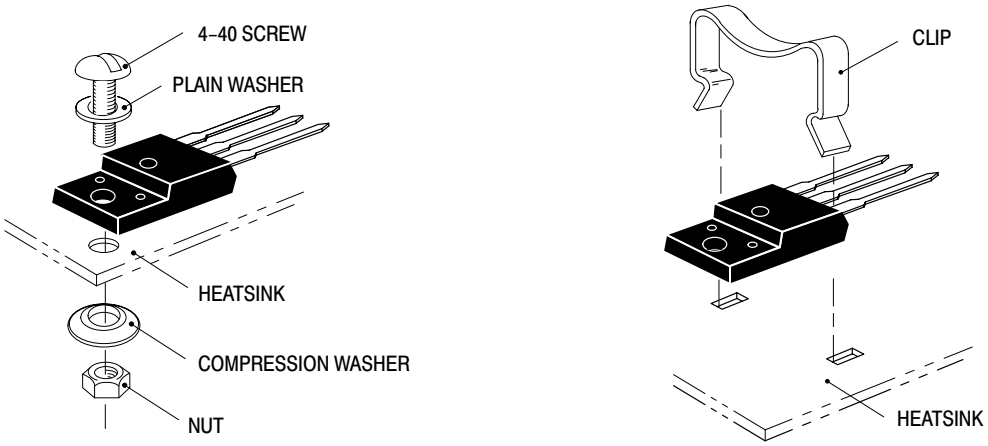


Figure 17. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Darlington Silicon Power Transistors

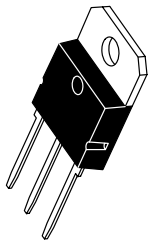
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc —
  h_{FE} = 400 Min (All Types)
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJH11018, 17
  = 200 Vdc (Min) — MJH11020, 19
  = 250 Vdc (Min) — MJH11022, 21
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.2 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction

PNP
MJH11017*
MJH11019*
MJH11021*
NPN
MJH11018*
MJH11020*
MJH11022*

*ON Semiconductor Preferred Device

15 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 150, 200, 250 VOLTS 150 WATTS



CASE 340D–02

MAXIMUM RATINGS

Rating	Symbol	MJH 11018 11017	MJH 11020 11019	MJH 11022 11021	Unit
Collector–Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector–Base Voltage	V_{CB}	150	200	250	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous — Peak (1)	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	150 1.2			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance. Junction to Case	$R_{\theta JC}$	0.83	°C/W

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
MJH11017/D

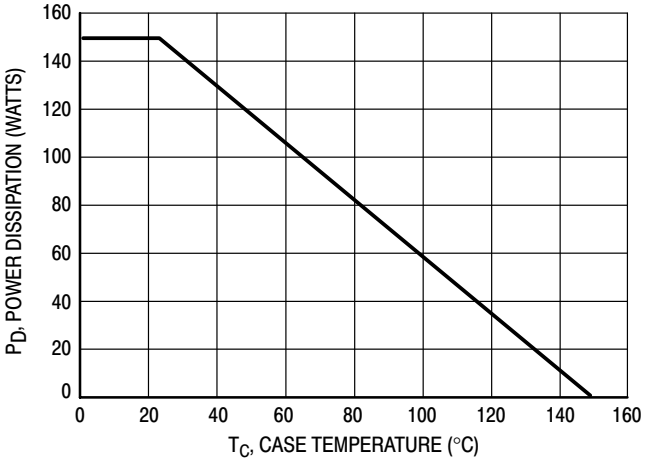


Figure 1. Power Derating

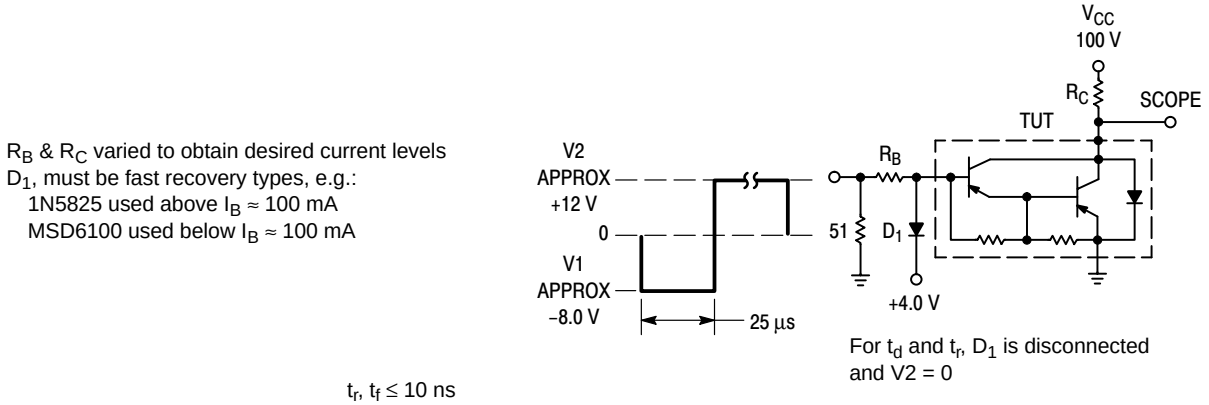
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	MJH11017, MJH11018		150	—	
	MJH11019, MJH11020		200	—	
	MJH11021, MJH11022		250	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 75 Vdc, I_B = 0)	MJH11017, MJH11018		—	1.0	
(V_{CE} = 100 Vdc, I_B = 0)	MJH11019, MJH11020		—	1.0	
(V_{CE} = 125 Vdc, I_B = 0)	MJH11021, MJH11022		—	1.0	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			—	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)			—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	400	15,000	—
(I_C = 15 Adc, V_{CE} = 5.0 Vdc)			100	—	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA)		$V_{CE(sat)}$	—	2.5	Vdc
(I_C = 15 Adc, I_B = 150 mA)			—	4.0	
Base–Emitter On Voltage (I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	3.0	—	—
Output Capacitance	MJH11018, MJH11020, MJH11022	C_{ob}	—	400	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH11017, MJH11019, MJH11021		—	600	
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	2.5	2.5	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.



R_B & R_C varied to obtain desired current levels
D_1, must be fast recovery types, e.g.:
1N5825 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA

For t_d and t_r, D_1 is disconnected and V2 = 0

t_r, $t_f \leq$ 10 ns
Duty Cycle = 1.0%

For NPN test circuit, reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

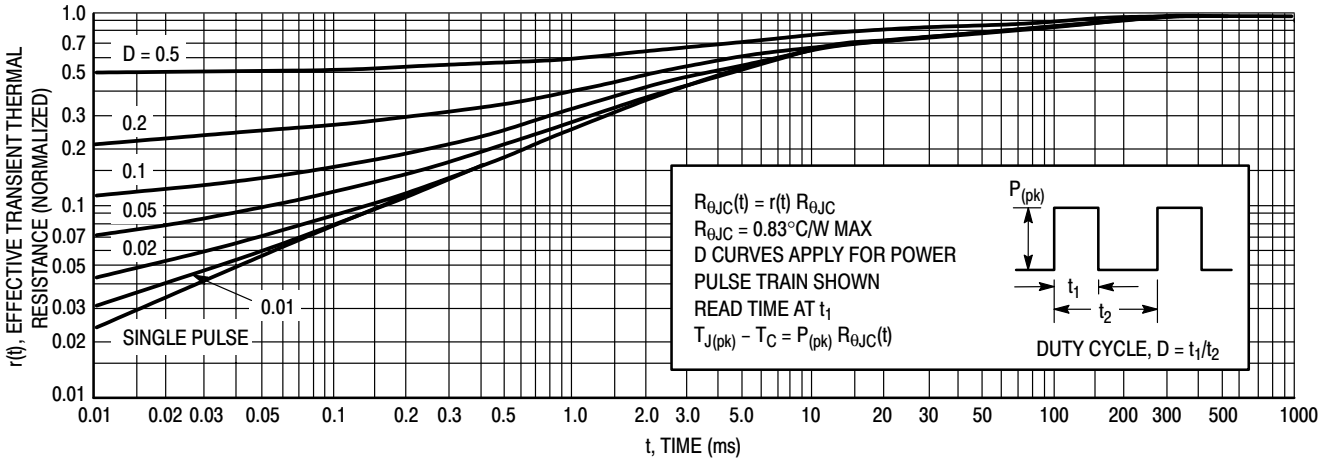


Figure 3. Thermal Response

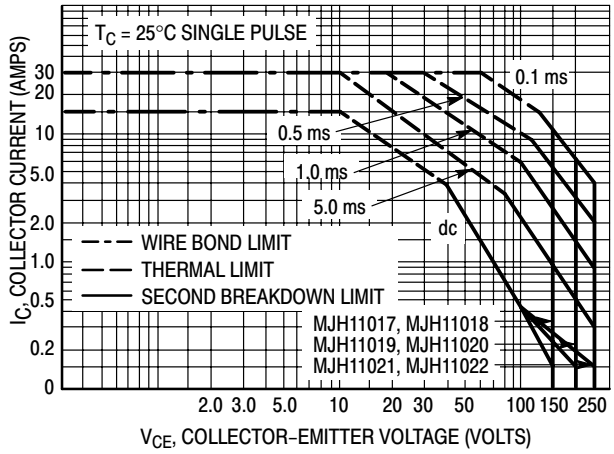


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

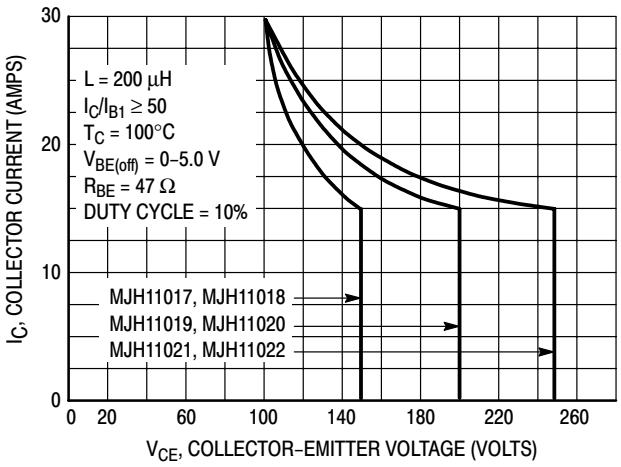


Figure 5. Maximum Rated Reverse Bias Safe Operating Area (RBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

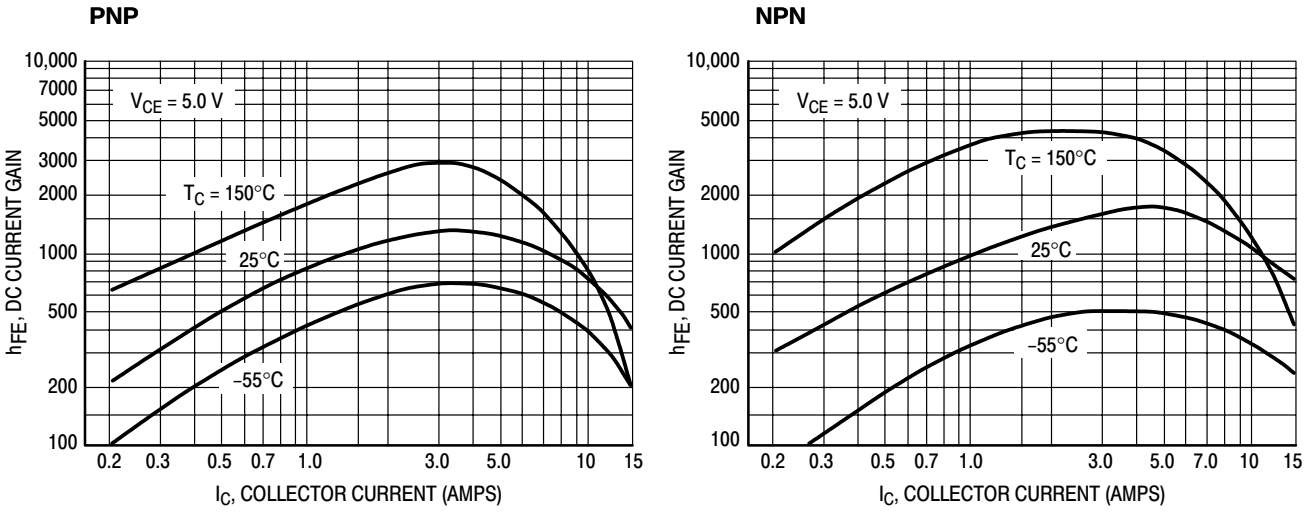


Figure 6. DC Current Gain

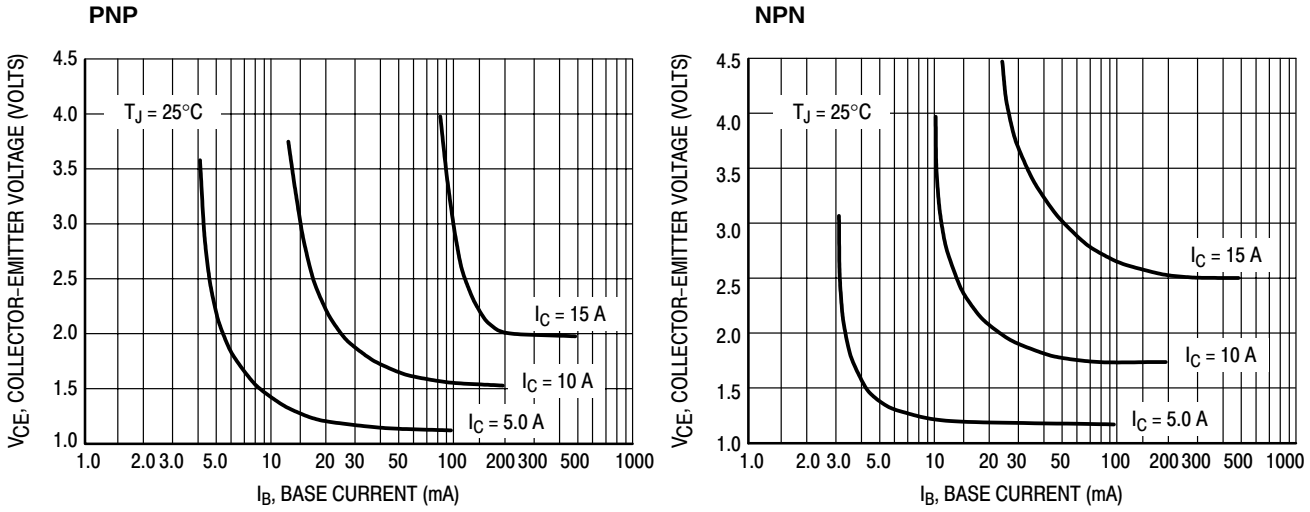


Figure 7. Collector Saturation Region

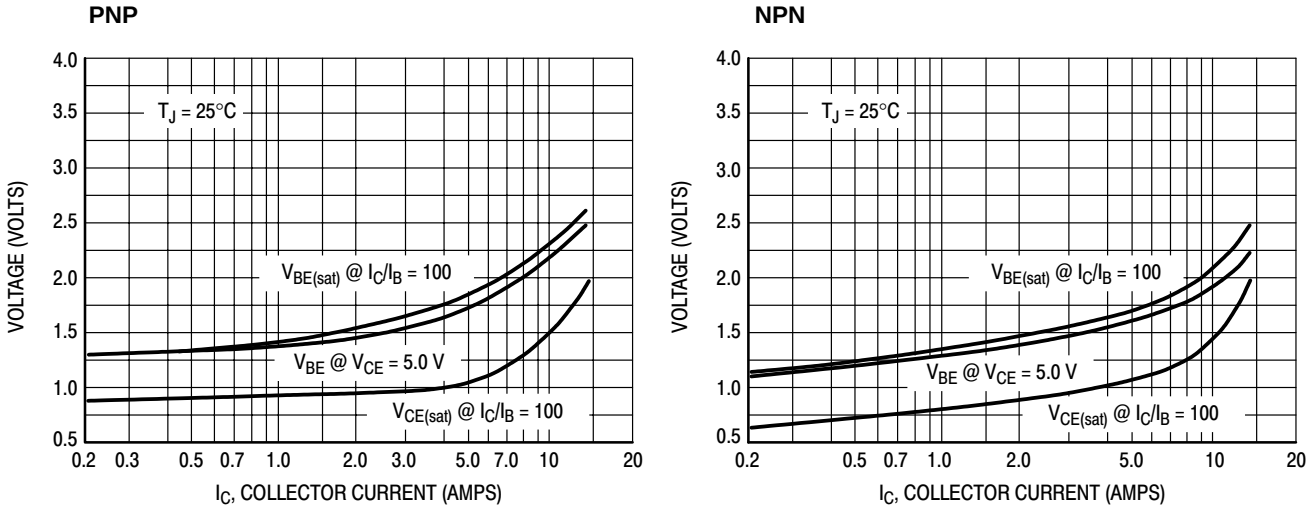


Figure 8. “On” Voltages

PNP **NPN**

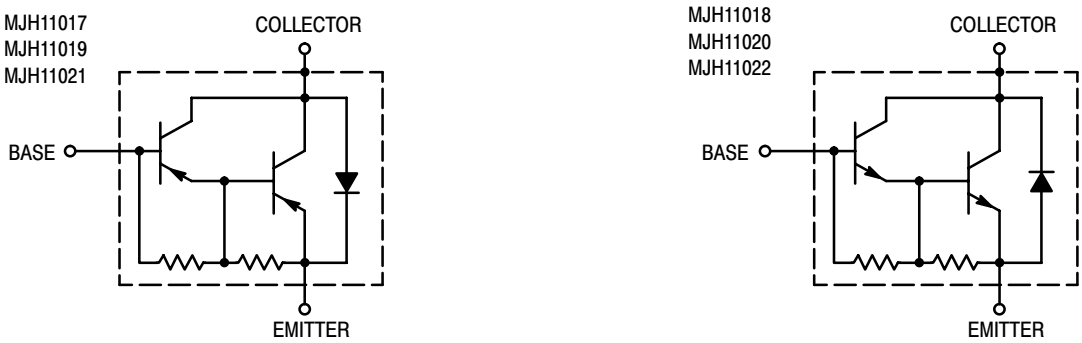


Figure 9. Darlington Schematic

Darlington Complementary Silicon Power Transistors

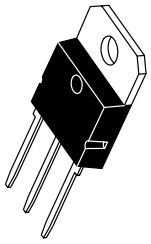
. . . designed for general–purpose amplifier and low–speed switching motor control applications.

- Similar to the Popular NPN 2N6284 and the PNP 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built–in Collector–Emitter Diode

NPN
MJH6284
PNP
MJH6287

ON Semiconductor Preferred Devices

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
100 VOLTS
160 WATTS



CASE 340D–02

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	20 40	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 160 1.28	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	°C/W

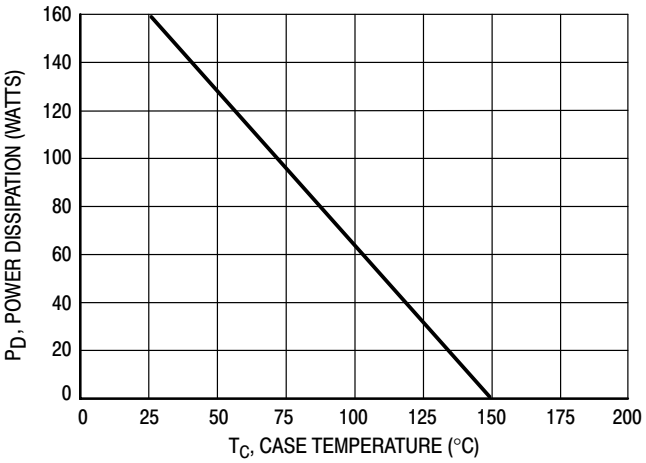


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

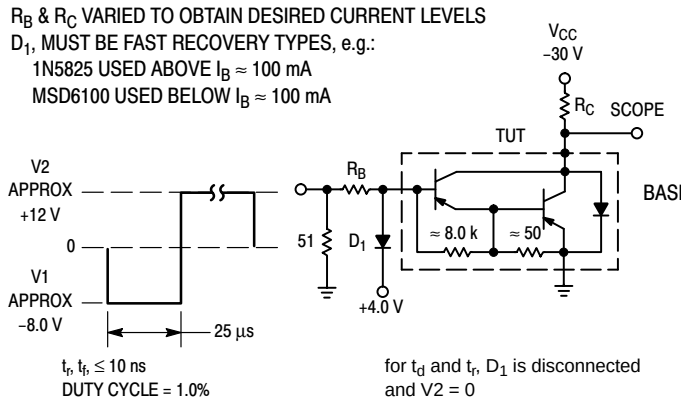
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	750 100	18,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	4.0	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJH6284 MJH6287	C_{ob}	— —	400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	—	—

SWITCHING CHARACTERISTICS

Resistive Load		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	V_{CC} = 30 Vdc, I_C = 10 Adc I_{B1} = I_{B2} = 100 mA Duty Cycle = 1.0%	t_d	0.1	0.1	μs
Rise Time		t_r	0.3	0.3	
Storage Time		t_s	1.0	1.0	
Fall Time		t_f	3.5	2.0	

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

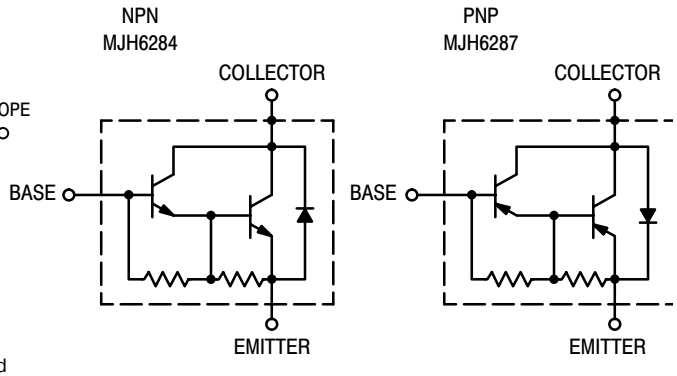


Figure 3. Darlington Schematic

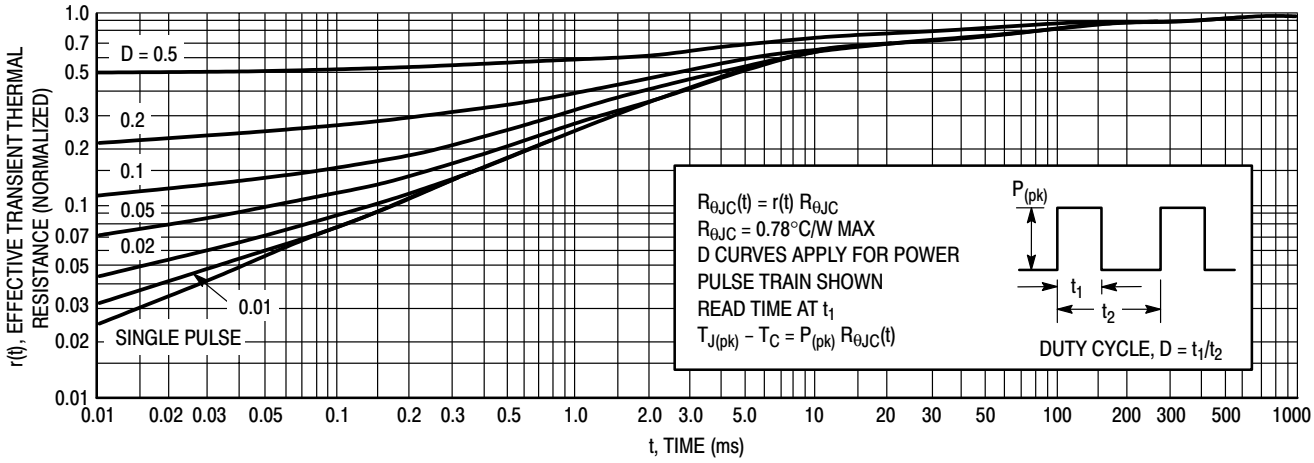


Figure 4. Thermal Response

FBSOA, FORWARD BIAS SAFE OPERATING AREA

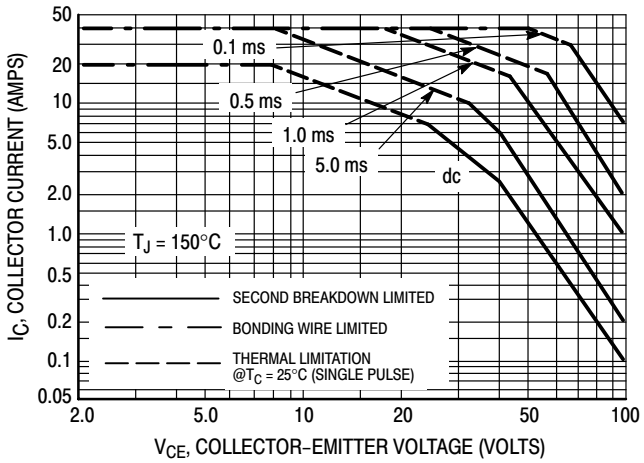


Figure 5. MJH6284, MJH6287

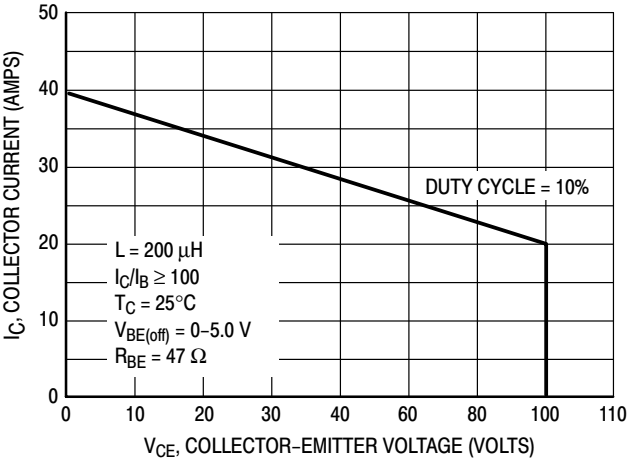


Figure 6. Maximum RBSOA, Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN **PNP**

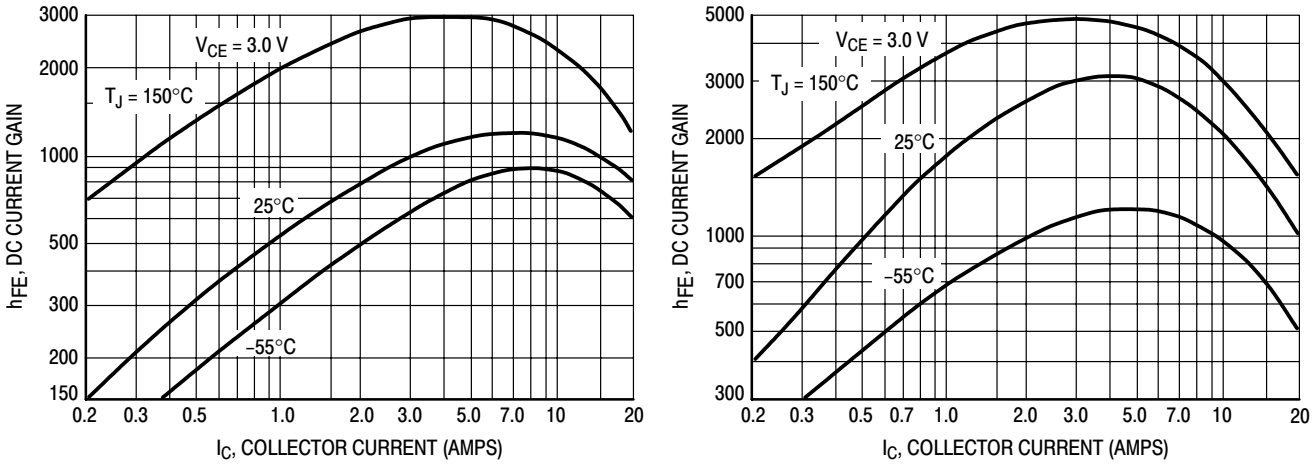


Figure 7. DC Current Gain

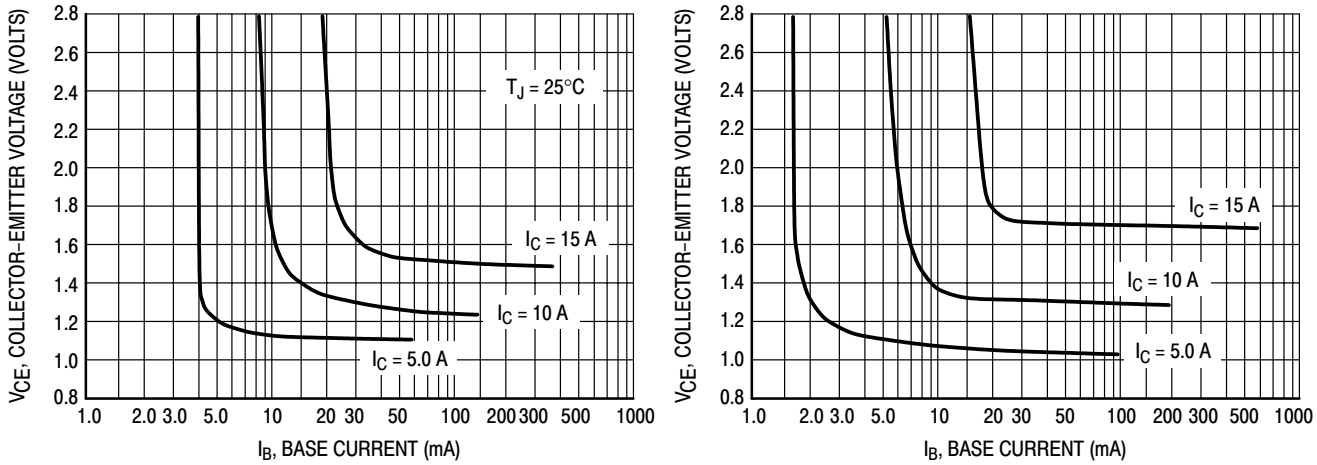


Figure 8. Collector Saturation Region

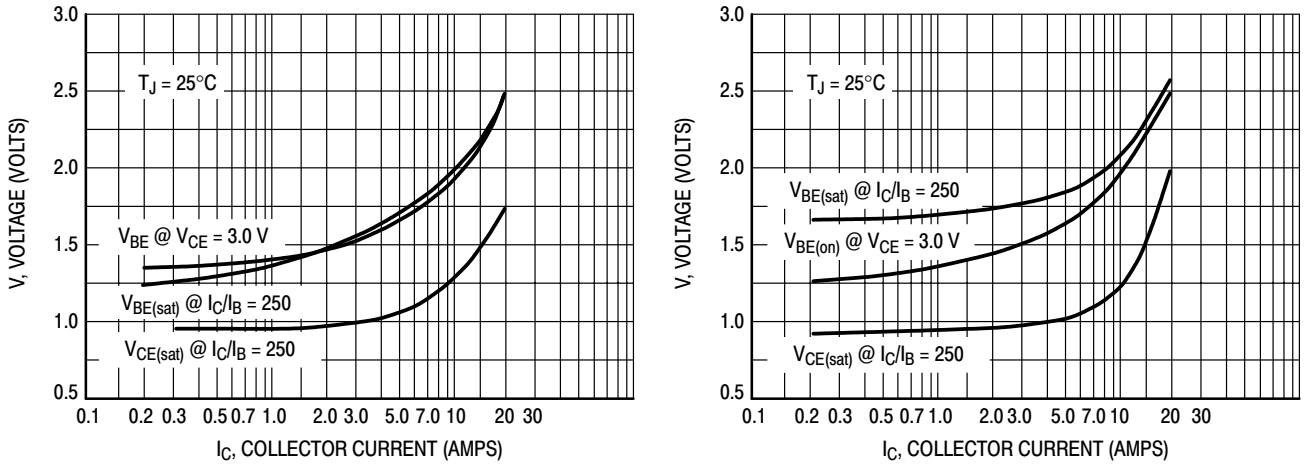


Figure 9. “On” Voltages

Silicon Power Transistors

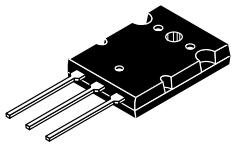
PNP
MJL21193*
NPN
MJL21194*

*ON Semiconductor Preferred Device

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS

The MJL21193 and MJL21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –
  h_{FE} = 25 Min @ I_C
  = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second



CASE 340G–02
TO–3PBL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 2
Publication Order Number:
MJL21193/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non–repetitive)) (V_{CE} = 80 Vdc, t = 1 s (non–repetitive))	$I_{S/b}$	 4.0 2.25	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, I_B = 5 Adc)	h_{FE}	 25 8	 — —	 75 —	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 — —	 1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 — —	 0.8 0.08	 — —	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJL21193

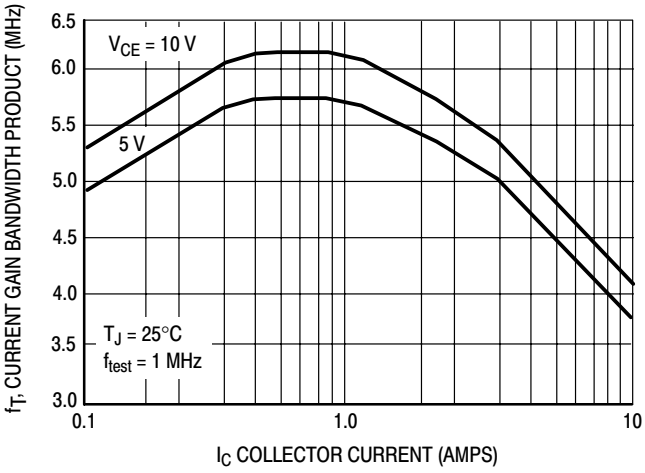


Figure 1. Typical Current Gain Bandwidth Product

NPN MJL21194

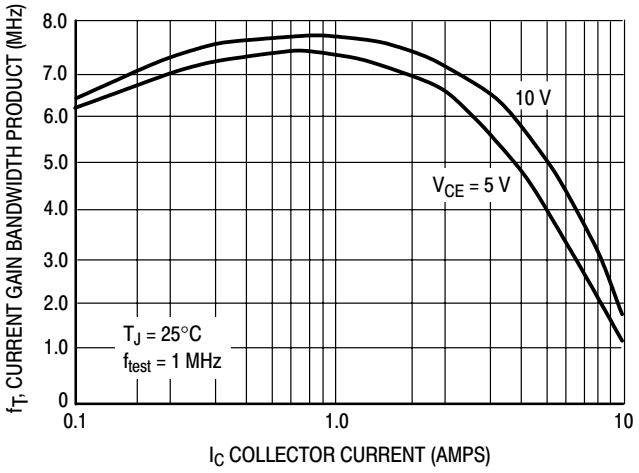


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJL21193

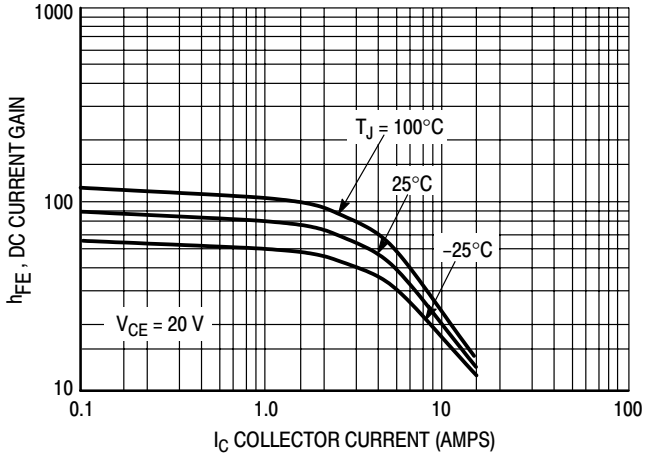


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJL21194

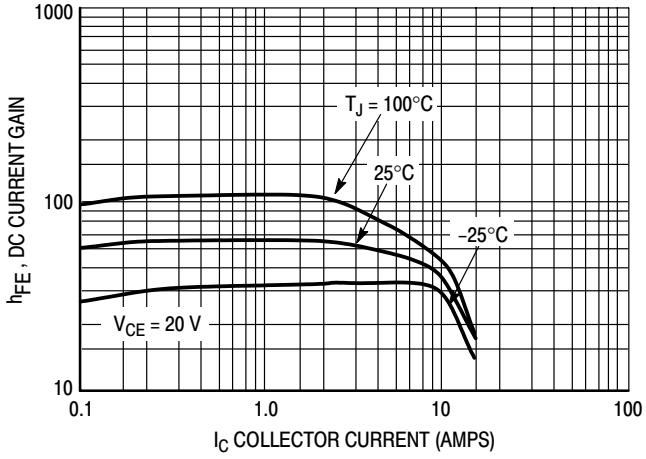


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJL21193

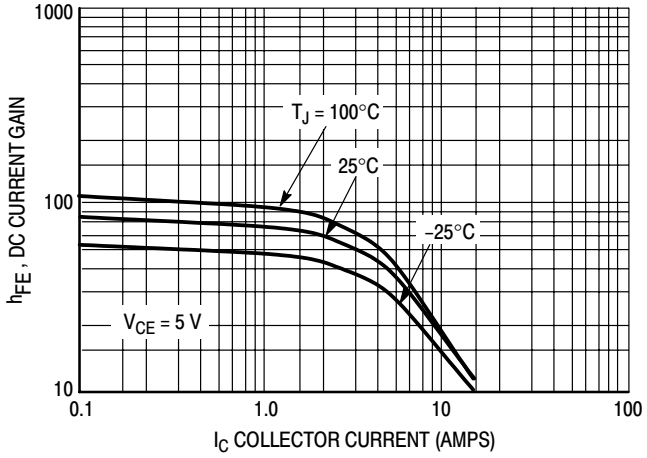


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJL21194

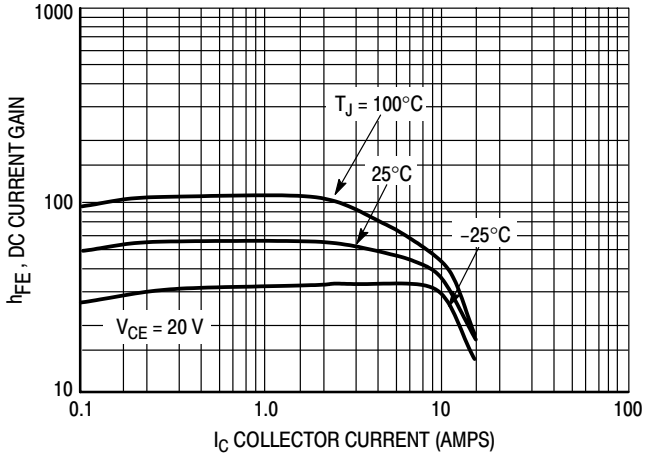
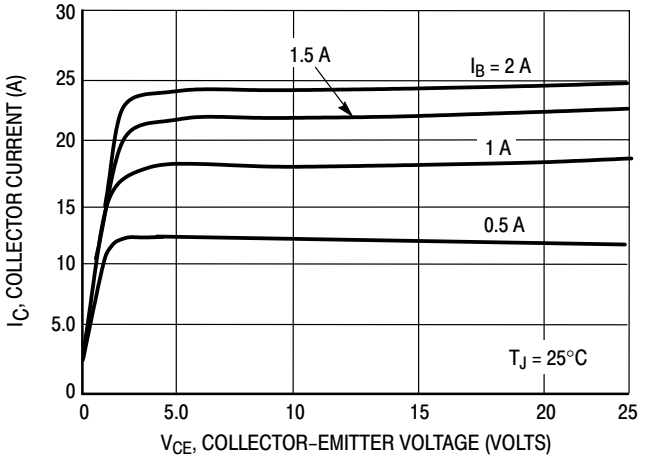
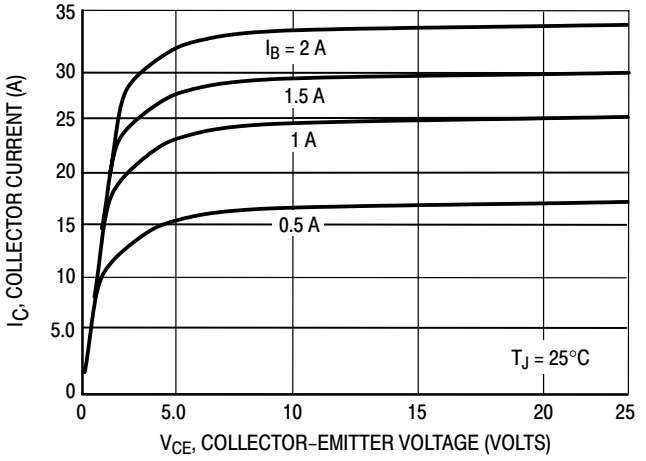


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJL21193



NPN MJL21194



TYPICAL CHARACTERISTICS

PNP MJL21193

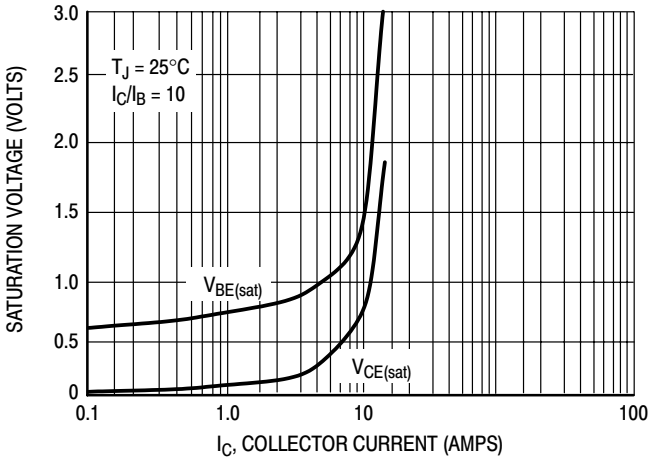


Figure 9. Typical Saturation Voltages

NPN MJL21194

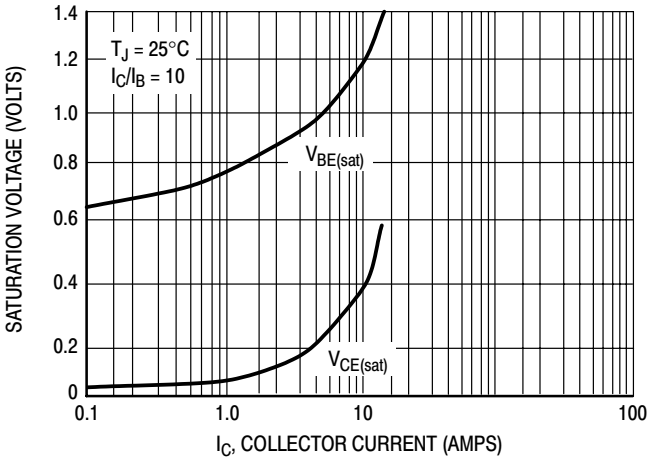


Figure 10. Typical Saturation Voltages

PNP MJL21193

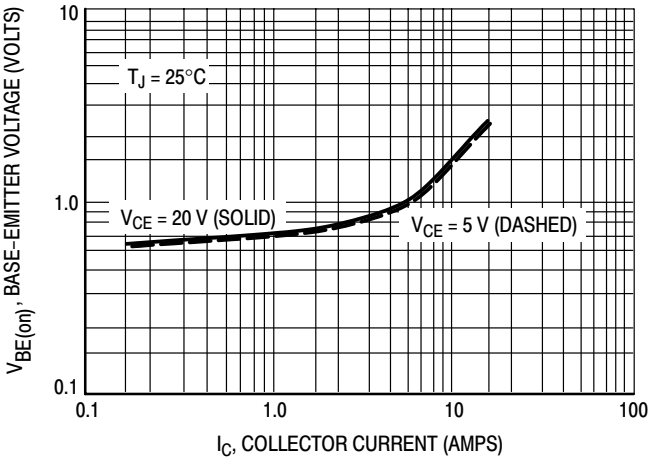


Figure 11. Typical Base–Emitter Voltage

NPN MJL21194

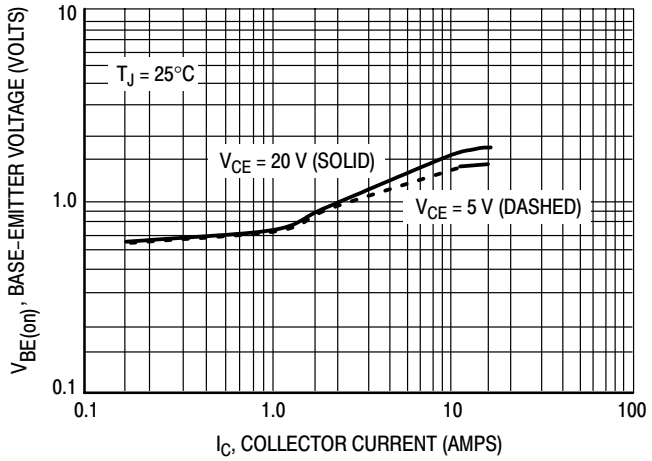


Figure 12. Typical Base–Emitter Voltage

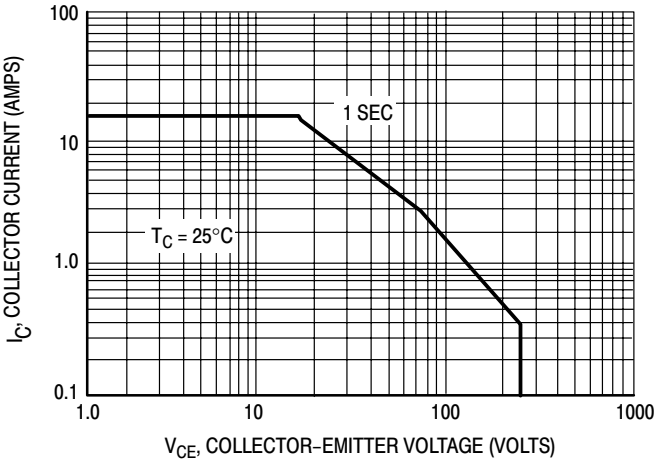


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

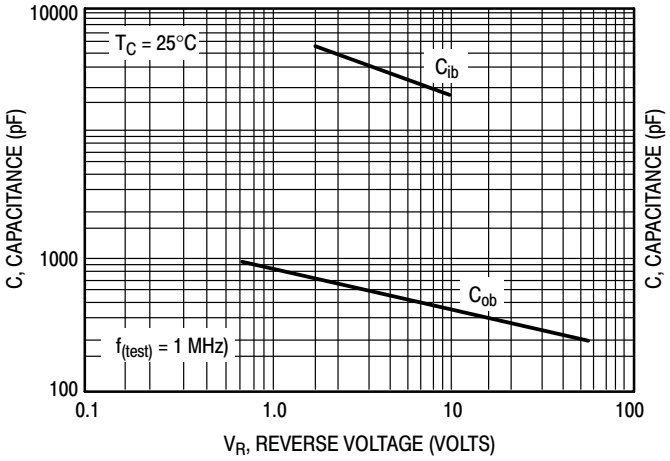


Figure 14. MJL21193 Typical Capacitance

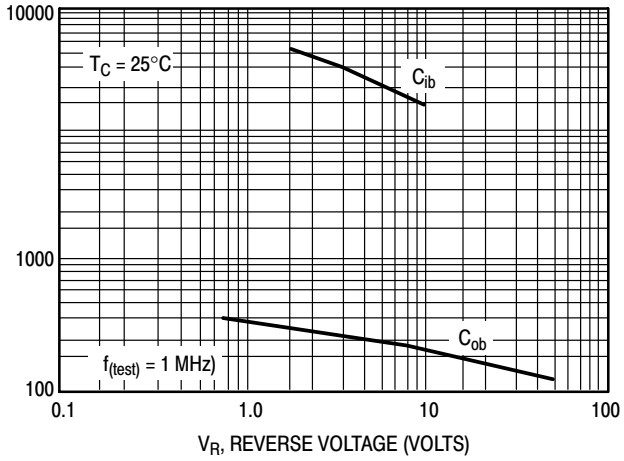


Figure 15. MJL21194 Typical Capacitance

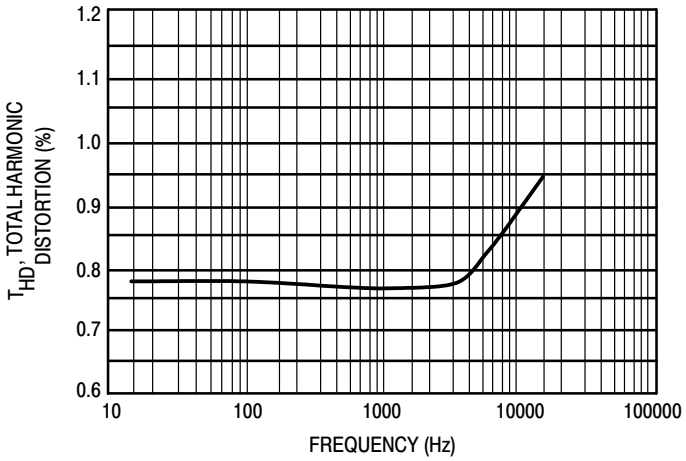


Figure 16. Typical Total Harmonic Distortion

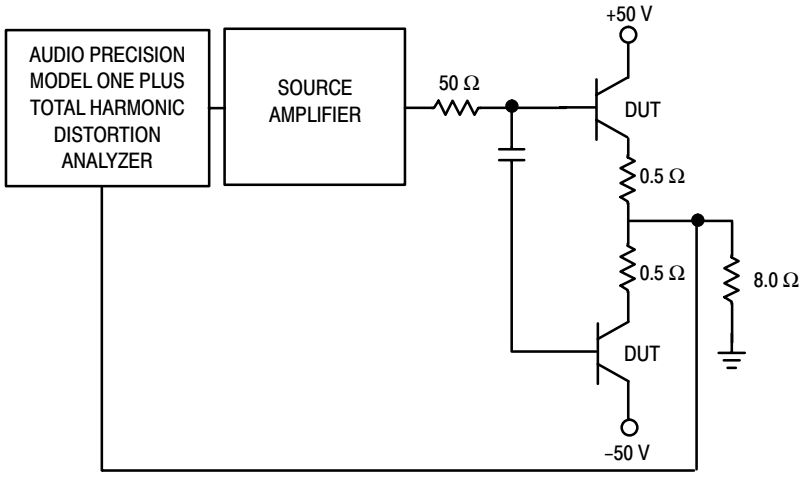


Figure 17. Total Harmonic Distortion Test Circuit

PNP
MJL21195*
NPN
MJL21196*

*ON Semiconductor Preferred Device

Silicon Power Transistors

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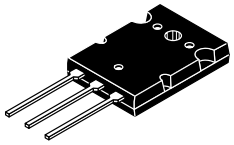
16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



CASE 340G–02 TO–3PBL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 1
Publication Order Number:
MJL21195/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive)		4.0	—	—	
(V_{CE} = 80 Vdc, t = 1 s (non–repetitive)		2.25	—	—	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 8 Adc, V_{CE} = 5 Vdc)		25	—	100	
(I_C = 16 Adc, I_B = 5 Adc)		8	—	—	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)		—	—	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)		—	—	4	
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output	T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched		—	0.8	—	
(Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched		—	0.08	—	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJL21195

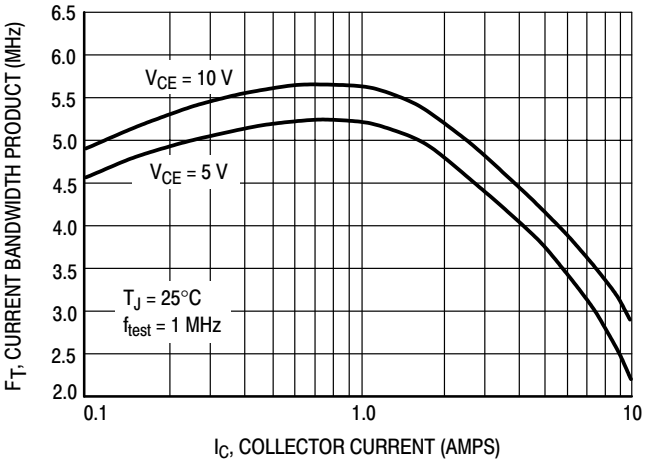


Figure 1. Typical Current Gain Bandwidth Product

NPN MJL21196

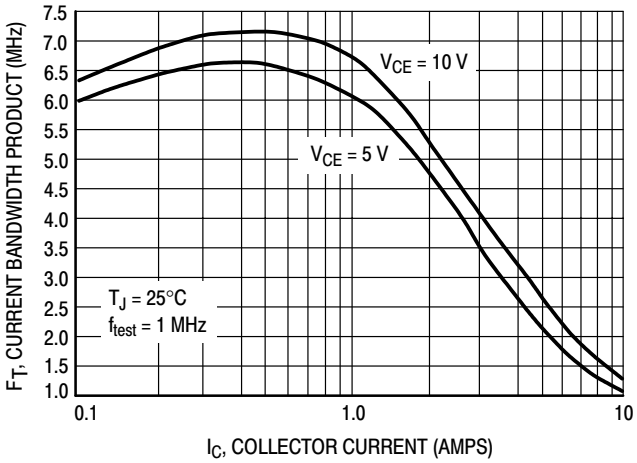


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJL21195

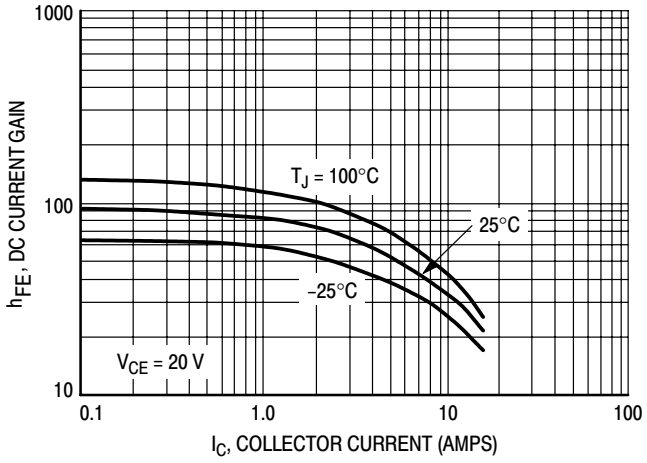


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJL21196

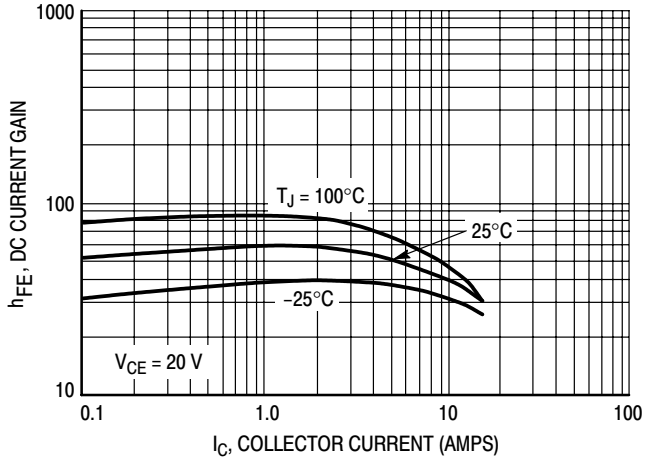


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJL21195

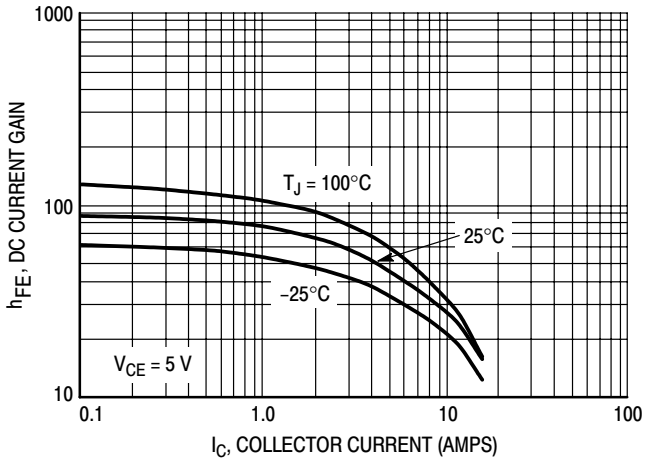


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJL21196

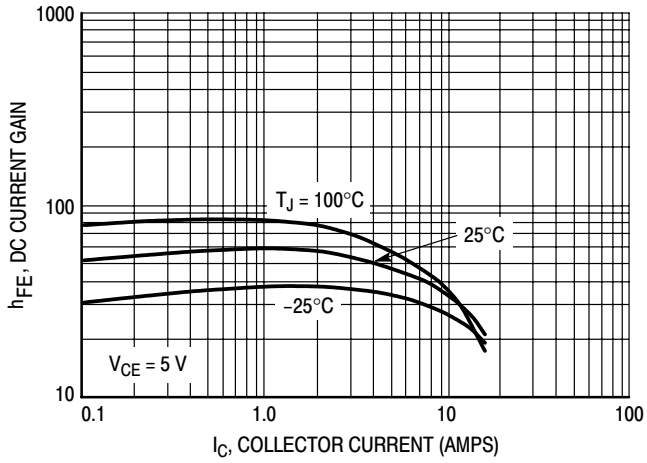


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJL21195

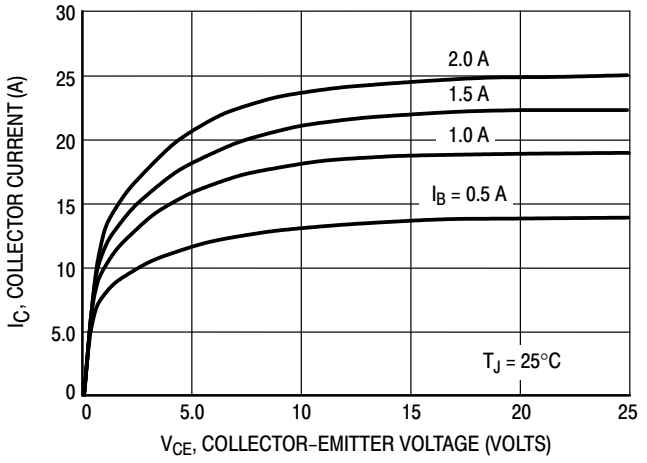


Figure 7. Typical Output Characteristics

NPN MJL21196

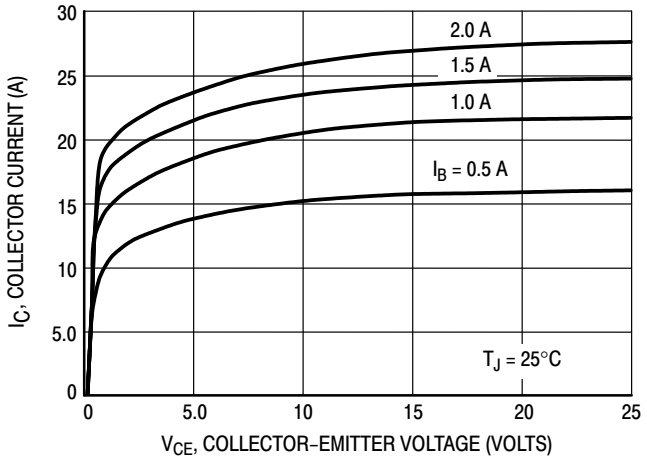


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJL21195

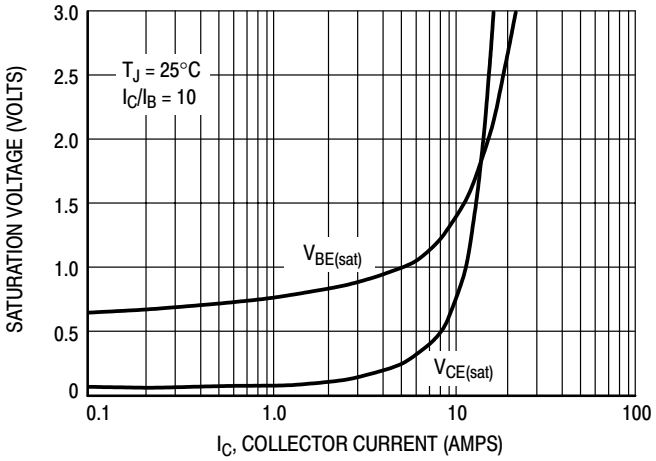


Figure 9. Typical Saturation Voltages

NPN MJL21196

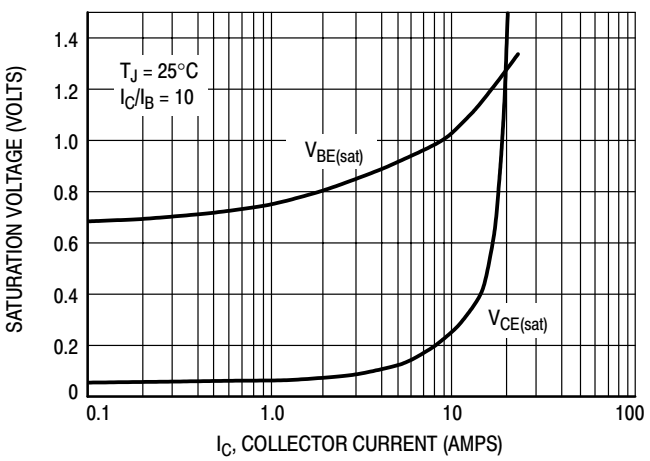


Figure 10. Typical Saturation Voltages

PNP MJL21195

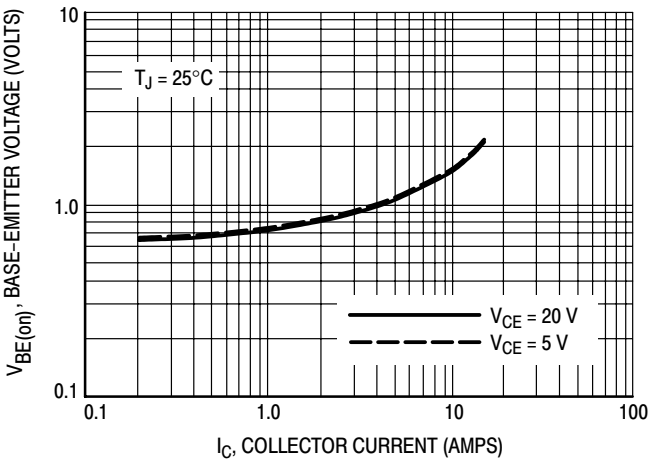


Figure 11. Typical Base–Emitter Voltage

NPN MJL21196

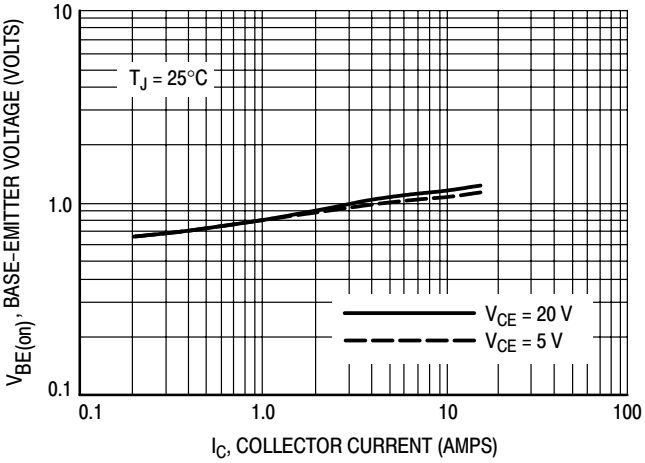


Figure 12. Typical Base–Emitter Voltage

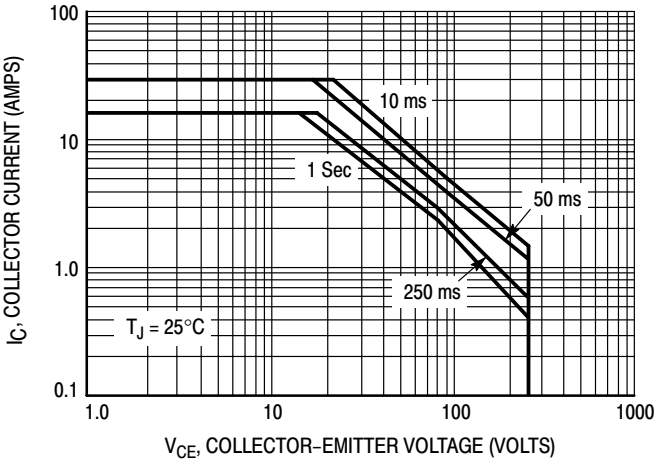


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

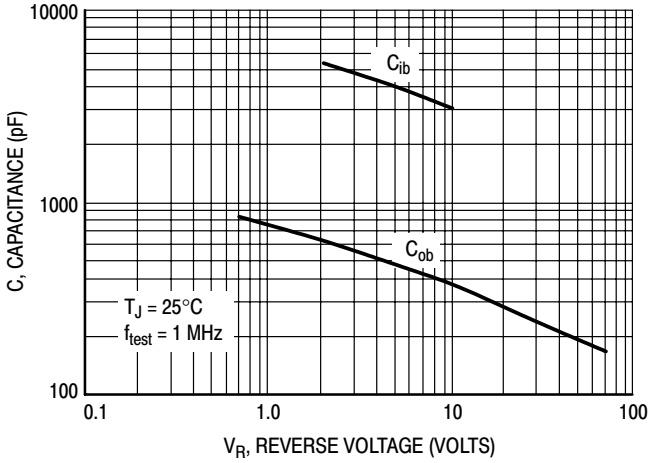


Figure 14. MJL21195 Typical Capacitance

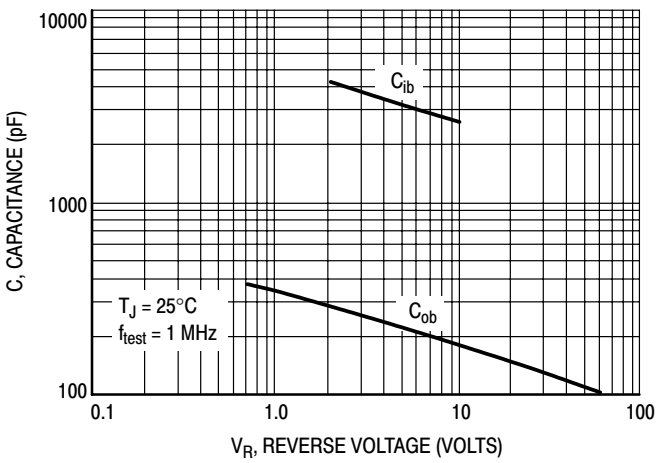


Figure 15. MJL21196 Typical Capacitance

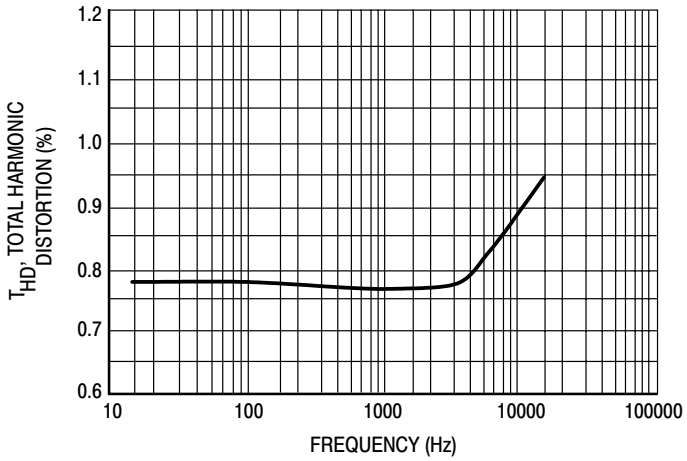


Figure 16. Typical Total Harmonic Distortion

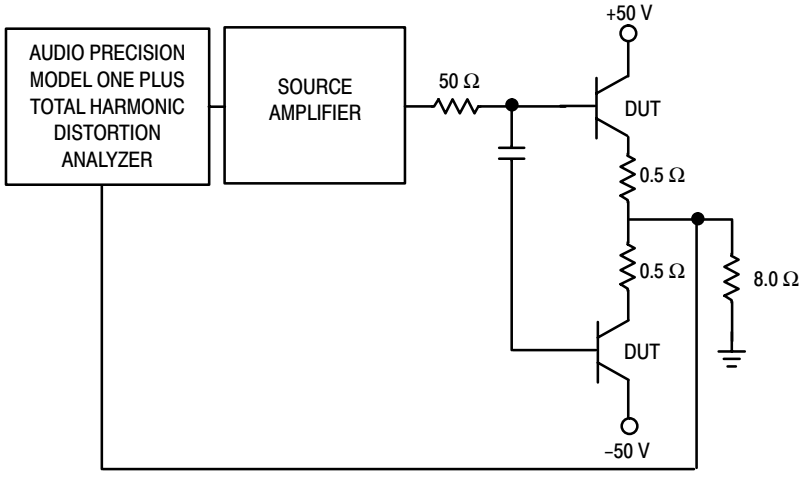


Figure 17. Total Harmonic Distortion Test Circuit

NPN
MJL3281A*
PNP
MJL1302A*

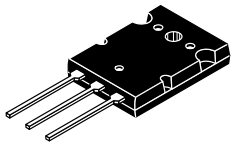
*ON Semiconductor Preferred Device

Complementary NPN-PNP Silicon Power Bipolar Transistor

The MJL3281A and MJL1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  Gain Linearity from 100 mA to 7 A
  High Gain — 60 to 175
  h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area — 1 A/100 V @ 1 Second
- High f_T — 30 MHz Typical

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 200 VOLTS 200 WATTS



CASE 340G–02, STYLE 2 TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CBO}	200	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	200	Vdc
Collector Current — Continuous — Peak (1)	I_C	15 25	Adc
Base Current — Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	—	Vdc
Emitter–Base Voltage (I_E = 100 μAdc, I_C = 0)	V_{EBO}	7	—	—	Vdc

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	—	—	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	5	μAdc
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non–repetitive) (V_{CE} = 100 Vdc, t = 1 s (non–repetitive)	$I_{S/b}$	 4 1	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc) (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 7 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	 60 60 60 60 60 45 12	 125 — — — 115 — 35	 175 175 175 175 175 — —	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	—	—	3	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	—	30	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	600	pF

PNP MJL1302A

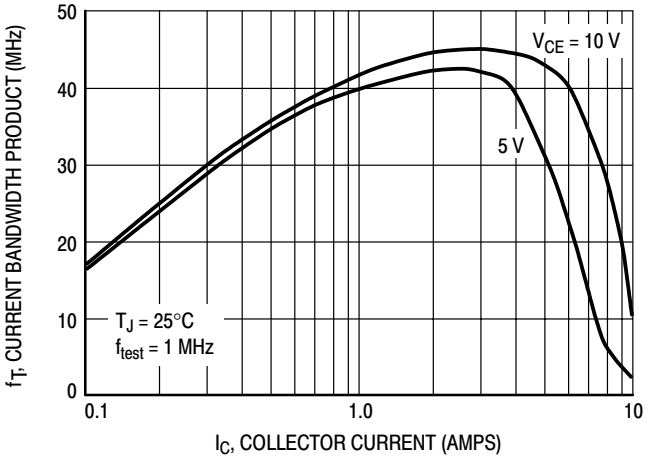


Figure 18. Typical Current Gain Bandwidth Product

NPN MJL3281A

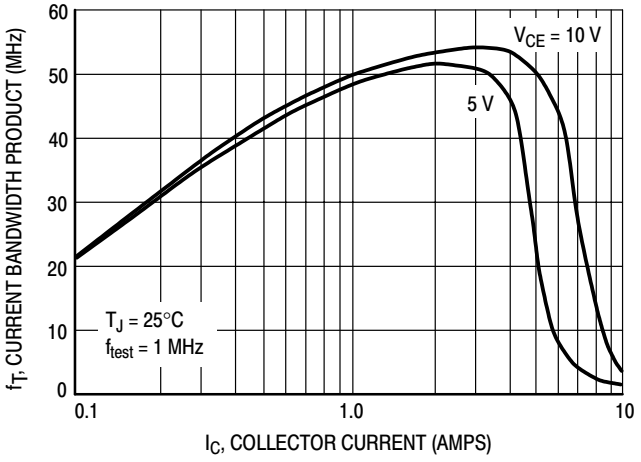


Figure 19. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJL1302A

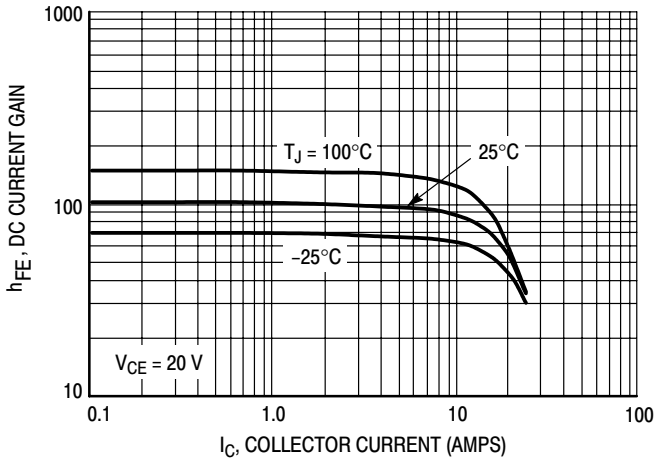


Figure 20. DC Current Gain, V_{CE} = 20 V

NPN MJL3281A

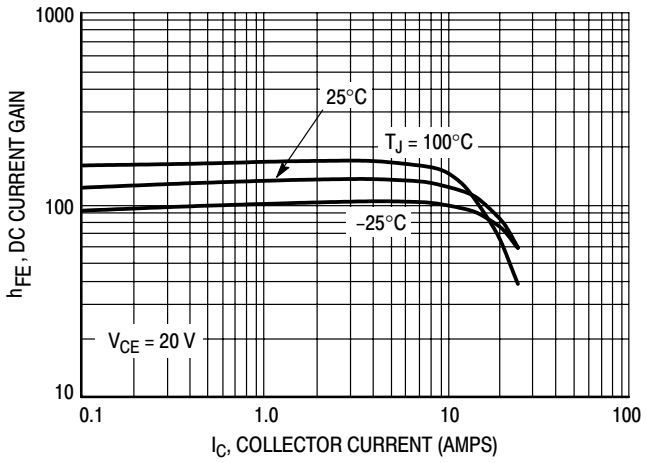


Figure 21. DC Current Gain, V_{CE} = 20 V

PNP MJL1302A

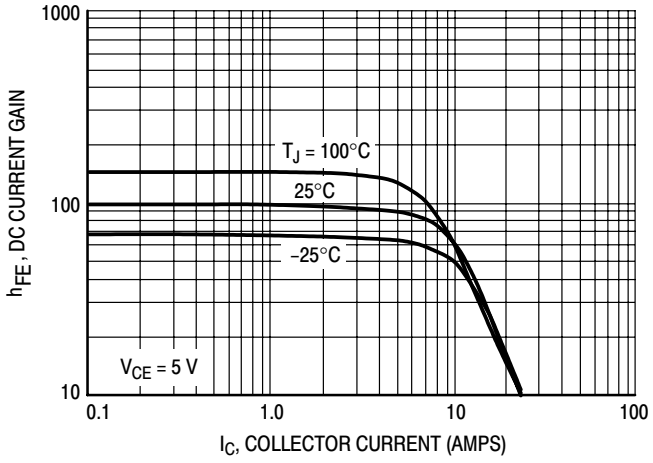


Figure 22. DC Current Gain, V_{CE} = 5 V

NPN MJL3281A

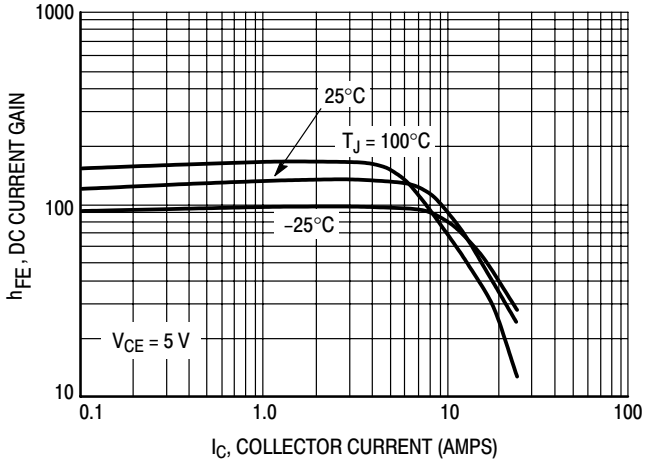


Figure 23. DC Current Gain, V_{CE} = 5 V

PNP MJL1302A

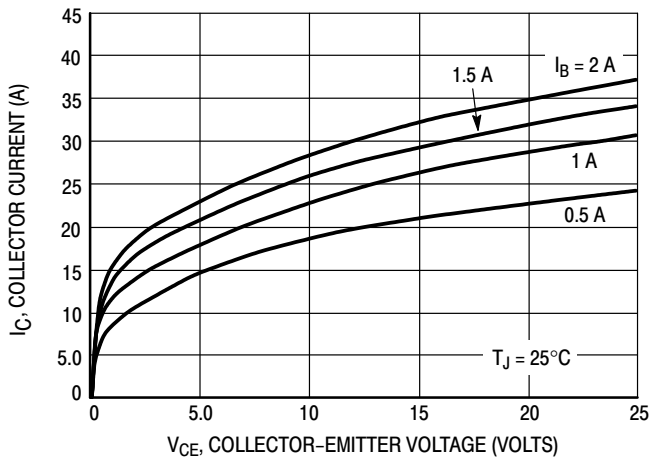


Figure 24. Typical Output Characteristics

NPN MJL3281A

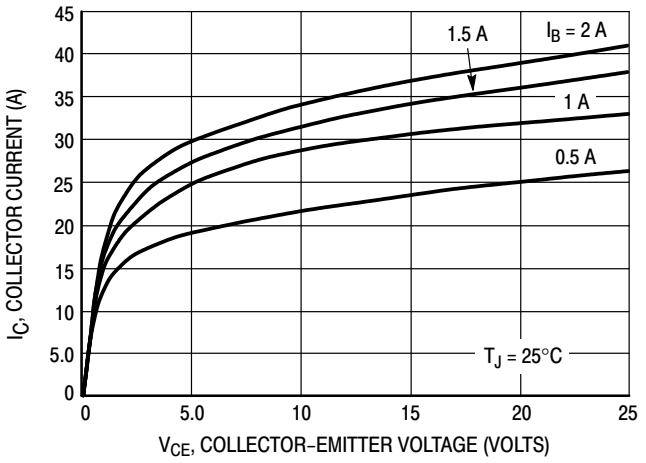


Figure 25. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJL1302A

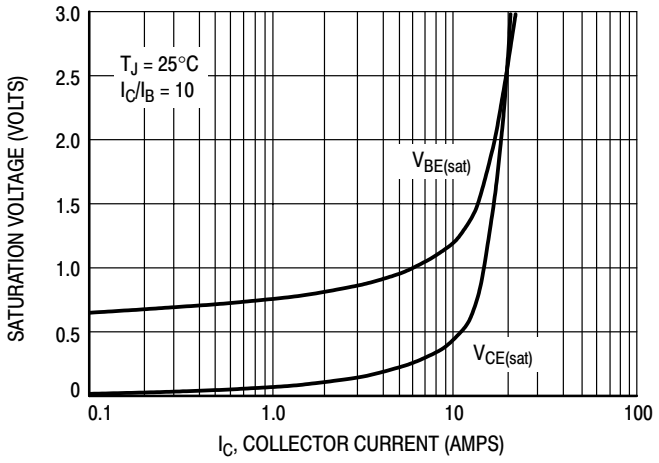


Figure 26. Typical Saturation Voltages

NPN MJL3281A

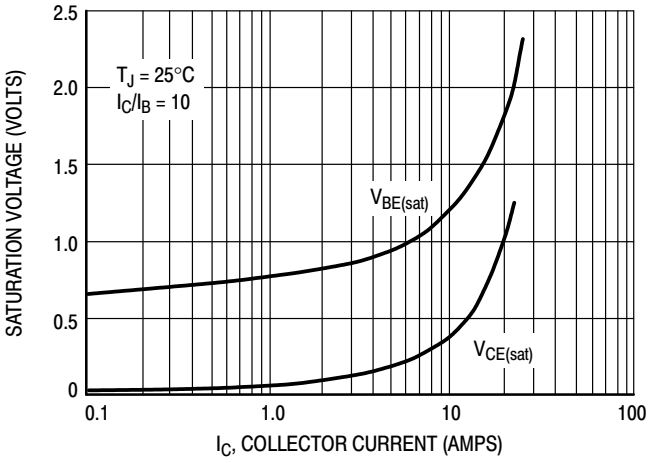


Figure 27. Typical Saturation Voltages

PNP MJL1302A

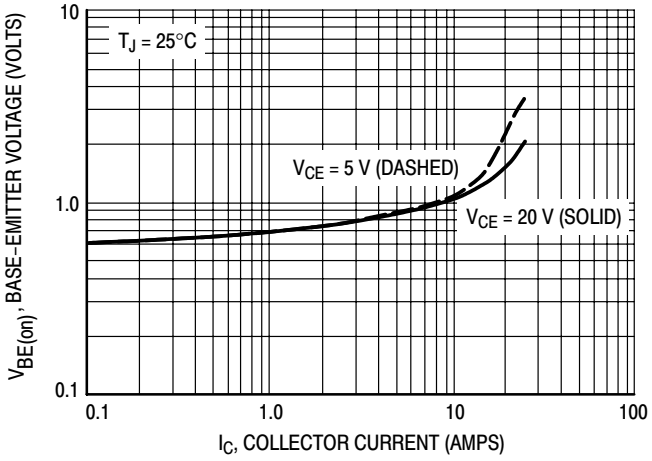


Figure 28. Typical Base–Emitter Voltage

NPN MJL3281A

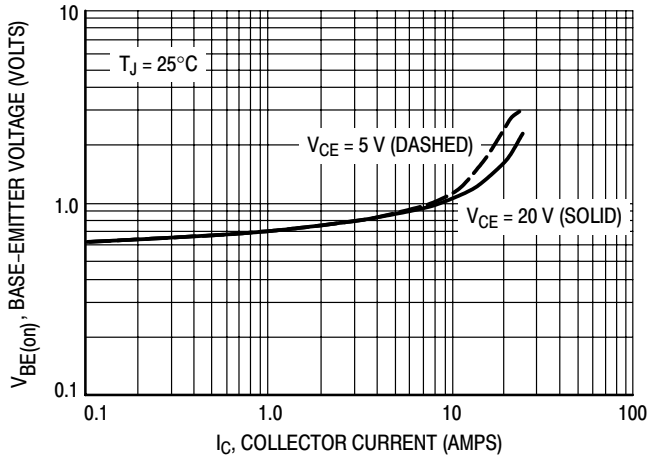


Figure 29. Typical Base–Emitter Voltage

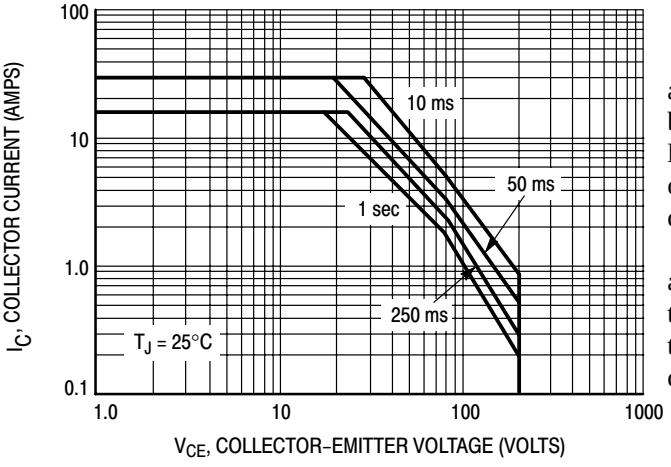


Figure 30. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 30 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

PNP MJL1302A

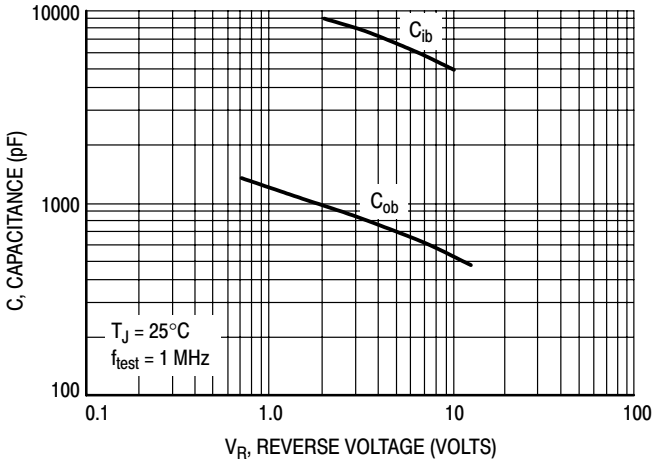


Figure 31. MJL1302A Typical Capacitance

NPN MJL3281A

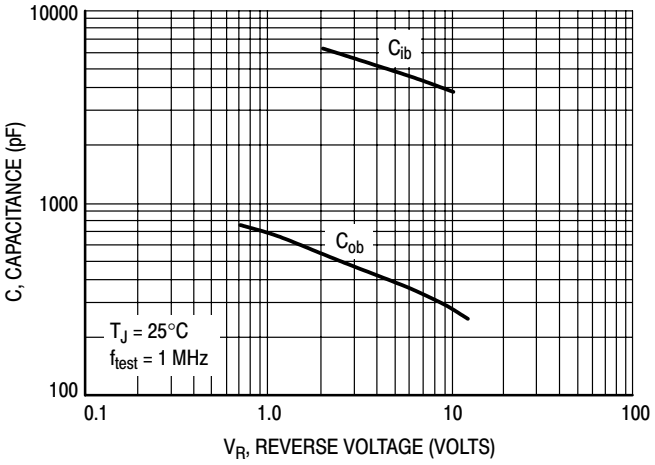


Figure 32. MJL3281A Typical Capacitance

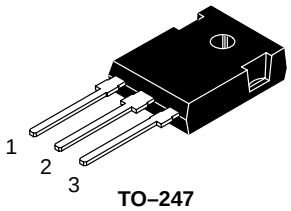
Complementary Silicon Plastic Power Transistors

Specifically designed for power audio output, or high power drivers in audio amplifiers.

- DC Current Gain Specified up to 8.0 Amperes at Temperature
- All On Characteristics at Temperature
- High SOA: 20 A, 18 V, 100 ms
- TO–247AE Package

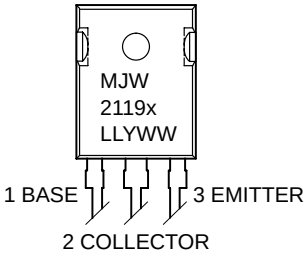
NPN
MJW21192
PNP
MJW21191

8.0 AMPERES
POWER TRANSISTORS
COMPLEMENTARY SILICON
150 VOLTS
125 WATTS



TO–247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW2119x = Device Code
x = 1 or 2
LL = Location Code
Y = Year
WW = Work Week

MAXIMUM RATINGS

Rating	Symbol	MJW21191 MJW21192	Unit
Collector–Emitter Voltage	V_{CEO}	150	Vdc
Collector–Base Voltage	V_{CB}	150	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	8.0 16	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	°C/W

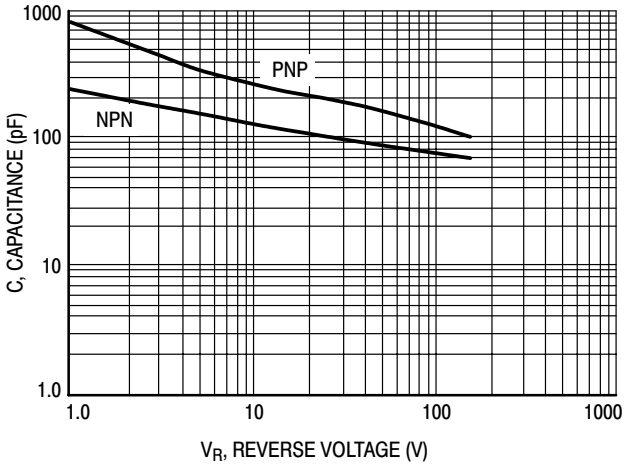


Figure 1. Typical Capacitance @ 25°C

May, 2001 – Rev. 1
Publication Order Number:
MJW21192/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current (V_{CB} = 250 Vdc, I_E = 0)	I_{CES}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	15 5.0	— —	— 100
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 8.0 Adc, I_B = 1.6 Adc)	$V_{CE(sat)}$	— —	1.0 2.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

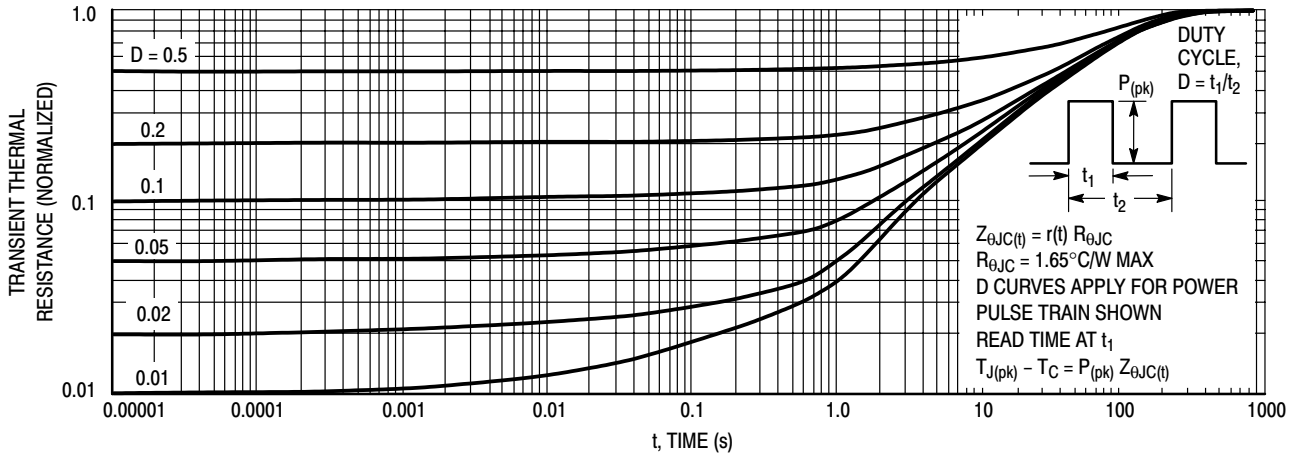


Figure 2. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN — MJW21192

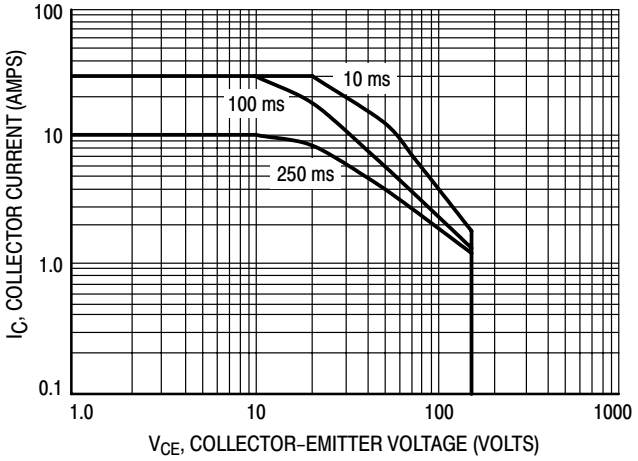


Figure 3. NPN — MJW21192 Safe Operating Area

PNP — MJW21191

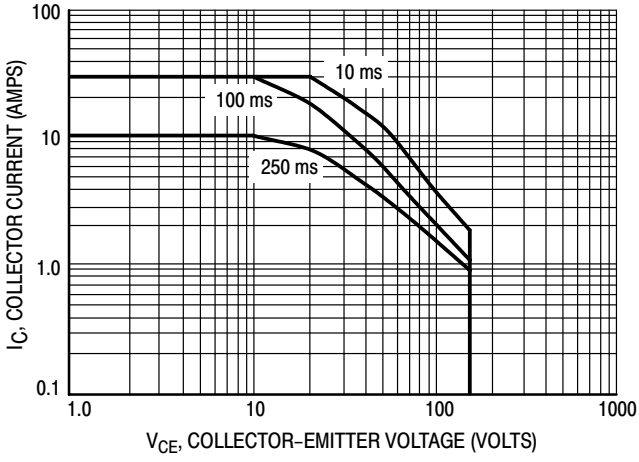


Figure 4. PNP — MJW21191 Safe Operating Area

TYPICAL CHARACTERISTICS

NPN — MJW21192

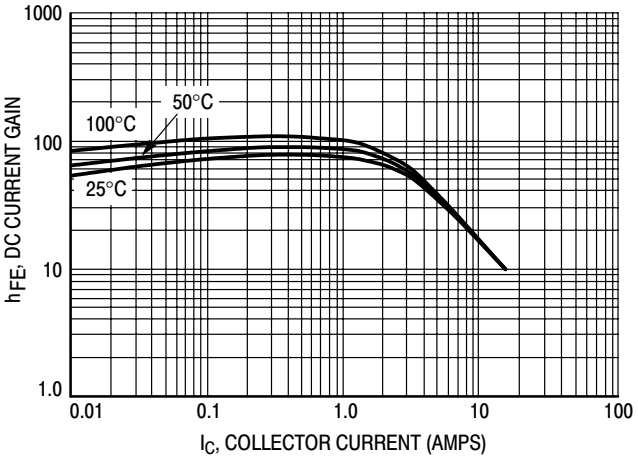


Figure 5. NPN — MJW21192 V_{CE} = 2.0 V DC Current Gain

PNP — MJW21191

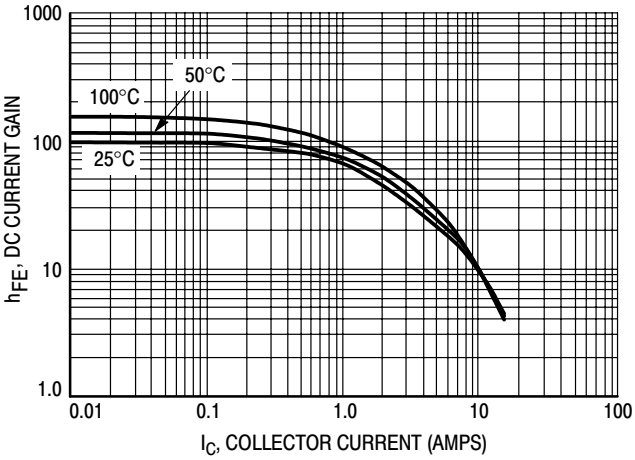


Figure 6. PNP — MJW21191 V_{CE} = 2.0 V DC Current Gain

NPN — MJW21192

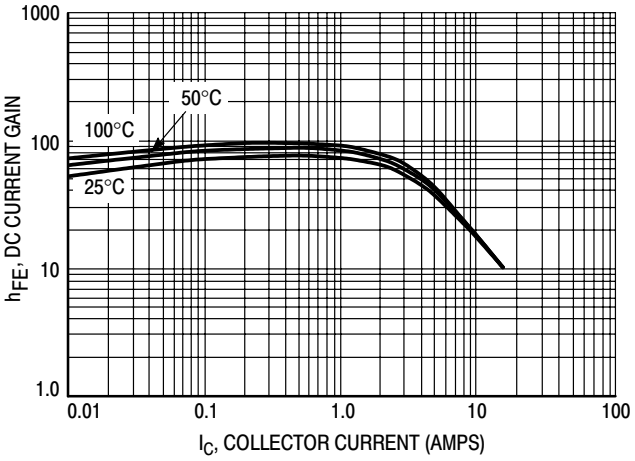


Figure 7. NPN — MJW21192
V_{CE} = 5.0 V DC Current Gain

PNP — MJW21191

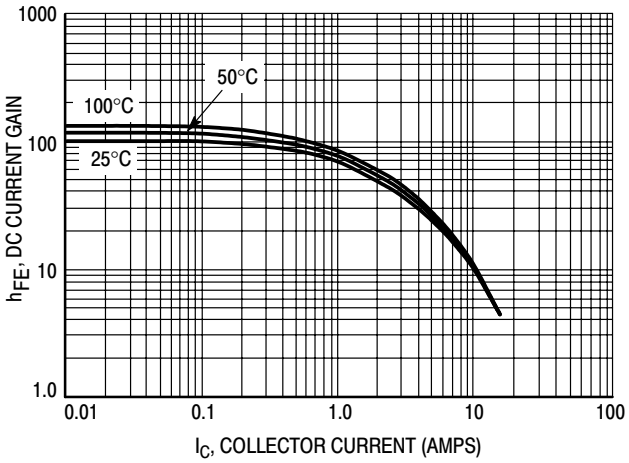


Figure 8. PNP — MJW21191
V_{CE} = 5.0 V DC Current Gain

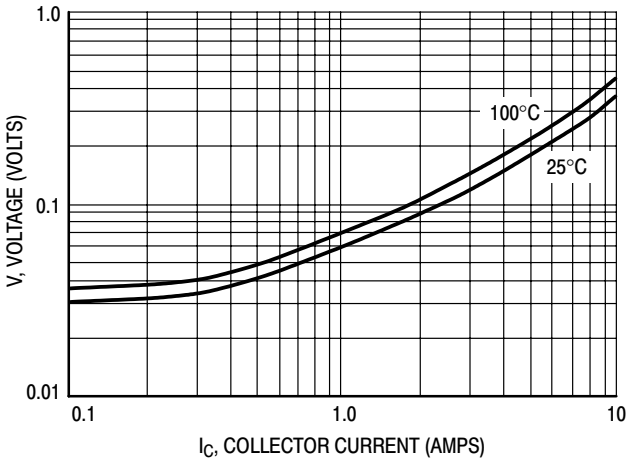


Figure 9. NPN — MJW21192
$V_{CE(sat)}$ I_C/I_B = 5.0

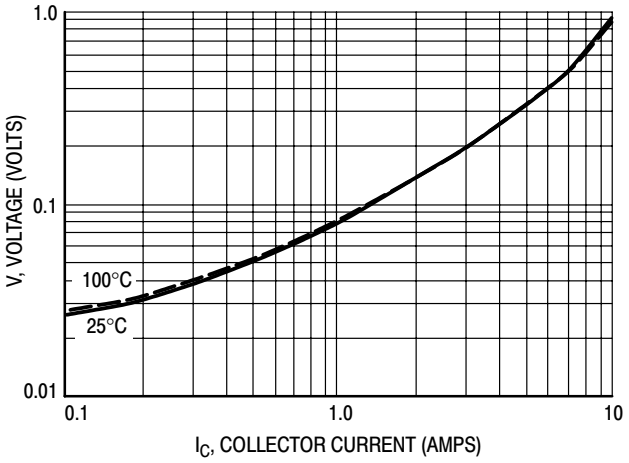


Figure 10. PNP — MJW21191
$V_{CE(sat)}$ I_C/I_B = 5.0

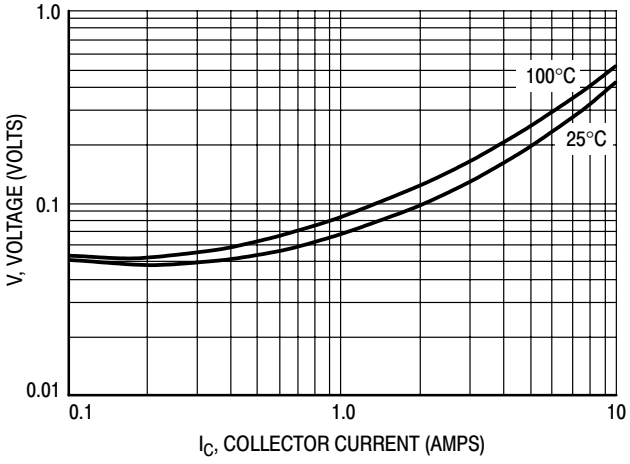


Figure 11. NPN — MJW21192
$V_{CE(sat)}$ I_C/I_B = 10

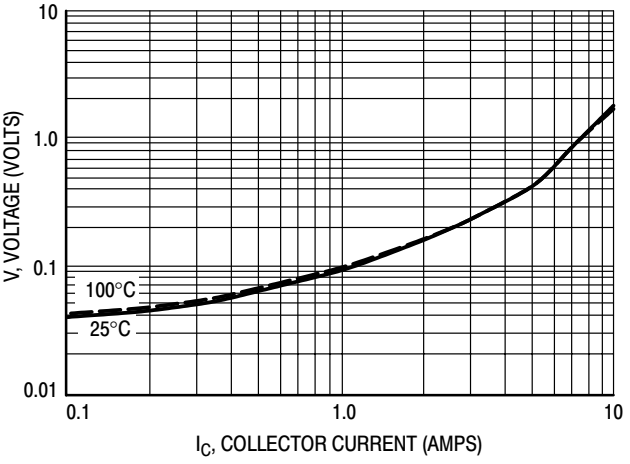


Figure 12. PNP — MJW21191
$V_{CE(sat)}$ I_C/I_B = 10

NPN — MJW21192

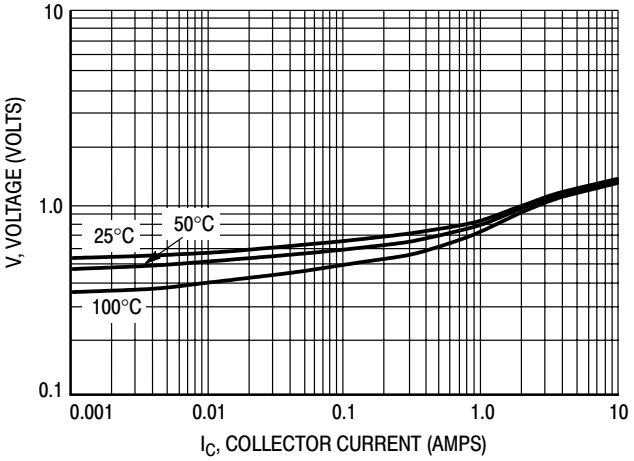


Figure 13. NPN — MJW21192
V_{CE} = 2.0 V $V_{BE(on)}$ Curve

PNP — MJW21191

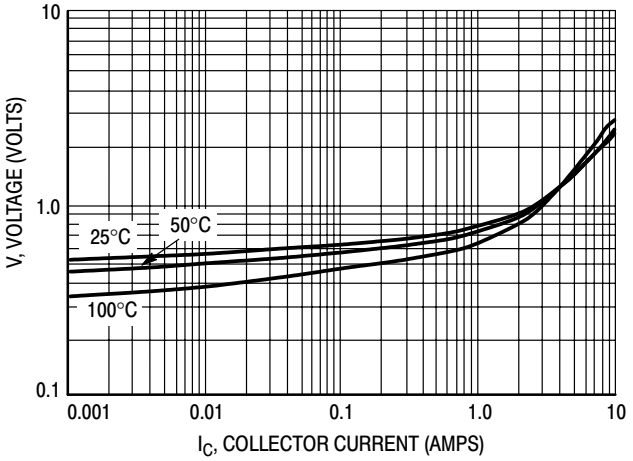


Figure 14. PNP — MJW21191
V_{CE} = 2.0 V $V_{BE(on)}$ Curve

MJW21193 (PNP)
MJW21194 (NPN)

Preferred Devices

Silicon Power Transistors

The MJW21193 and MJW21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –
  h_{FE} = 20 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current – Continuous – Peak (Note 1.)	I_C	16 30	Adc
Base Current – Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

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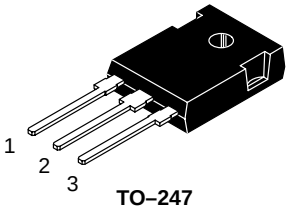
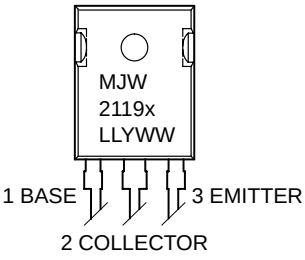
16 AMPERES
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
200 WATTS



TO–247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW2119x = Device Code
x = 3 or 4
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW21193	TO–247	30 Units/Rail
MJW21194	TO–247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	–	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive)		4.0	–	–	
(V_{CE} = 80 Vdc, t = 1 s (non–repetitive)		2.25	–	–	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 8 Adc, V_{CE} = 5 Vdc)		20	–	60	
(I_C = 16 Adc, I_B = 5 Adc)		8	–	–	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	–	–	2.2	Vdc
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)		–	–	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)		–	–	4	
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output	T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched		–	0.8	–	
(Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched		–	0.08	–	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	–	500	pF

PNP MJW21193

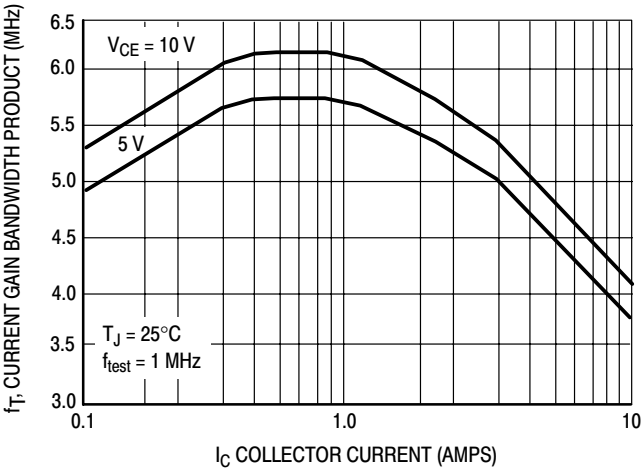


Figure 1. Typical Current Gain Bandwidth Product

NPN MJW21194

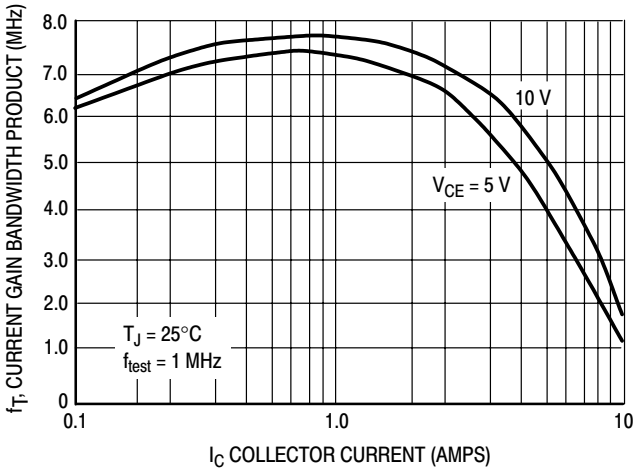


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW21193

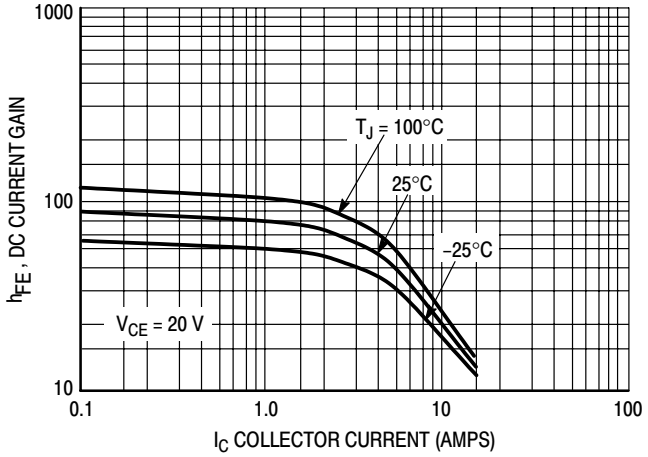


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJW21194

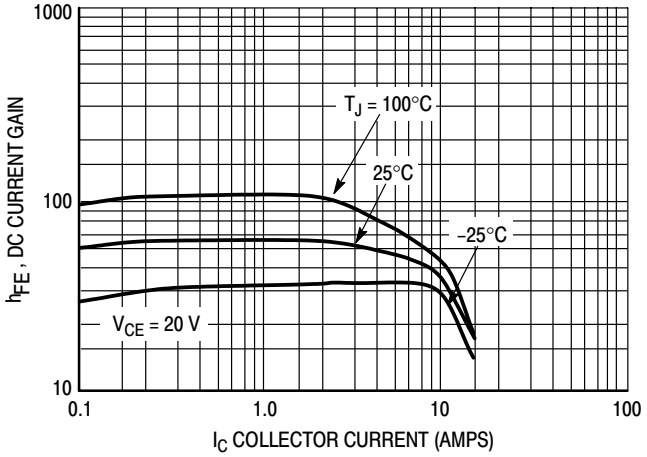


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJW21193

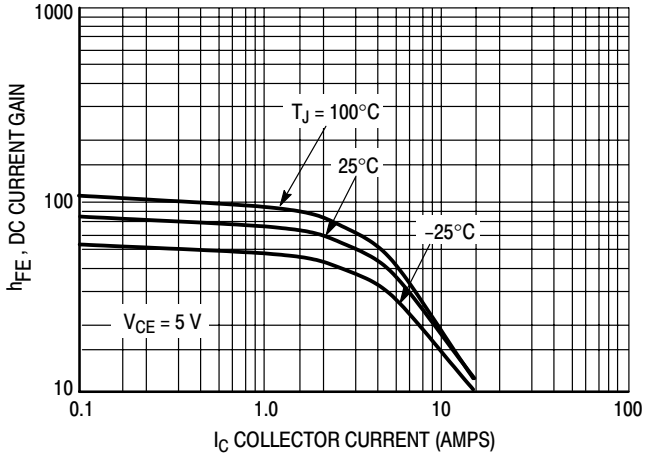


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJW21194

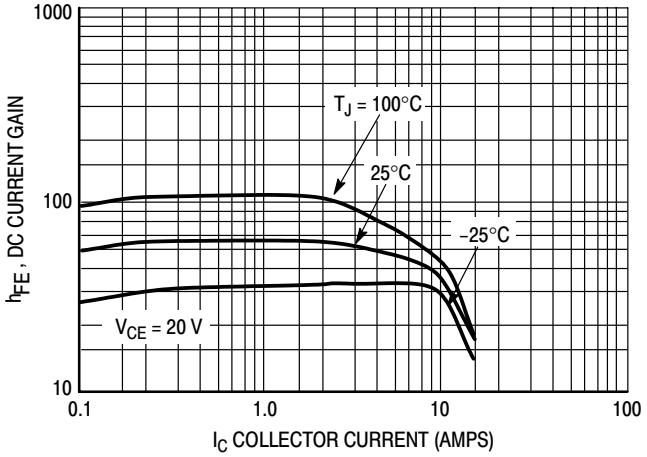


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJW21193

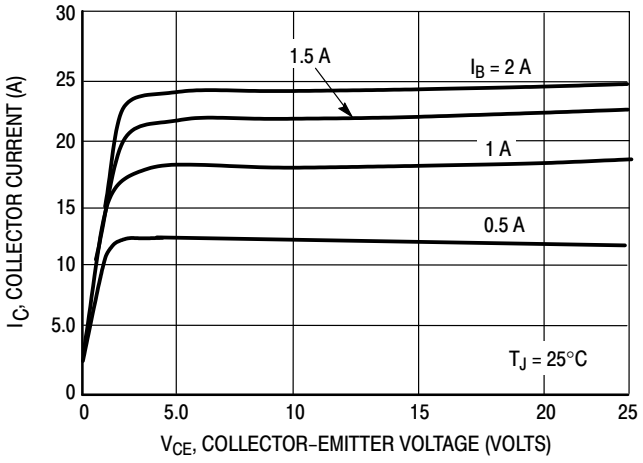


Figure 7. Typical Output Characteristics

NPN MJW21194

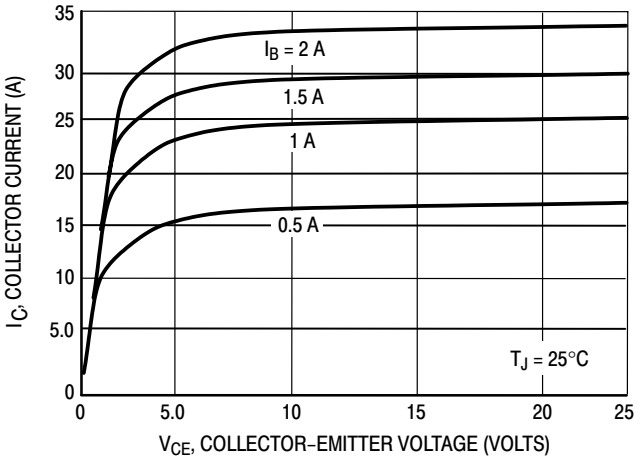


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW21193

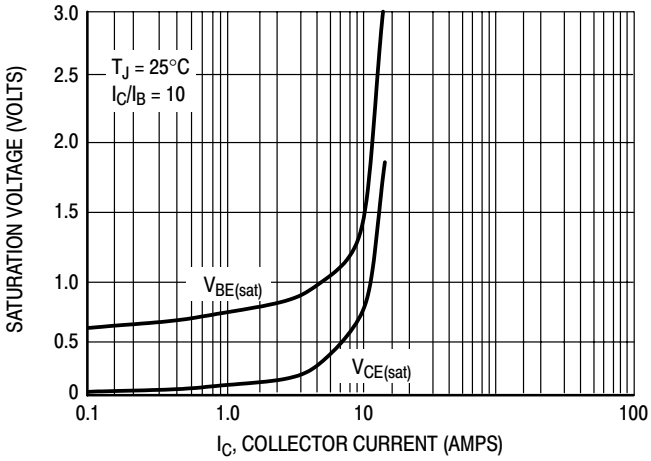


Figure 9. Typical Saturation Voltages

NPN MJW21194

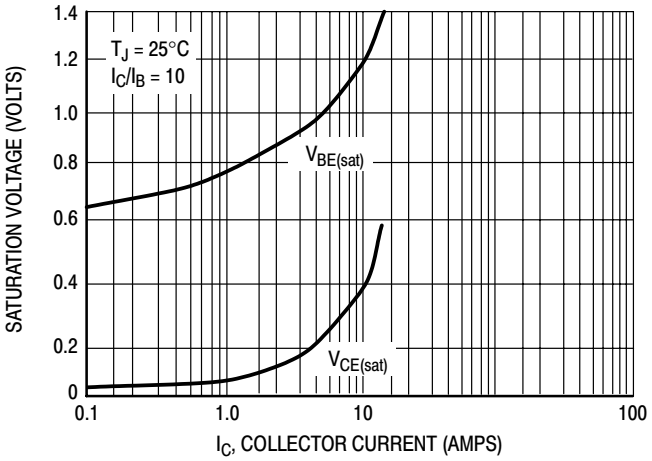


Figure 10. Typical Saturation Voltages

PNP MJW21193

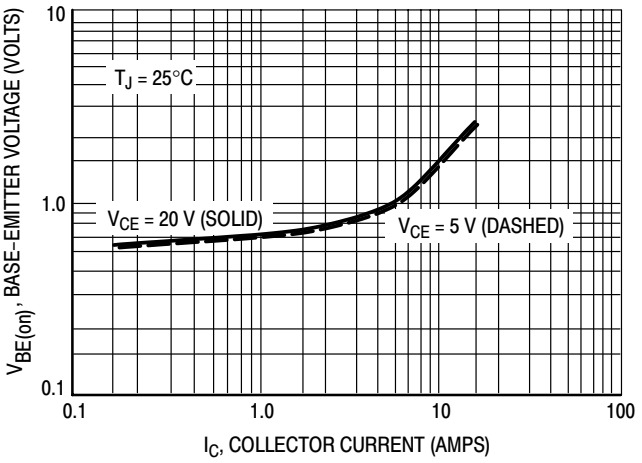


Figure 11. Typical Base−Emitter Voltage

NPN MJW21194

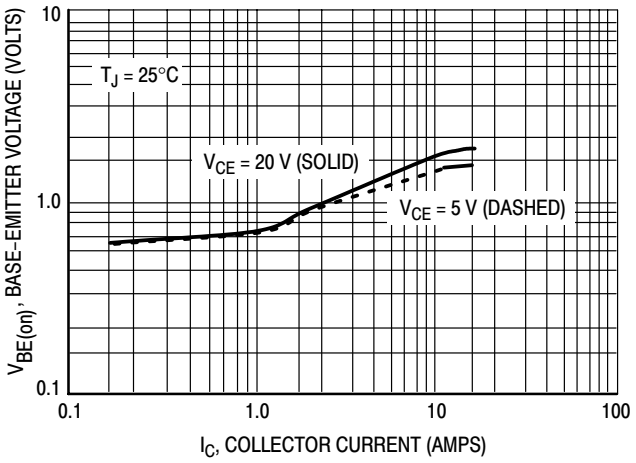


Figure 12. Typical Base−Emitter Voltage

PNP MJW21193

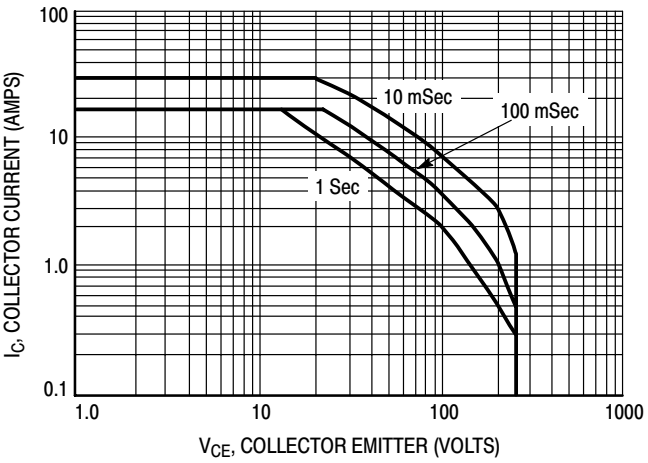


Figure 13. Active Region Safe Operating Area

NPN MJW21194

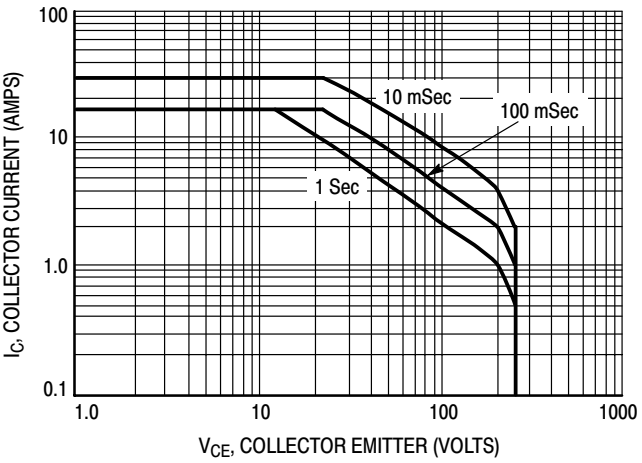


Figure 14. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

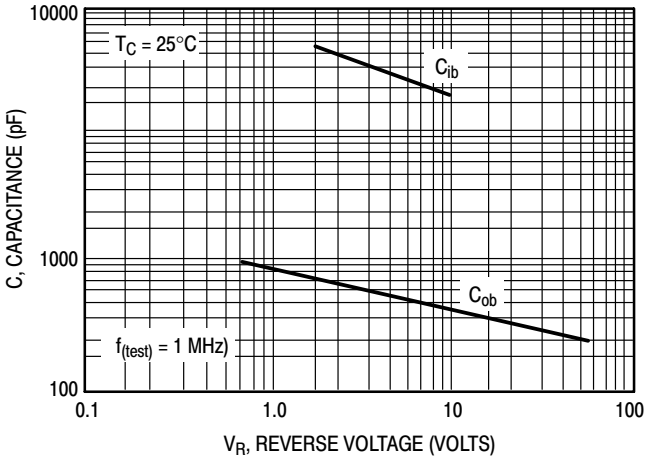


Figure 15. MJW21193 Typical Capacitance

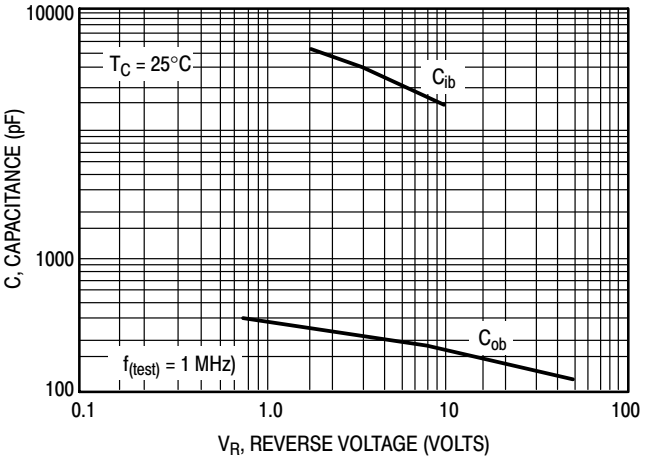


Figure 16. MJW21194 Typical Capacitance

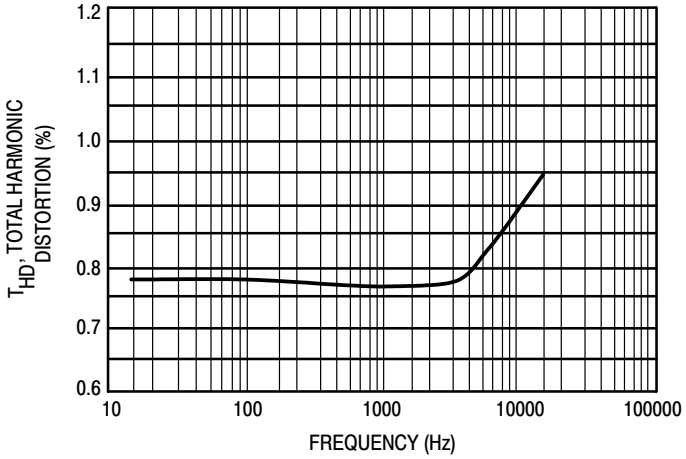


Figure 17. Typical Total Harmonic Distortion

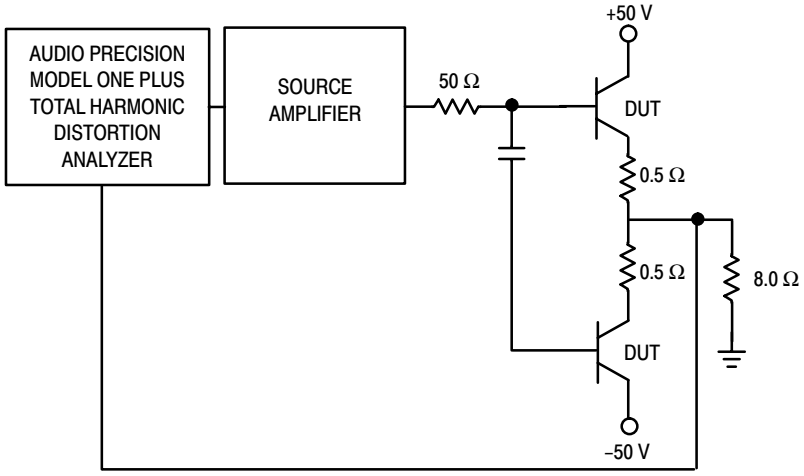


Figure 18. Total Harmonic Distortion Test Circuit

MJW21195 (PNP)
MJW21196 (NPN)

Preferred Devices

Silicon Power Transistors

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- High DC Current Gain – h_{FE} = 20 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current – Continuous – Peak (Note 1.)	I_C	16 30	Adc
Base Current – Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

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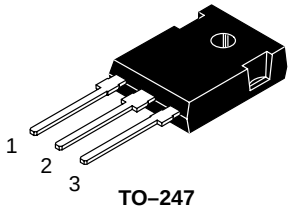
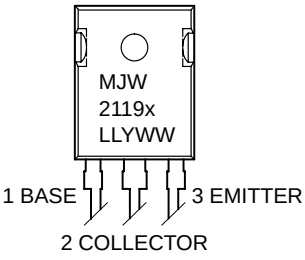
16 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



TO–247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW2119x = Device Code
x = 5 or 6
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW21195	TO–247	30 Units/Rail
MJW21196	TO–247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	50	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	–	50	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non–repetitive) (V_{CE} = 80 Vdc, t = 1 s (non–repetitive)	$I_{S/b}$	 4.0 2.25	 – –	 – –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, I_B = 5 Adc)	h_{FE}	 20 8	 – –	 80 –	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	–	–	2.0	Vdc
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 – –	 – –	 1.0 3	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 – –	 0.8 0.08	 – –	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	–	500	pF

PNP MJW21195

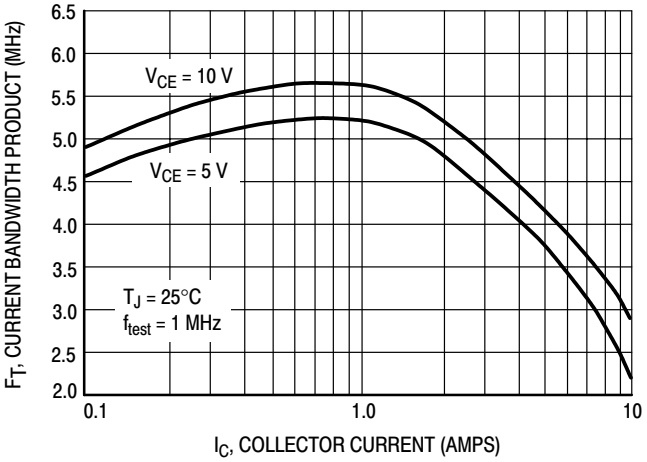


Figure 1. Typical Current Gain Bandwidth Product

NPN MJW21196

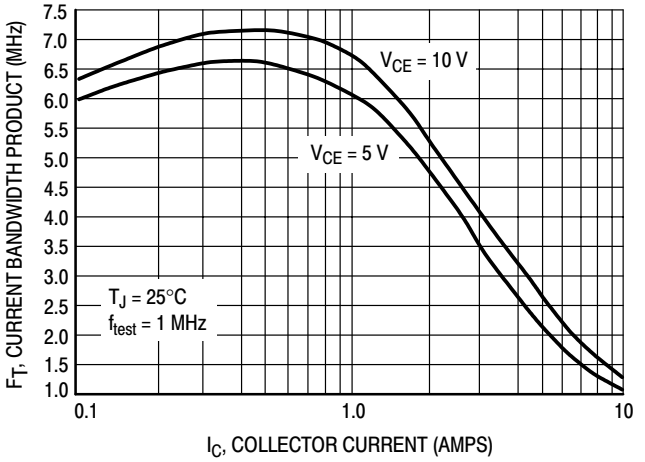


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW21195

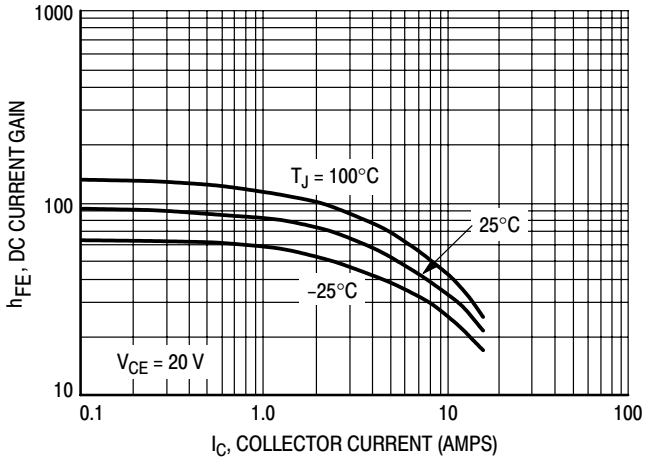


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJW21196

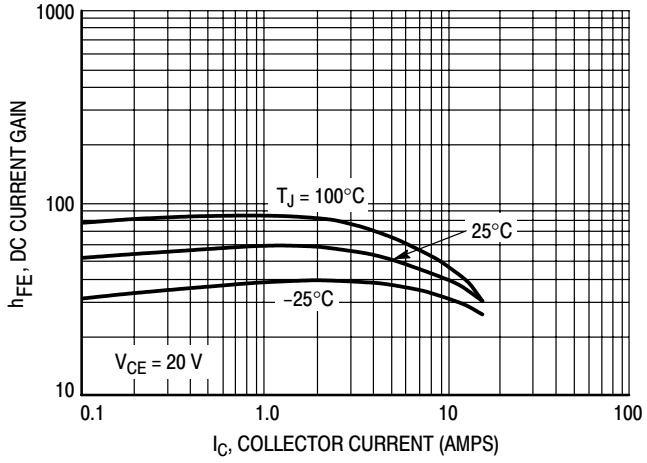


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJW21195

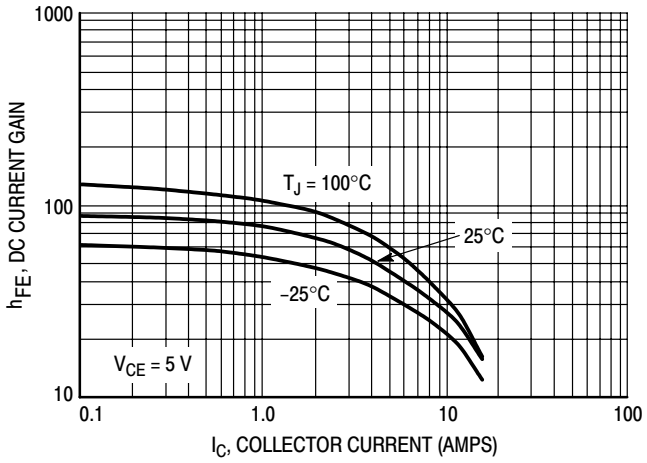


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJW21196

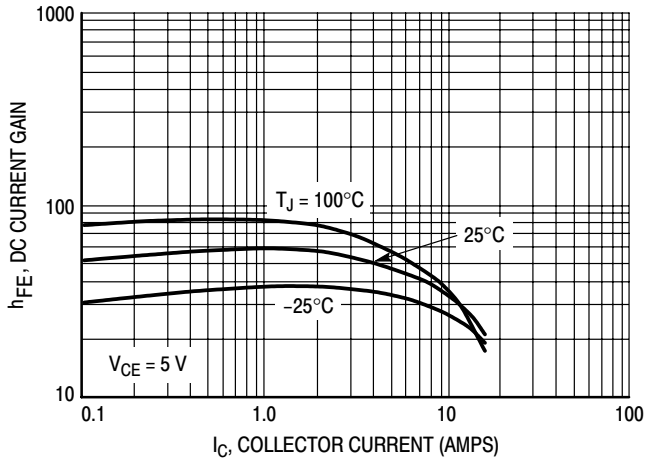


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJW21195

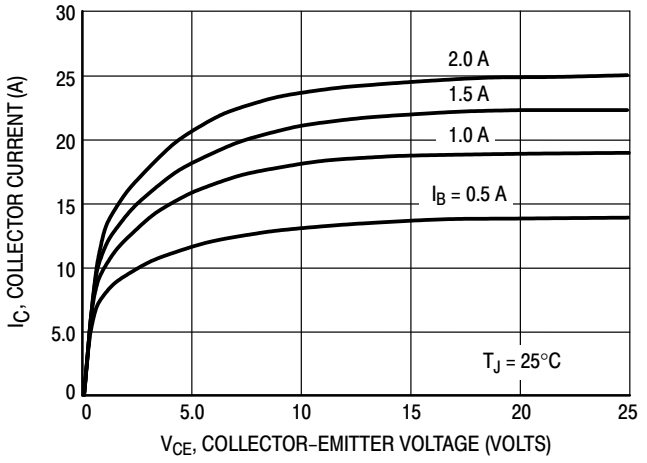


Figure 7. Typical Output Characteristics

NPN MJW21196

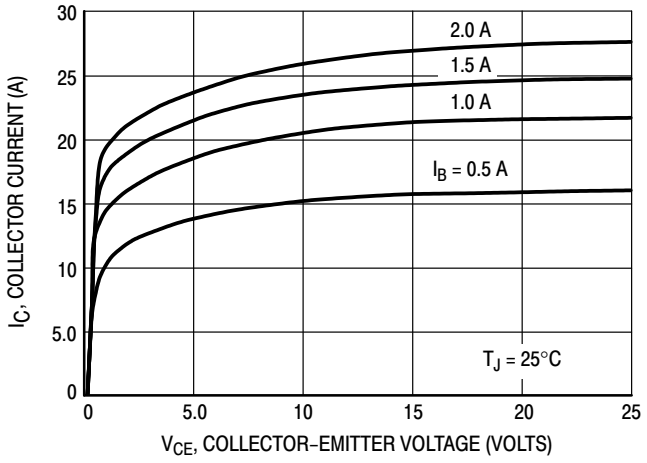


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW21195

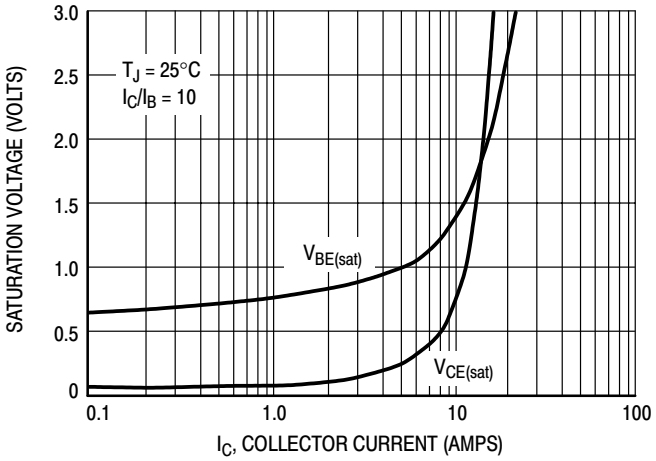


Figure 9. Typical Saturation Voltages

NPN MJW21196

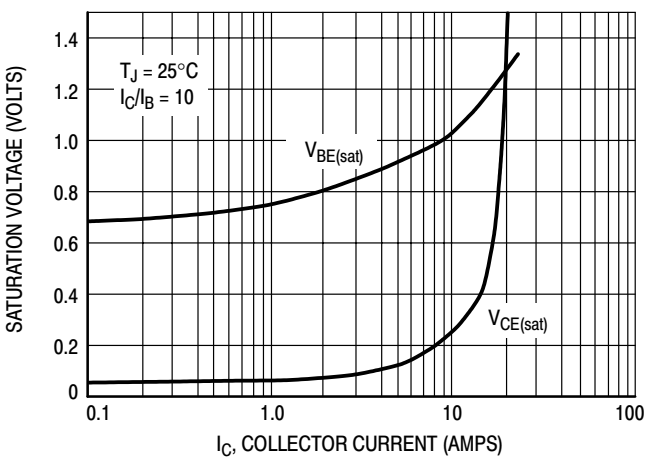


Figure 10. Typical Saturation Voltages

PNP MJW21195

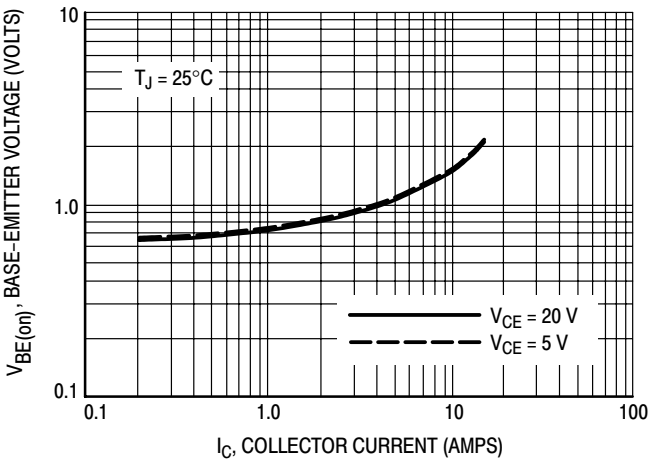


Figure 11. Typical Base–Emitter Voltage

NPN MJW21196

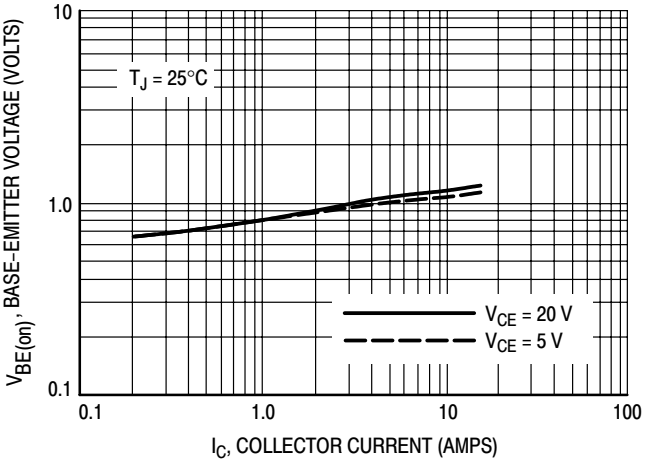


Figure 12. Typical Base–Emitter Voltage

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

PNP MJW21195

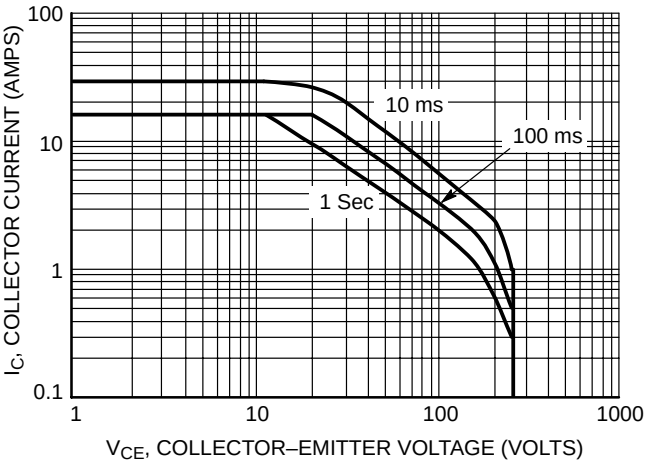


Figure 13. Active Region Safe Operating Area

NPN MJW21196

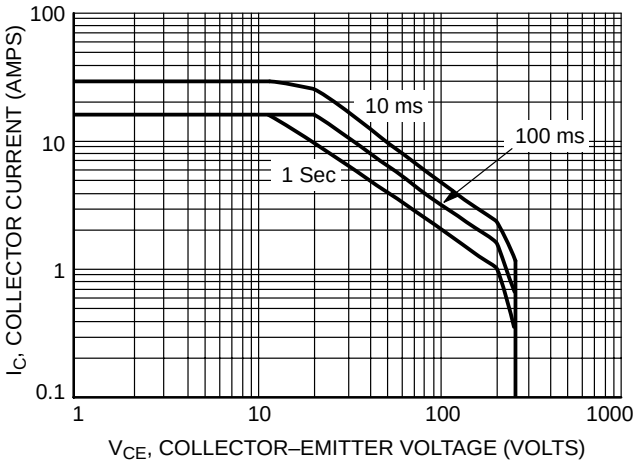


Figure 14. Active Region Safe Operating Area

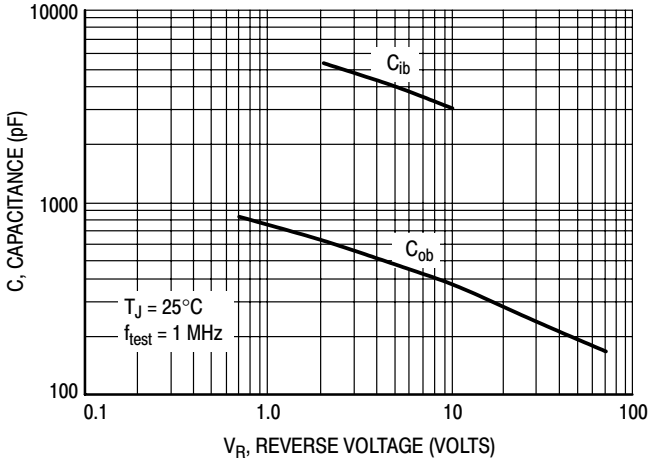


Figure 15. MJW21195 Typical Capacitance

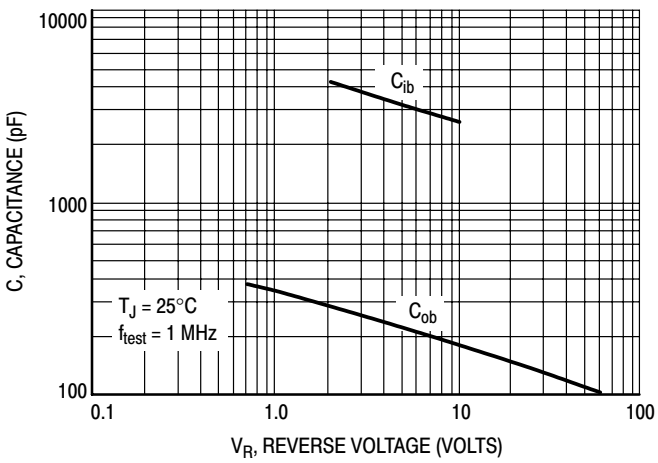


Figure 16. MJW21196 Typical Capacitance

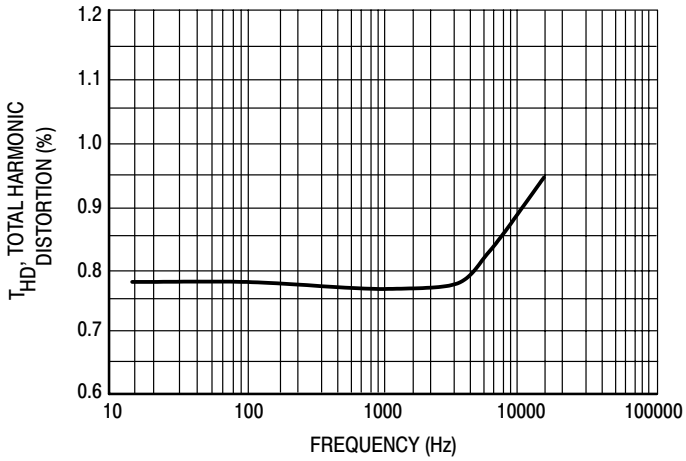


Figure 17. Typical Total Harmonic Distortion

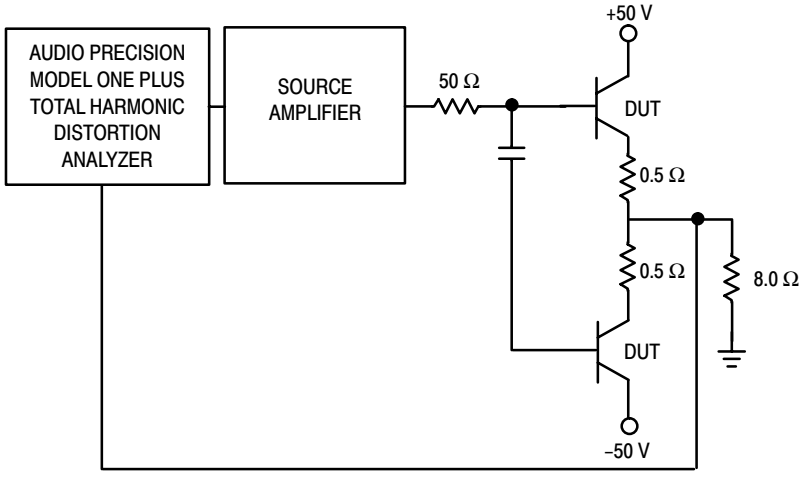


Figure 18. Total Harmonic Distortion Test Circuit

MJW3281A (NPN)
MJW1302A (PNP)

Preferred Devices

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJW3281A and MJW1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  Gain Linearity from 100 mA to 7 A
  h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area – 1 A/100 V @ 1 Second
- High f_T – 30 MHz Typical

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	230	Vdc
Collector–Base Voltage	V_{CBO}	230	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	230	Vdc
Collector Current – Continuous – Peak (Note 1.)	I_C	15 25	Adc
Base Current – Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

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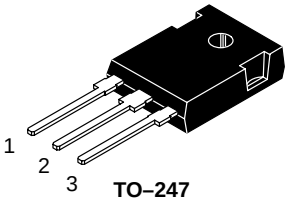
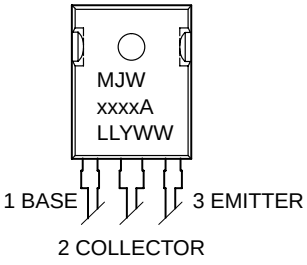
15 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 230 VOLTS 200 WATTS



TO–247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJWxxxxA = Device Code
xxxx = 3281 OR 1302
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW3281A	TO–247	30 Units/Rail
MJW1302A	TO–247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	230	–	–	Vdc
Collector Cutoff Current (V_{CB} = 230 Vdc, I_E = 0)	I_{CBO}	–	–	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	5	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non–repetitive) (V_{CE} = 100 Vdc, t = 1 s (non–repetitive)	$I_{S/b}$	4 1	– –	– –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc) (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 7 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	 50 50 50 50 50 45 12	 125 – – – 115 – 35	 200 200 200 200 200 – –	–
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	–	0.4	2	Vdc
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	–	–	2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	–	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	–	600	pF

PNP MJW1302A

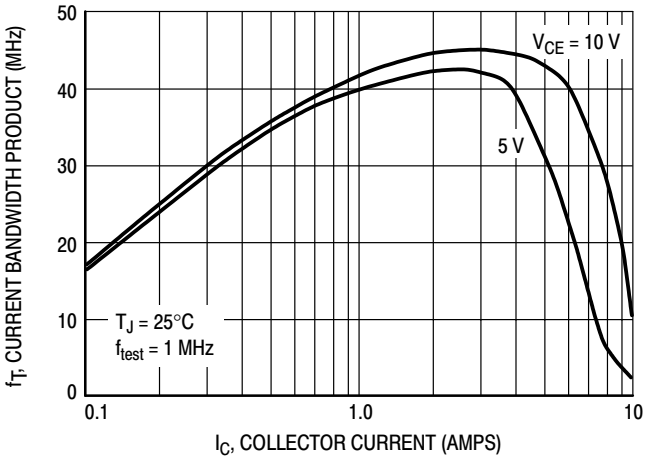


Figure 19. Typical Current Gain Bandwidth Product

NPN MJW3281A

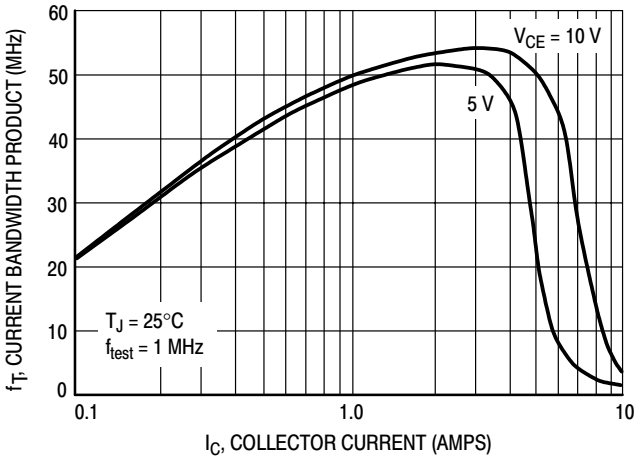


Figure 20. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW1302A

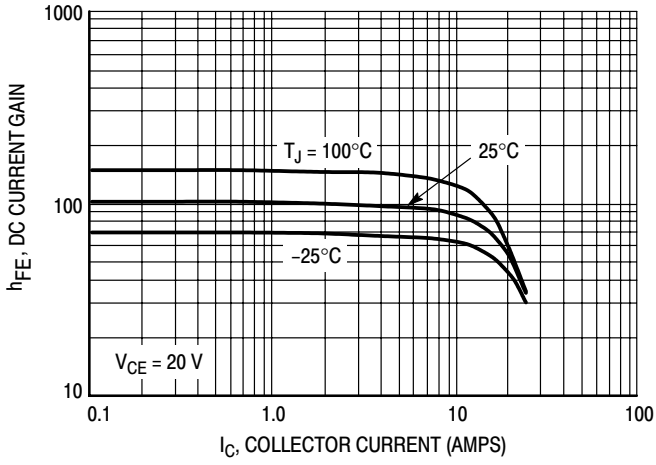


Figure 21. DC Current Gain, V_{CE} = 20 V

NPN MJW3281A

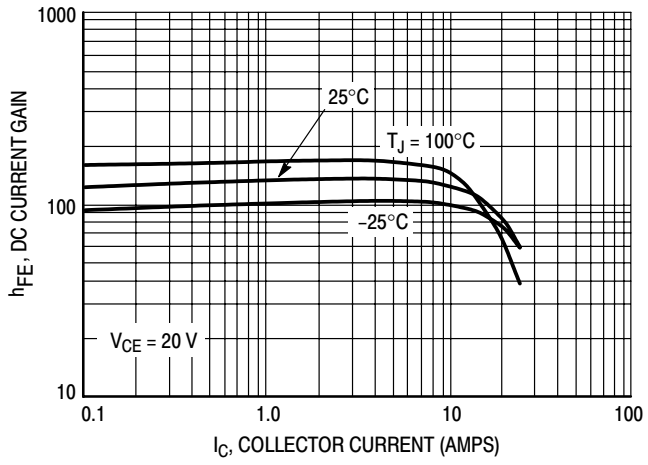


Figure 22. DC Current Gain, V_{CE} = 20 V

PNP MJW1302A

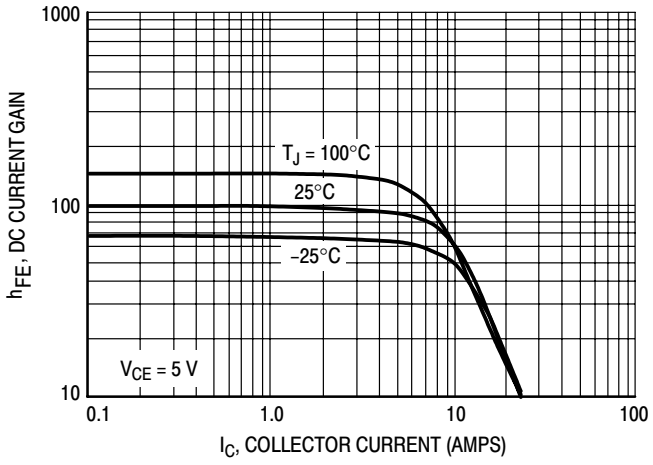


Figure 23. DC Current Gain, V_{CE} = 5 V

NPN MJW3281A

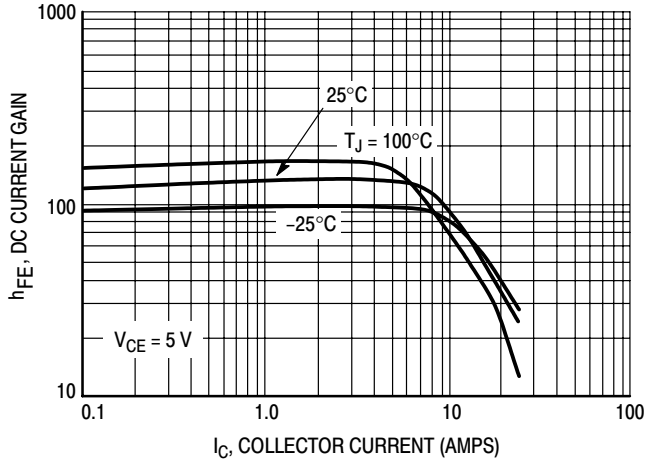


Figure 24. DC Current Gain, V_{CE} = 5 V

PNP MJW1302A

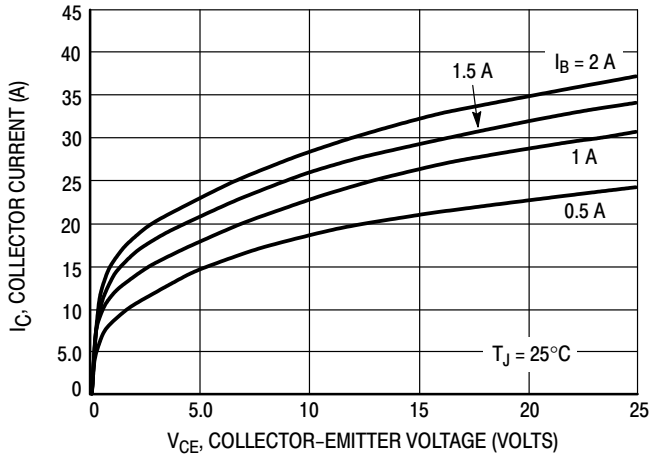


Figure 25. Typical Output Characteristics

NPN MJW3281A

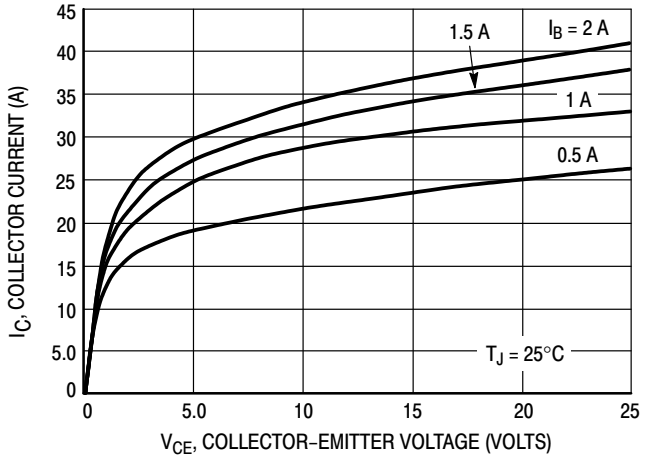


Figure 26. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW1302A

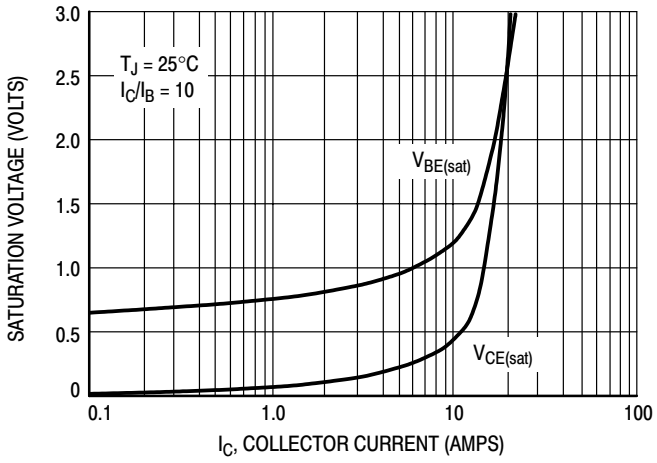


Figure 27. Typical Saturation Voltages

NPN MJW3281A

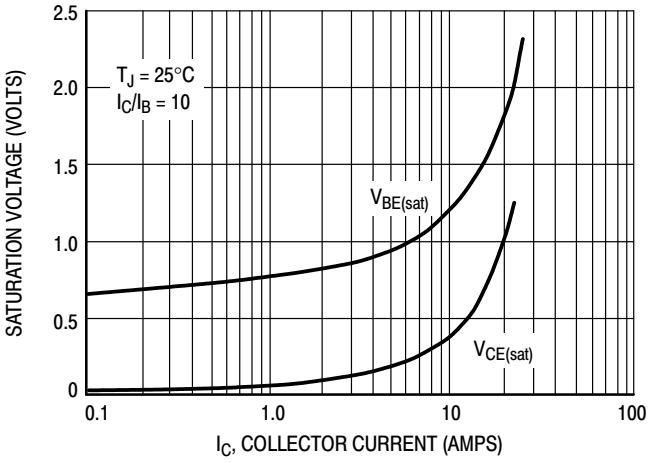


Figure 28. Typical Saturation Voltages

PNP MJW1302A

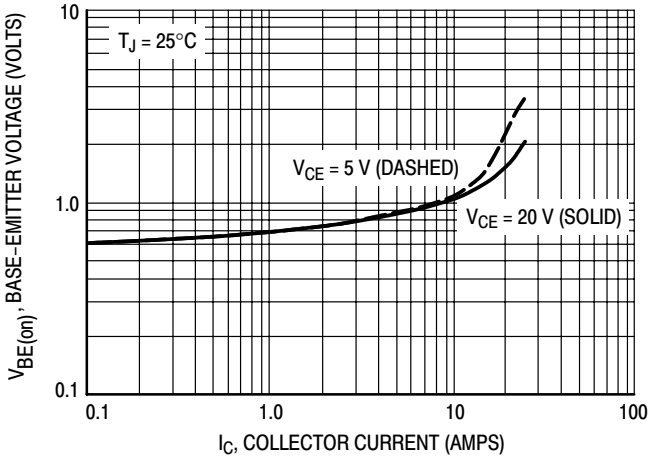


Figure 29. Typical Base−Emitter Voltage

NPN MJW3281A

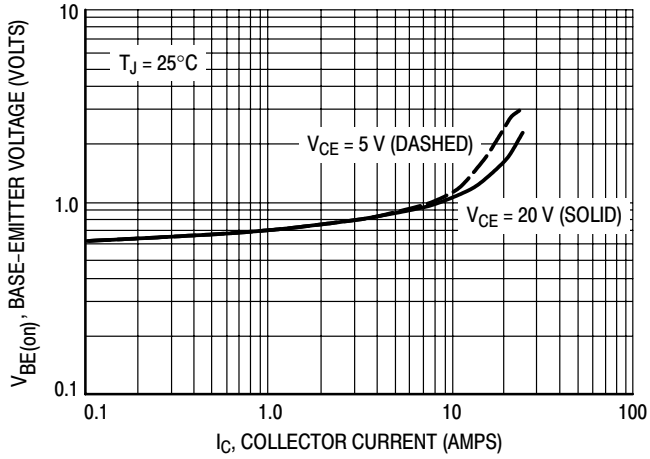


Figure 30. Typical Base−Emitter Voltage

PNP MJW1302A

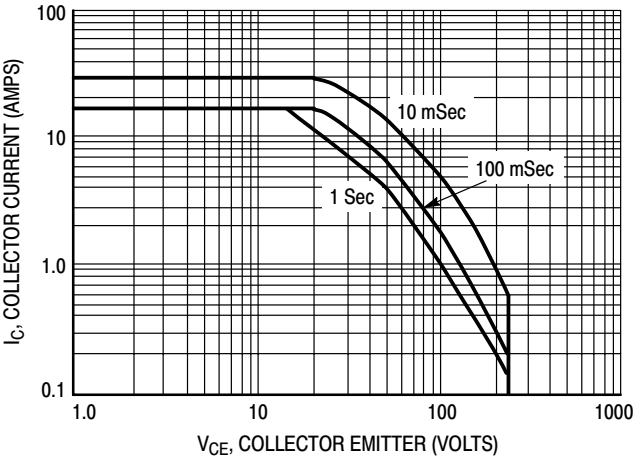


Figure 31. Active Region Safe Operating Area

NPN MJW3281A

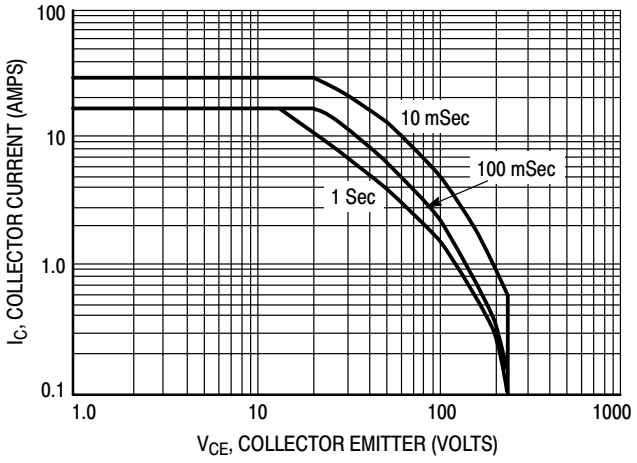


Figure 32. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 31 and 32 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

PNP MJW1302A

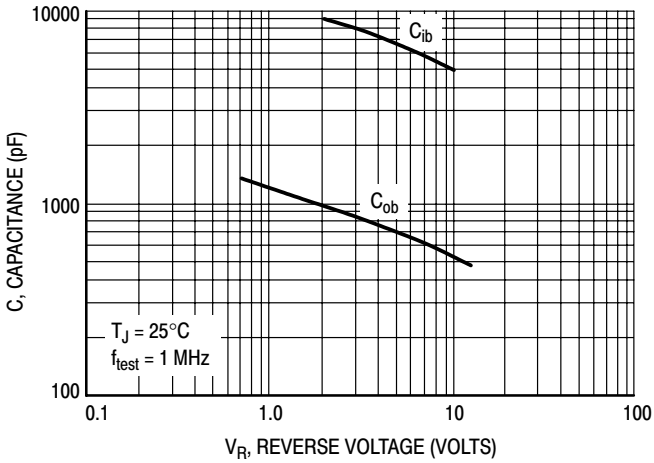


Figure 33. MJW1302A Typical Capacitance

NPN MJW3281A

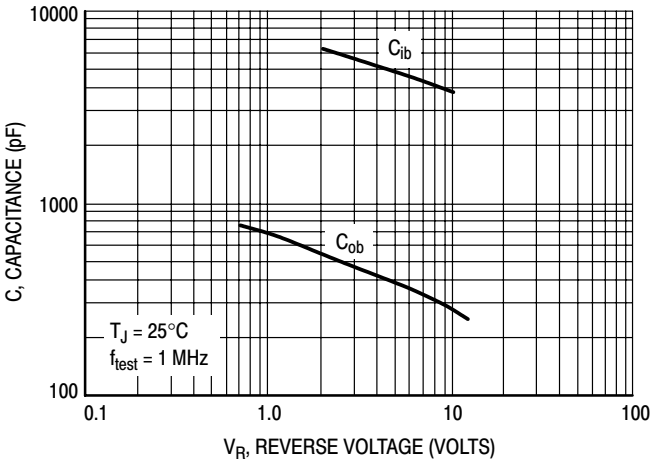


Figure 34. MJW3281A Typical Capacitance

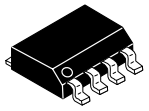
MMDJ3N03BJT

ON Semiconductor Preferred Device

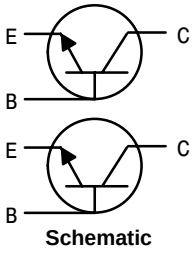
Plastic Power Transistors
SO–8 for Surface Mount Applications

- Collector –Emitter Sustaining Voltage — $V_{CEO(sus)}$
  = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE}= 85 (Min) @ I_C = 0.8 Adc
  = 60 (Min) @ I_C = 3.0 Adc
- Low Collector –Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.18 Vdc (Max) @ I_C = 1.2 Adc
  = 0.45 Vdc (Max) @ I_C = 3.0 Adc
- Miniature SO–8 Surface Mount Package – Saves Board Space

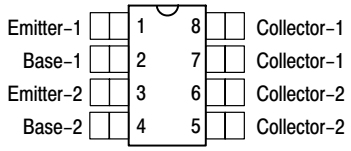
DUAL BIPOLAR POWER TRANSISTOR NPN SILICON 30 VOLTS 3 AMPERES



CASE 751–07, Style 16 (SO–8)



Schematic



Top View
Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	45	Vdc
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Emitter–Base Voltage	V_{EB}	±6.0	Vdc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Base Current — Continuous	I_B	1.0	Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Ambient on 1″ sq. (645 sq. mm) Collector pad on FR–4 board material with one die operating. Thermal Resistance – Junction to Ambient on 0.012″ sq. (7.6 sq. mm) Collector pad on FR–4 board material with one die operating.	$R_{\theta JA}$	 100 185	°C/W
Total Power Dissipation @ T_A = 25°C mounted on 1″ sq. (645 sq. mm) Collector pad on FR–4 board material with one die operating. Derate above 25°C	P_D	 1.25 10	 Watts mW/°C
Maximum Temperature for Soldering	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 4
Publication Order Number:
MMDJ3N03BJT/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter–Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω)	I_{CER}	—	—	20	μAdc
(V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)		—	—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS(1)					
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	0.105	0.15	Vdc
(I_C = 1.2 Adc, I_B = 20 mAdc)		—	—	0.18	
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	—	0.45	
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	85	195	—	—
(I_C = 1.2 Adc, V_{CE} = 1.0 Vdc)		80	—	—	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		60	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	85	135	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	200	—	pF
Current–Gain — Bandwidth Product(2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, F_{test} = 1.0 MHz)	f_T	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{FE}| \cdot f_{test}$

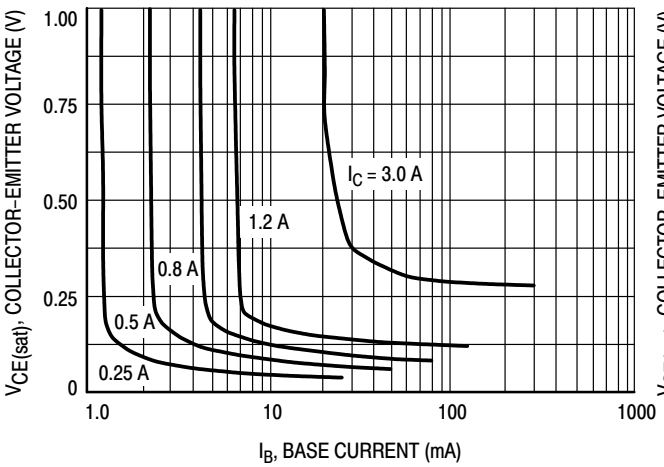


Figure 1. Collector Saturation Region

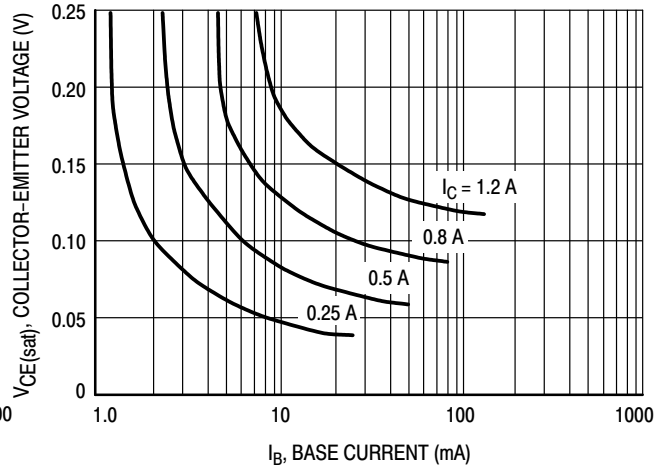


Figure 2. Collector Saturation Region

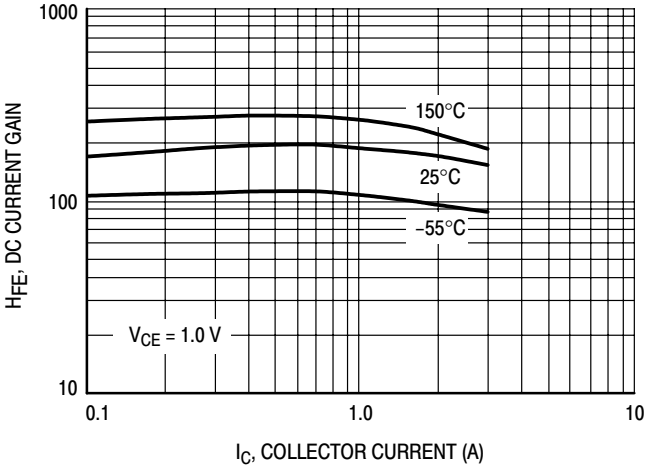


Figure 3. DC Current Gain

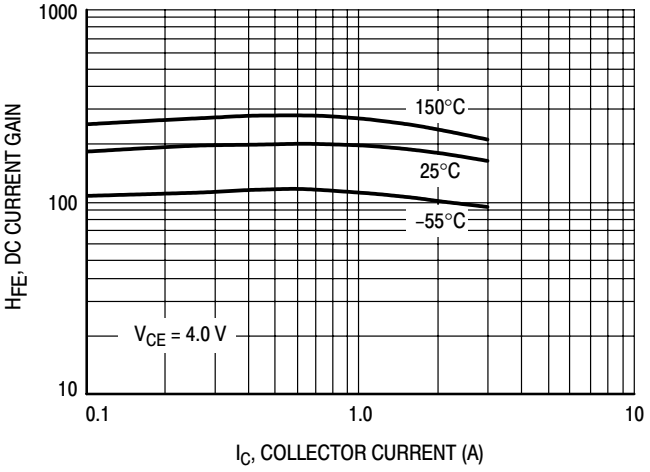


Figure 4. DC Current Gain

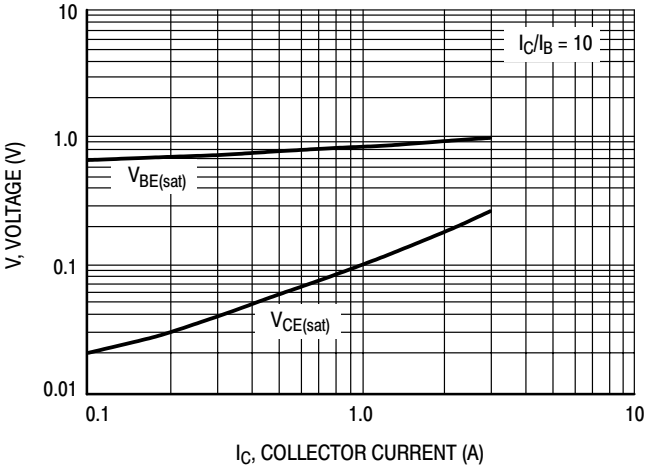


Figure 5. “On” Voltages

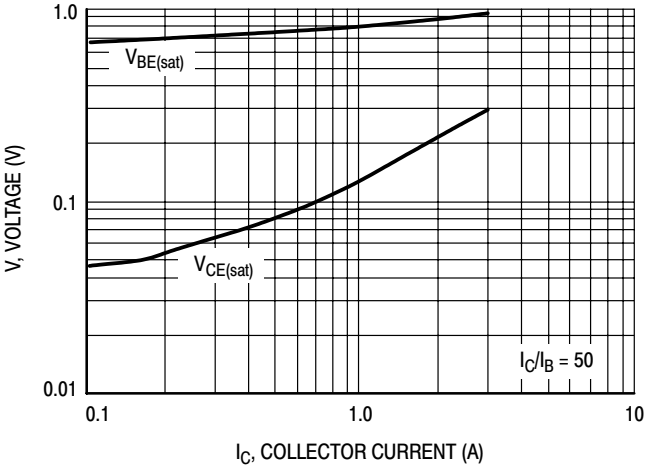


Figure 6. “On” Voltages

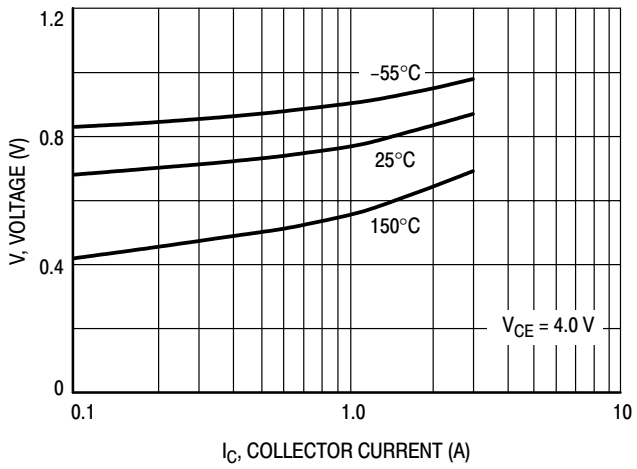


Figure 7. $V_{BE(on)}$ Voltage

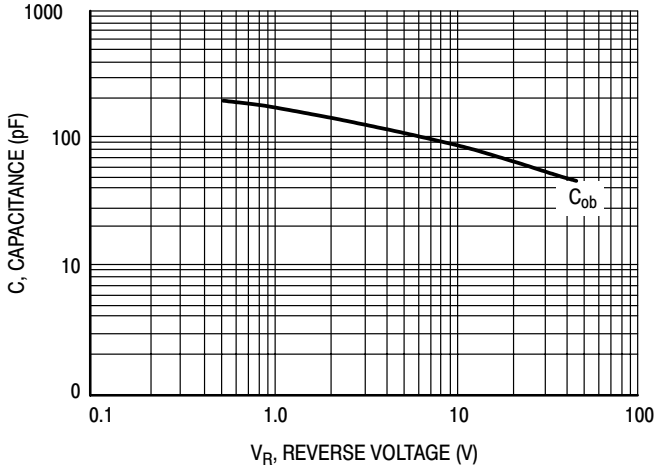


Figure 8. Capacitance

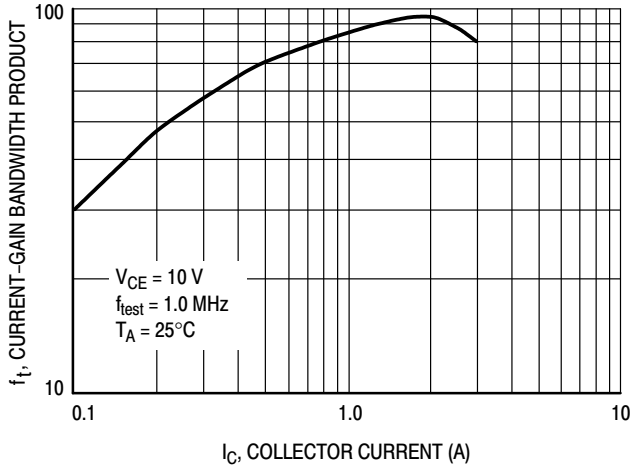


Figure 9. Current–Gain Bandwidth Product

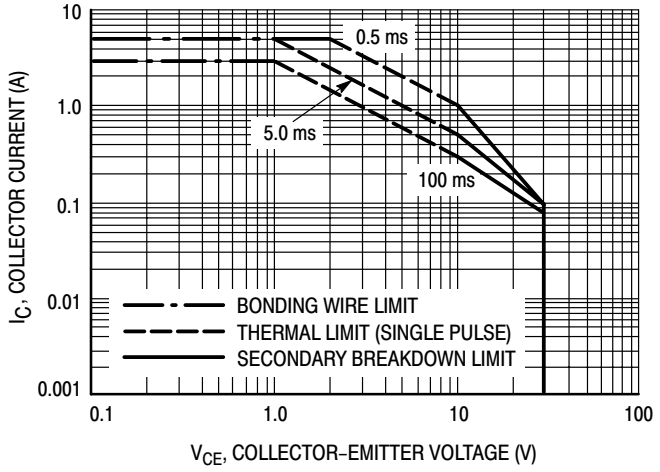


Figure 10. Active Region Safe Operating Area

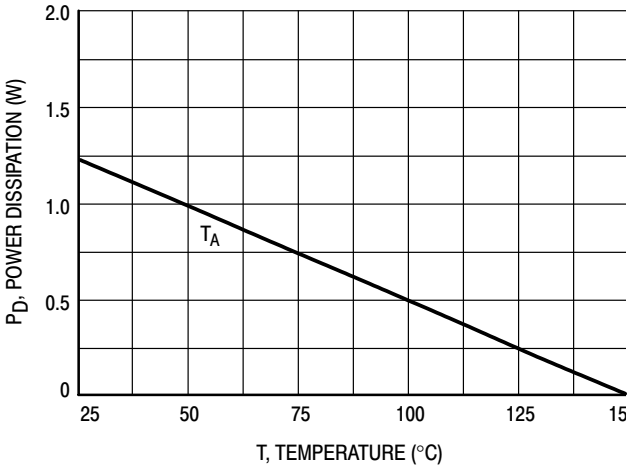


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

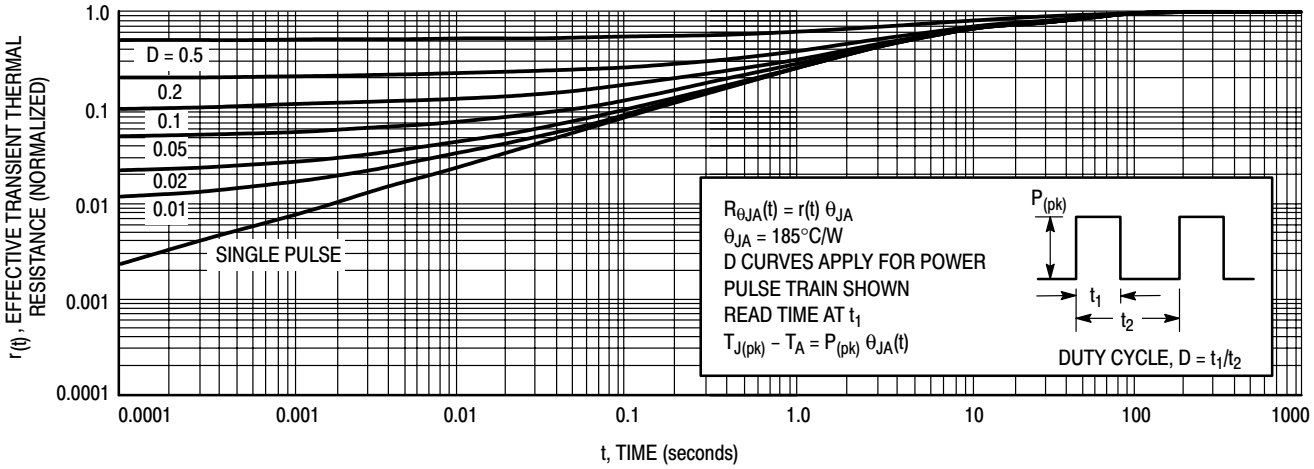


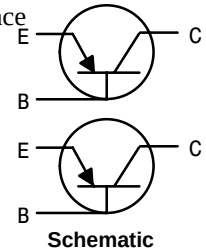
Figure 12. Thermal Response

MMDJ3P03BJT

ON Semiconductor Preferred Device

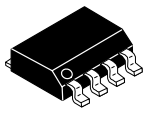
Plastic Power Transistors
SO–8 for Surface Mount Applications

- Collector –Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 125 (Min) @ I_C = 0.8 Adc
  = 90 (Min) @ I_C = 3.0 Adc
- Low Collector –Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.24 Vdc (Max) @ I_C = 1.2 Adc
  = 0.55 Vdc (Max) @ I_C = 3.0 Adc
- Miniature SO–8 Surface Mount Package – Saves Board Space

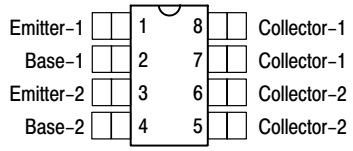


Schematic

DUAL BIPOLAR POWER TRANSISTOR PNP SILICON 30 VOLTS 3 AMPERES



CASE 751–07, Style 16 (SO–8)



Top View
Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	45	Vdc
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Emitter–Base Voltage	V_{EB}	±6.0	Vdc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Base Current — Continuous	I_B	1.0	Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Ambient on 1″ sq. (645 sq. mm) Collector pad on FR–4 board material with one die operating. Thermal Resistance – Junction to Ambient on 0.012″ sq. (7.6 sq. mm) Collector pad on FR–4 board material with one die operating.	$R_{\theta JA}$	 100 185	°C/W
Total Power Dissipation @ T_A = 25°C mounted on 1″ sq. (645 sq. mm) Collector pad on FR–4 board material with one die operating. Derate above 25°C	P_D	 1.25 10	 Watts mW/°C
Maximum Temperature for Soldering	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 4
Publication Order Number:
MMDJ3P03BJT/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter–Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω)	I_{CER}	—	—	20	μAdc
(V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)		—	—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS(1)					
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	0.15	0.21	Vdc
(I_C = 1.2 Adc, I_B = 20 mAdc)		—	—	0.24	
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	—	0.55	
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	125	260	—	—
(I_C = 1.2 Adc, V_{CE} = 1.0 Vdc)		110	—	—	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		90	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	100	150	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	135	—	pF
Current–Gain — Bandwidth Product(2) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T	—	110	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{FE}| \bullet f_{test}$

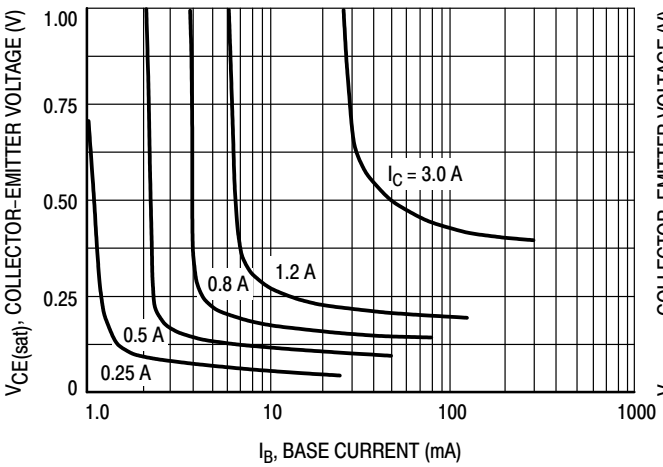


Figure 1. Collector Saturation Region

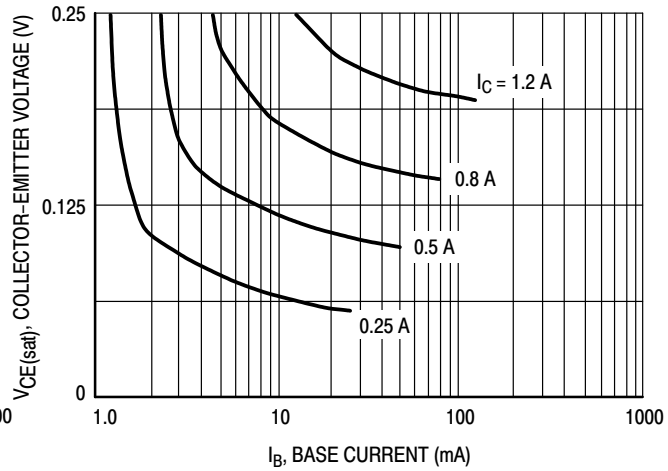


Figure 2. Collector Saturation Region

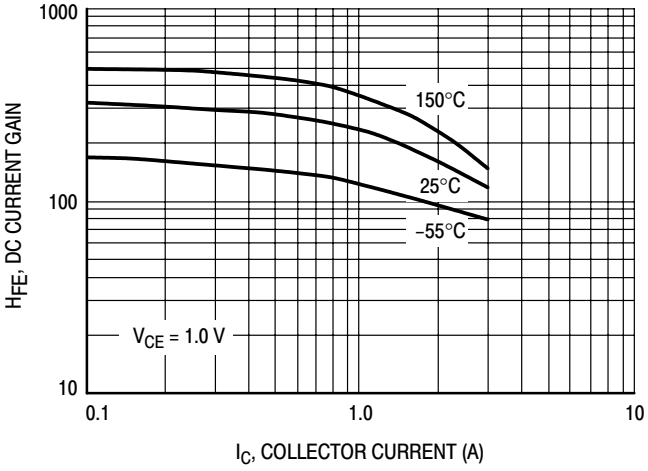


Figure 3. DC Current Gain

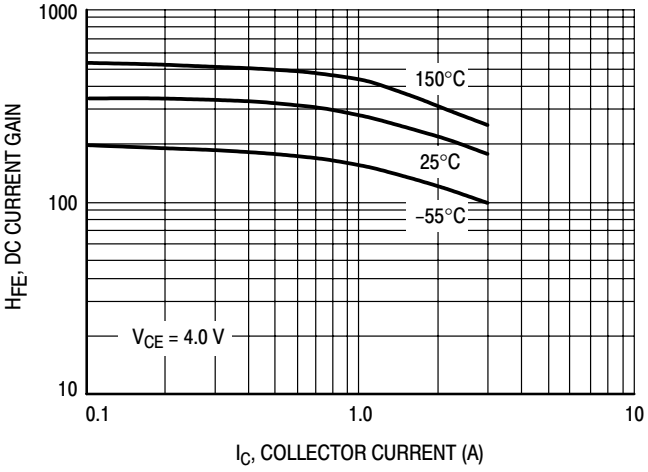


Figure 4. DC Current Gain

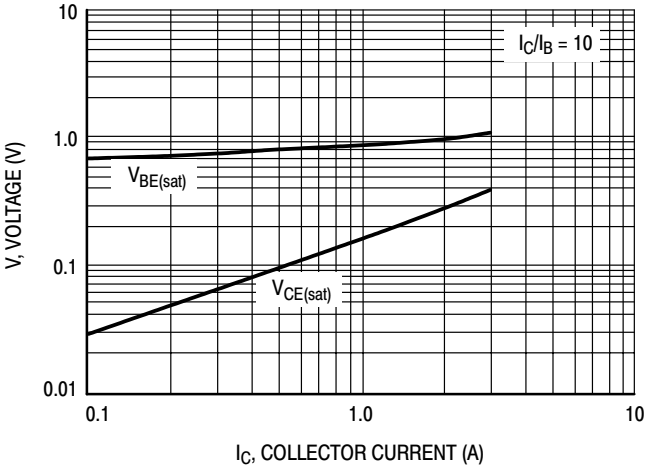


Figure 5. “On” Voltages

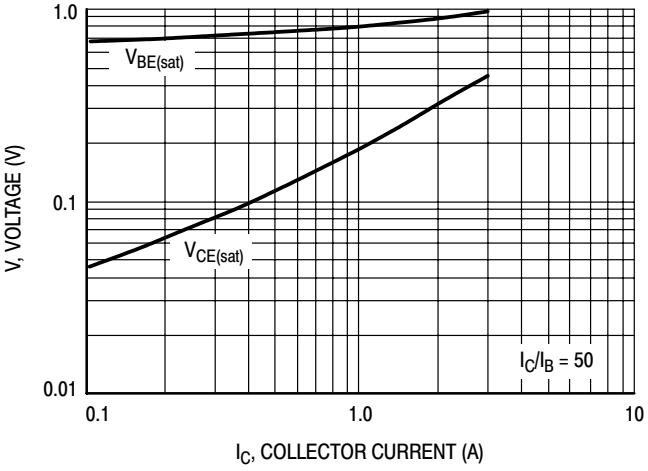


Figure 6. “On” Voltages

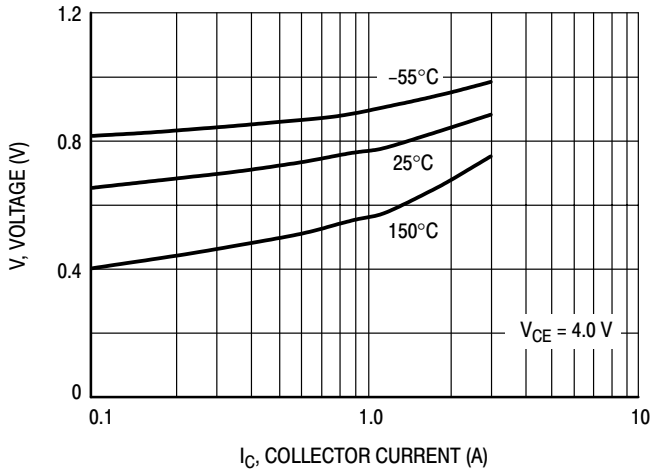


Figure 7. $V_{BE(on)}$ Voltage

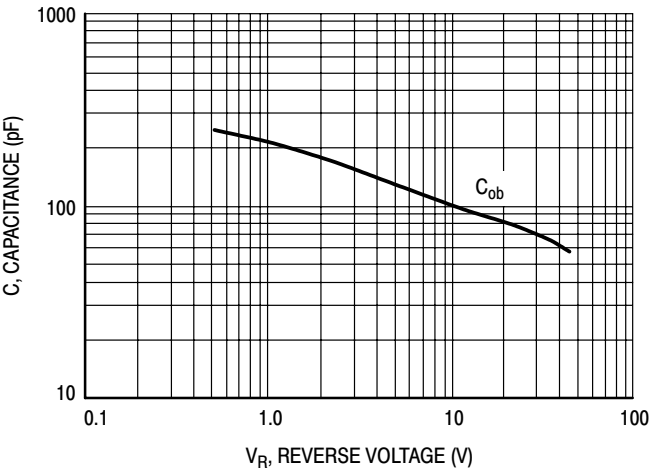


Figure 8. Output Capacitance

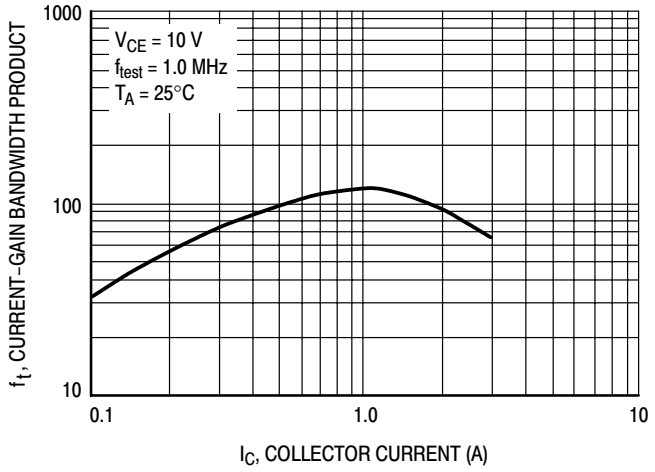


Figure 9. Current–Gain Bandwidth Product

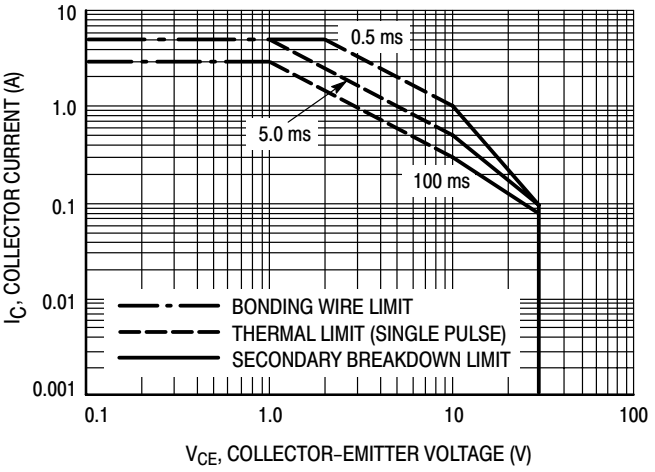


Figure 10. Active Region Safe Operating Area

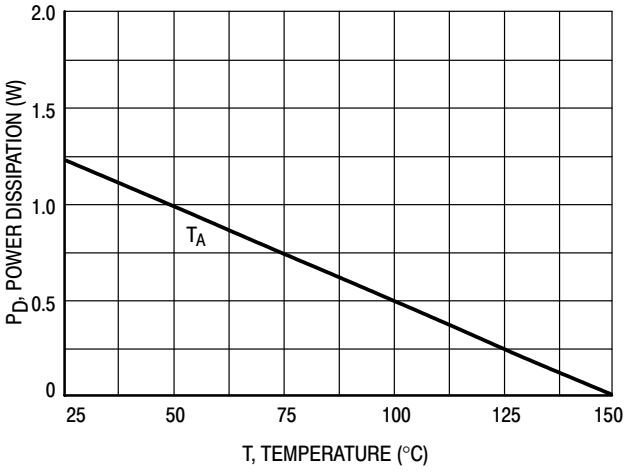


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

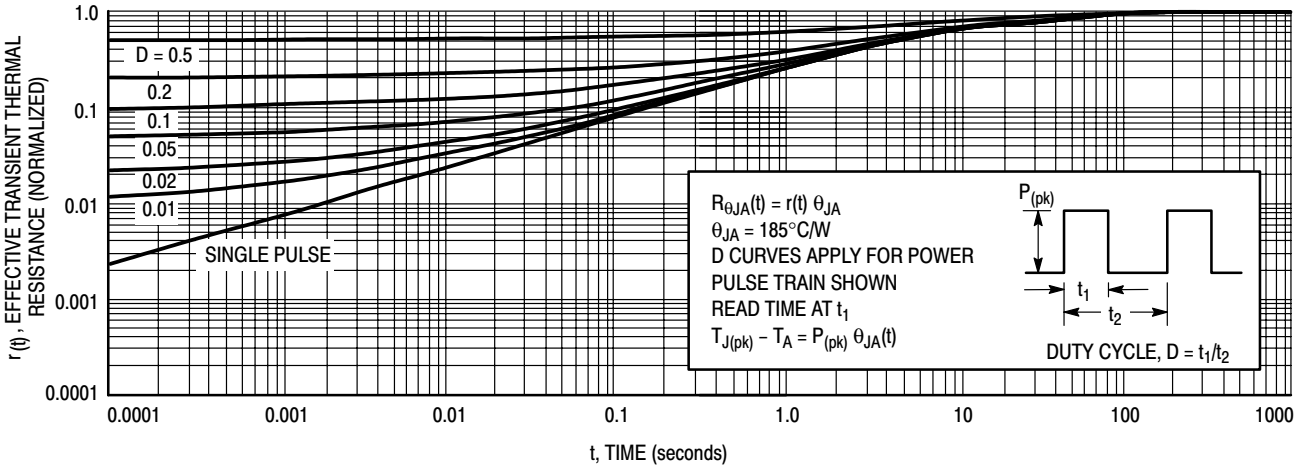


Figure 12. Thermal Response

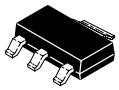
MMJT350T1

Bipolar Power Transistors
PNP Silicon

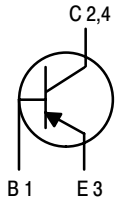
0.5 AMPERE
POWER TRANSISTOR
PNP SILICON
300 VOLTS
2.75 WATTS

. . . designed for use in line–operated applications such as low power, line–operated series pass and switching regulators requiring PNP capability.

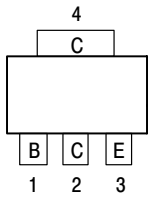
- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 300 Vdc @ I_C
  = 1.0 mAdc
- Excellent DC Current Gain —
  h_{FE} = 30–240 @ I_C
  = 50 mAdc



CASE 318E–04, Style 1



Schematic



Top View Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Collector–Base Voltage	V_{CB}	300	Vdc
Emitter–Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous — Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P_D	2.75 22 1.40 0.65	Watts mW/°C Watts Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	45 85 190	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

June, 2001 – Rev. 0
Publication Order Number:
MMJT350T1/D

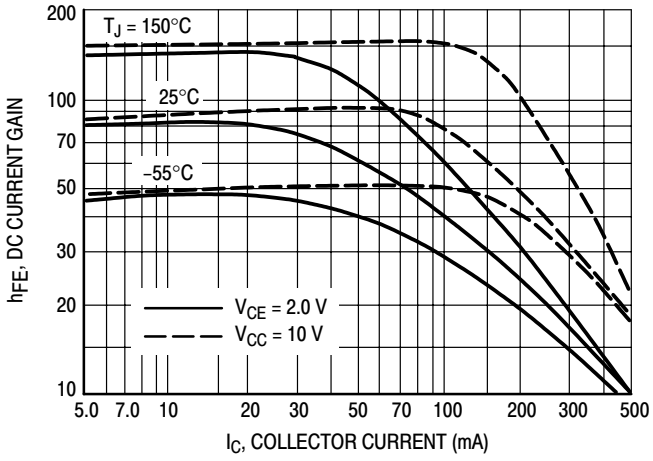


Figure 1. DC Current Gain

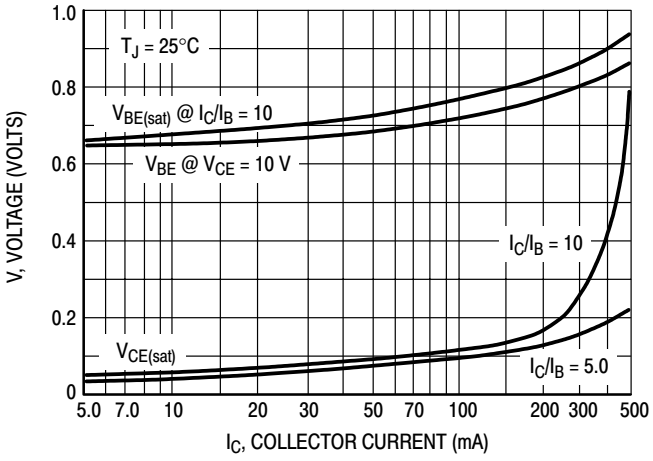


Figure 2. "On" Voltages

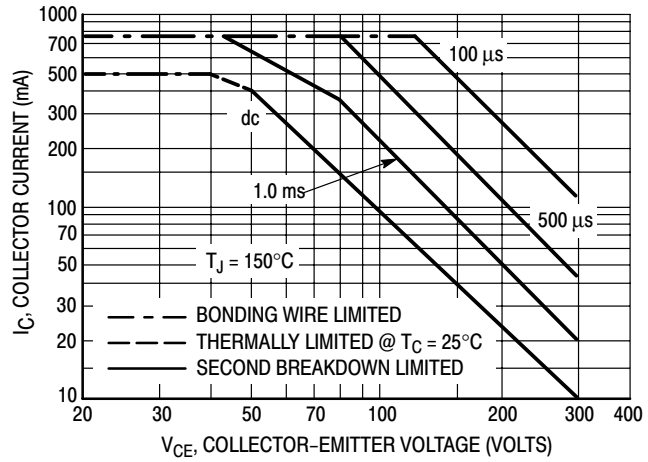


Figure 3. Active−Region Safe Operating Area

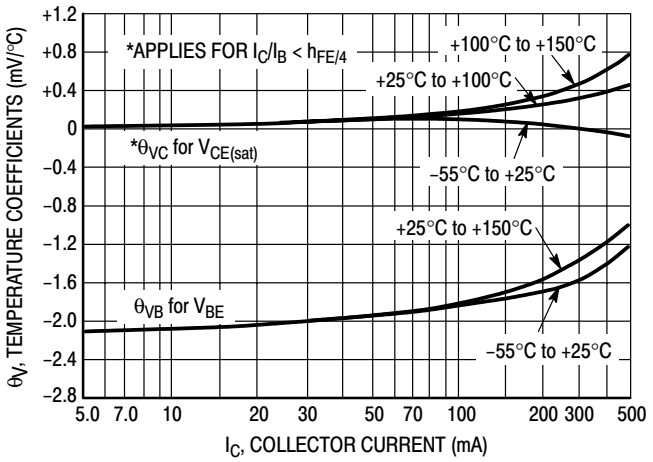


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

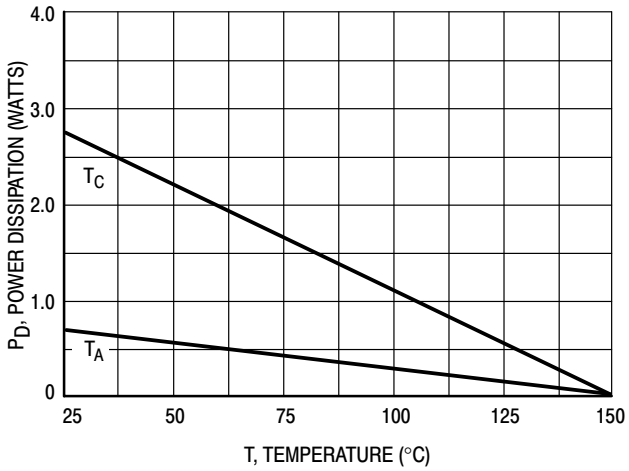


Figure 5. Power Derating

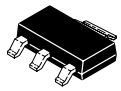
MMJT9410

ON Semiconductor Preferred Device

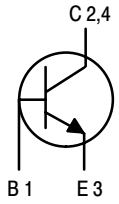
Bipolar Power Transistors
NPN Silicon

- Collector –Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 85 (Min) @ I_C = 0.8 Adc
  = 60 (Min) @ I_C = 3.0 Adc
- Low Collector –Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.2 Vdc (Max) @ I_C = 1.2 Adc
  = 0.45 Vdc (Max) @ I_C = 3.0 Adc
- SOT–223 Surface Mount Packaging

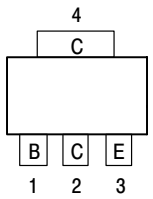
POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.2 VOLTS



CASE 318E–04, Style 1



Schematic



Top View Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	± 6.0	Vdc
Base Current — Continuous	I_B	1.0	Adc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P_D	3.0 24 1.7 0.75	Watts mW/°C Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 75 165	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
MMJT9410/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter–Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω) (V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)	I_{CER}	— —	— —	20 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS[1]					
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc) (I_C = 1.2 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	— — —	0.105 0.150 —	0.150 0.200 0.450	Vdc
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.2 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	85 80 60	200 — —	— — —	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	85	135	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	200	—	pF
Current–Gain — Bandwidth Product[2] (I_C = 500 mA, V_{CE} = 10 Vdc, F_{test} = 1.0 MHz)	f_T	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{FE}| \cdot f_{test}$

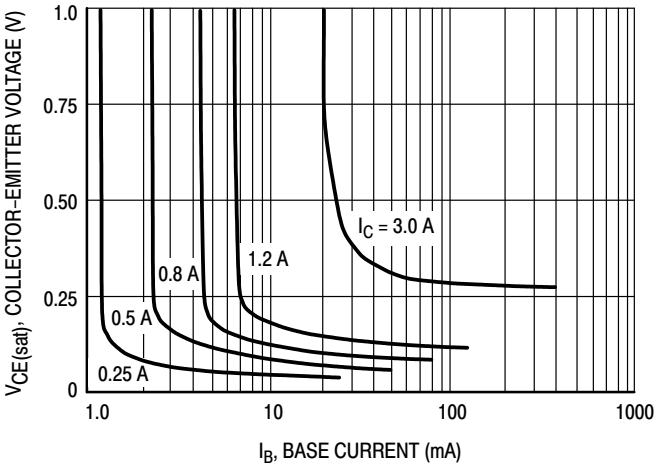


Figure 1. Collector Saturation Region

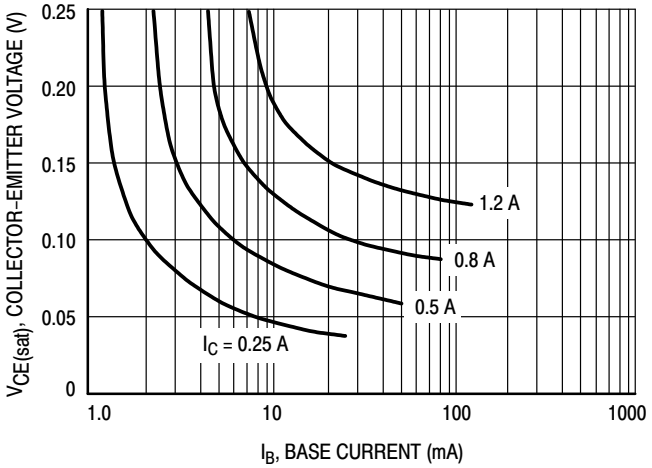


Figure 2. Collector Saturation Region

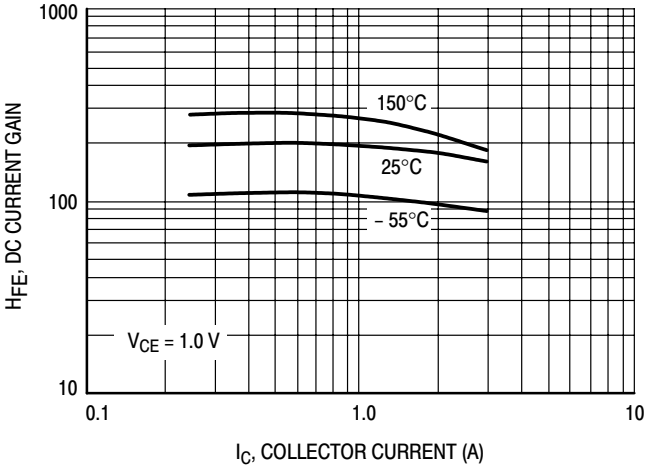


Figure 3. DC Current Gain

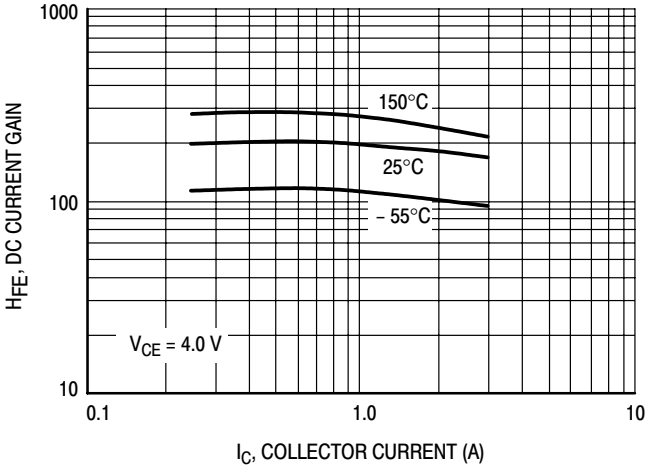


Figure 4. DC Current Gain

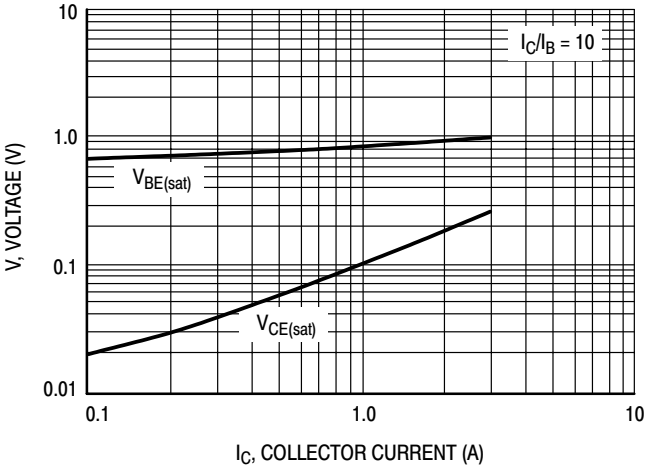


Figure 5. “On” Voltages

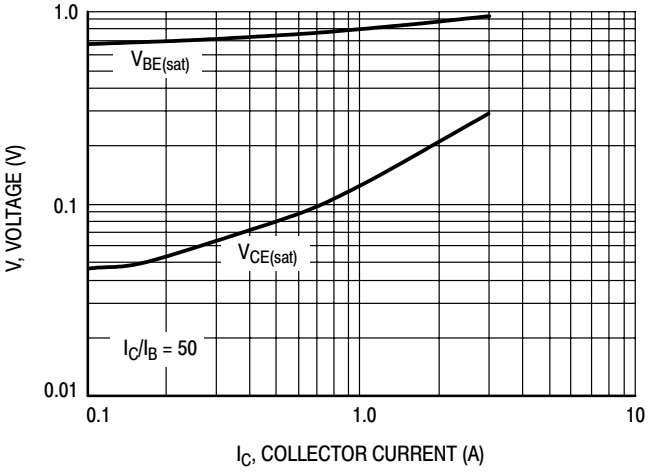


Figure 6. “On” Voltages

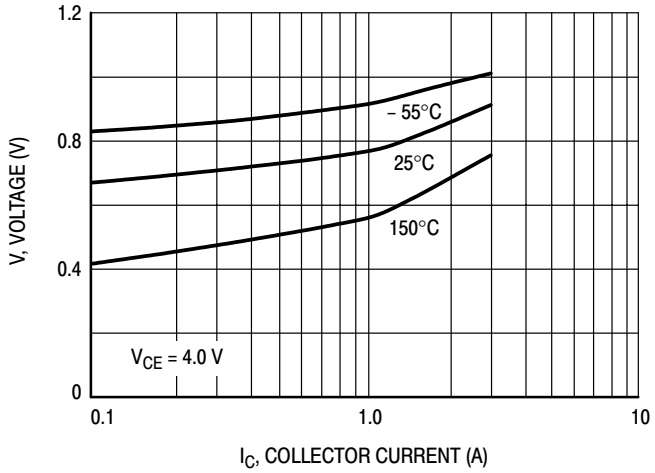


Figure 7. $V_{BE(on)}$ Voltage

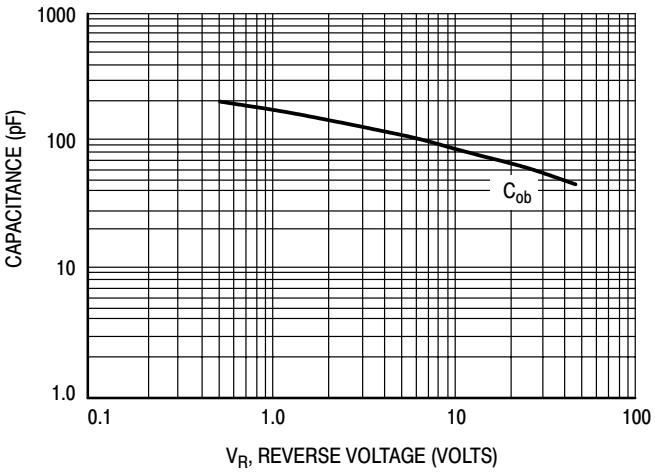


Figure 8. Capacitance

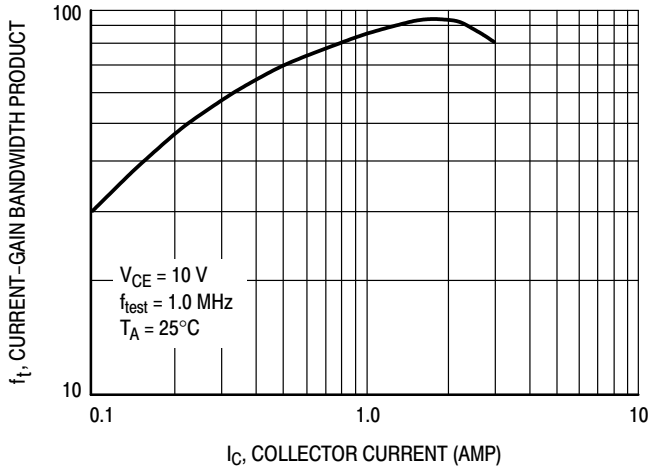


Figure 9. Current–Gain Bandwidth Product

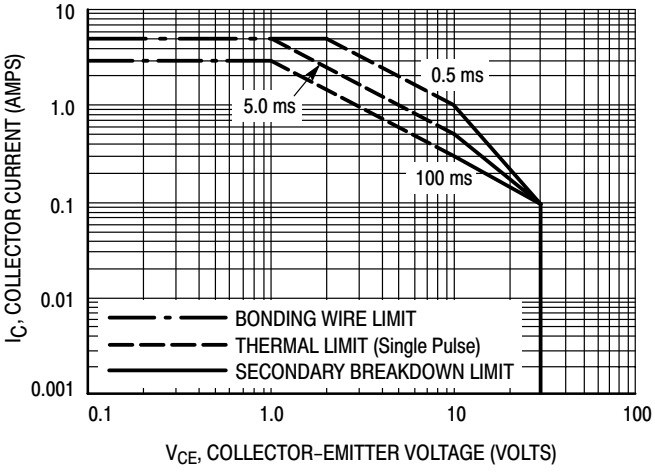


Figure 10. Active Region Safe Operating Area

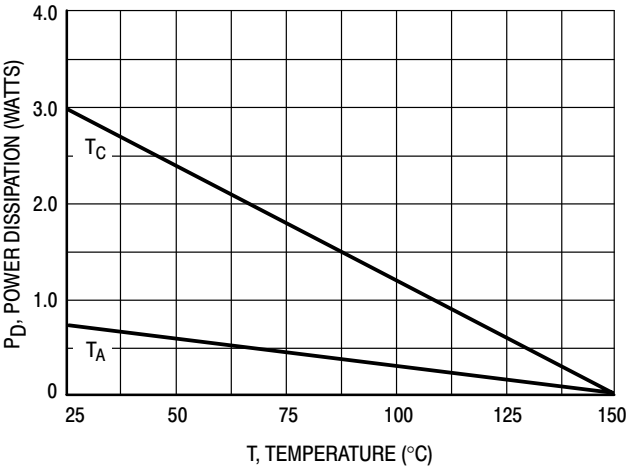


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

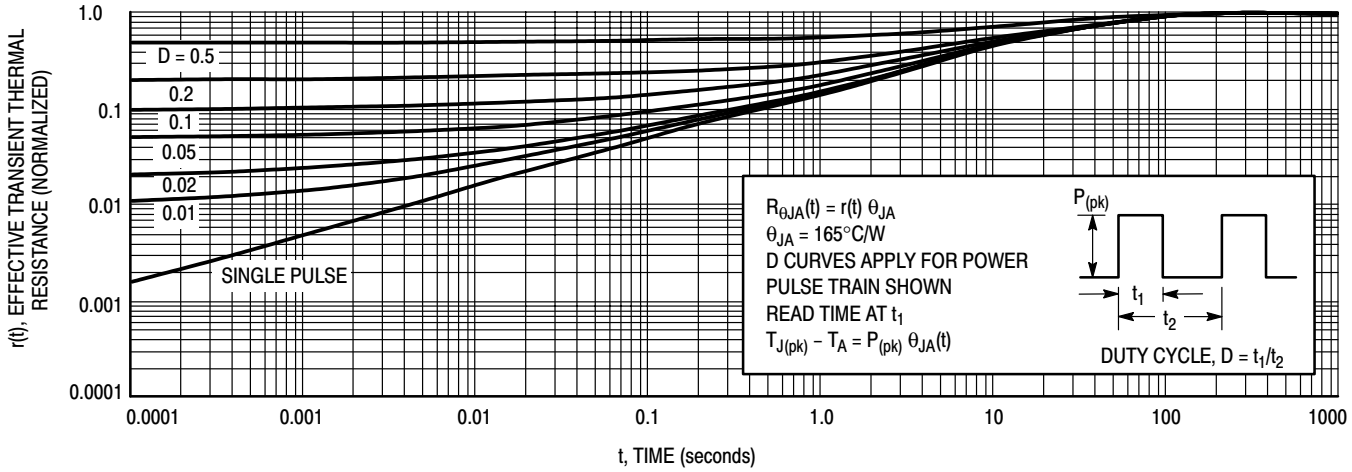


Figure 12. Thermal Response

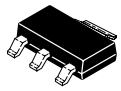
MMJT9435

ON Semiconductor Preferred Device

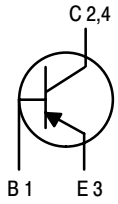
Bipolar Power Transistors
PNP Silicon

- Collector –Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 125 (Min) @ I_C = 0.8 Adc
  = 90 (Min) @ I_C = 3.0 Adc
- Low Collector –Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.275 Vdc (Max) @ I_C = 1.2 Adc
  = 0.55 Vdc (Max) @ I_C = 3.0 Adc
- SOT–223 Surface Mount Packaging

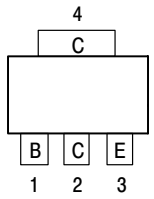
POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.275 VOLTS



CASE 318E–04, Style 1



Schematic



Top View Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	±6.0	Vdc
Base Current — Continuous	I_B	1.0	Adc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P_D	3.0 24 1.56 0.72	Watts mW/°C Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Case – Junction to Ambient on 1” sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction to Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR–4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 80 174	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
MMJT9435/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter–Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω)	I_{CER}	—	—	20	μAdc
(V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)		—	—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS(1)					
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	0.155	0.210	Vdc
(I_C = 1.2 Adc, I_B = 20 mAdc)		—	—	0.275	
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	—	0.550	
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	125	220	—	—
(I_C = 1.2 Adc, V_{CE} = 1.0 Vdc)		110	—	—	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		90	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	100	150	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	135	—	pF
Current–Gain — Bandwidth Product(2) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T	—	110	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{FE}| \cdot f_{test}$

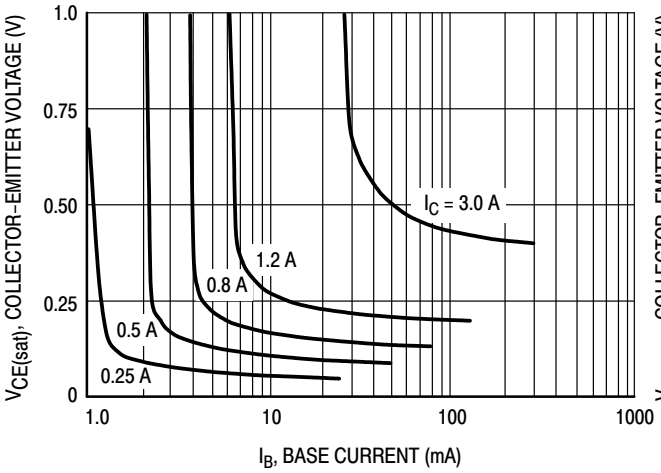


Figure 1. Collector Saturation Region

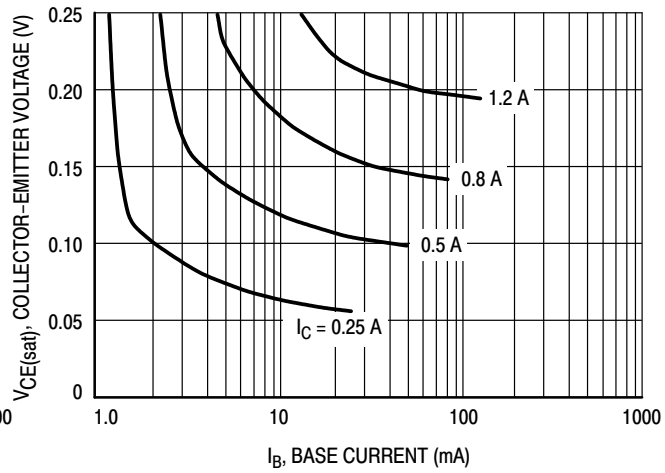


Figure 2. Collector Saturation Region

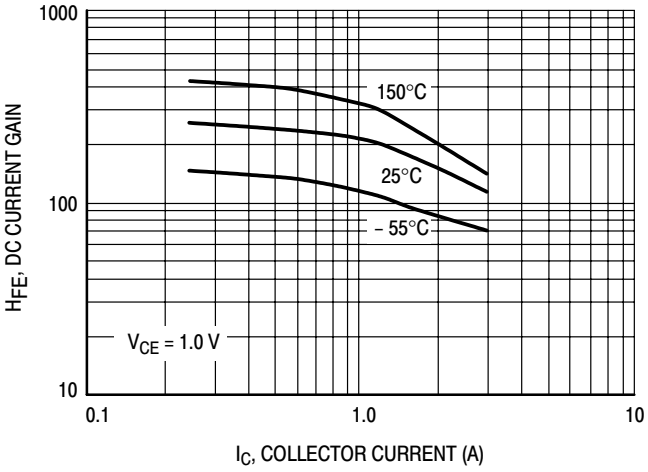


Figure 3. DC Current Gain

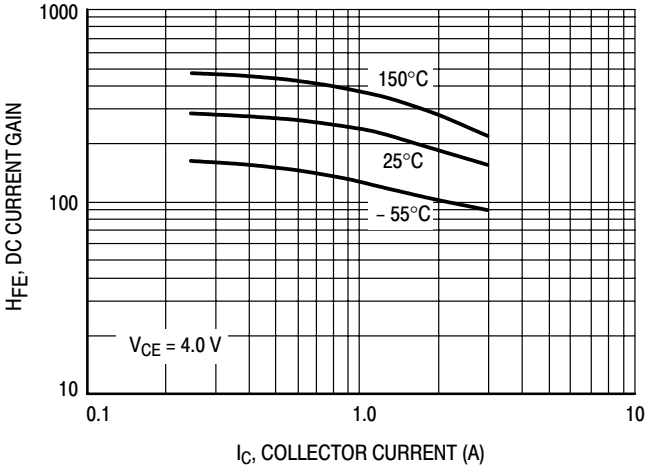


Figure 4. DC Current Gain

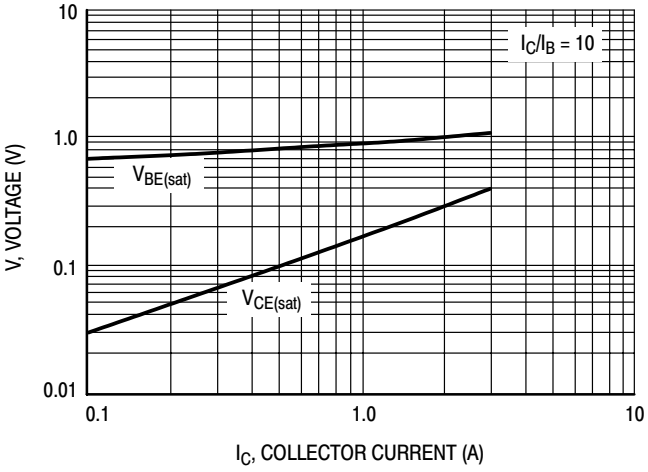


Figure 5. “On” Voltages

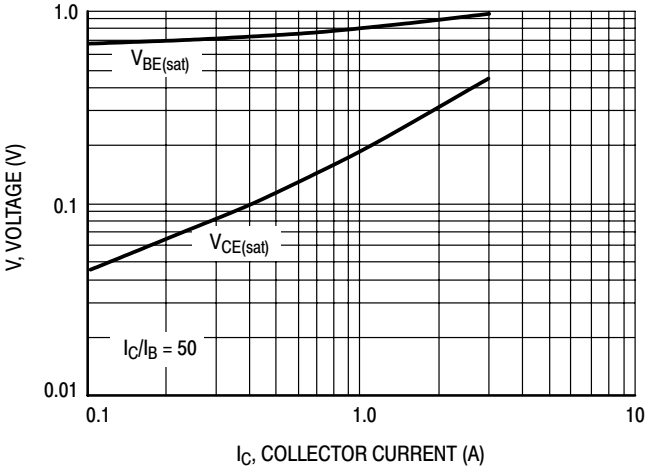


Figure 6. “On” Voltages

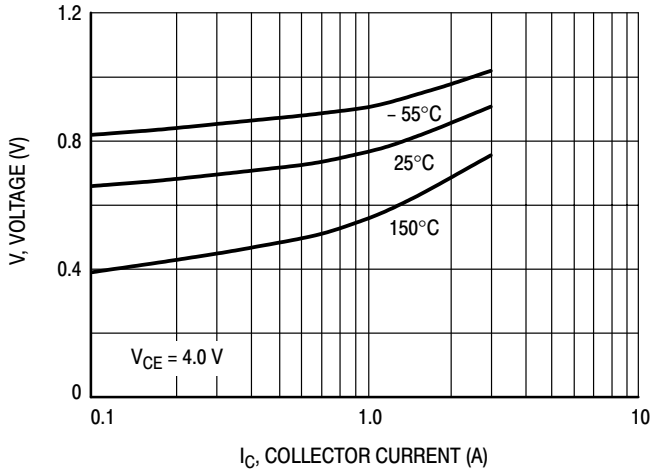


Figure 7. $V_{BE(on)}$ Voltage

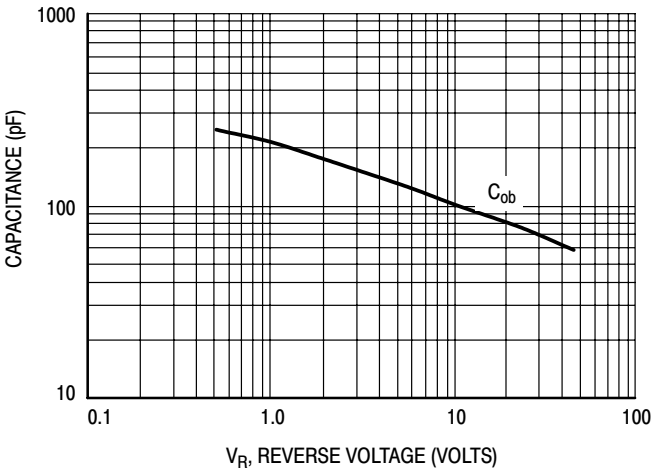


Figure 8. Output Capacitance

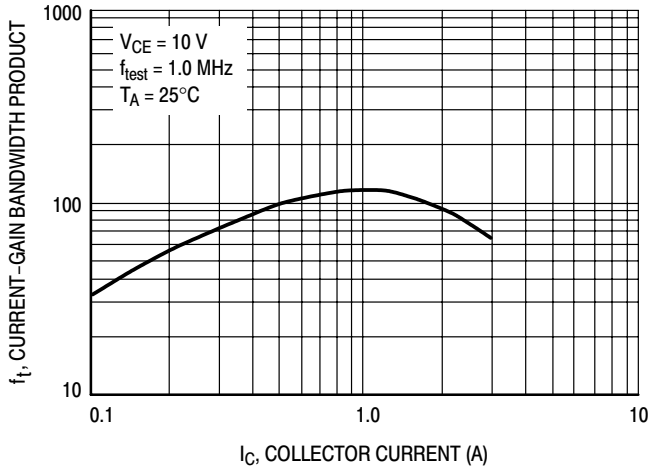


Figure 9. Current–Gain Bandwidth Product

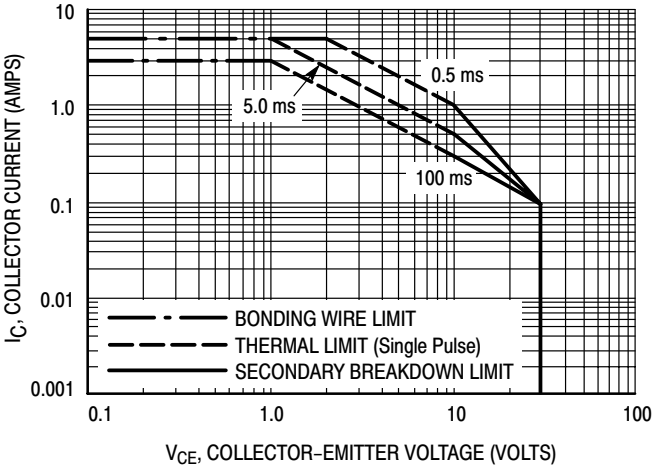


Figure 10. Active Region Safe Operating Area

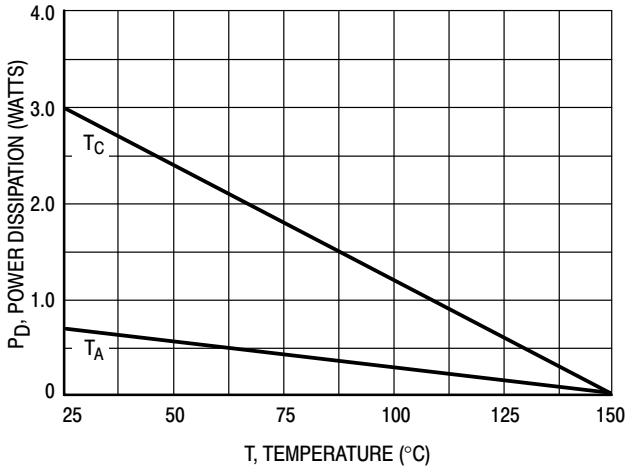


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

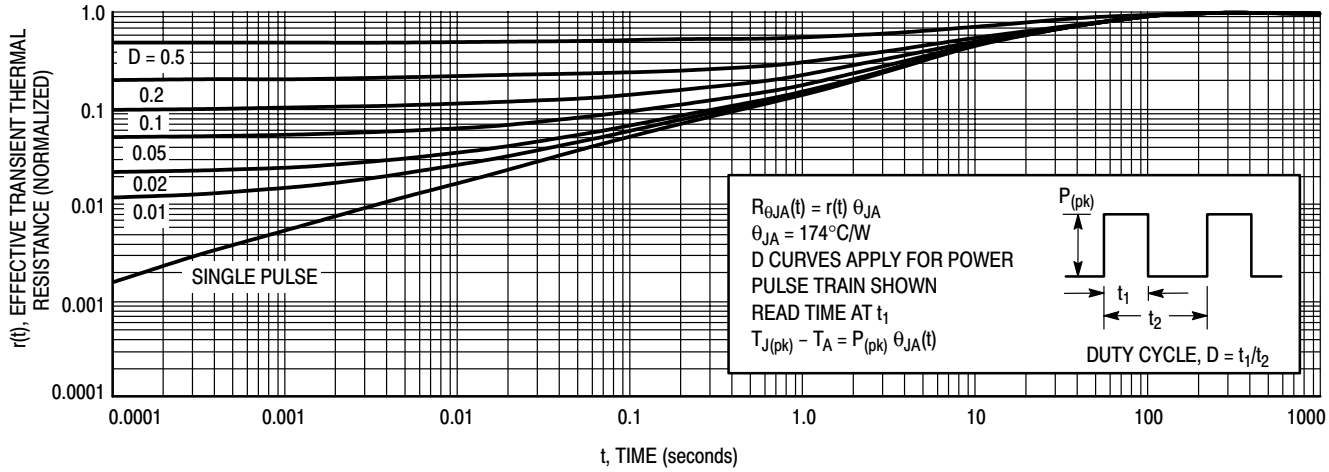


Figure 12. Thermal Response

Plastic Medium-Power Complementary Silicon Transistors

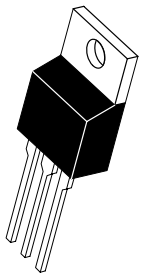
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP100, TIP105
  = 80 Vdc (Min) — TIP101, TIP106
  = 100 Vdc (Min) — TIP102, TIP107
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP100
TIP101*
TIP102*
PNP
TIP105
TIP106*
TIP107*

***ON Semiconductor Preferred Device**

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60–80–100 VOLTS
80 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 15			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64			Watts W/°C
Unclamped Inductive Load Energy (1)	E	30			mJ
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

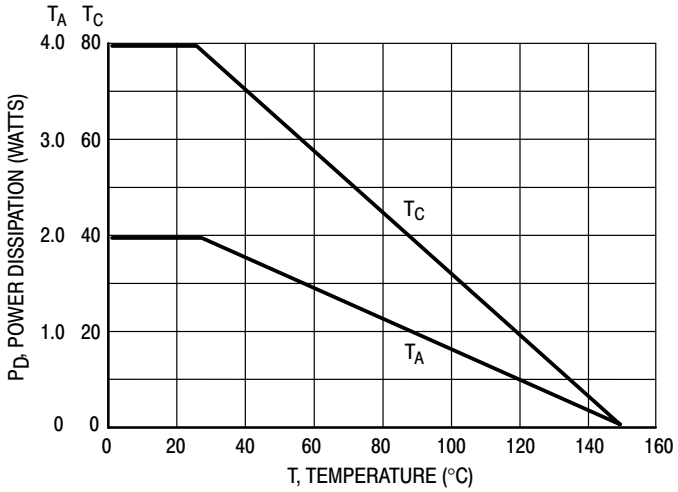


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP100, TIP105		60	—	
	TIP101, TIP106		80	—	
	TIP102, TIP107		100	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP100, TIP105		—	50	
(V_{CE} = 40 Vdc, I_B = 0)	TIP101, TIP106		—	50	
(V_{CE} = 50 Vdc, I_B = 0)	TIP102, TIP107		—	50	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP100, TIP105		—	50	
(V_{CB} = 80 Vdc, I_E = 0)	TIP101, TIP106		—	50	
(V_{CB} = 100 Vdc, I_E = 0)	TIP102, TIP107		—	50	
Emitter Cutoff Current		I_{EBO}	—	8.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)			200	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 6.0 mAdc)			—	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			—	2.5	
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.8	Vdc
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	4.0	—	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					—
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107		—	300	
	TIP100, TIP101, TIP102		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

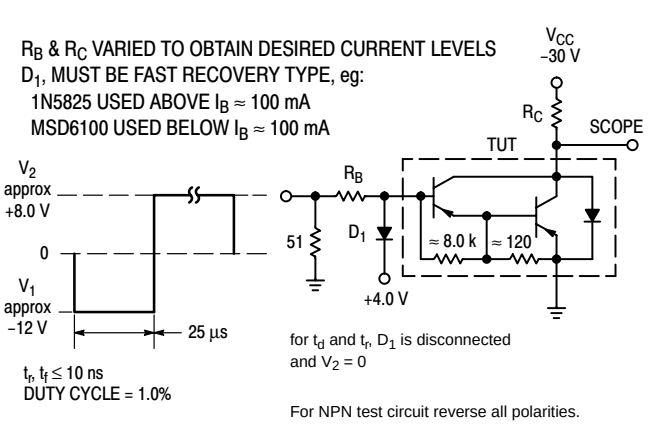


Figure 2. Switching Times Test Circuit

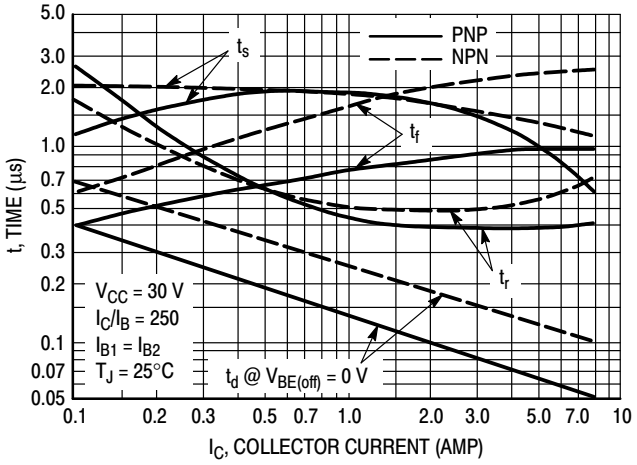


Figure 3. Switching Times

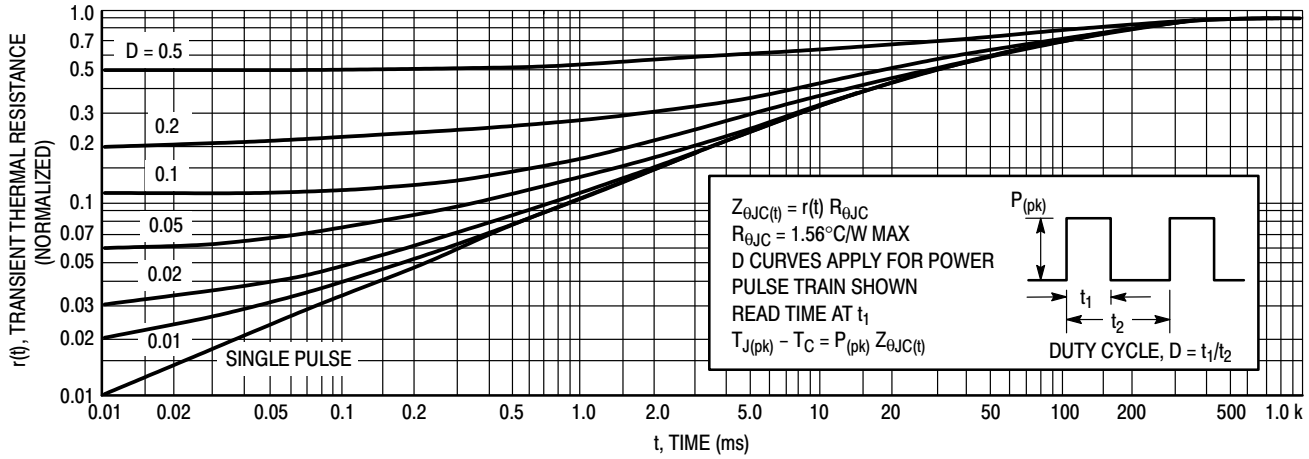


Figure 4. Thermal Response

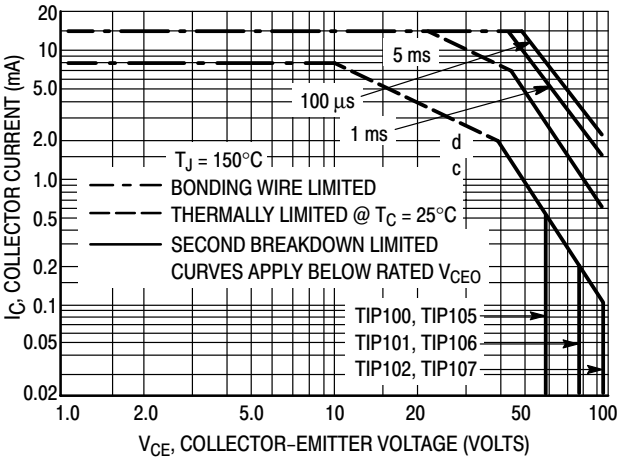


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

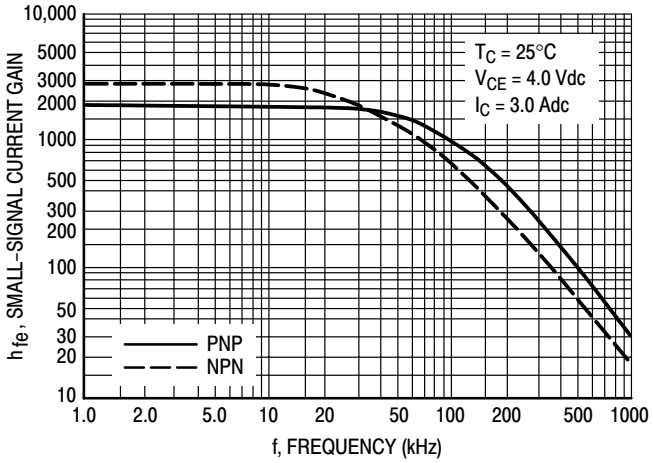


Figure 6. Small–Signal Current Gain

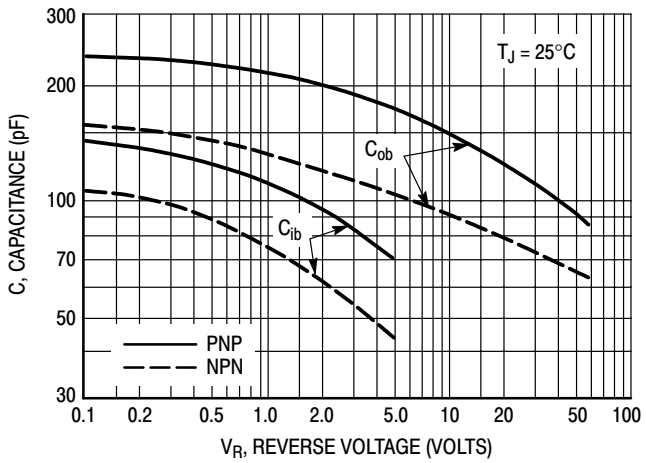
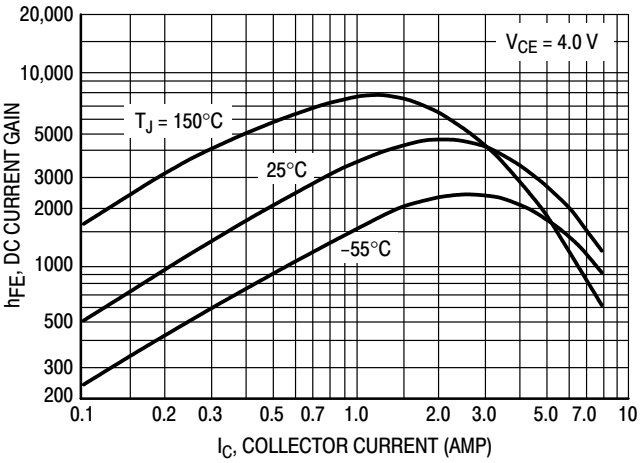


Figure 7. Capacitance

NPN
TIP100, TIP101, TIP102



PNP
TIP105, TIP106, TIP107

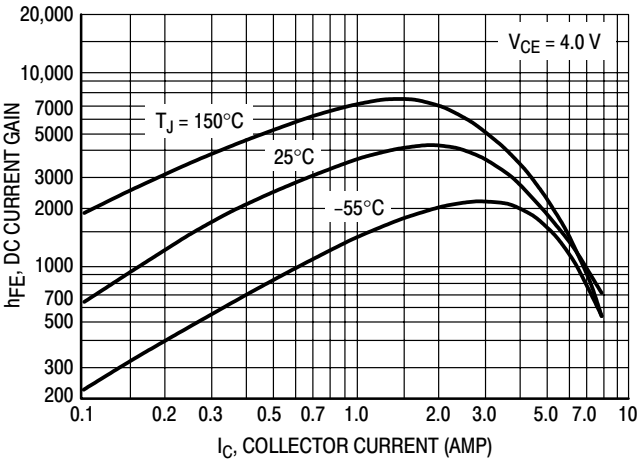
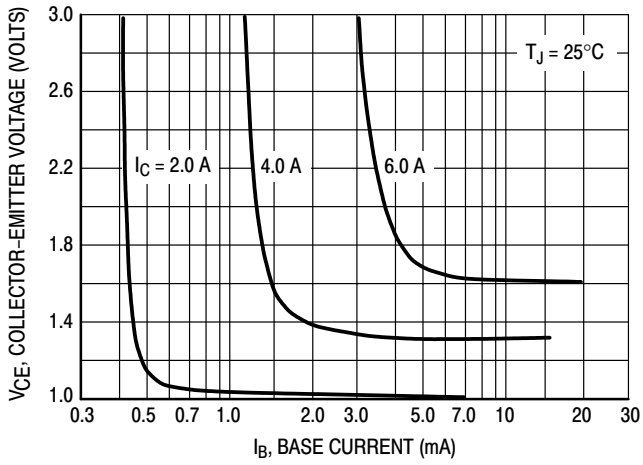


Figure 8. DC Current Gain



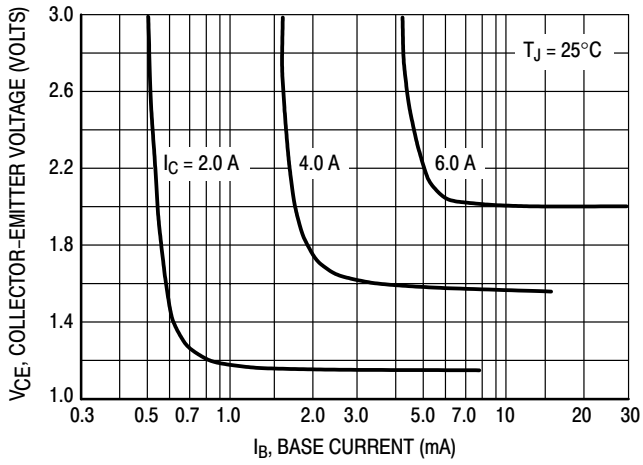
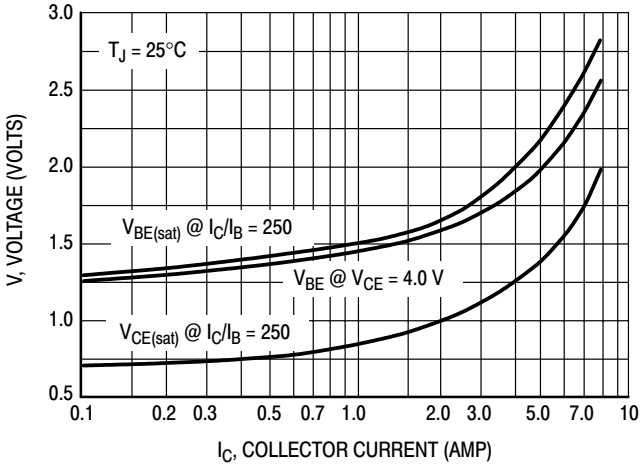


Figure 9. Collector Saturation Region



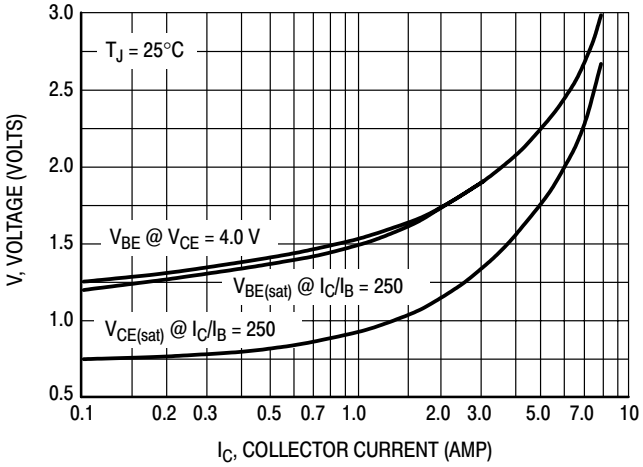


Figure 10. “On” Voltages

Plastic Medium-Power Complementary Silicon Transistors

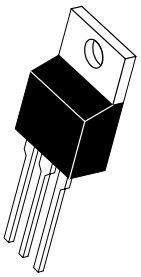
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C
  = 1.0 Adc
- Collector–Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP110, TIP115
  = 80 Vdc (Min) — TIP111, TIP116
  = 100 Vdc (Min) — TIP112, TIP117
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C
  = 2.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP110
TIP111*
TIP112*
PNP
TIP115
TIP116*
TIP117*

***ON Semiconductor Preferred Device**

DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60–80–100 VOLTS
50 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	2.0 4.0			Adc
Base Current	I_B	50			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy — Figure 13	E	25			mJ
Operating and Storage Junction	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
TIP110/D

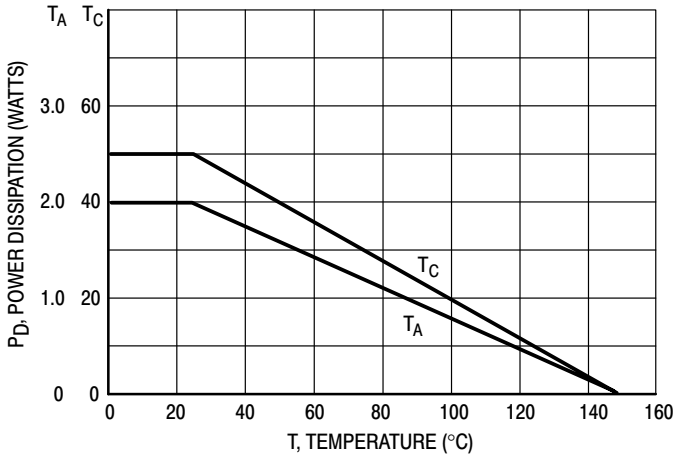


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP110, TIP115		60	—	
	TIP111, TIP116		80	—	
	TIP112, TIP117		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP110, TIP115		—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP111, TIP116		—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP112 ,TIP117		—	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP110, TIP115		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	TIP111, TIP116		—	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	TIP112, TIP117		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			1000	—	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			500	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	2.5	Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.8	Vdc
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	25	—	—
(I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117		—	200	
	TIP110, TIP111, TIP112		—	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

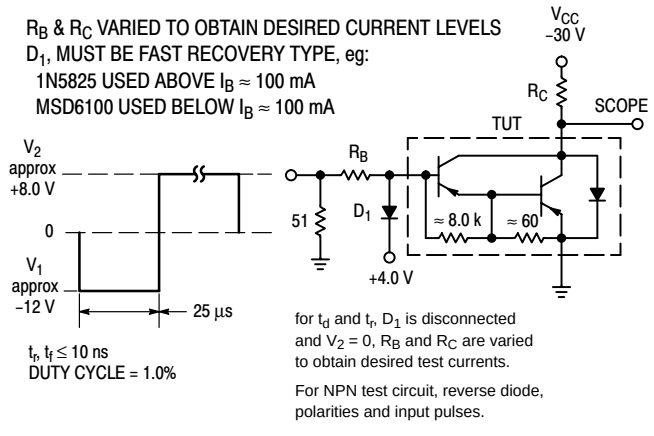


Figure 2. Switching Times Test Circuit

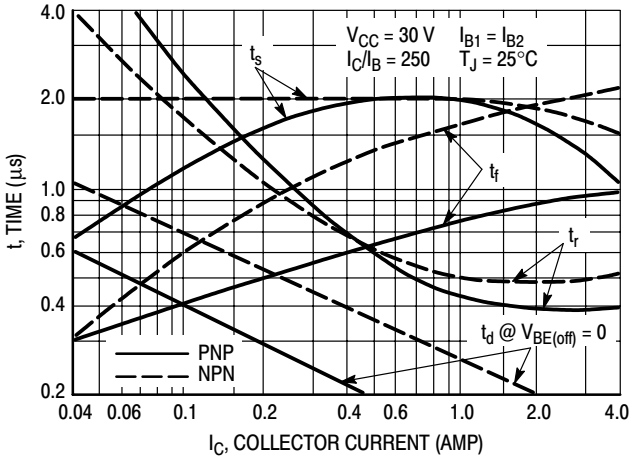


Figure 3. Switching Times

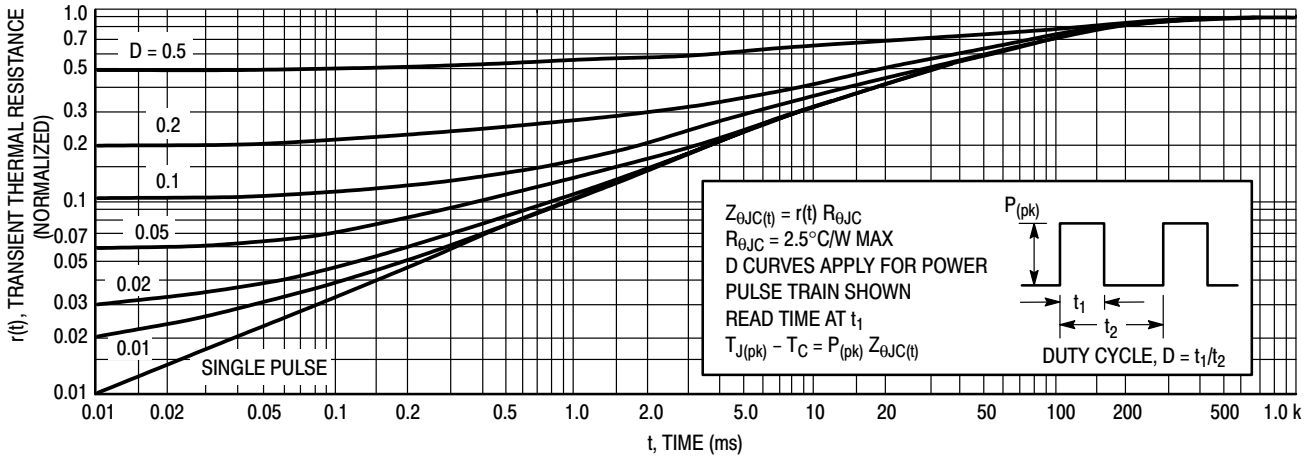


Figure 4. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

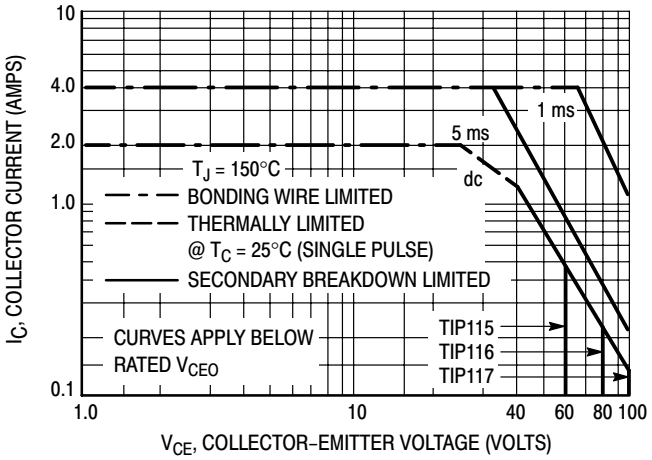


Figure 5. TIP115, 116, 117

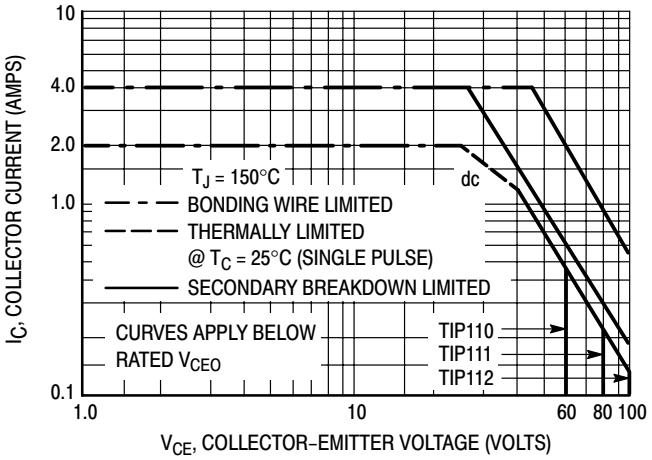


Figure 6. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

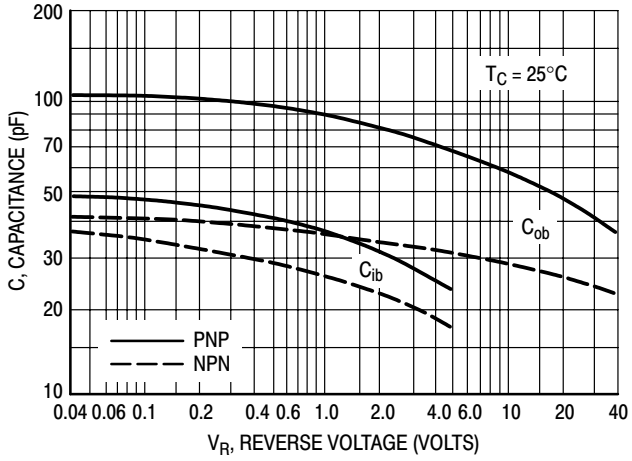
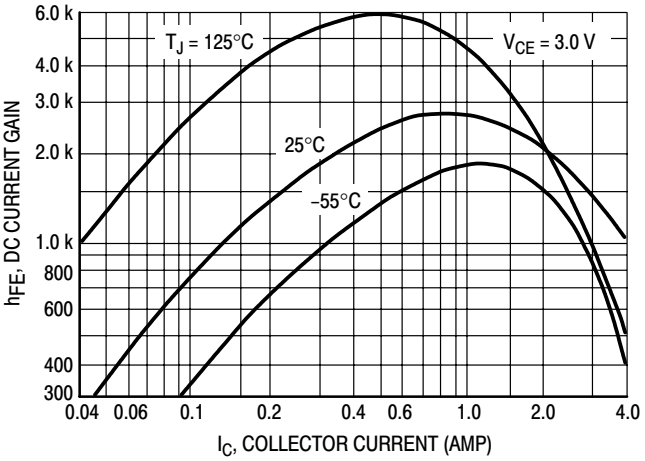


Figure 7. Capacitance

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

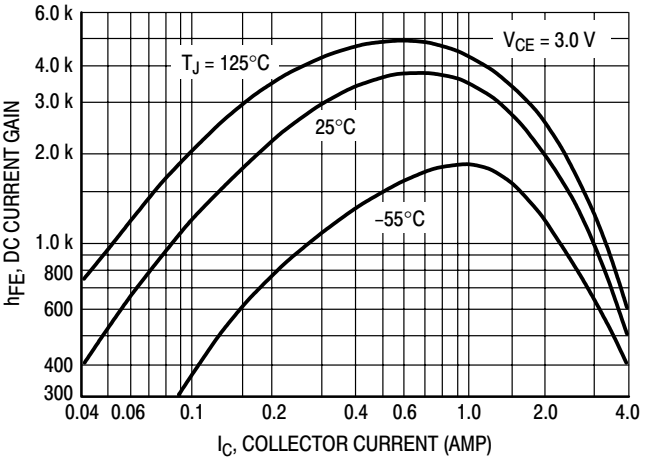
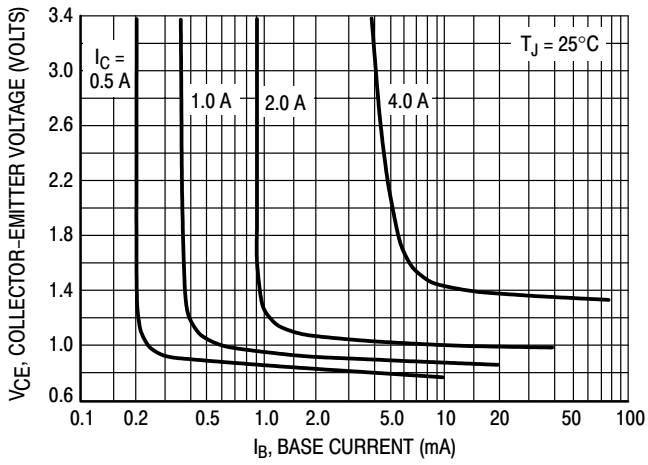


Figure 8. DC Current Gain



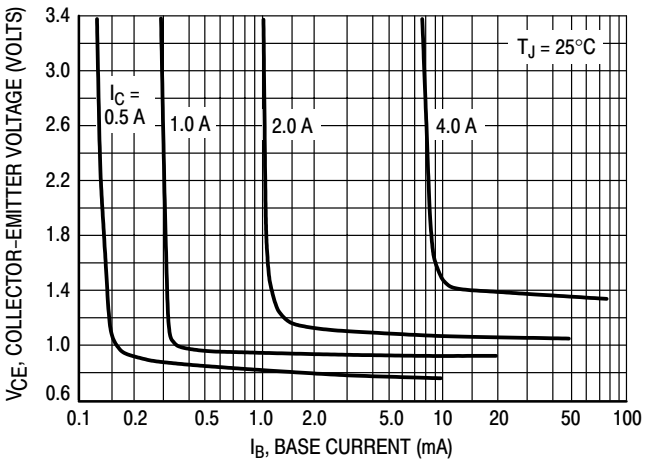
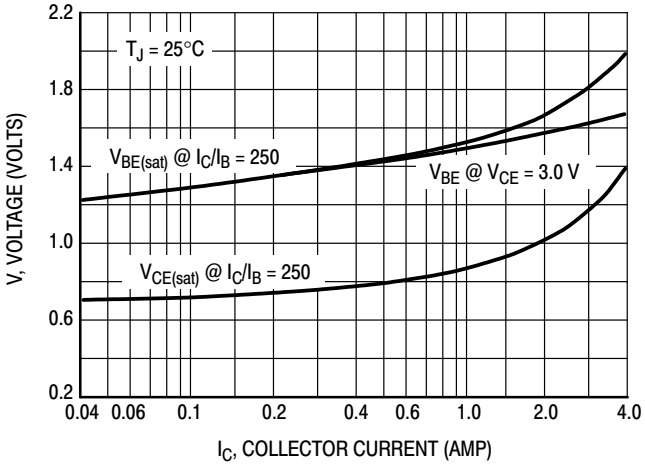


Figure 9. Collector Saturation Region



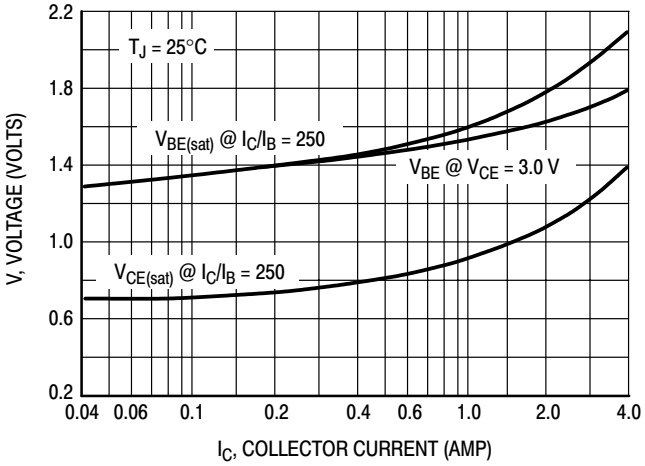
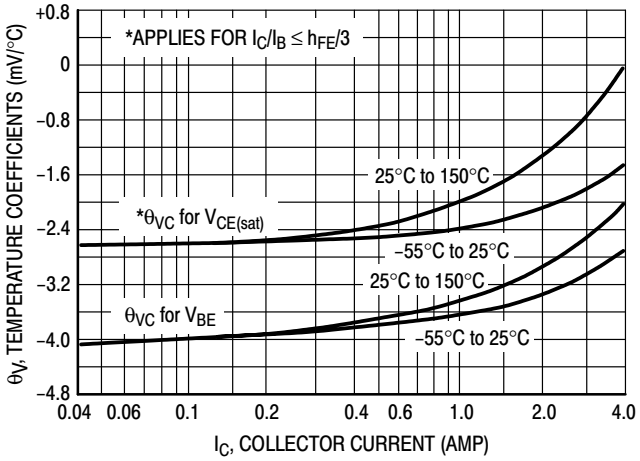


Figure 10. “On” Voltages

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

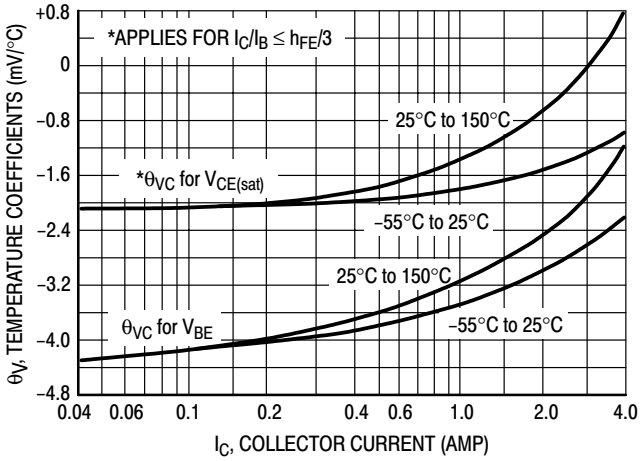
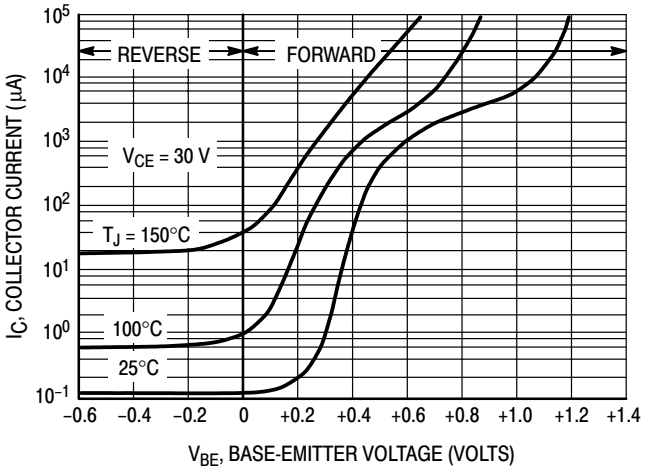


Figure 11. Temperature Coefficients



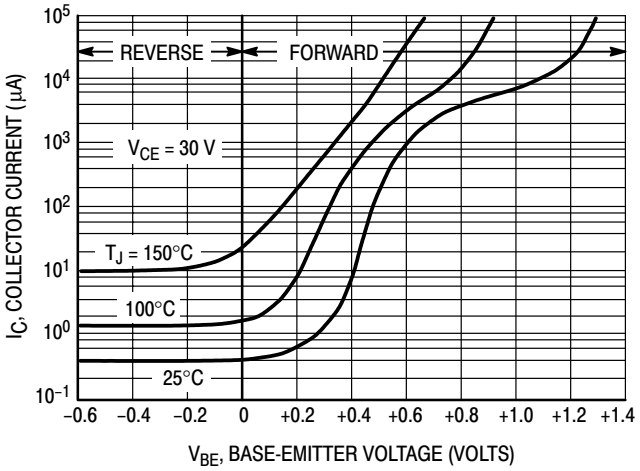
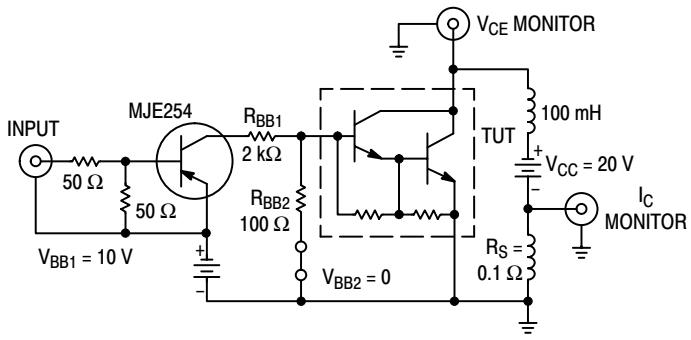
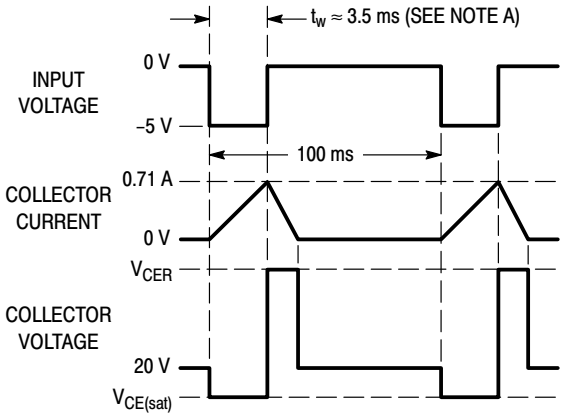


Figure 12. Collector Cut-Off Region

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



Note A: Input pulse width is increased until I_{CM} = 0.71 A,
NPN test shown; for PNP test
reverse all polarity and use MJE224 driver.

Figure 13. Inductive Load Switching

Plastic Medium-Power Complementary Silicon Transistors

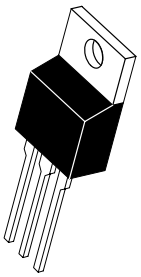
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP120, TIP125
  = 80 Vdc (Min) — TIP121, TIP126
  = 100 Vdc (Min) — TIP122, TIP127
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP120*
TIP121*
TIP122*
PNP
TIP125*
TIP126*
TIP127*

*ON Semiconductor Preferred Device

DARLINGTON
5 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60–80–100 VOLTS
65 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	5.0 8.0			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 4
Publication Order Number:
TIP120/D

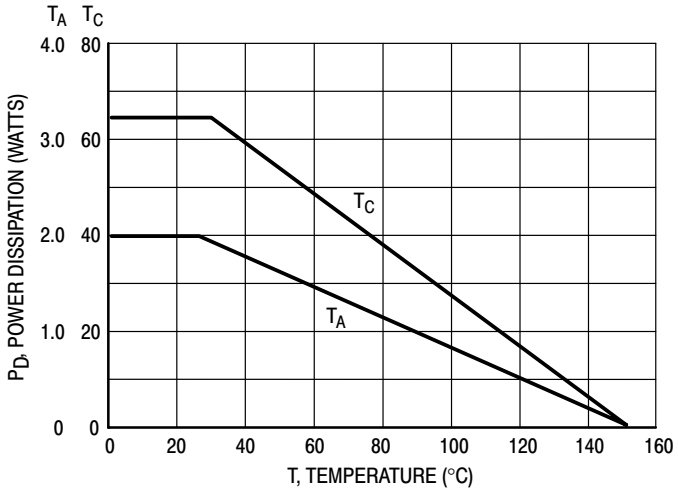


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	TIP120, TIP125		60	—	
	TIP121, TIP126		80	—	
	TIP122, TIP127		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP120, TIP125		—	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	TIP121, TIP126		—	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	TIP122, TIP127		—	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP120, TIP125		—	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	TIP121, TIP126		—	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	TIP122, TIP127		—	0.2	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			1000	—	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			—	2.0	
(I_C = 5.0 Adc, I_B = 20 mAdc)			—	4.0	
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.5	Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	4.0	—	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz	TIP125, TIP126, TIP127		—	300	
	TIP120, TIP121, TIP122		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

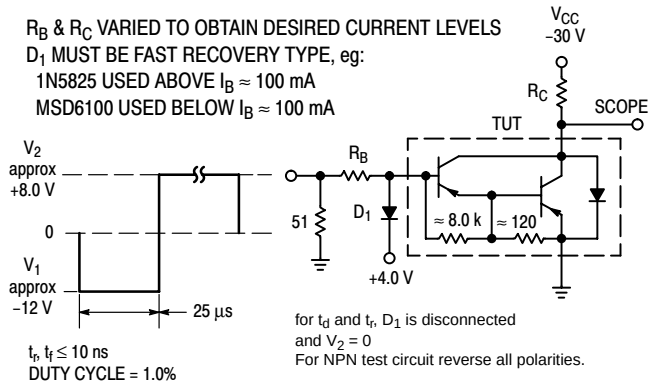


Figure 2. Switching Times Test Circuit

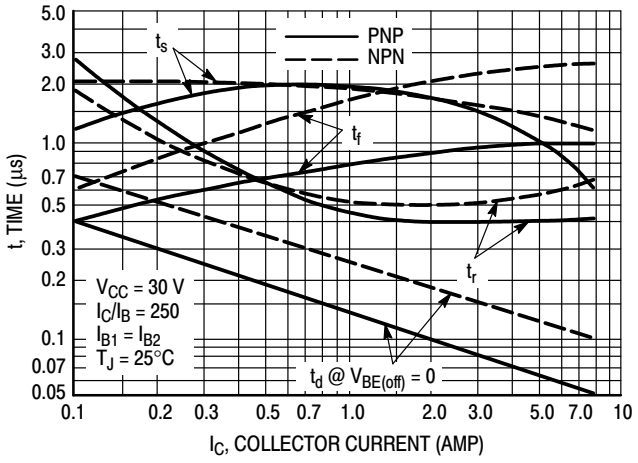


Figure 3. Switching Times

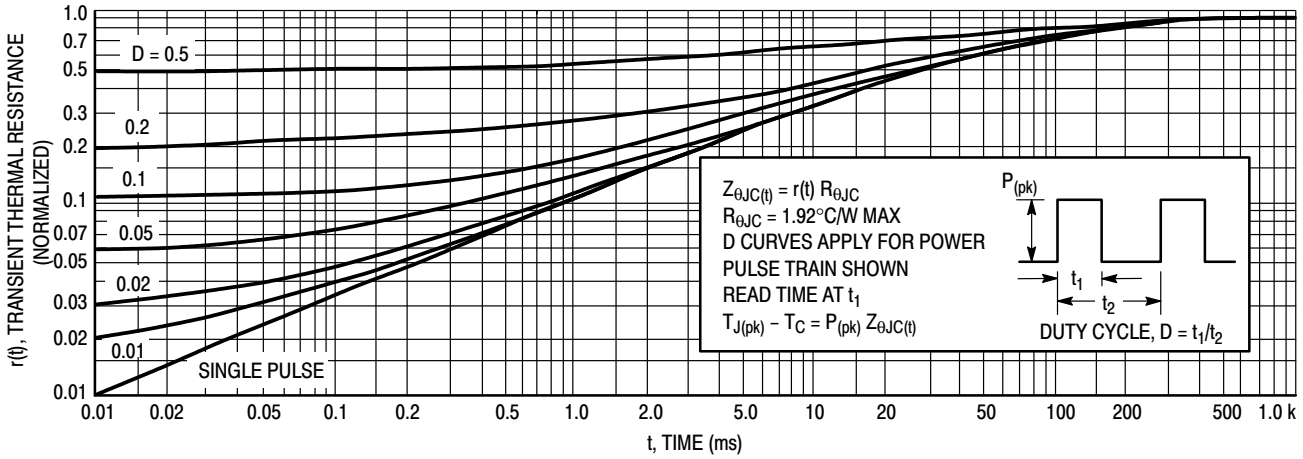


Figure 4. Thermal Response

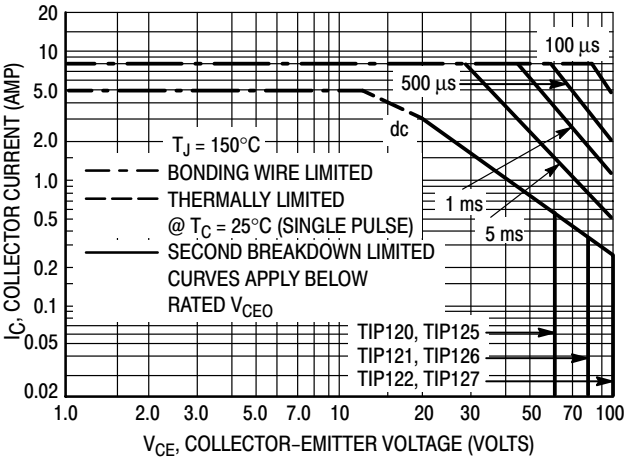


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

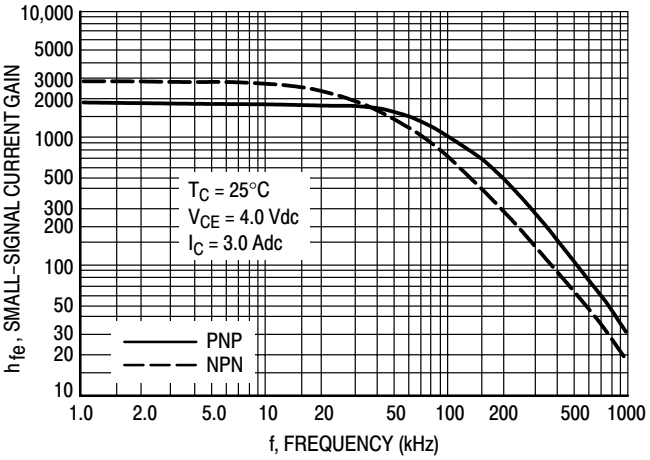


Figure 6. Small−Signal Current Gain

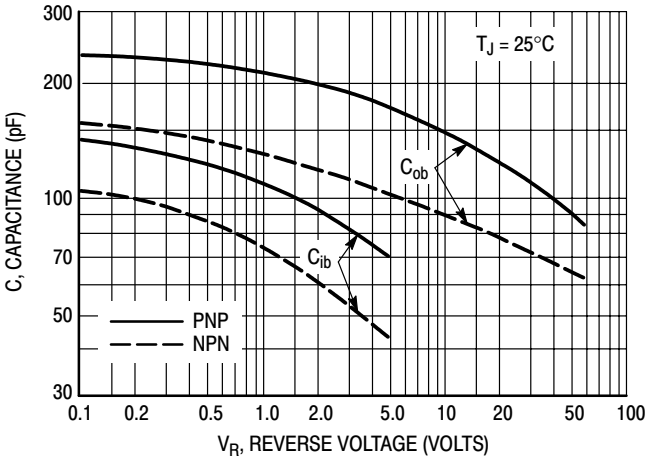
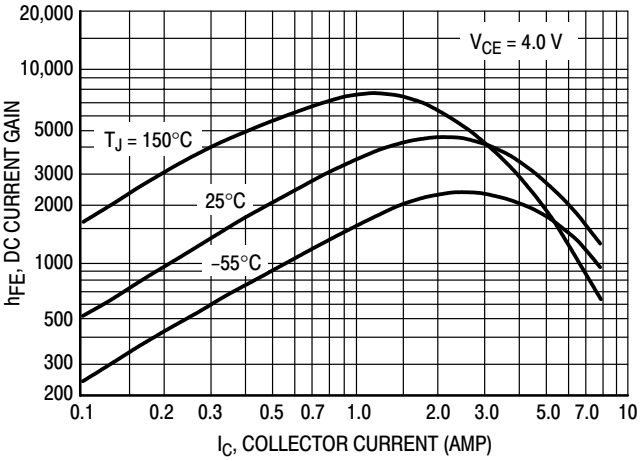


Figure 7. Capacitance

NPN
TIP120, TIP121, TIP122



PNP
TIP125, TIP126, TIP127

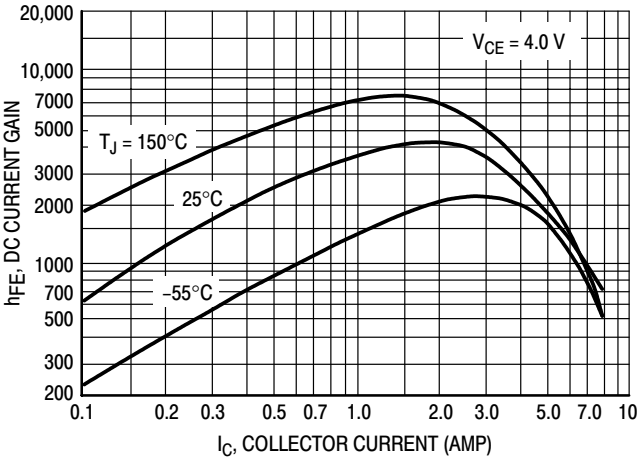
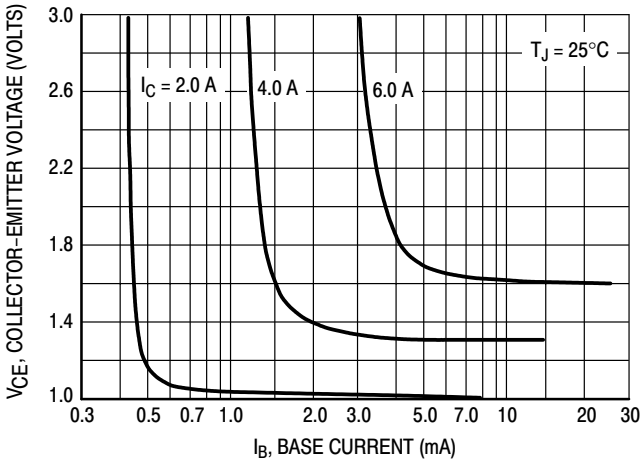


Figure 8. DC Current Gain



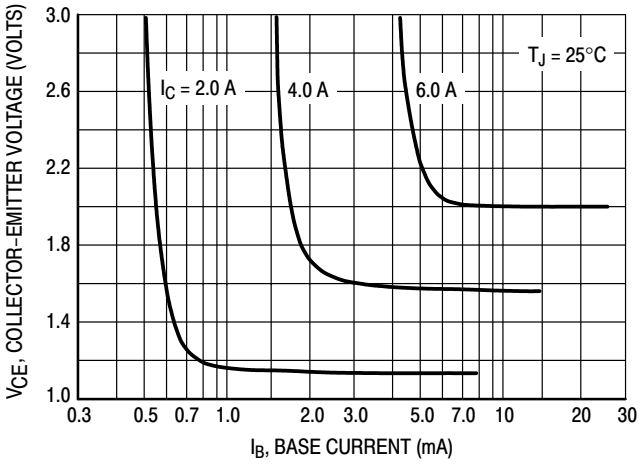
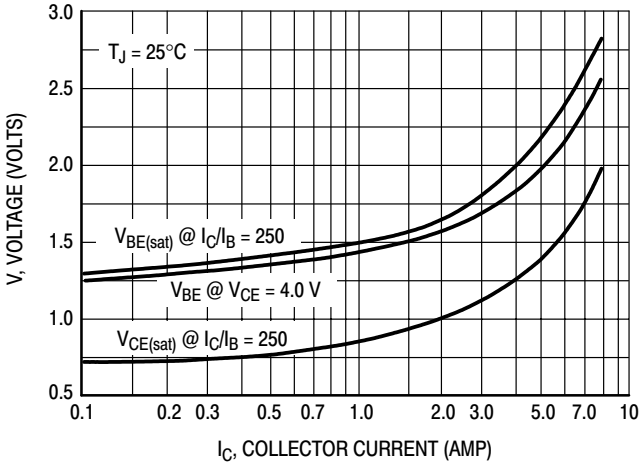


Figure 9. Collector Saturation Region



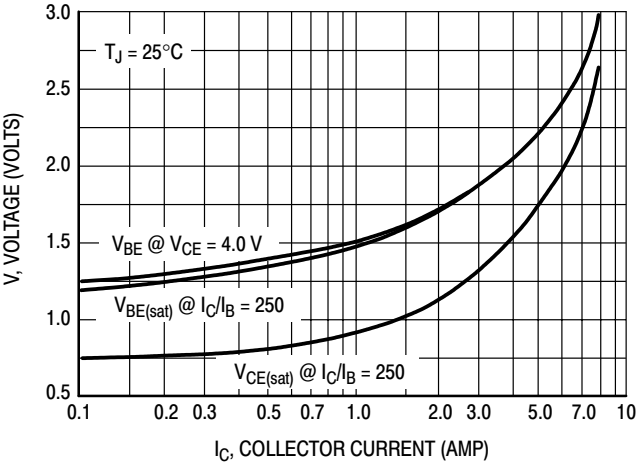


Figure 10. “On” Voltages

Darlington Complementary Silicon Power Transistors

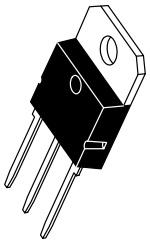
. . . designed for general–purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  Min h_{FE} = 1000 @ I_C
  = 5 A, V_{CE} = 4 V
- Collector–Emitter Sustaining Voltage — @ 30 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP140, TIP145
  80 Vdc (Min) — TIP141, TIP146
  100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor

NPN
TIP140
TIP141*
TIP142*
PNP
TIP145
TIP146*
TIP147*

***ON Semiconductor Preferred Device**

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS 125 WATTS



CASE 340D–02

MAXIMUM RATINGS

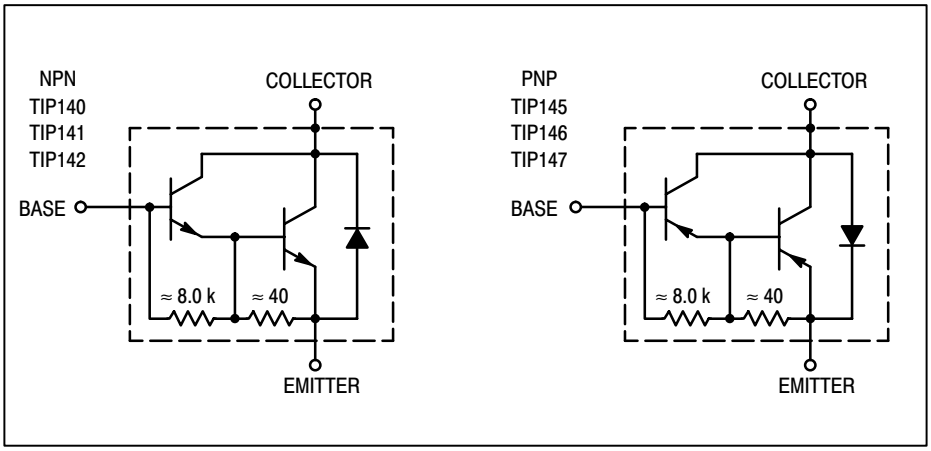
Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	10 15			Adc
Base Current — Continuous	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C	P_D	125			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	°C/W

(1) 5 ms, ≤ 10% Duty Cycle.

DARLINGTON SCHEMATICS



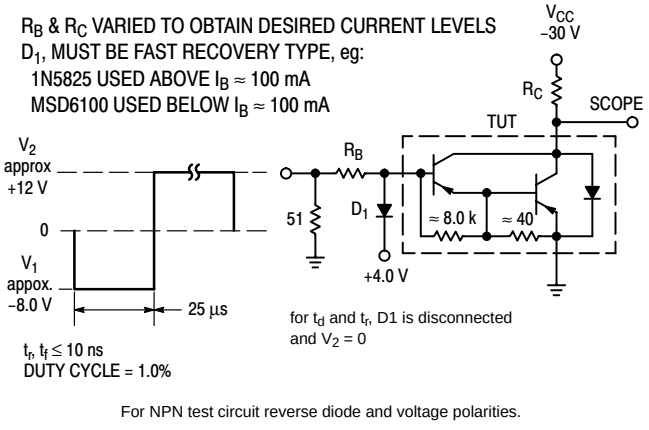
Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
TIP140/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 30 mA, I_B = 0)	TIP140, TIP145		60	—	—	
	TIP141, TIP146		80	—	—	
	TIP142, TIP147		100	—	—	
Collector Cutoff Current		I_{CEO}				mA
(V_{CE} = 30 Vdc, I_B = 0)	TIP140, TIP145		—	—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP141, TIP146		—	—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP142, TIP147		—	—	2.0	
Collector Cutoff Current		I_{CBO}				mA
(V_{CB} = 60 V, I_E = 0)	TIP140, TIP145		—	—	1.0	
(V_{CB} = 80 V, I_E = 0)	TIP141, TIP146		—	—	1.0	
(V_{CB} = 100 V, I_E = 0)	TIP142, TIP147		—	—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 V)		I_{EBO}	—	—	2 0	mA
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 5.0 A, V_{CE} = 4.0 V)			1000	—	—	
(I_C = 10 A, V_{CE} = 4.0 V)			500	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 A, I_B = 10 mA)			—	—	2.0	
(I_C = 10 A, I_B = 40 mA)			—	—	3.0	
Base–Emitter Saturation Voltage (I_C = 10 A, I_B = 40 mA)		$V_{BE(sat)}$	—	—	3.5	Vdc
Base–Emitter On Voltage (I_C = 10 A, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	—	3.0	Vdc
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	(V_{CC} = 30 V, I_C = 5.0 A, I_B = 20 mA, Duty Cycle ≤ 2.0%, I_{B1} = I_{B2}, R_C & R_B Varied, T_J = 25°C)	t_d	—	0.15	—	μs
Rise Time		t_r	—	0.55	—	μs
Storage Time		t_s	—	2.5	—	μs
Fall Time		t_f	—	2.5	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 11. Switching Times Test Circuit

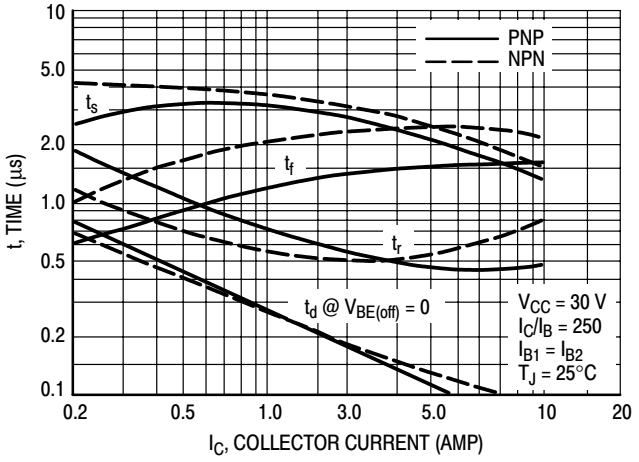


Figure 12. Switching Times

TYPICAL CHARACTERISTICS

NPN
TIP140, TIP141, TIP142

PNP
TIP145, TIP146, TIP147

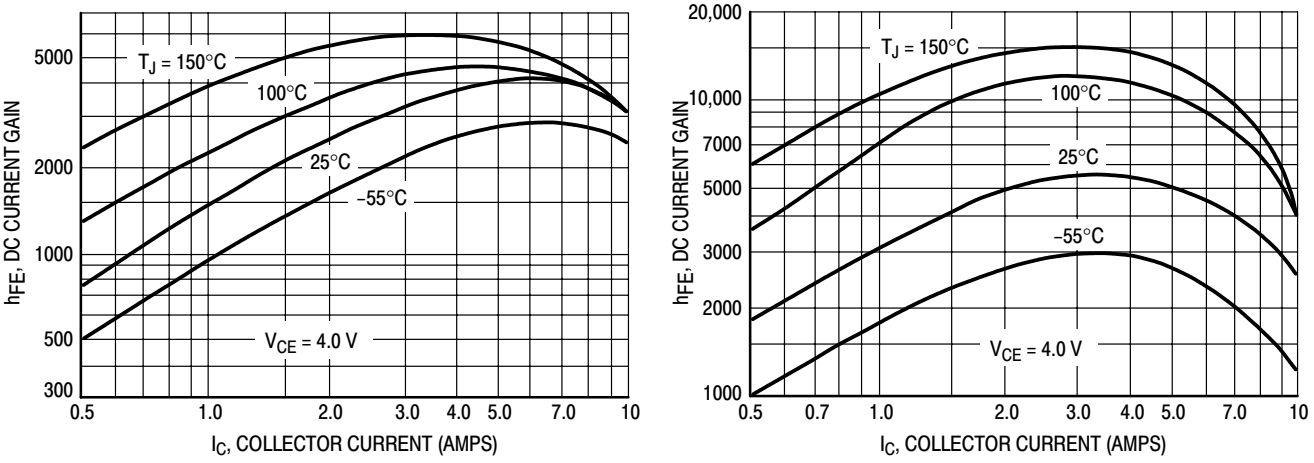


Figure 13. DC Current Gain versus Collector Current

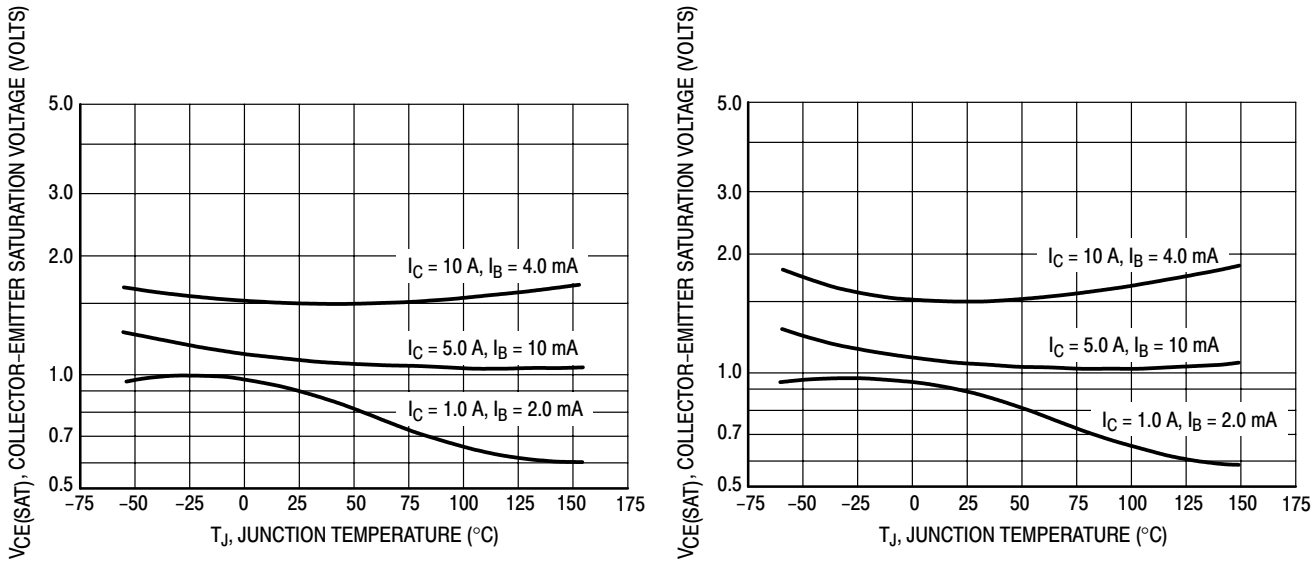


Figure 14. Collector−Emitter Saturation Voltage

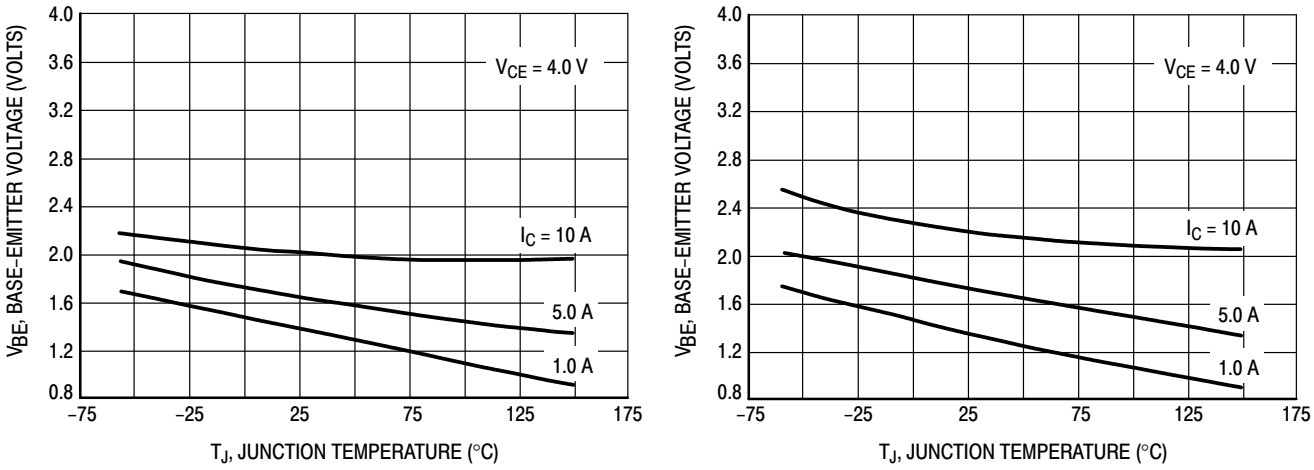


Figure 15. Base−Emitter Voltage

ACTIVE−REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

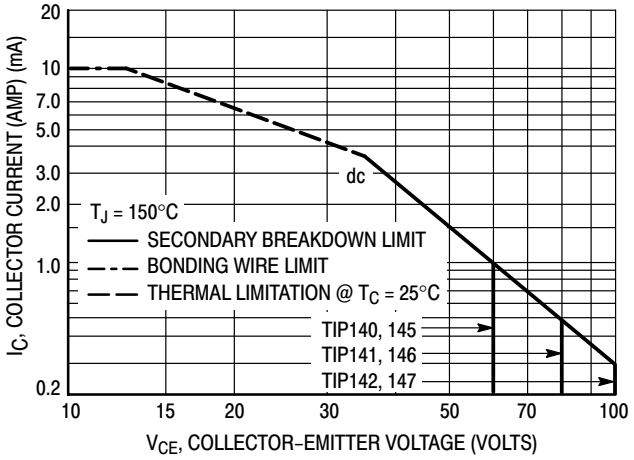


Figure 16. Active−Region Safe Operating Area

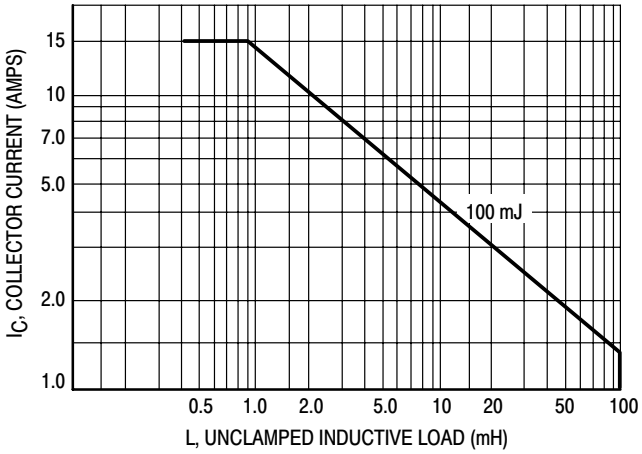
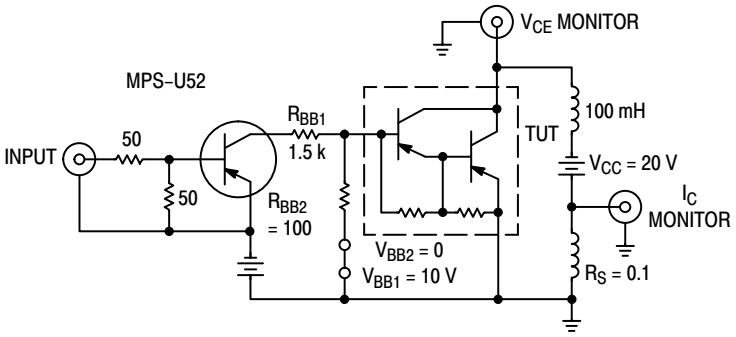
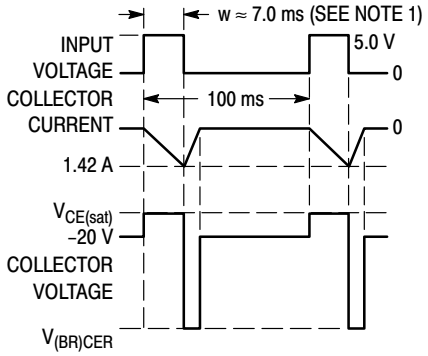


Figure 17. Unclamped Inductive Load



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE 1: Input pulse width is increased until I_{CM} = 1.42 A.
NOTE 2: For NPN test circuit reverse polarities.

Figure 18. Inductive Load

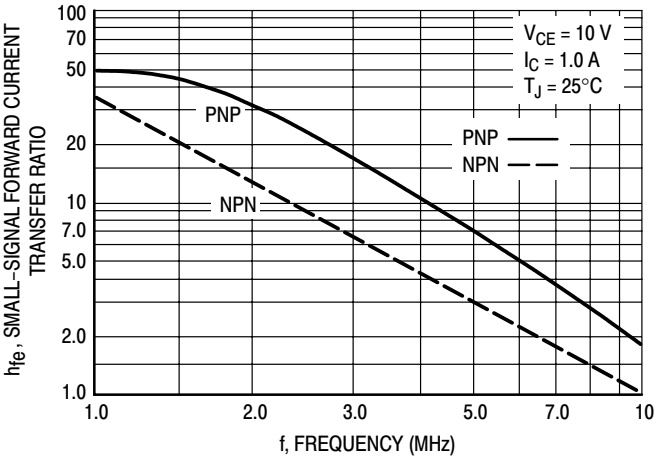


Figure 19. Magnitude of Common Emitter Small−Signal Short−Circuit Forward Current Transfer Ratio

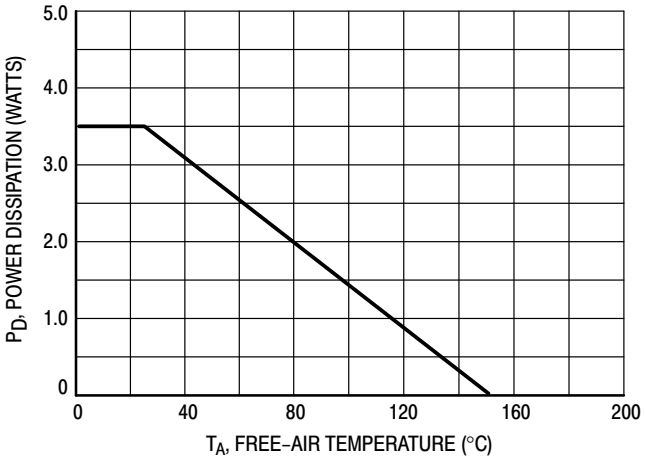


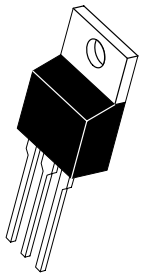
Figure 20. Free−Air Temperature Power Derating

Complementary Silicon Plastic Power Transistors

. . . designed for use in general purpose amplifier and switching applications. Compact TO–220 AB package.

NPN
TIP29B
TIP29C
PNP
TIP30B
TIP30C

1 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80–100 VOLTS
30 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	1.0 3.0		Adc
Base Current	I_B	0.4		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Unclamped Inductive Load Energy (See Note 3)	E	32		mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP29B, TIP30B TIP29C, TIP30C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)		I_{CEO}	—	0.3	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	 TIP29B, TIP30B TIP29C, TIP30C	I_{CES}	 — —	 200 200	µAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	40 15	— 75	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$	—	0.7	Vdc
Base–Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F = 10 Hz.

April, 2001 – Rev. 3
Publication Order Number:
TIP29B/D

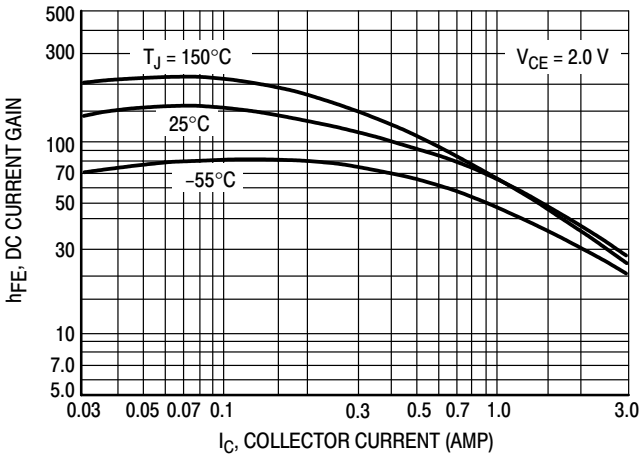


Figure 21. DC Current Gain

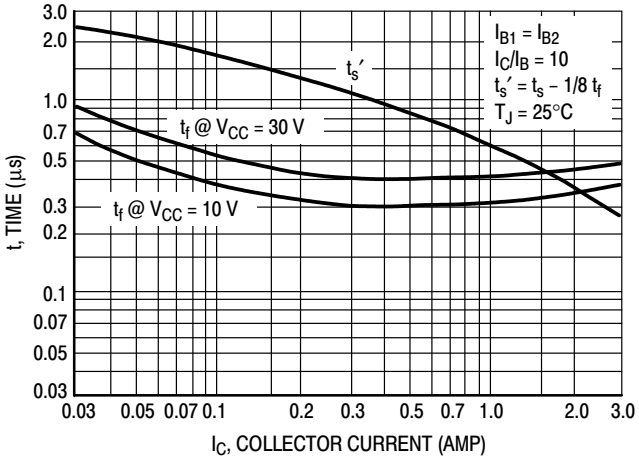


Figure 22. Turn−Off Time

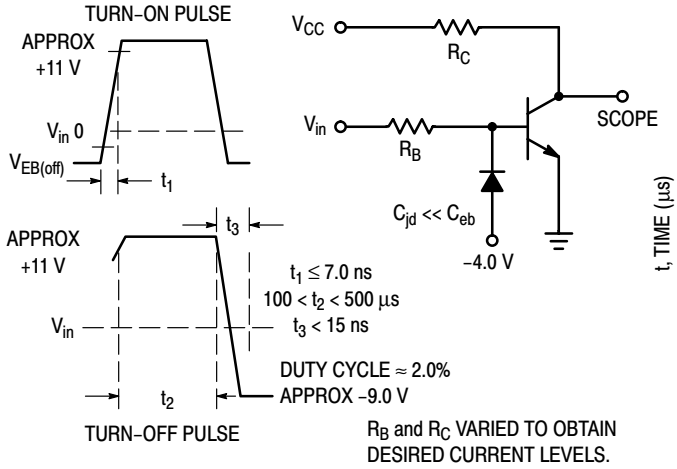


Figure 23. Switching Time Equivalent Circuit

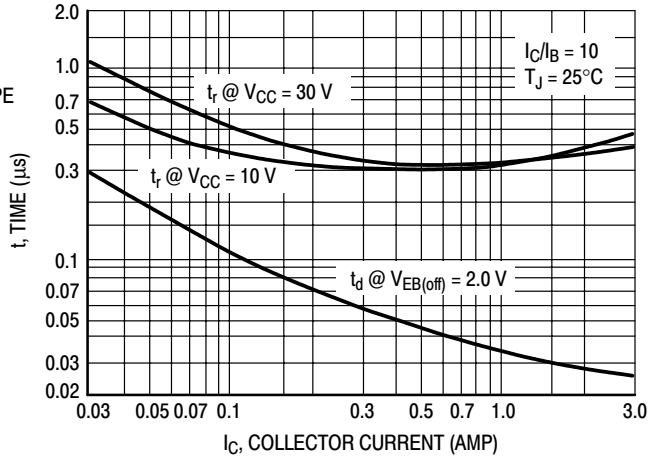


Figure 24. Turn−On Time

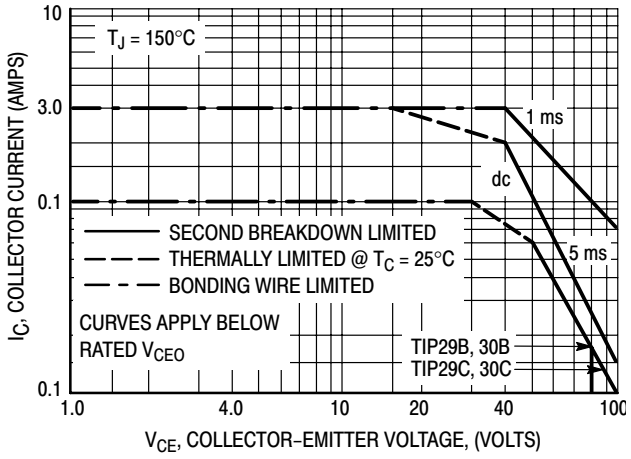


Figure 25. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 25 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

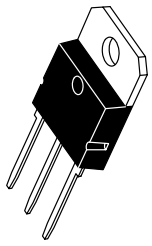
Complementary Silicon Power Transistors

. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain —
  h_{FE} = 20–70 @ I_C
  = 4.0 Adc
- Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C
  = 4.0 Adc
- Excellent Safe Operating Area

NPN
TIP3055
PNP
TIP2955

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
90 WATTS



CASE 340D–02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	1 5	Adc
Base Current	I_B	7.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.72	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	°C/W

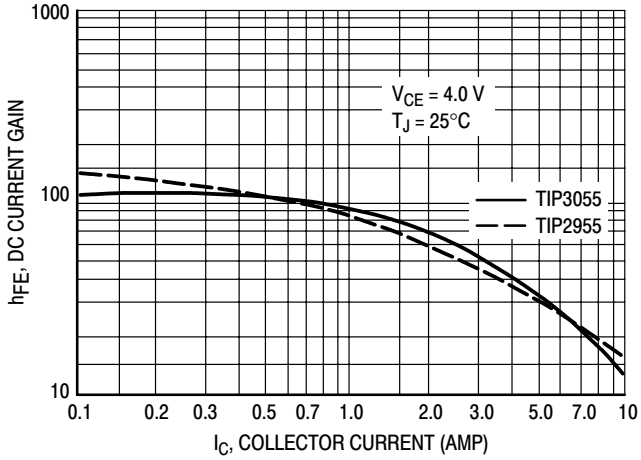


Figure 1. DC Current Gain

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, R_{BE} = 100 Ohms)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 3.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 30 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
Small–Signal Current Gain (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
NOTE: For additional design curves, refer to electrical characteristics curves of 2N3055.

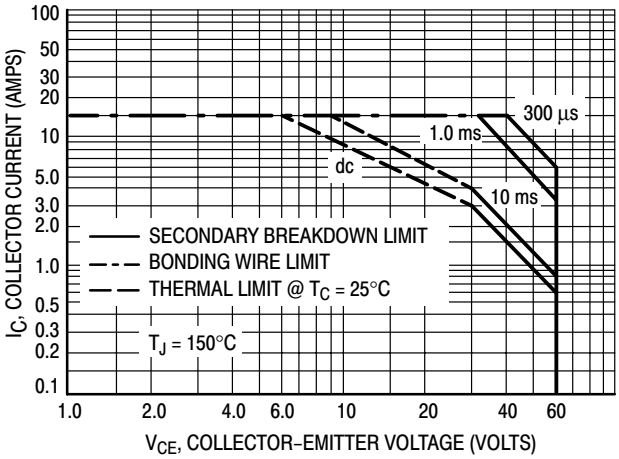


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

Complementary Silicon Plastic Power Transistors

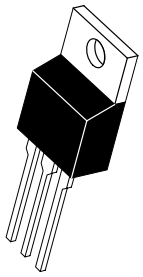
. . . designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C
  = 3.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP31A, TIP32A
  = 80 Vdc (Min) — TIP31B, TIP32B
  = 100 Vdc (Min) — TIP31C, TIP32C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C
  = 500 mAdc
- Compact TO–220 AB Package

NPN
TIP31A
TIP31B*
MJF31C*
PNP
TIP31C
TIP32A*
TIP32B*
TIP32C
MJF32C

***ON Semiconductor Preferred Device**

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80–100 VOLTS
40 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP31A TIP32A	TIP318 TIP32B	TIP31C TIP32C	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	3.0 5.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	32			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

(1) I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω..

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 4
Publication Order Number:
TIP31A/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP31A, TIP32A		60	—	
	TIP31B, TIP32B		80	—	
	TIP31C, TIP32C		100	—	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	TIP31A, TIP32A	I_{CEO}	—	0.3	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C		—	0.3	
	TIP32B, TIP32C		—	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		—	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		—	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	25	—	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	—	1.2	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

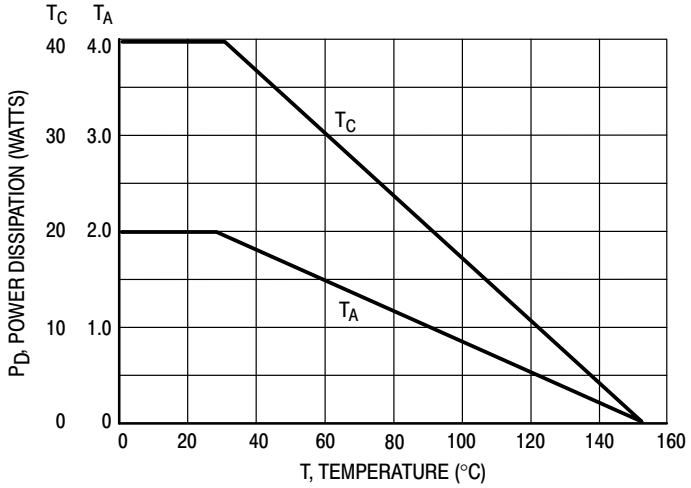


Figure 1. Power Derating

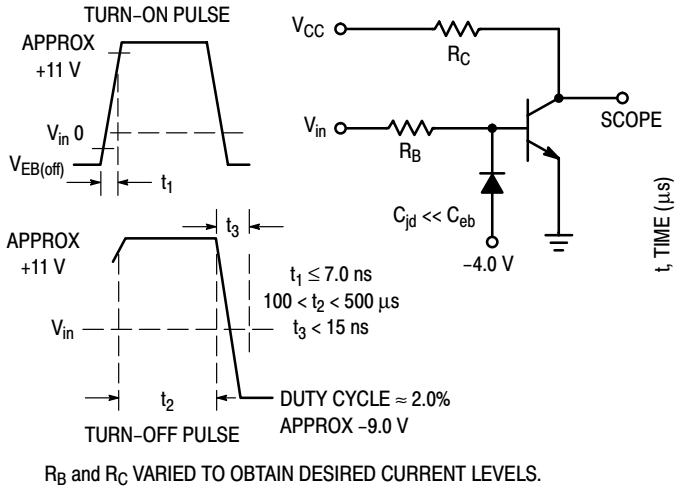


Figure 2. Switching Time Equivalent Circuit

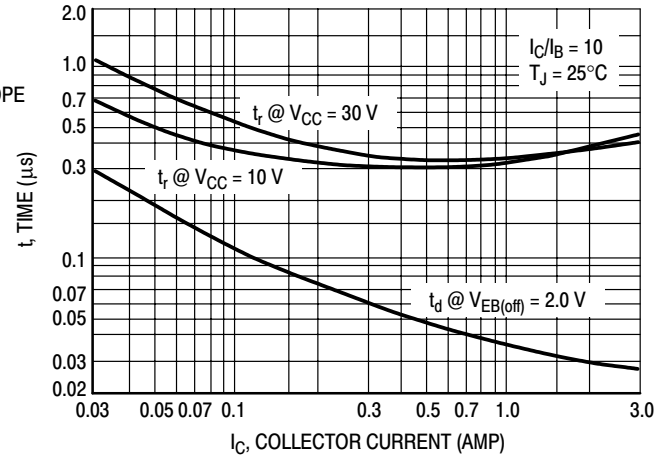


Figure 3. Turn−On Time

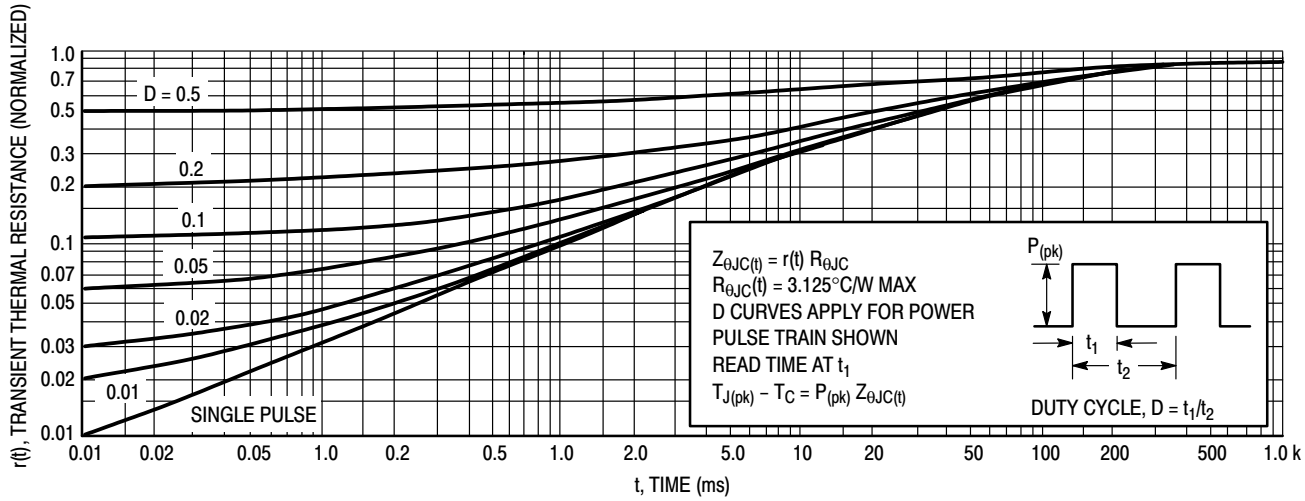


Figure 4. Thermal Response

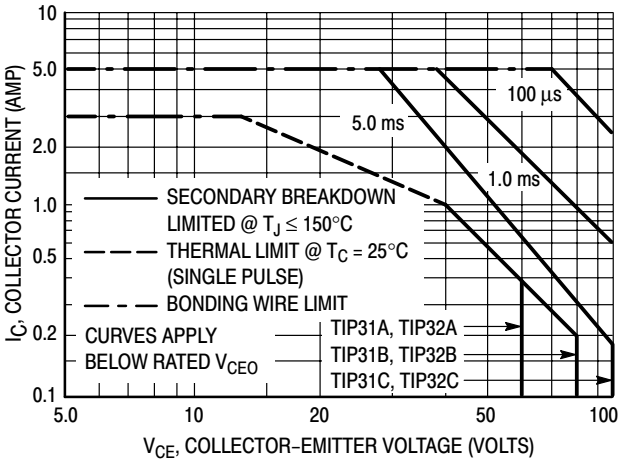


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

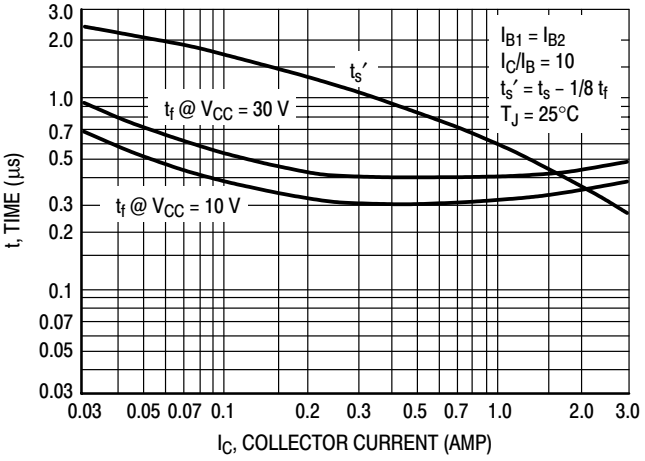


Figure 6. Turn–Off Time

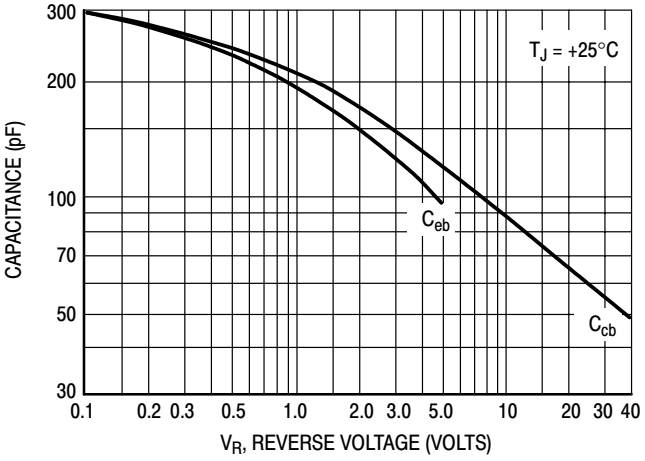


Figure 7. Capacitance

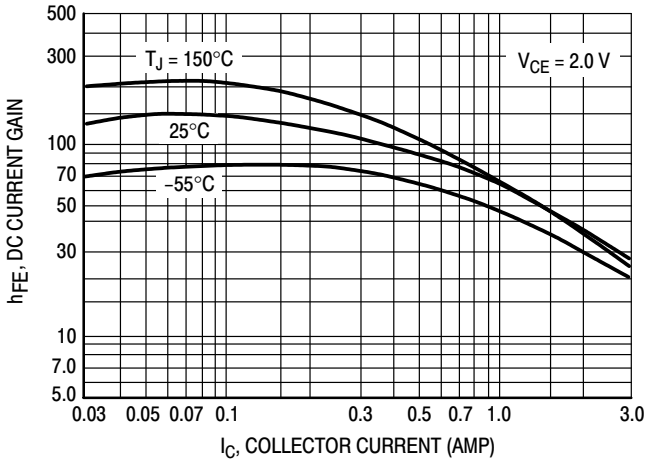


Figure 8. DC Current Gain

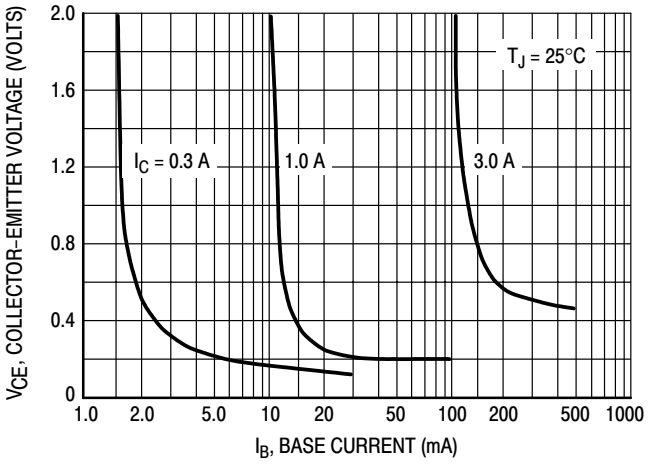


Figure 9. Collector Saturation Region

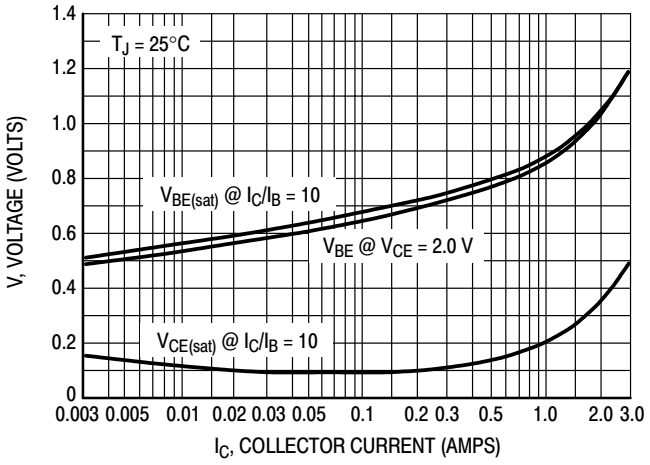


Figure 10. “On” Voltages

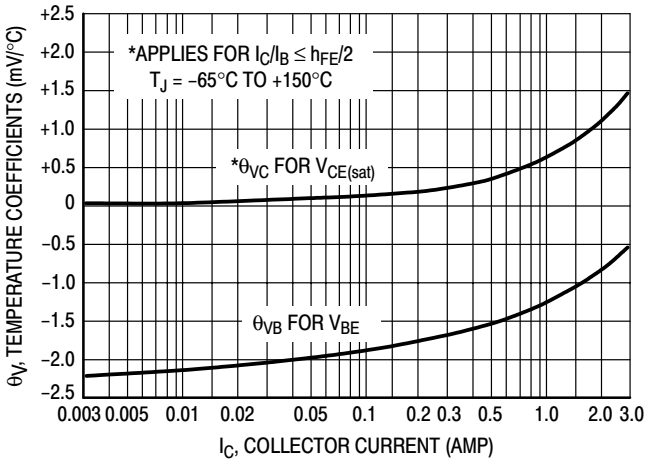


Figure 11. Temperature Coefficients

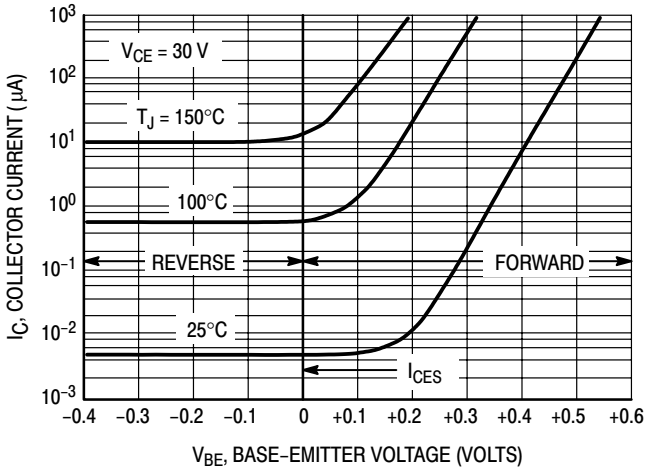


Figure 12. Collector Cut−Off Region

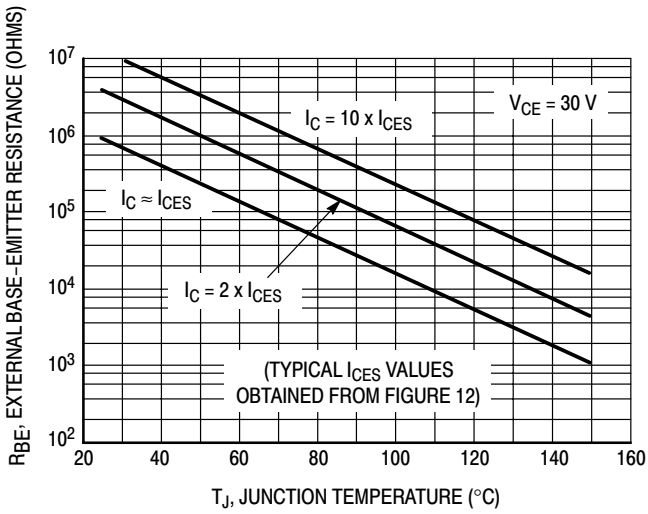


Figure 13. Effects of Base−Emitter Resistance

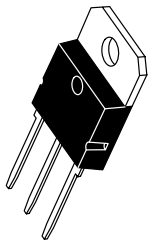
Complementary Silicon High-Power Transistors

. . . for general–purpose power amplifier and switching applications.

- 10 A Collector Current
- Low Leakage Current —
  I_{CEO} = 0.7 mA @ 60 V
- Excellent dc Gain —
  h_{FE} = 40 Typ @ 3.0 A
- High Current Gain Bandwidth Product —
  h_{fe} = 3.0 min @ I_C
  = 0.5 A,
  f = 1.0 MHz

NPN
TIP33C
PNP
TIP34C

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
100 VOLTS
80 WATTS



CASE 340D–02
TO–218AC

MAXIMUM RATINGS

Rating	Symbol	TIP33C TIP34C	Unit
Collector–Emitter Voltage	V_{CEO}	100 V	Vdc
Collector–Base Voltage	V_{CB}	100 V	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C	10 15	Adc
Base Current — Continuous	I_B	3.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 80 0.64	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

May, 2001 – Rev. 0
Publication Order Number:
TIP33C/D

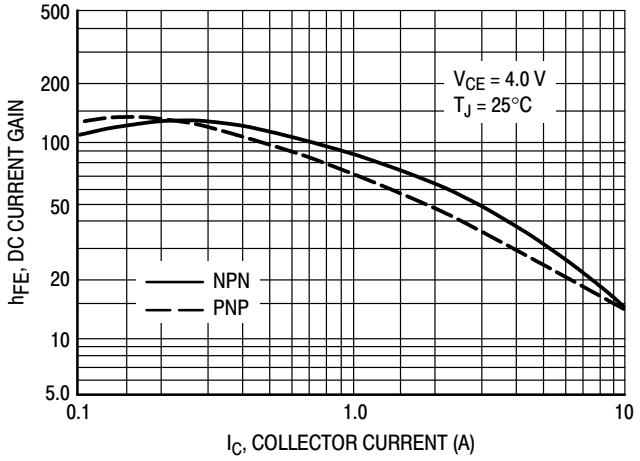


Figure 1. DC Current Gain

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 60 V, I_B = 0)	I_{CEO}	—	0.7	mA
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	—	0.4	mA
Emitter–Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 A, V_{CE} = 4.0 V) (I_C = 3.0 A, V_{CE} = 4.0 V)	h_{FE}	40 20	— 100	—
Collector–Emitter Saturation Voltage (I_C = 3.0 A, I_B = 0.3 A) (I_C = 10 A, I_B = 2.5 A)	$V_{CE(sat)}$	— —	1.0 4.0	Vdc
Base–Emitter On Voltage (I_C = 3.0 A, V_{CE} = 4.0 V) (I_C = 10 A, V_{CE} = 4.0 V)	$V_{BE(on)}$	— —	1.6 3.0	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	20	—	—
Current–Gain — Bandwidth Product (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

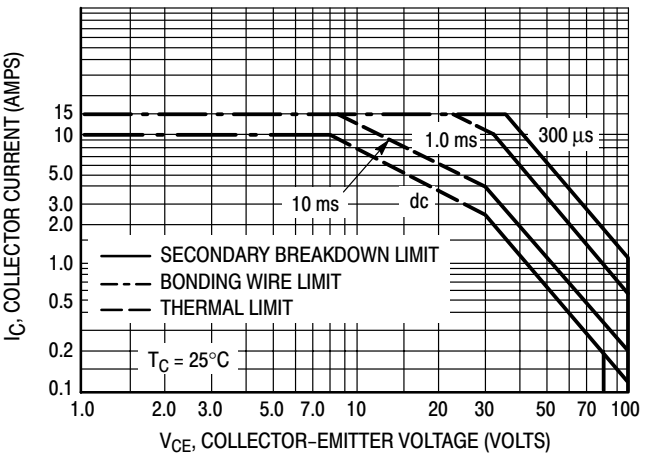


Figure 2. Maximum Rated Forward Bias Safe Operating Area

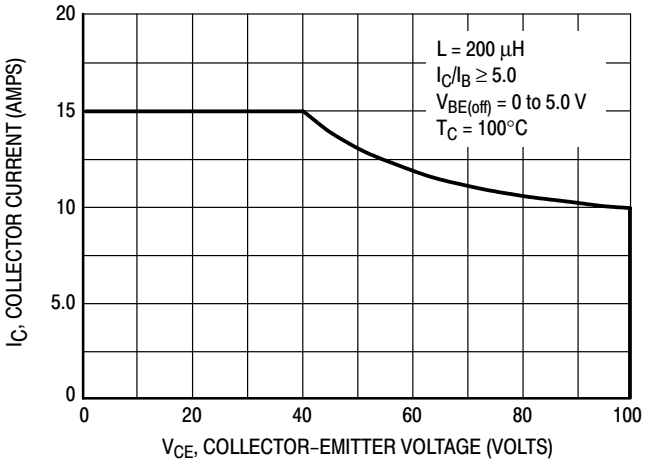


Figure 3. Maximum Rated Forward Bias Safe Operating Area

FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for $T_C > 25°C$.

REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn–off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

Complementary Silicon High-Power Transistors

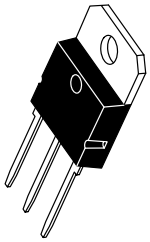
. . . for general–purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current —
  I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent DC Gain —
  h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product —
  $|h_{fe}|$ = 3.0 min @ I_C
  = 1.0 A, f = 1.0 MHz

NPN
TIP35A
TIP35B*
TIP35C*
PNP
TIP36A
TIP36B*
TIP36C*

***ON Semiconductor Preferred Device**

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS 125 WATTS



CASE 340D–02
TO–218AC

MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector–Emitter Voltage	V_{CEO}	60 V	80 V	100 V	Vdc
Collector–Base Voltage	V_{CB}	60 V	80 V	100 V	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	25 40			Adc
Base Current — Continuous	I_B	5.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C
Unclamped Inductive Load	E_{SB}	90			mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2001 – Rev. 3
Publication Order Number:
TIP35A/D

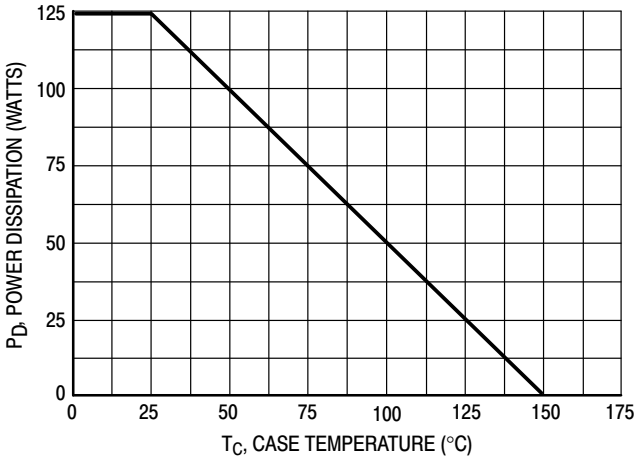


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	 TIP35A, TIP36A TIP35B, TIP36B TIP35C, TIP36C	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) (V_{CE} = 60 V, I_B = 0)	 TIP35A, TIP36A TIP35B, TIP35C, TIP36B, TIP36C	I_{CEO}	 — —	 1.0 1.0	mA
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.7	mA
Emitter–Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.5 A, V_{CE} = 4.0 V) (I_C = 15 A, V_{CE} = 4.0 V)		h_{FE}	 25 15	 — 75	—
Collector–Emitter Saturation Voltage (I_C = 15 A, I_B = 1.5 A) (I_C = 25 A, I_B = 5.0 A)		$V_{CE(sat)}$	 — —	 1.8 4.0	Vdc
Base–Emitter On Voltage (I_C = 15 A, V_{CE} = 4.0 V) (I_C = 25 A, V_{CE} = 4.0 V)		$V_{BE(on)}$	 — —	 2.0 4.0	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	25	—	—
Current–Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

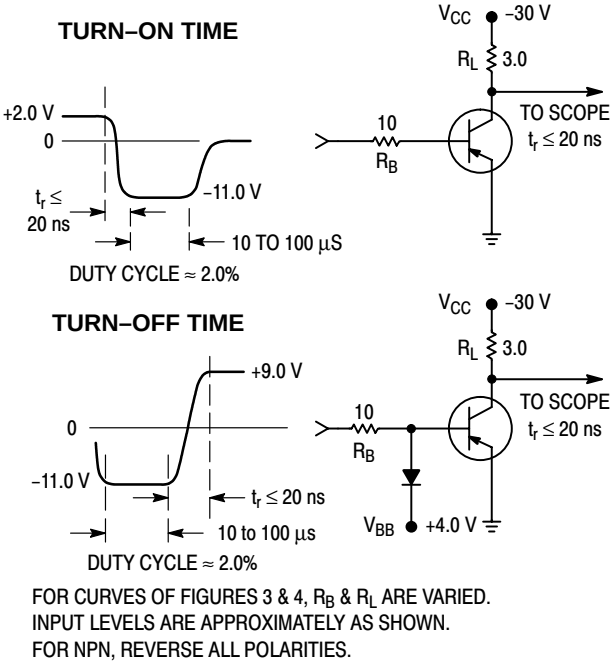


Figure 2. Switching Time Equivalent Test Circuits

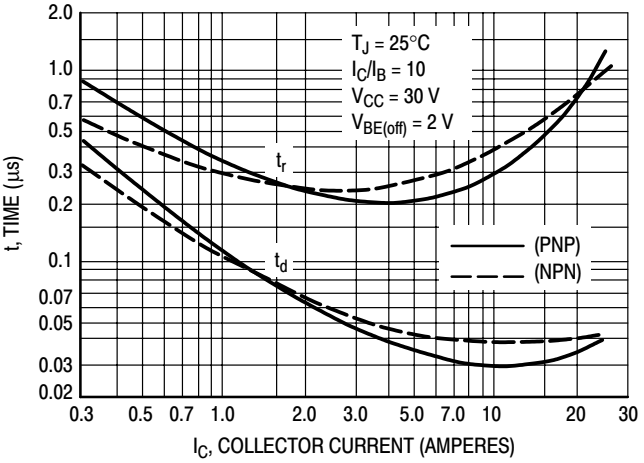


Figure 3. Turn–On Time

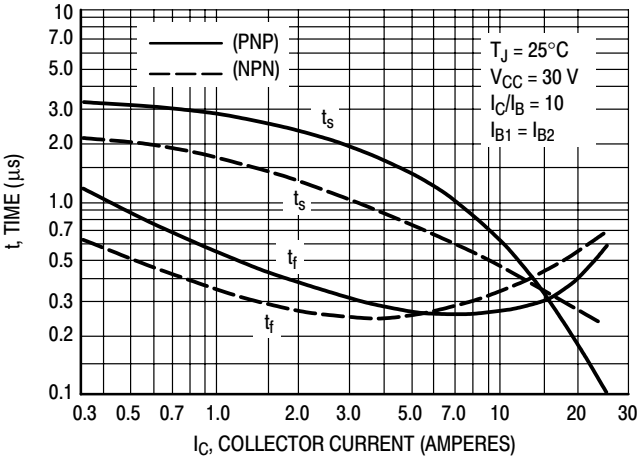


Figure 4. Turn–Off Time

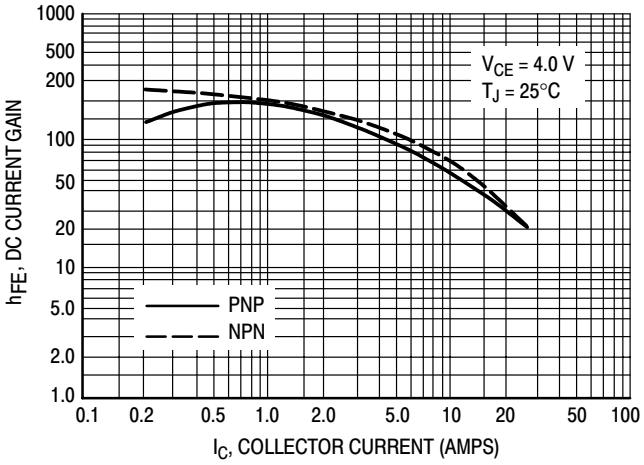


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

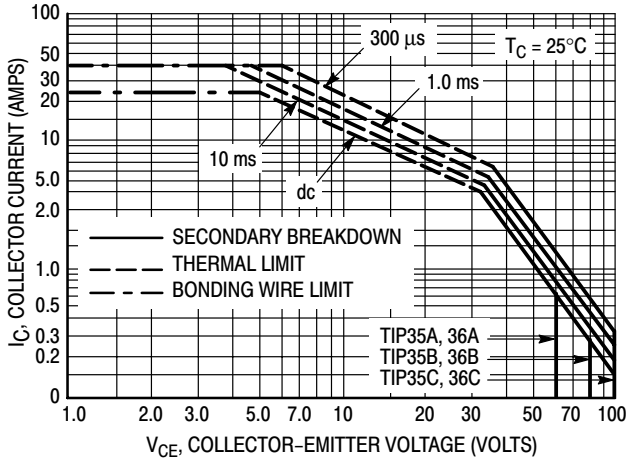


Figure 6. Maximum Rated Forward Bias Safe Operating Area

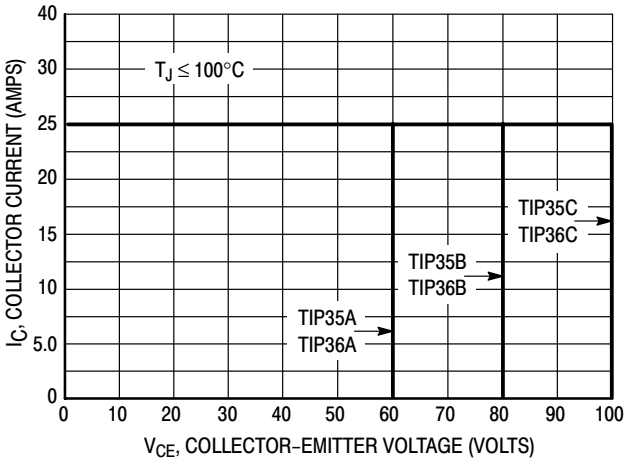
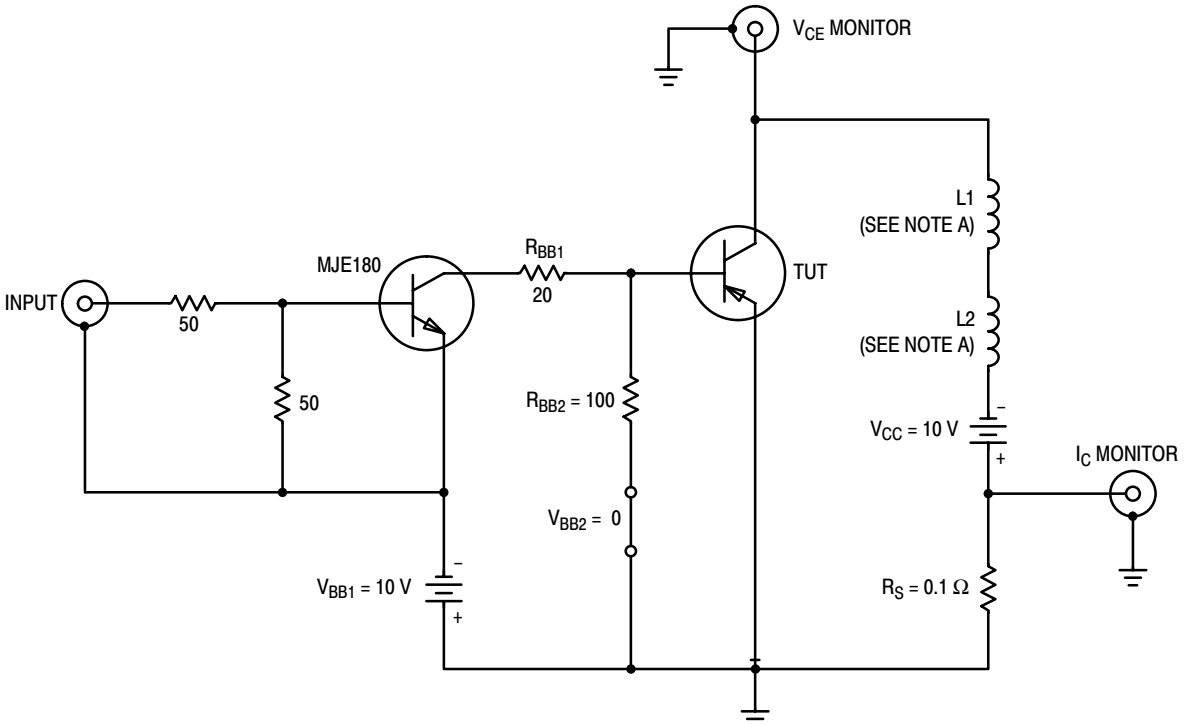
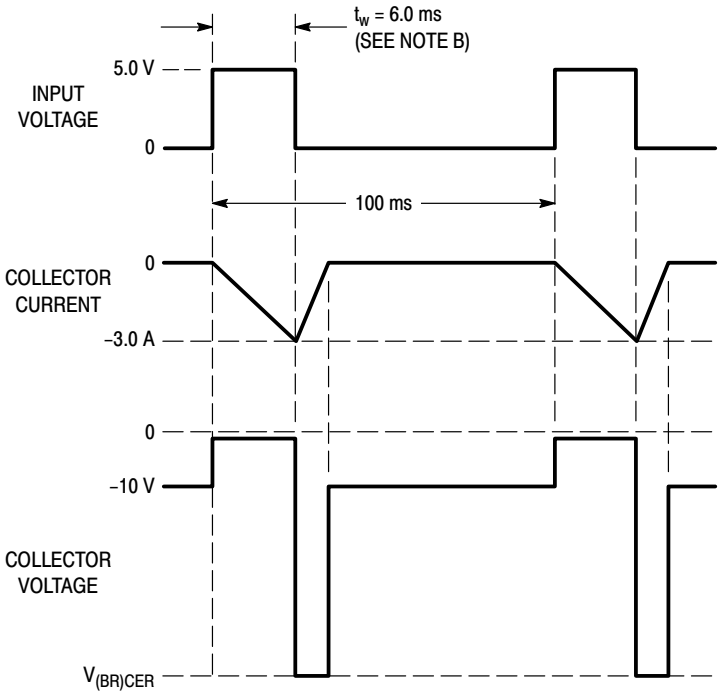


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C–2688, or equivalent.
B. Input pulse width is increased until I_{CM} = –3.0 A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

Complementary Silicon Plastic Power Transistors

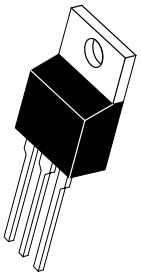
. . . designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP41A, TIP42A
  = 80 Vdc (Min) — TIP41B, TIP42B
  = 100 Vdc (Min) — TIP41C, TIP42C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
TIP41A
TIP41B*
TIP41C*
PNP
TIP42A
TIP42B*
TIP42C*

***ON Semiconductor Preferred Device**

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80–100 VOLTS
65 WATTS



CASE 221A–09
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	6 10			Adc
Base Current	I_B	2.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	62.5			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

(1) I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP41A, TIP42A TIP41B, TIP41C TIP42B, TIP42C	I_{CEO}	— — —	0.7 0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I_{CES}	 — — —	 400 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	— 75	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

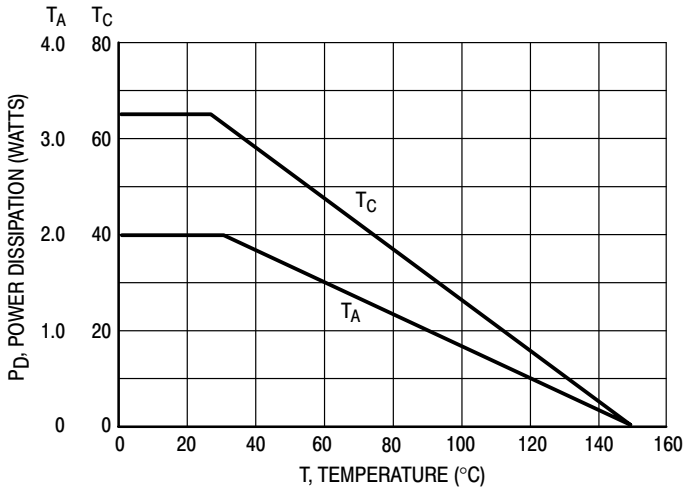
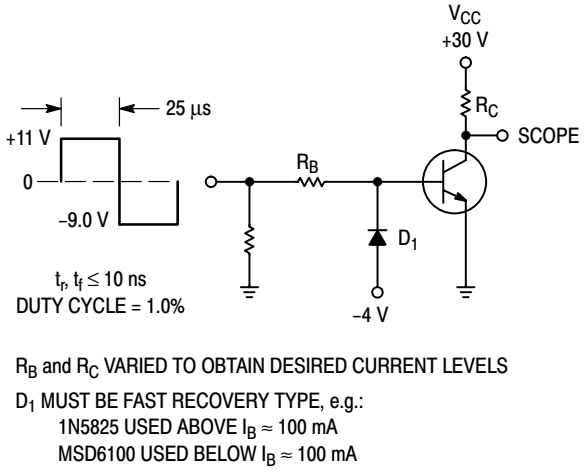


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Figure 2. Switching Time Test Circuit

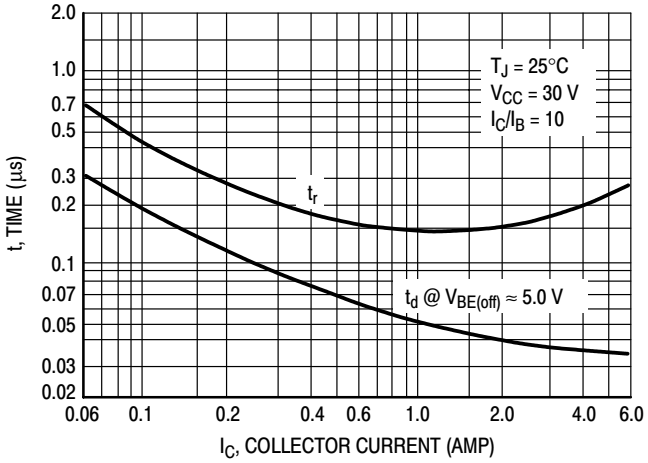


Figure 3. Turn−On Time

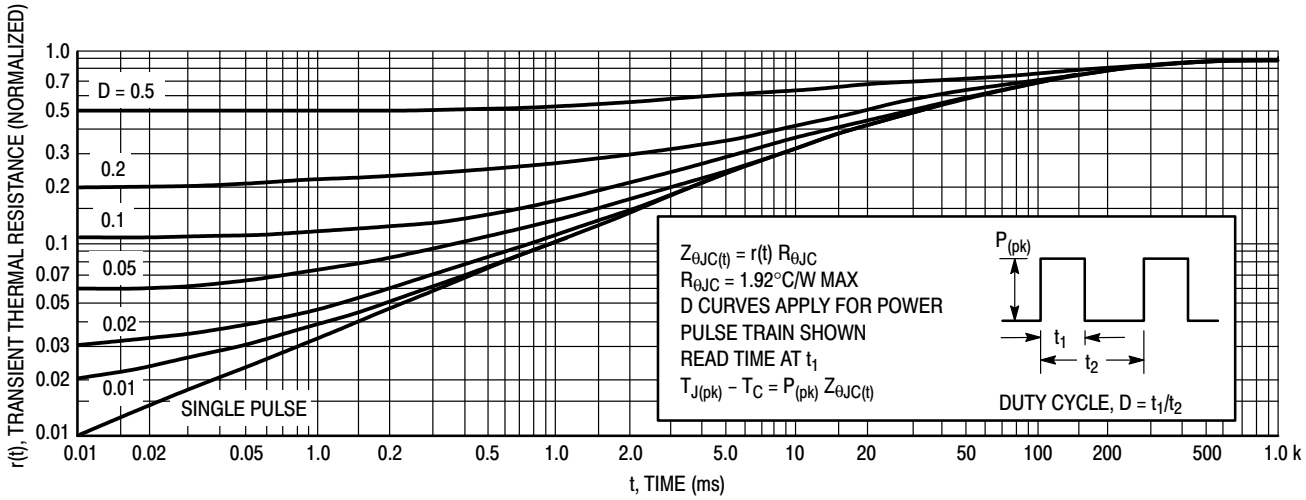


Figure 4. Thermal Response

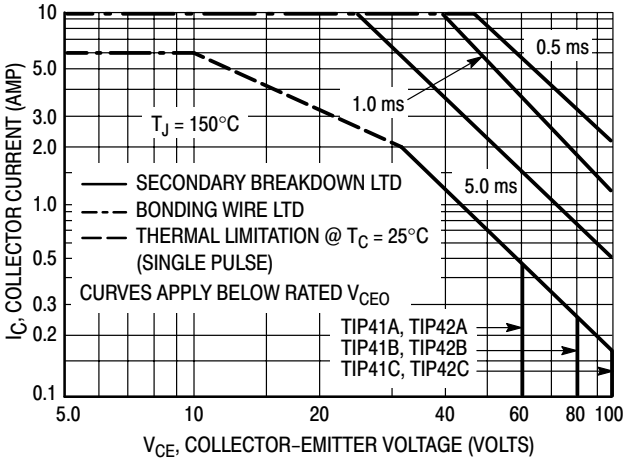


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

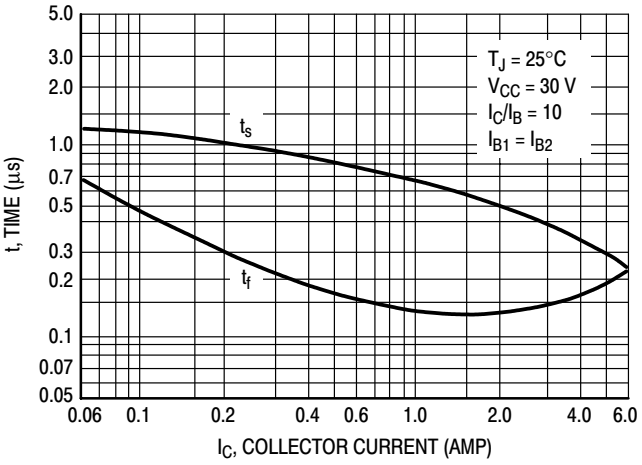


Figure 6. Turn–Off Time

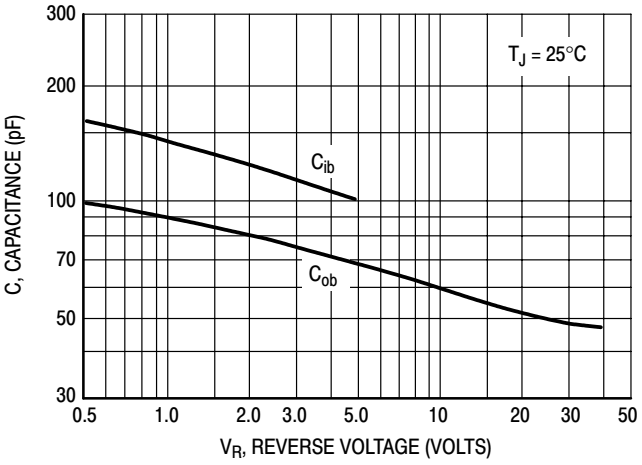


Figure 7. Capacitance

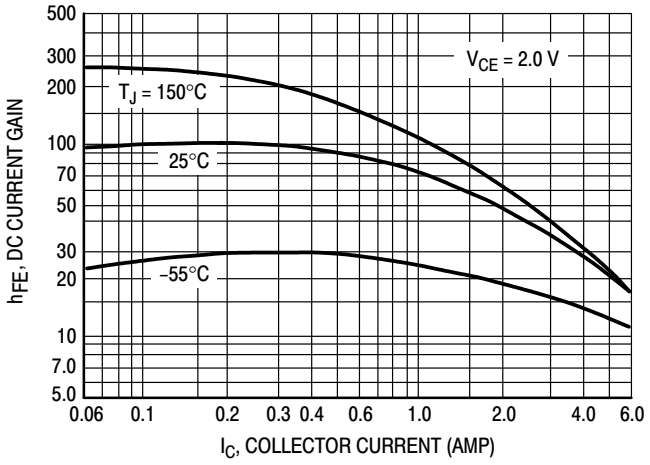


Figure 8. DC Current Gain

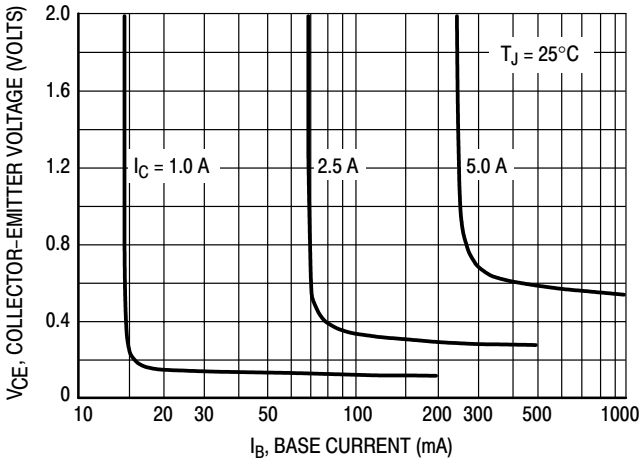


Figure 9. Collector Saturation Region

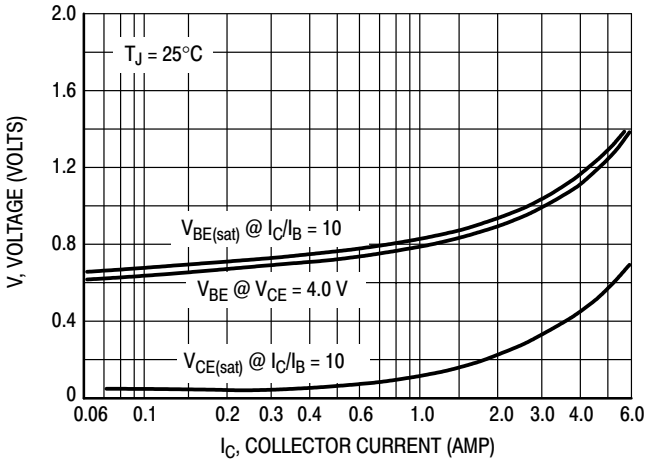


Figure 10. “On” Voltages

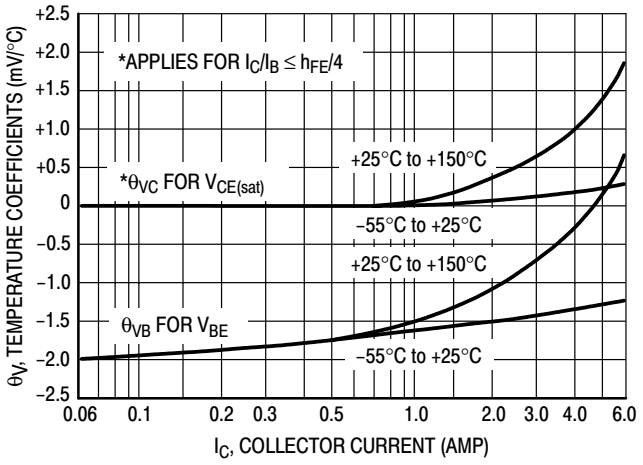


Figure 11. Temperature Coefficients

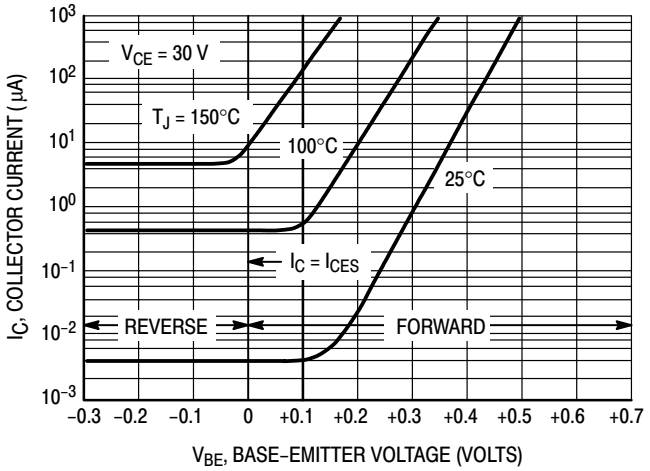


Figure 12. Collector Cut−Off Region

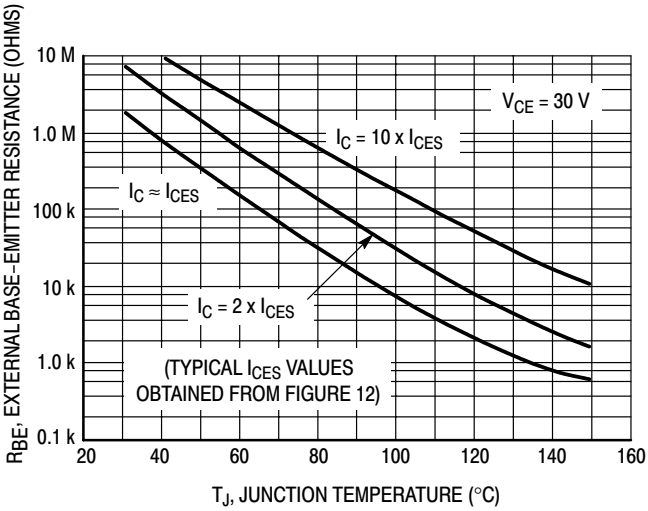


Figure 13. Effects of Base−Emitter Resistance

High Voltage NPN Silicon Power Transistors

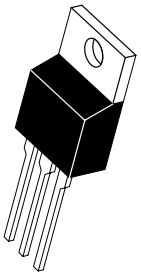
. . . designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- 250 V to 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO–220 Plastic Package

TIP47*
TIP48*
TIP50*

*ON Semiconductor Preferred Device

1.0 AMPERE
POWER TRANSISTORS
NPN SILICON
250–300–350–400 VOLTS
40 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	TIP47	TIP48	TIP50	Unit
Collector–Emitter Voltage	V_{CEO}	250	300	400	Vdc
Collector–Base Voltage	V_{CB}	350	400	500	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	1.0 2.0			Adc
Base Current	I_B	0.6			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inducting Load Energy (See Figure 8)	E	20			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

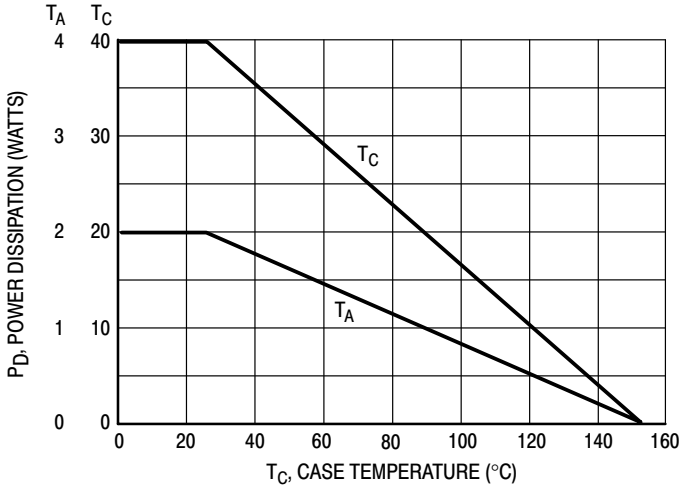


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 4
Publication Order Number:
TIP47/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP47 TIP48 TIP50	$V_{CEO(sus)}$	250 300 400	— — —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 TIP47 TIP48 TIP50	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 400 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	 TIP47 TIP48 TIP50	I_{CES}	 — — —	 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 —	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	—	MHz
Small–Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2.0%.

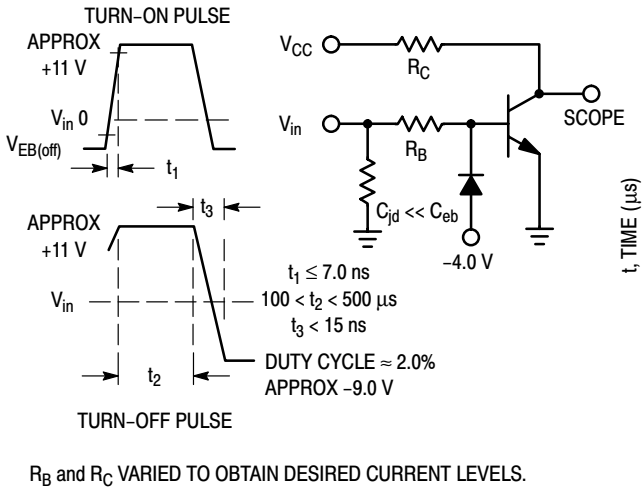


Figure 2. Switching Time Equivalent Circuit

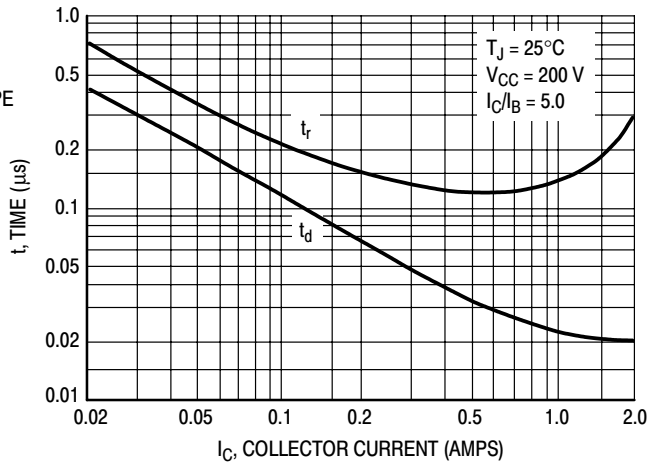


Figure 3. Turn–On Time

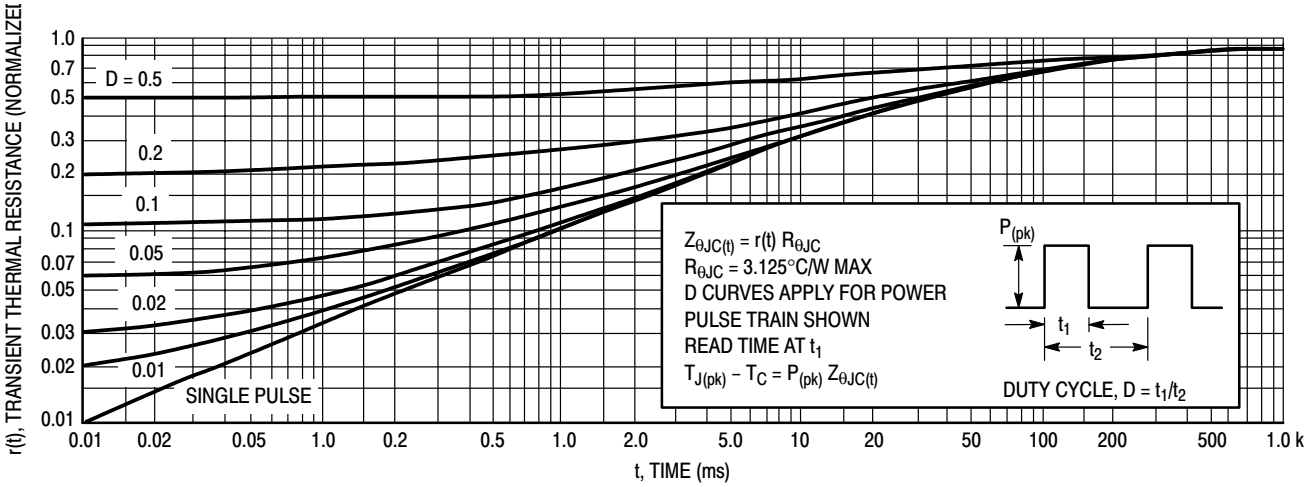


Figure 4. Thermal Response

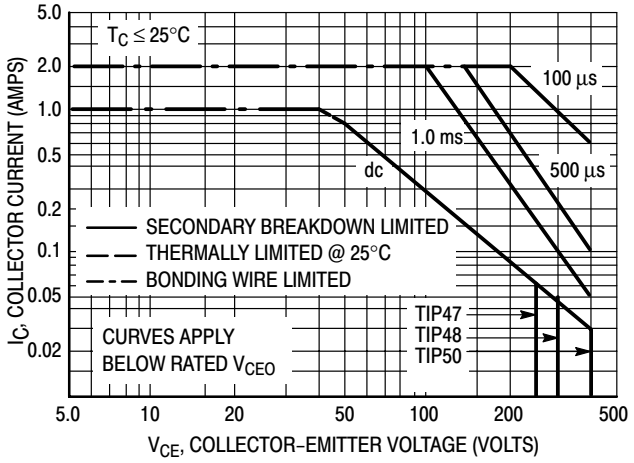


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

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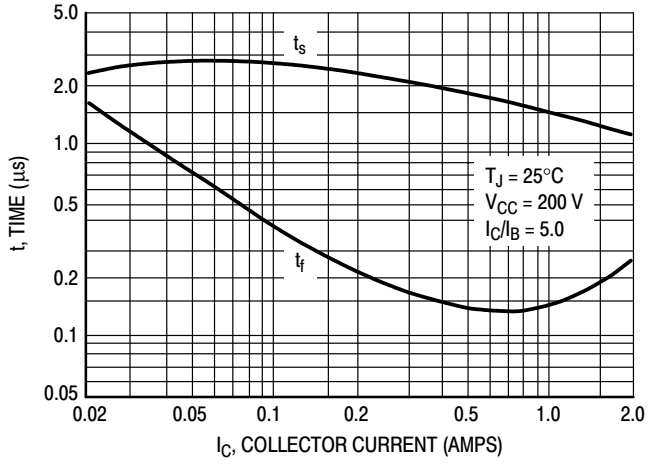


Figure 6. Turn–Off Time

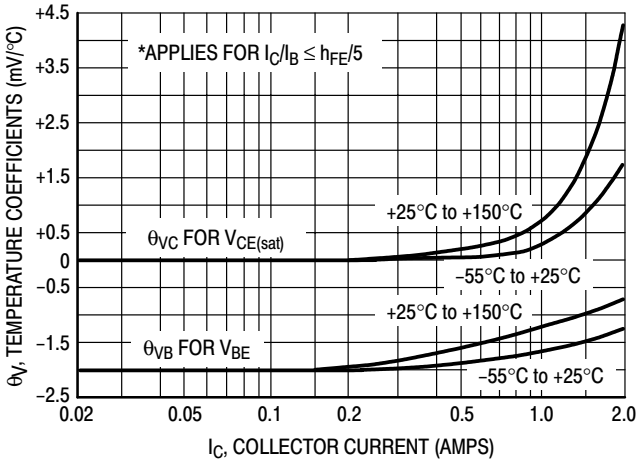
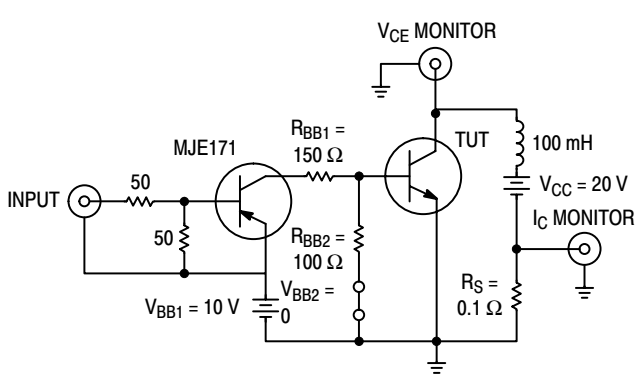
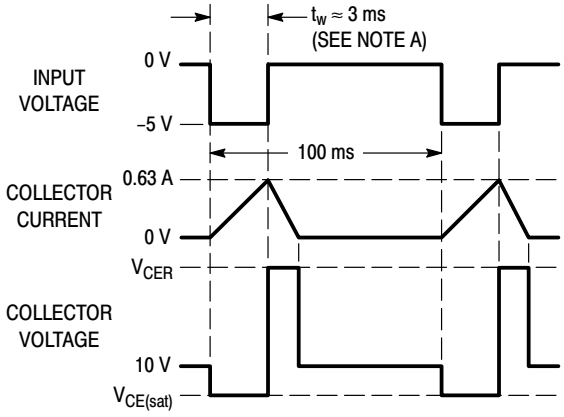


Figure 7. Temperature Coefficients





Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Figure 8. Inductive Load Switching

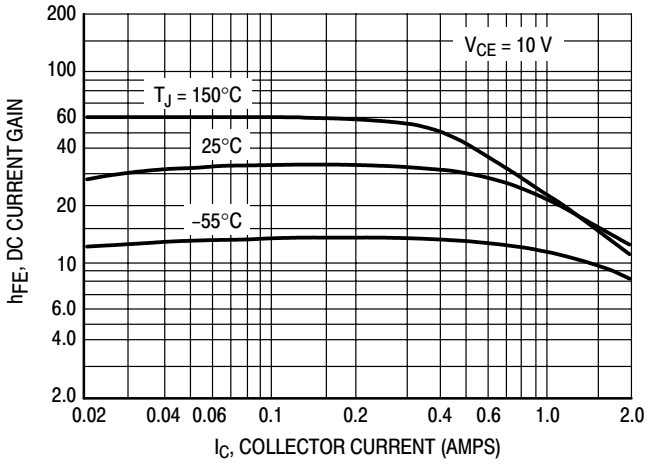


Figure 9. DC Current Gain

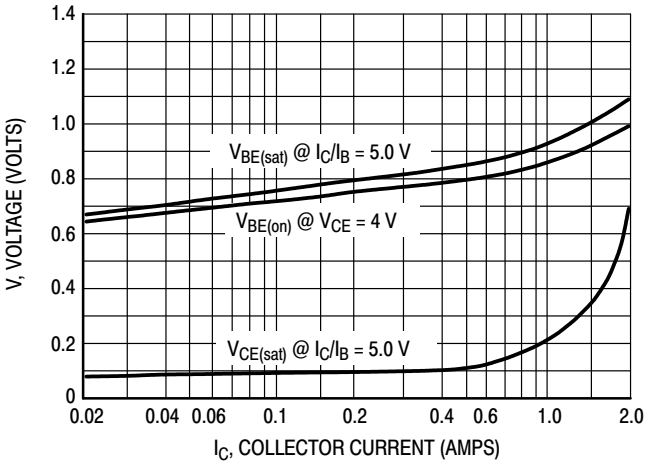


Figure 10. “On” Voltages

CHAPTER 3
Applications Information and Case Outlines

AN1040/D

A High–Performance Video Amplifier for High Resolution CRT Applications

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

Prepared by: Bill Roehr

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic–packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 1 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent – an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet–metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all, poor mounting practices would be covered.

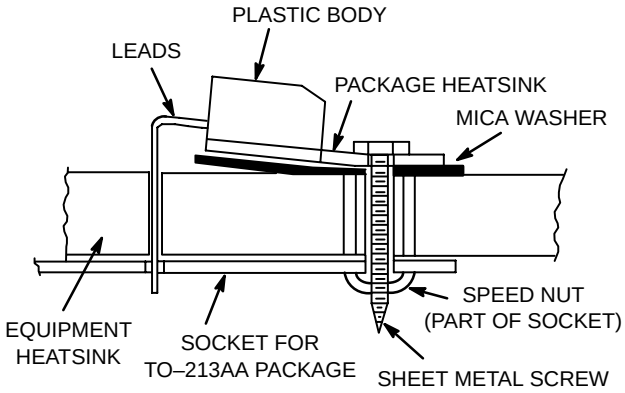


Figure 1. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)

In many situations, the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

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AN1040/D

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high–power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, Δh/TlR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

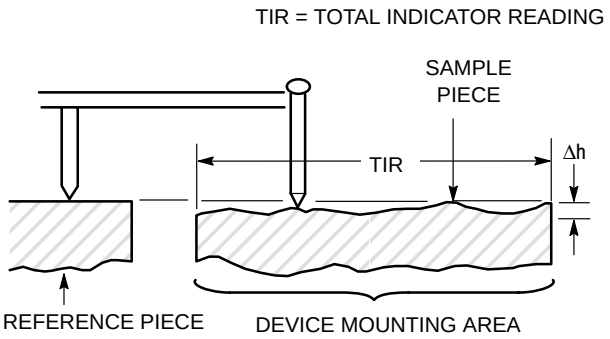


Figure 2. Surface Flatness Measurement

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy, Inc., using a copper TO–204 (TO–3) package with a typical 32–microinch finish, showed that heatsink finishes between 16 and 64 μ–in caused less than ± 2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high–power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical, but negligible thermal insulation; it need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromateacid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise, the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock–marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal, therefore, they partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well–mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct, a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range is less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil®, a dry graphite compound, is shown in the data of Figure 3 through Figure 6. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called Kon–Dux™. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Table 1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed in ON Semiconductor Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions.
Unless otherwise noted, the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal–to–Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In–Lb	Dry	Lubed	Dry	Lubed	Type	See Note
DO–203AA, TO–210AA TO–208AB	10–32 Stud 7/16″ Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO–203AB, TO–210AC TO–208	1/4–28 Stud 11/16″ Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO–208AA	Pressfit, 1/2″	–	0.15	0.1	–	–	–	
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–213AA (TO–66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO–126	Thermopad 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO–220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figure 3 through Figure 7 for additional data on TO–3 and TO–220 packages.
2. Screw not insulated. See Figure 20.

INSULATION CONSIDERATIONS

Since most power semiconductors use vertical device construction, it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non–isolated packages. In these situations, insulators are used to isolate the individual components from the heatsink. Newer packages, such as the ON Semiconductor FULLPAK™ and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials, reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, are shown in Figure 3 through Figure 6, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3 through Figure 6, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraded, as the dust is highly toxic.) Thermafilm® is a filled polymide material which is used for isolation (variation of Kapton®). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost, but it certainly should be used with grease.

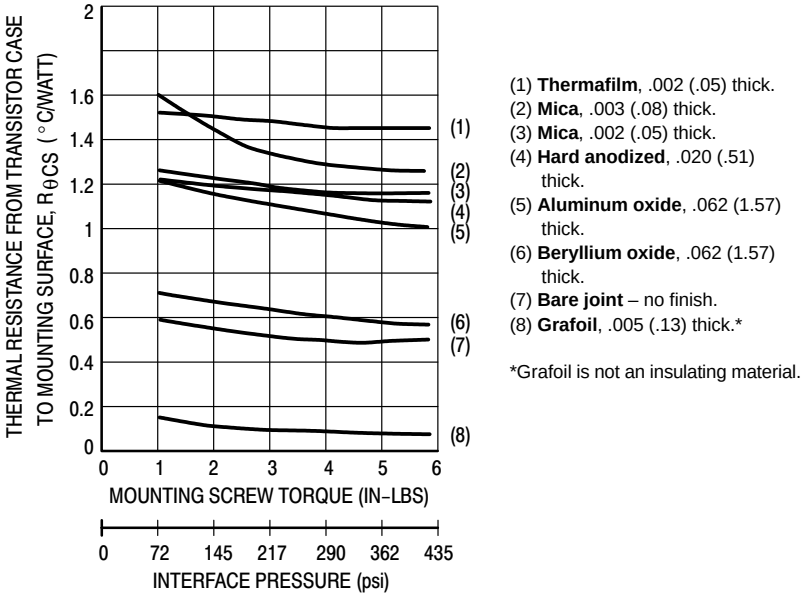


Figure 3. TO–204AA (TO–3) Without Thermal Grease

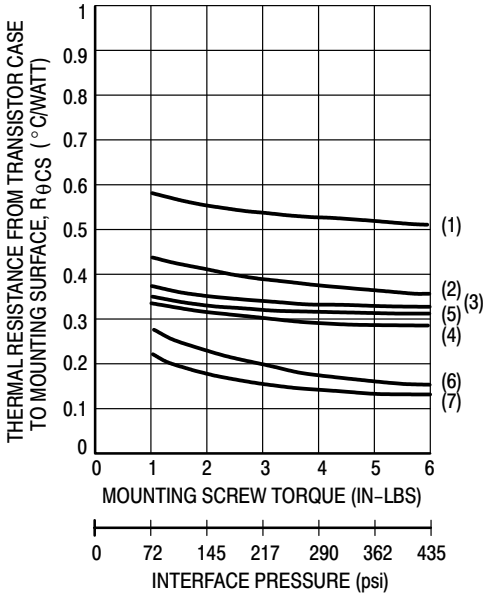


Figure 4. TO–204AA (TO–3) With Thermal Grease

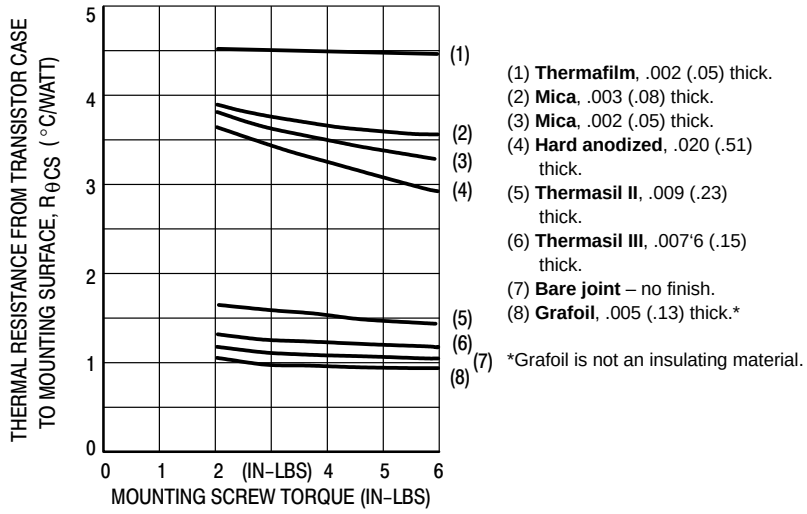


Figure 5. TO–220 Without Thermal Grease

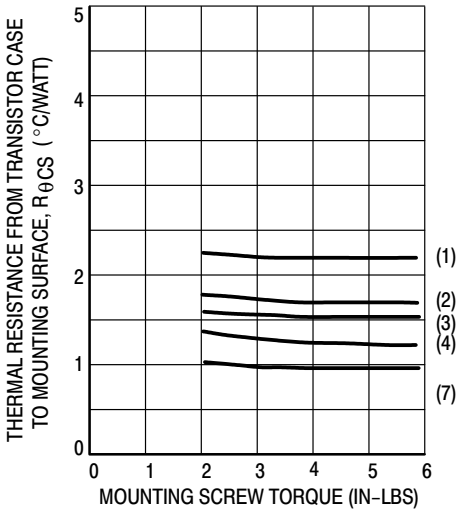


Figure 6. TO–220 With Thermal Grease

INTERFACE THERMAL RESISTANCE FOR TO–204, TO–3, AND TO–220 PACKAGES USING DIFFERENT INSULATING MATERIALS AS A FUNCTION OF MOUNTING SCREW TORQUE (DATA COURTESY THERMALLOY)

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figure 5 and Figure 6, it can be noted that Thermasil™, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

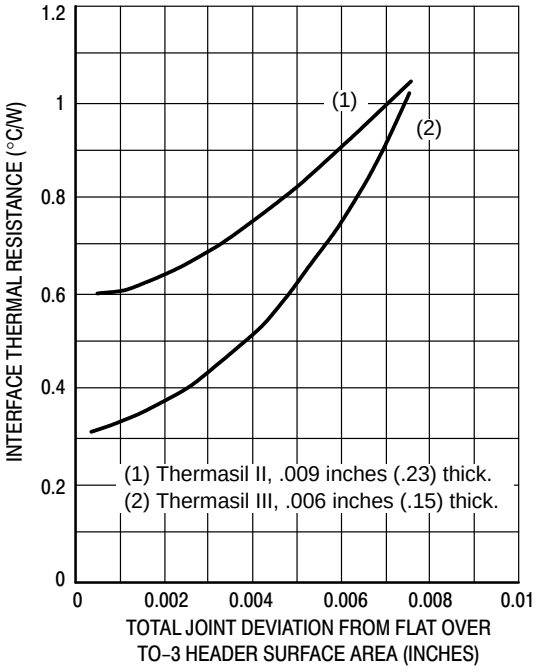
A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10® pad, for example, is described as having about 2/3 the interface resistance of the Sil–Pad® 1000 which would place its performance close to the Chomerics 1671 pad. Aavid also offers an isolated pad called Rubber–Duc™, however, it is only available vulcanized to a heatsink and, therefore, was not included in the comparison. Published data from Aavid shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified, so a comparison cannot be made with other data in this note.

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173–7	.790	1.175
Bergquist	Sil–Pad K–4®	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil–Pad 400–9®	.735	1.205
Thermalloy	Thermasil II	.680	1.045
Shin–Etsu	TC–30AG	.664	1.260
Bergquist	Sil–Pad 400–7®	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174–9	.574	.755
Bergquist	Sil–Pad 1000®	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermasil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86–1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown in Figure 7. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 7. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the CHO–THERM® 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing, ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will outperform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 3. Performance of Silicon Rubber Insulators Tested Per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Bergquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	–
CHO–THERM, 1617	0.233	–
Q Pad (non–insulated)	–	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	–
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
CHO–THERM 1674	0.433	–
Thermasil II	0.500	–
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the matting surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system, but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late 80's, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The Energy Management Series (EMS) modules, shown in Figure 16, Case 806 (ICePAK™) and Case 388A (TO–258AA) (see Figure 16) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The isolated, Case 221C, illustrated in 21, is an example of parts in the second category.

Parts in the first category (those with an exposed metal flange or tab) are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 8, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection – generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a "sync nut," the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.(4)

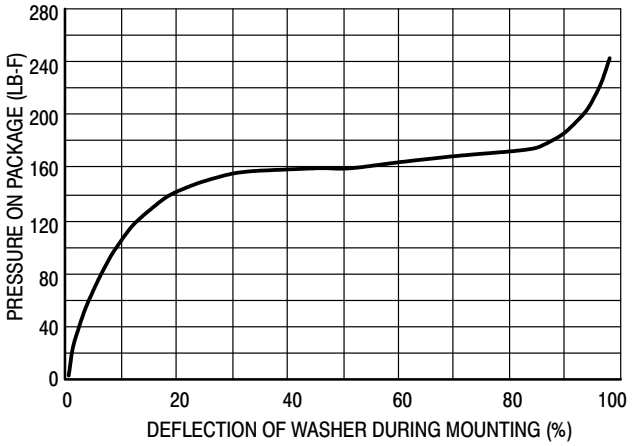


Figure 8. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board–mounted or free–standing heat dissipaters with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync nuts) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case could occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet–metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self–tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange–mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field serviceable systems or low strength types for field serviceable systems. Adhesive bonding is attractive when case–mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in the following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel– or gold–plated. Consequently, precautions must be taken not to mar the finish.

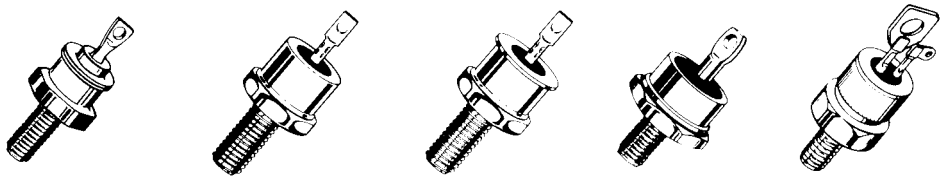
Another factor to be considered is that when a copper–based part is rigidly mounted to an aluminum heatsink, a bi–metallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws, the semiconductor chip could be damaged.

Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some can slip between surfaces as the temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

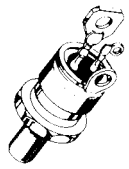
Stud Mount

Parts which fall into the stud–mount classification are shown in Figure 8 through Figure 11. Mounting errors with non–insulated stud–mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heatsink hole. Both of these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer. The details are shown in Figure 12.



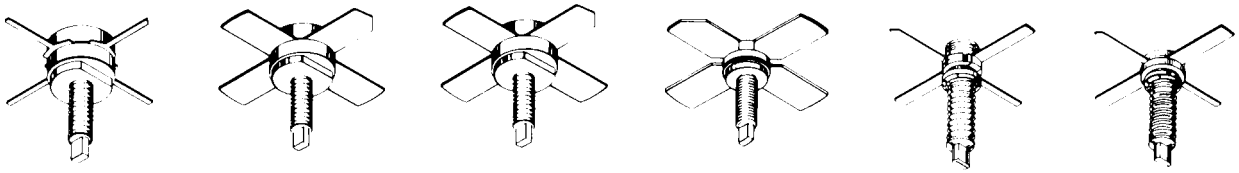
CASE 42A (DO–5) | **CASE 56–03 DO–203AA (DO–4)** | **CASE 245 (DO–4)** | **CASE 257 DO–203AB (DO–5)** | **CASE 263–04**

Figure 9. Standard Non–Isolated Types



CASE 311–02

Figure 10. Isolated Type



CASE 144B–05 (.380″ STUD) | **CASE 145A–09 (.380″ STUD)** | **CASE 145A–10 (.500″ STUD)** | **CASE 244–04 (.280″ STUD)** | **CASE 305–01 (.204″ STUD)** | **CASE 332–04 (.380″ STUD)**

Figure 11. RF Stripline Opposed Emitter (SOE) Series

A VARIETY OF STUD–MOUNT PARTS

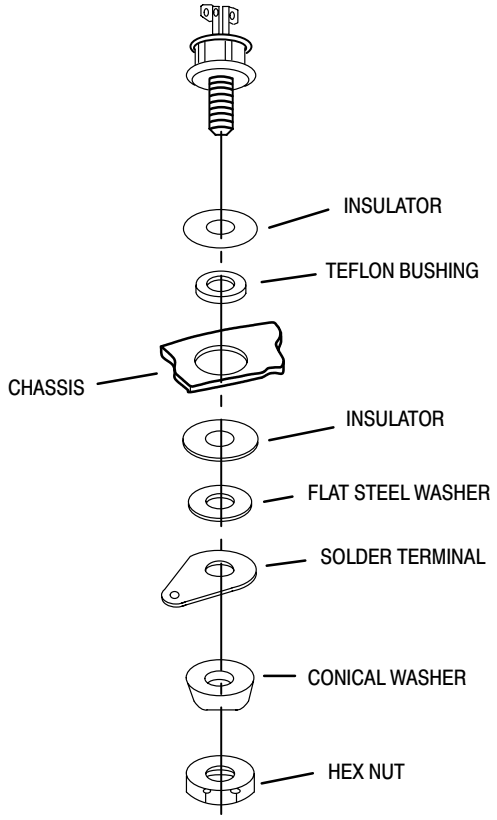


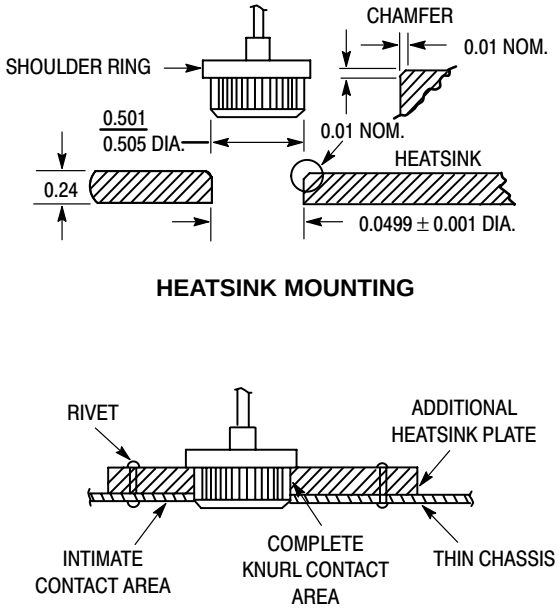
Figure 12. Isolating Hardware Used for a Non–Isolated Stud–Mount Package

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non–insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a beryllium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

RF transistors in the stud–mount Stripline Opposed Emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic – metal interface are discussed in the section entitled, “Connecting and Handling Terminals.”

Press Fit

For most applications, the press–fit case should be mounted according to the instructions shown in Figure 13. A special fixture, meeting the necessary requirements, must be used.



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press–in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper–less than 50 on the Rockwell F scale; aluminum–less than 65 on the Brinell scale. A heatsink as thin as 1/8″ may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Figure 13. Press–Fit Package

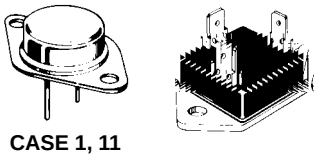
Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 14 through Figure 17. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is, therefore, good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight, the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 18. Machine screws (preferred), self–tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section, “Fastener and Hardware Characteristics.”

The copper flange of the Energy Management Series (EMS) modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, 15, final torque should be applied first to the center position.

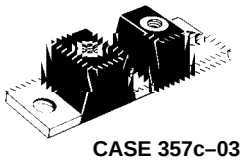
The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in Engineering Bulletin EB107/D, “Mounting Considerations for ON Semiconductor RF Power Modules.” Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.



CASE 1, 11
TO–204AA
(TO–3)

CASE 383–01

Figure 14. TO–3 Variations



CASE 357c–03

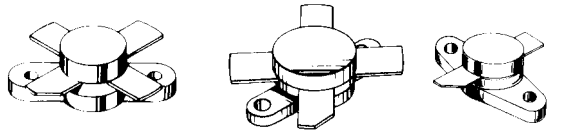
Figure 15. Plastic Power Tap

CASE 373–01 CASE 807–03 CASE 807A–03 CASE 808–01

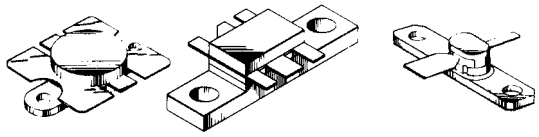
CASE 809–02 CASE 812–02 CASE 813–02

CASE 814–02 CASE 816–02 CASE 819–02

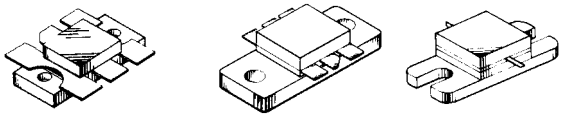
Figure 16. Energy Management Series (Isolated Base Plate)



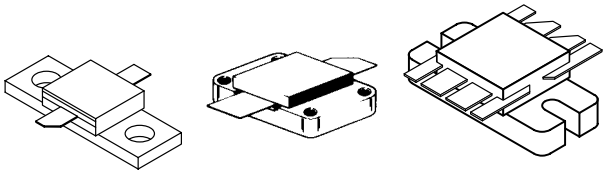
CASE 211–07 CASE 211–11 CASE 215–02



CASE 316–01 CASE 319–07 (CS–12) CASE 328A–03



CASE 333–04 CASE 333A–02 (MAAC PAC) CASE 336–03



CASE 337–02 CASE 368–03 (HOG PAC) CASE 744A–01

Figure 17. RF Stripline Isolated Output Opposed Emitter (SOE) Series

A LARGE ARRAY OF PARTS FIT INTO THE FLANGE–MOUNT CLASSIFICATION

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area, Case 368–03 (HOG PAC), will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4–40 mounting screws is 5 in./lbs. Spring and flat washers are recommended. Over–torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas, have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length; instead, it bends upward in the mid–section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With

sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it. Deformations of 2 – 3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore, thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

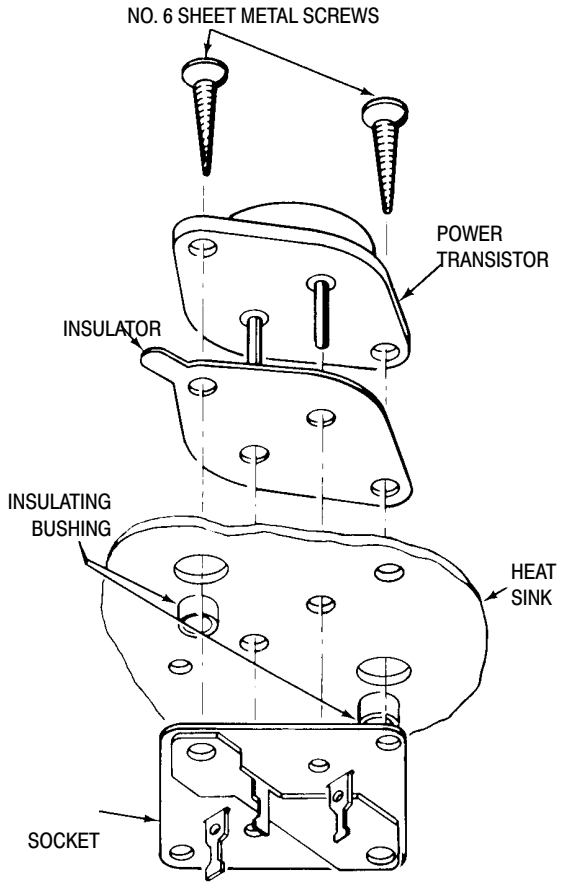


Figure 18. Hardware Used for a TO–204AA (TO–3) Flange Mount Part

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 19. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 20. The rectangular washer shown in Figure 20a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 in. (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 in./lbs is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, ON Semiconductor TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

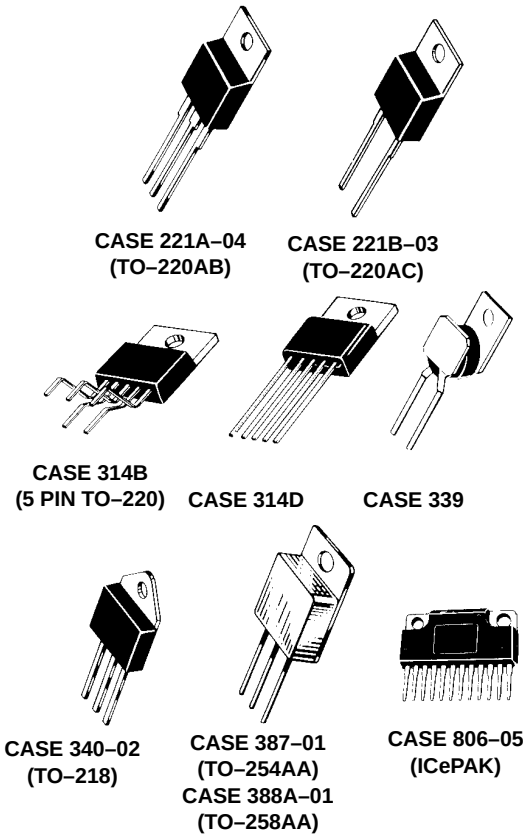


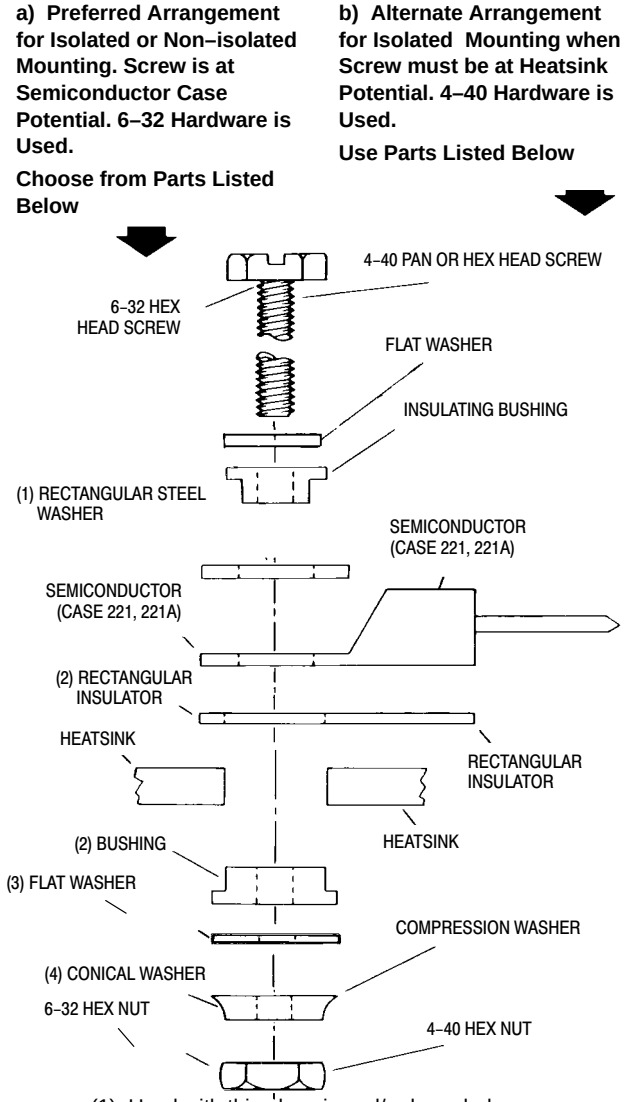
Figure 19. Several Types of Tab–Mount Parts

The popular TO–220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure 36.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 27.

To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806–05) is basically an elongated TO–220 package with isolated chips. The mounting precautions for the TO–220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 20. Mounting Arrangements for Tab Mount TO–220

Plastic Body Mount

The Thermopad™ and isolated plastic power packages shown in Figure 21 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts, this is accomplished by die–bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The isolated (Case 221C–02) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.

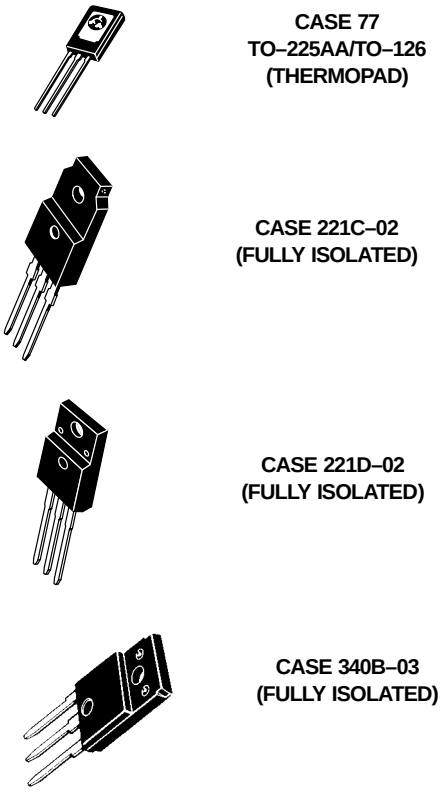


Figure 21. Plastic Body–Mount Packages

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 8.

Figure 22 through Figure 24 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The isolated, (Case 221C, 221D, and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 27, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure 36 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 26 may also be used, but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 25.

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 28, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

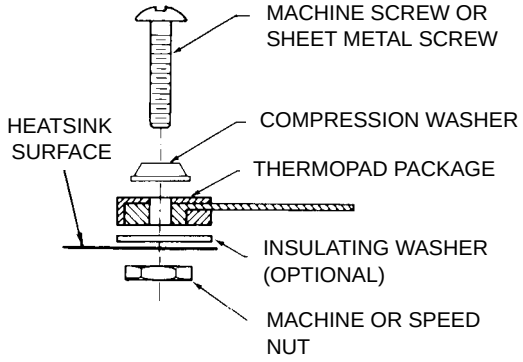
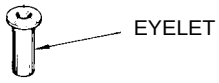


Figure 22. Machine Screw Mounting



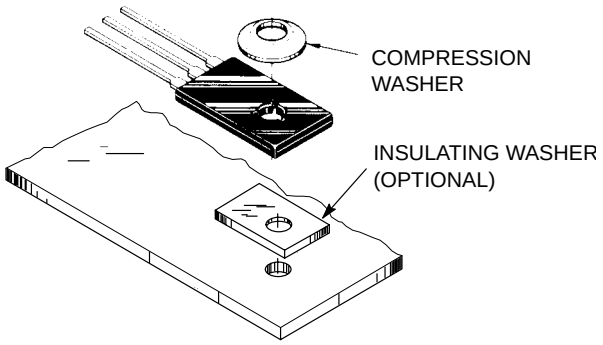


Figure 23. Eyelet Mounting

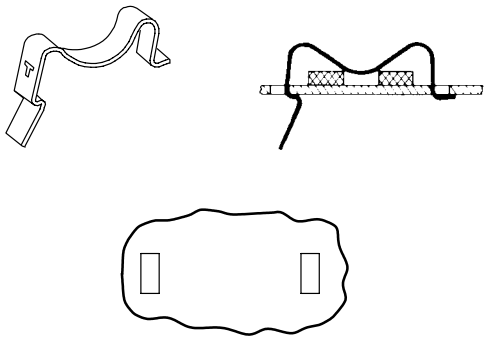


Figure 24. Clips

RECOMMENDED MOUNTING ARRANGEMENTS FOR TO–225AA (TO–126) THERMOPAD PACKAGES

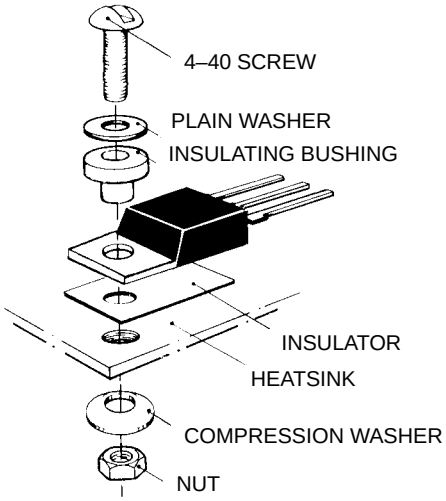


Figure 25. Screw–Mounted TO–220

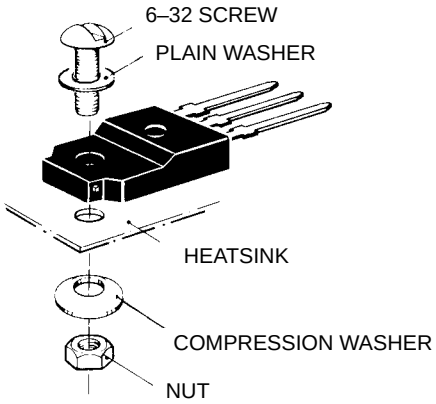


Figure 26. Screw–Mounted Isolated Package

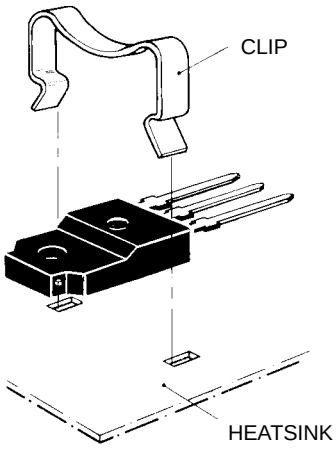


Figure 27. Clip–Mounted Isolated Package

MOUNTING ARRANGEMENTS FOR THE ISOLATED PACKAGE AS COMPARED TO A CONVENTIONAL

CASE 369–07 CASE 369A–13

Figure 28. Surface Mount D–PAK Parts

Standard Glass–Epoxy 2–ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 29 shows, thermal resistance asymptotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one– or two–ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.[7] The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

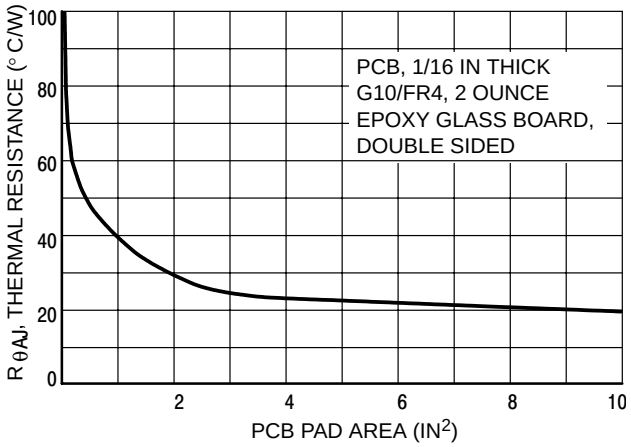


Figure 29. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board

FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice, however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the Case 77 (TO–225AA) (TO–127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 30 and Figure 31. The arrangement of Figure 30 could be used with any plastic package, but the scheme of Figure 31 is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

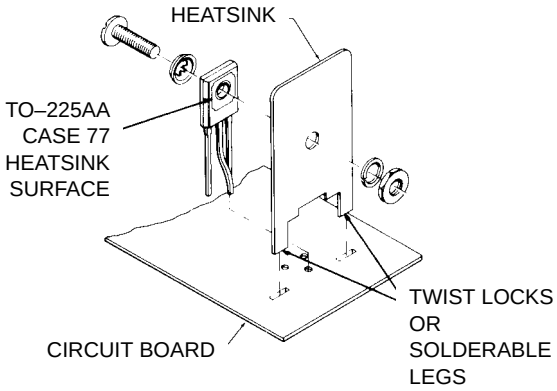


Figure 30. Simple Plate, Vertically Mounted

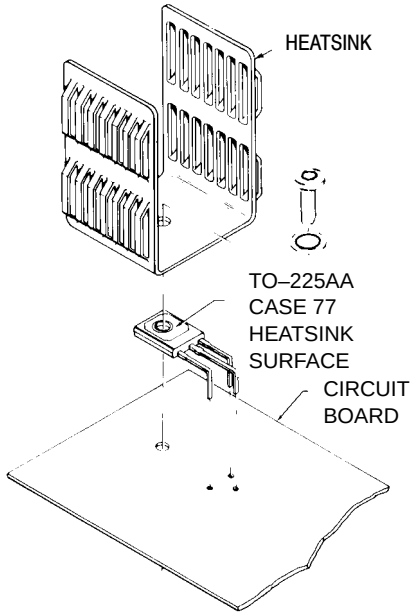


Figure 31. Commercial Sink, Horizontally Mounted

METHODS OF USING SMALL HEATSINKS WITH PLASTIC SEMICONDUCTOR PACKAGES

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from ON Semiconductor. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions, as a result of thermal cycling over operating temperature extremes, must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped, although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from ON Semiconductor on large quantity orders. Preformed leads remove the users' risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO–225AA (CASE 77) and 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire–wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 32 through Figure 34. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic–to–metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 33 shows a cross–section of a printed circuit board and heatsink assembly for mounting a stud–type stripline device. H is the distance from the top surface of the printed circuit board to the D–flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud – BeO ceramic joint. If, however, H is greater than the package

dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead–soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger; this may result in device failure as power is applied.

Figure 34 shows a typical mounting technique for flange–type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see ON Semiconductor Application Note, AN569/D.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

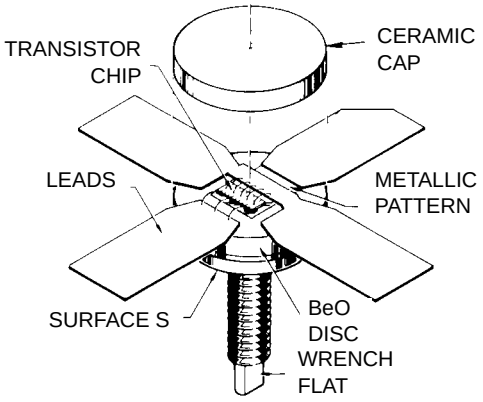


Figure 32. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed

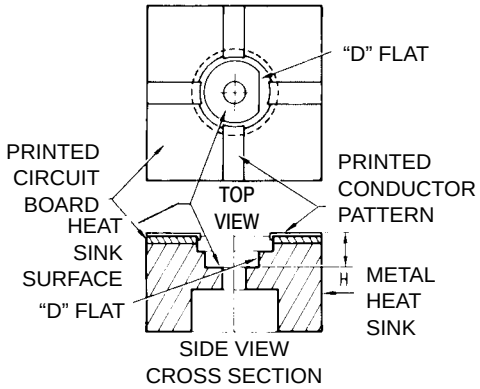


Figure 33. Typical Stud Type SOE Transistor Mounting Method

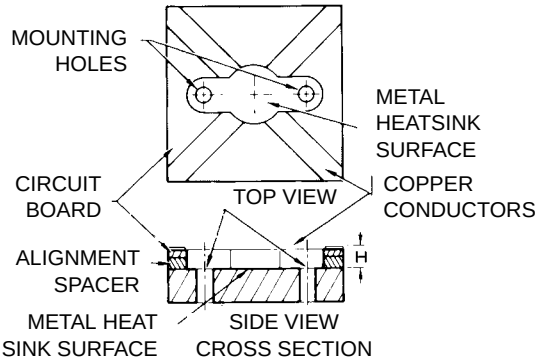


Figure 34. Flange Type SOE Transistor Mounting Method

MOUNTING DETAILS FOR SOE TRANSISTORS

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction–to case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure 35.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D (R_{\theta JC} + P_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
PD = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat–sink),
$R_{\theta SA}$ = heat sink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications, such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

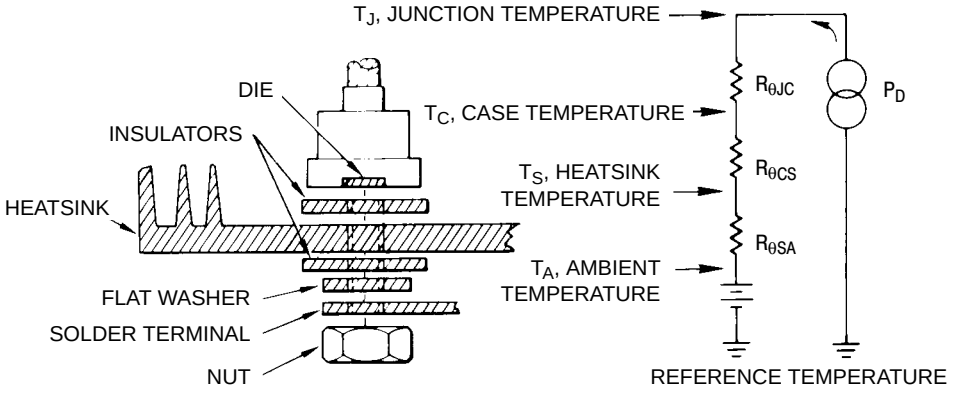


Figure 35. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The ON Semiconductor fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in 36. The mounting pressure at one end causes the other end – where the die is located – to lift off the mounting surface slightly. To improve contact, ON Semiconductor TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

1. The ON Semiconductor location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.
2. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.
3. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

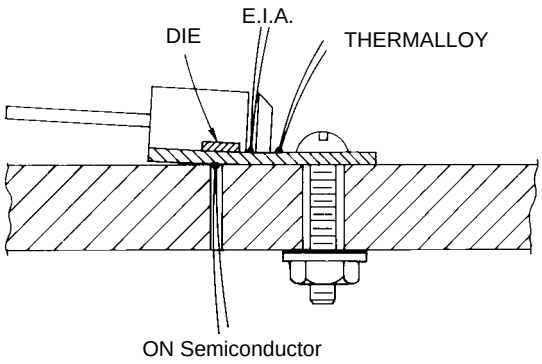


Figure 36. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the ON Semiconductor location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the "case" temperature thermocouple readings become warmer. Thus, the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower, but close to the temperature at the EIA location as the lateral heat flow is generally small. The ON Semiconductor location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The ON Semiconductor location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink, to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ–inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is, therefore, application–oriented. It is also easy to use, but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber		
Aavid	–	–	–	–	–	–	X	X	X	X
AHAM–TOR	–	–	–	–	–	–	–	–	X	–
Asheville–Schoonmaker	–	–	–	–	–	X	–	–	–	–
Astrodynamis	X	–	–	–	–	–	–	–	X	–
Delbert Blinn	–	–	X	–	X	X	X	X	X	–
IERC	X	–	–	–	–	–	–	–	X	–
Staver	–	–	–	–	–	–	–	–	X	–
Thermalloy	X	X	X	X	X	X	X	X	X	X
Tran–tec	X	–	X	X	X	X	–	X	X	–
Wakefield	X	X	X	–	X	–	–	X	X	X

Other Sources for silicone rubber pads: Chomerics, Bergquist

Suppliers Addresses

Aavid Engineering, Inc., P.O. Box 400, Laconia, New Hampshire 03247 (603) 524–1478
AHAM–TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676–4151
Asheville–Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607 (804) 244–7311
Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935–4944
Bergquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835–2322
Chomerics, Inc.,16 Flagstone Drive, Hudson, New Hampshire 03051 1–800–633–8800
Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 623–1257
International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849–2481
The Staver Company, Inc., 41–51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666–8000
Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243–4321
Tran–tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564–2748
Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245–5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non–related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re–registered to the new system as time permitted.

For example the venerable TO–3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO–204 family. The TO–204AA conforms to the original outline for the TO–3 having 40 mil pins while the TO–204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO–4, DO–5 and TO–3 still convey sufficient meaning for general verbal communication.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
001	TO-3	TO-204AA		Flange
003	TO-3		2	Flange
009	TO-61	TO-210AC		Stud
011	TO-3	TO-204AA	–	Flange
011A	TO-3	–	2	Flange
012	TO-3	–	2	Flange
036	TO-60	TO-210AB	–	Stud
042A	DO-5	DO-203AB	–	Stud
044	DO-4	DO-203AA	–	Stud
054	TO-3	–	2	Flange
056	DO-4	–	–	Stud
058	DO-5	–	2	Stud
61-04				Flange
63-02	TO-64	TO-208AB		Stud
63-03	TO-64	TO-2088AB		Stud
077	TO-126	TO-225AA	–	Plastic
080	TO-66	TO-213AA	–	Flange
086	–	TO-208	1	Stud
086L	–	TO-298	1	Stud
144B-05				Stud
145A-09				Stud
145A-10				Stud
145C	TO-232		1	Stud
157	–	DO-203	1	Stud
160-03	TO-59	TO-210AA	–	Stud
167	–	DO-203	1	Stud
174-04				Pressfit

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
175-03				Stud
197	–	TO-204AE	–	Flange
211-07				Flange
211-11				Flange
215-02				Flange
221	–	TO-220AB	–	Tab
221C-02				Plastic
221D-02	–	–	Isolated TO-220	Plastic
235	–	TO-208	1	Stud
235-03				Stud
238	–	TO-208	1	Stud
239	–	TO-208	–	Stud
244-04				Stud
245	DO-4	–	–	Stud
257-01	DO-5	–	–	Stud
263	–	TO-208	–	Stud
263-04				Stud
283	DO-4	–	–	Stud
289	–	TO-209	1	Stud
305-01				Stud
310-02				Pressfit
311-02			Isolated	Stud
311-02				Pressfit
311-02				Stud
314B-03				Tab

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
314D-03				Tab
316-01				Flange
319-06				Flange
328A-03				Flange
332-04				Stud
333-04				Flange
333A-02				Flange
336-03				Flange
337-02				Flange
340		TO-218AC		Tab
340A-02				Plastic
340B-03			Isolated TO-218	Plastic
342-01				Flange
357B-01				Flange
361-01				Flange
368-02				Flange
369-06		TO-251		Insertion
369A-12		TO-252		Surface
373-01			Isolated	Flange
383-01			Isolated	Flange
387-01		TO-254AA	Isolated 2	Tab
388A-01		TO-258AA	Isolated 2	Tab
744-02				Flange
744A-01				Flange
043-07	DO-21	DO-208AA		Pressfit

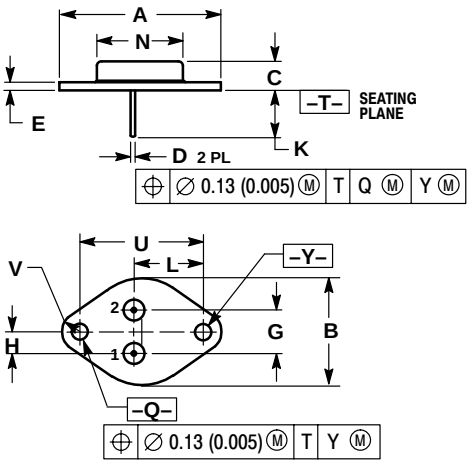
Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

(1) MIL–HANDBOOK – 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability – Design and Manufacturing Guidelines" NAVMAT P4855–1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
(3) Catalog #87–HS–9, (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.
(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.
(5) Robert Batson, Elliot Fraunglass and James P Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1 – 3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.
(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.
(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.

Case Outlines

Case Outlines

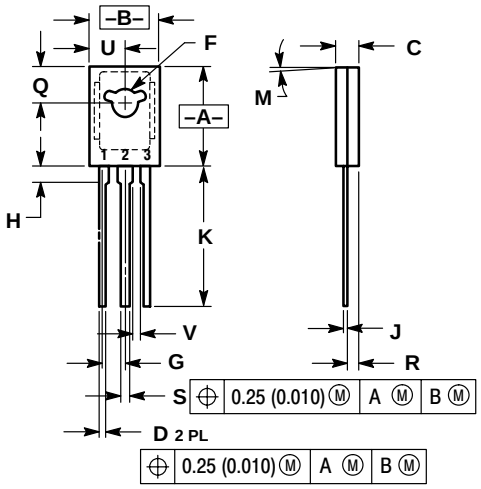
TO–204
CASE 1–07
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

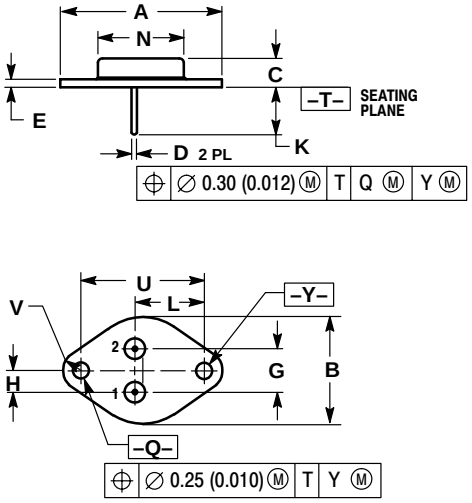
TO–225
CASE 77–09
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

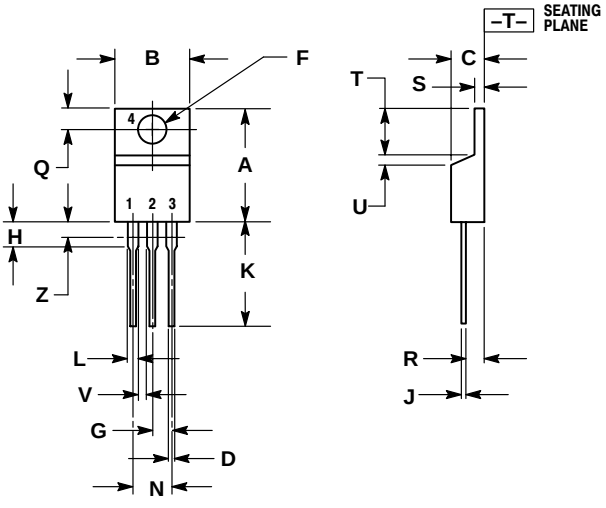
TO–204
CASE 197A–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

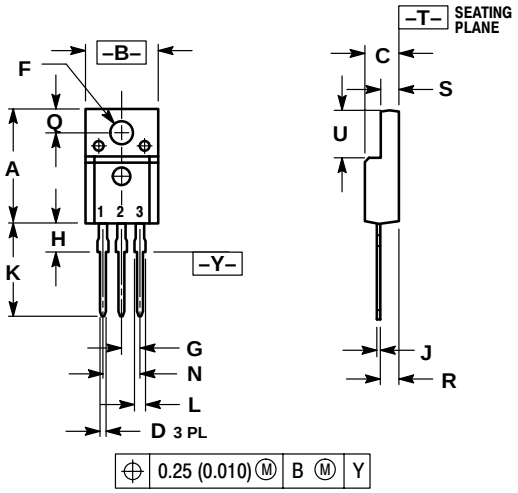
TO–220
CASE 221A–09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

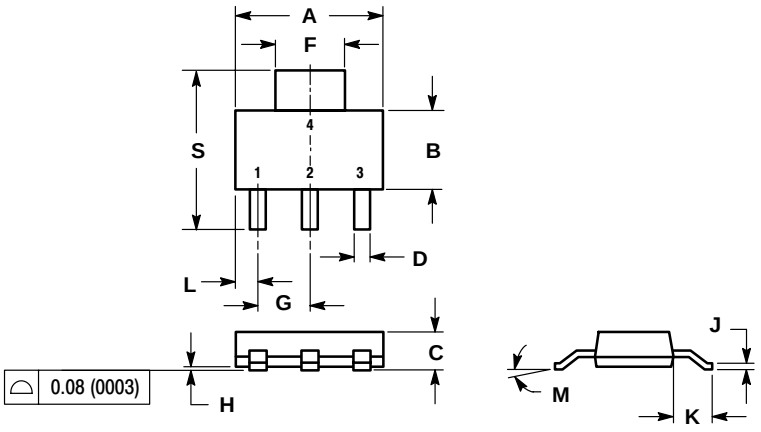
TO−220
CASE 221D−02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

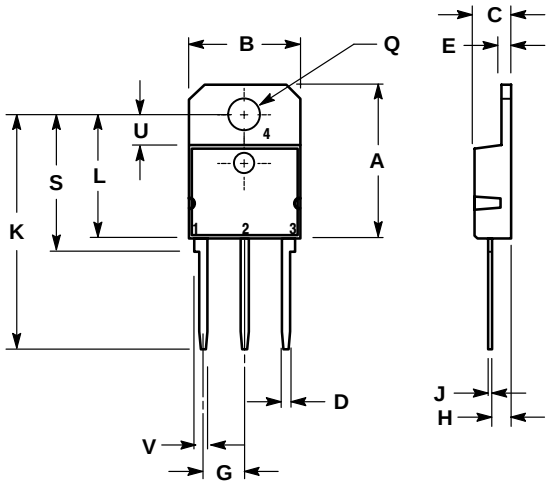
TO−261
CASE 318E−04
ISSUE K



NOTES:
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

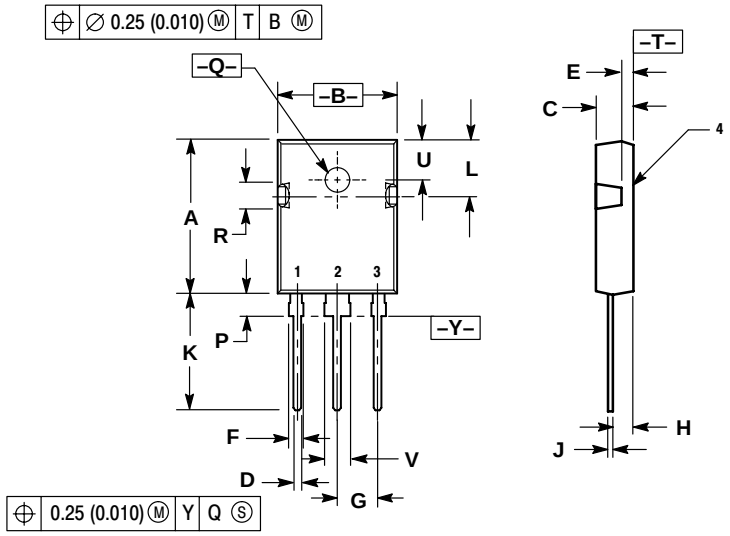
TO–218
CASE 340D–02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

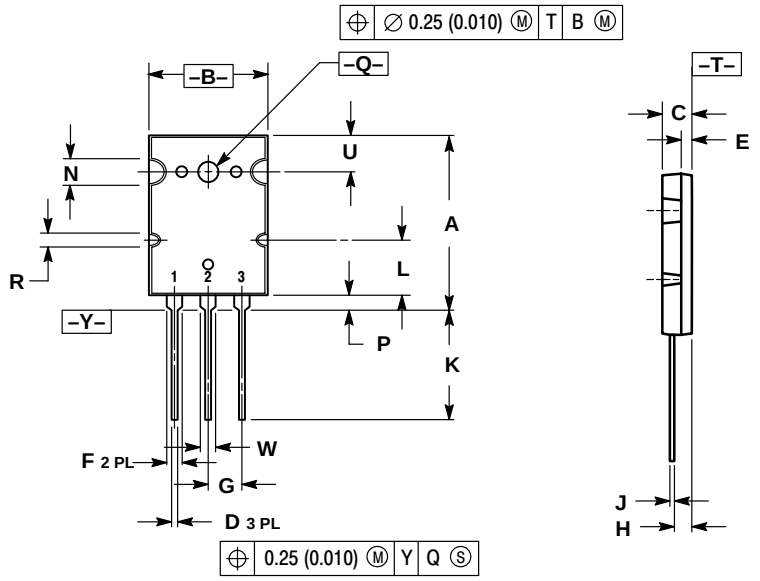
TO–207
CASE 340F–03
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

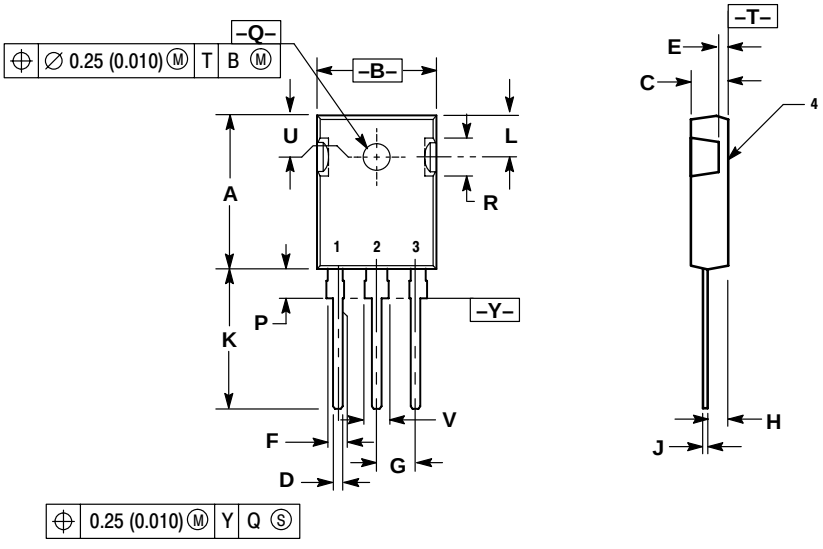
TO–264
CASE 340G–02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

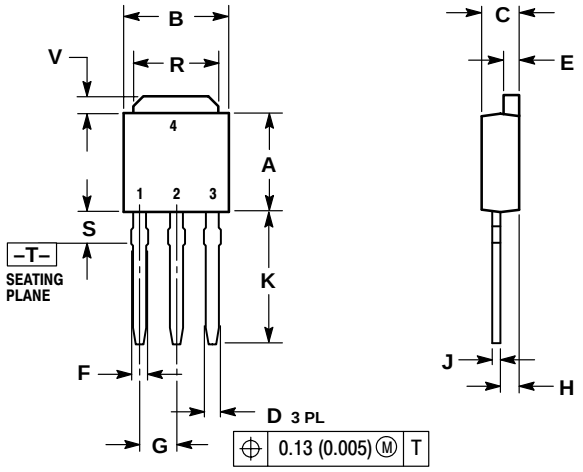
TO–247
CASE 340K–01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

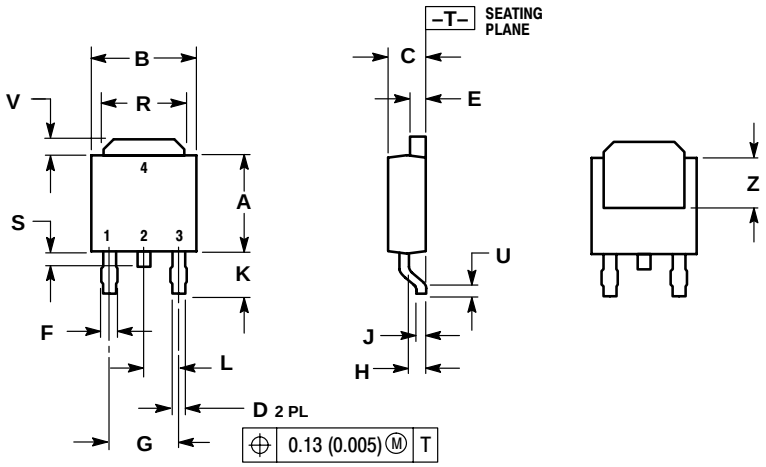
DPAK
CASE 369–07
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

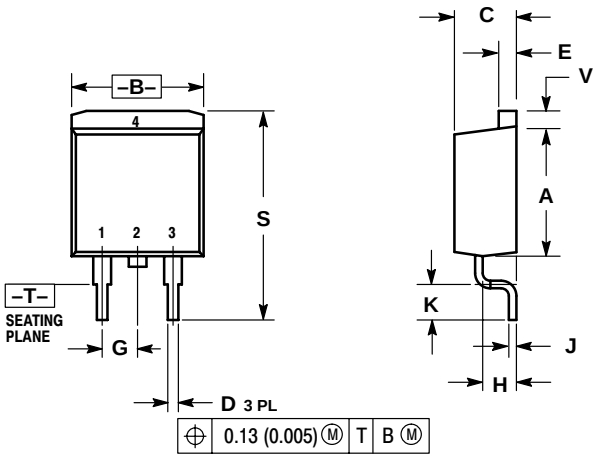
DPAK
CASE 369A–13
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

D²PAK
CASE 418B–03
ISSUE D

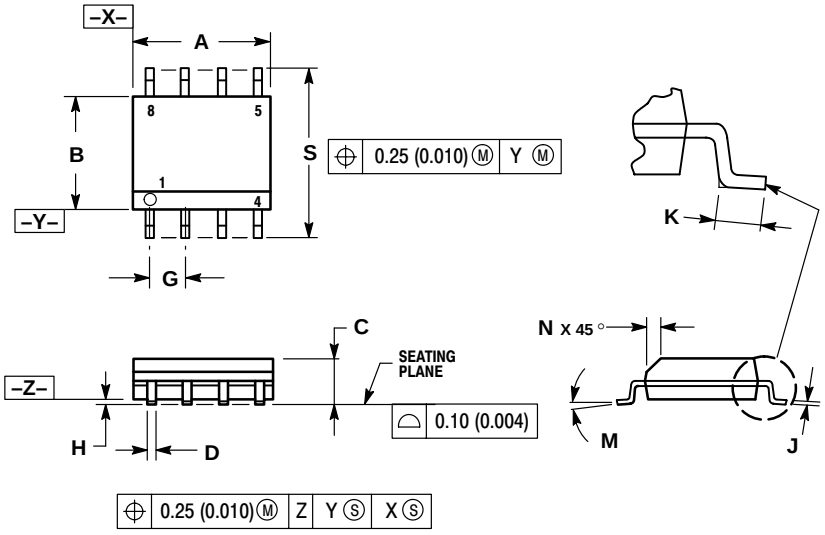


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOIC–8 NB
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

CHAPTER 4
Numeric Index

Device Index

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