

ICPL2631  
ICPL2630



**DUAL CHANNEL, HIGH CMR, VERY HIGH SPEED OPTICALLY COUPLED ISOLATOR LOGIC GATE OUTPUT**

**APPROVALS**

- UL recognised, File No. E91231

**DESCRIPTION**

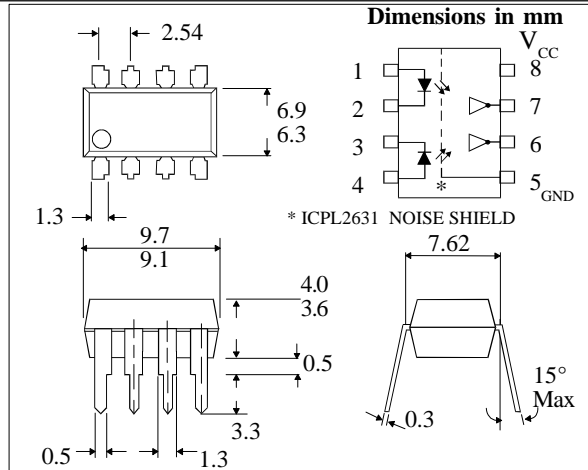
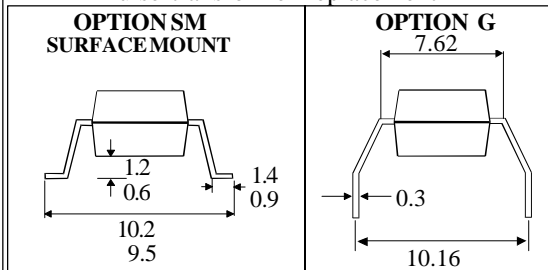
The ICPL2630 / ICPL2631 are dual channel optocouplers consisting of GaAsP light emitting diodes and high gain integrated photo detectors to provide 3500Volts<sub>RMS</sub> electrical isolation between input and output. The output of the detector I.C.'s are open collector Schottky clamped transistors. The ICPL2631 has an internal shield which provides a guaranteed common mode transient immunity specification of 1000V/μs minimum. This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The coupled parameters are guaranteed over the temperature range of 0°C to 70°C, such that a maximum input signal of 5mA will provide a minimum output sink current of 13mA (equivalent to fan-out of eight gates)

**FEATURES**

- High speed - 10MBit/s
- High Common Mode Transient Immunity 10kV/μs typical
- Logic gate output
- ICPL2631 has improved noise shield for superior common mode rejection
- Options :-  
10mm lead spread - add G after part no.  
Surface mount - add SM after part no.  
Tape&reel - add SMT&R after part no.

**APPLICATIONS**

- Line receiver, data transmission
- Computer-peripheral interface
- Data multiplexing
- Pulse transformer replacement



**ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise specified)**

Storage Temperature \_\_\_\_\_ -55°C to + 125°C  
Operating Temperature \_\_\_\_\_ 0°C to + 70°C  
Lead Soldering Temperature (1/16 inch (1.6mm) from case for 10 secs) 260°C

**INPUT DIODE**

Average Forward Current \_\_\_\_\_ 15mA (note 5)  
Peak Forward Current \_\_\_\_\_ 30mA (less than 1msec duration)(note 5)  
Reverse Voltage \_\_\_\_\_ 5V (note 5)

**DETECTOR**

Supply Voltage(V<sub>CC</sub>) \_\_\_\_\_ 7V (1 minute maximum)  
Output Current ( I<sub>O</sub> ) \_\_\_\_\_ 16mA (note 5)  
Output Voltage ( V<sub>O</sub> ) \_\_\_\_\_ 7V (note 5)  
Collector Output Power Dissipation \_\_\_\_\_ 60mW

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**ELECTRICAL CHARACTERISTICS ( T<sub>A</sub> = 0°C to 70°C Unless otherwise noted )**

PARAMETER	SYM	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITION
High Level Output Current (note 5)	I <sub>OH</sub>			2	250	μA	V <sub>CC</sub> = 5.5V, V <sub>O</sub> = 5.5V I <sub>F</sub> = 250μA
Low Level Output Voltage (note 5)	V <sub>OL</sub>			0.4	0.6	V	V <sub>CC</sub> = 5.5V, I <sub>F</sub> = 5mA I <sub>OL</sub> (sinking ) = 13mA
High Level Supply Current (both channels)	I <sub>CCH</sub>			14	30	mA	V <sub>CC</sub> = 5.5V, I <sub>F</sub> = 0mA
Low Level Supply Current (both channels)	I <sub>CCL</sub>			26	36	mA	V <sub>CC</sub> = 5.5V, I <sub>F</sub> = 10mA
Input Forward Voltage	V <sub>F</sub>			1.55	1.75	V	I <sub>F</sub> = 10mA, T <sub>A</sub> = 25°C
Input Reverse Breakdown Voltage	V <sub>BR</sub>		5			V	I <sub>R</sub> = 10μA, T <sub>A</sub> = 25°C
Input Capacitance	C <sub>IN</sub>			60		pF	V <sub>F</sub> = 0, f = 1MHz
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.4		mV/°C	I <sub>F</sub> = 10mA
Input-output Isolation Voltage (note 4)	V <sub>ISO</sub>		2500	5000		V <sub>RMS</sub>	R.H.equal to or less than 50%, t = 1min. T <sub>A</sub> = 25°C
Input-output Insulation Leakage Current (note 4)	I <sub>I-O</sub>				1	μA	R.H = 45% t = 5s, T <sub>A</sub> = 25°C V <sub>I-O</sub> = 3000V dc
Resistance (Input to Output) (note 4)	R <sub>I-O</sub>			10 <sup>12</sup>		Ω	V <sub>I-O</sub> = 500V dc
Capacitance (Input to Output) (note 4)	C <sub>I-O</sub>			0.6		pF	f = 1MHz
Input-input Insulation Leakage Current (note 6)	I <sub>I-I</sub>			0.005		μA	R.H = 45% t = 5s, T <sub>A</sub> = 25°C V <sub>I-O</sub> = 500V dc
Resistance (Input to input) (note 6)	R <sub>I-I</sub>			10 <sup>11</sup>		Ω	V <sub>I-O</sub> = 500V dc
Capacitance (Input to input) (note 6)	C <sub>I-I</sub>			0.6		pF	f = 1MHz

\* All typicals at T<sub>A</sub> = 25°C

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Current, Low Level	I <sub>FL</sub>	0	250	μA
Input Current, High Level	I <sub>FH</sub>	6.3*	15	mA
Supply Voltage, Output	V <sub>CC</sub>	4.5	5.5	V
Fan Out ( TTL Load )	N		8	
Operating Temperature	T <sub>A</sub>	0	70	°C

\*6.3mA is a guard banded value which allows for at least 20% CTR degradation.  
Initial input current threshold value is 5.0mA or less

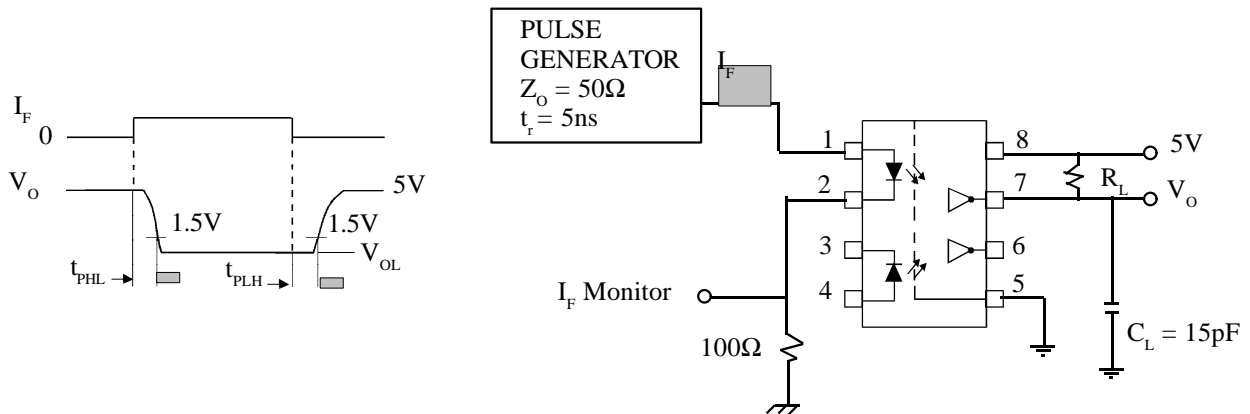
**SWITCHING SPECIFICATIONS AT  $T_A = 25^\circ\text{C}$  ( $V_{CC} = 5\text{V}$ ,  $I_F = 7.5\text{mA}$  Unless otherwise noted )**

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TEST CONDITION
Propagation Delay Time to Logic Low at Output ( fig 1 )( note2 )	$t_{PHL}$			55	75	ns	$R_L = 350\Omega$ , $C_L = 15\text{pF}$
Propagation Delay Time to Logic High at Output ( fig 1 )( note3 )	$t_{PLH}$			45	75	ns	$R_L = 350\Omega$ , $C_L = 15\text{pF}$
Common Mode Transient Immunity at Logic High Level Output ( fig 2 )( note7 )	$CM_H$	ICPL2630 ICPL2631	1000	10000 10000		V/ $\mu\text{s}$ V/ $\mu\text{s}$	$I_F = 0\text{mA}$ , $V_{CM} = 50V_{PP}$ $R_L = 350\Omega$ , $V_{OH} = 2V_{min.}$
Common Mode Transient Immunity at Logic Low Level Output ( fig 2 )( note8 )	$CM_L$	ICPL2630 ICPL2631	-1000	-10000 -10000		V/ $\mu\text{s}$ V/ $\mu\text{s}$	$V_{CM} = 50V_{PP}$ $R_L = 350\Omega$ , $V_{OL} = 0.8V_{max.}$

**NOTES:-**

- 1 Bypassing of the power supply line is required, with a  $0.01\mu\text{F}$  ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolator(s) should be separate from the bus for any active loads. Otherwise a larger value of bypass capacitor (up to  $0.1\mu\text{F}$ ) may be needed to suppress regenerative feedback via the power supply.
- 2 The  $t_{PHL}$  propagation delay is measured from the  $3.75\text{mA}$  level Low to High transition of the input current pulse to the  $1.5\text{V}$  level on the High to Low transition of the output voltage pulse.
- 3 The  $t_{PLH}$  propagation delay is measured from the  $3.75\text{mA}$  level High to Low transition of the input current pulse to the  $1.5\text{V}$  level on the Low to High transition of the output voltage pulse.
- 4 Device considered a two terminal device; pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
- 5 Each channel.
- 6 Measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together.
- 7  $CM_H$  is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (ie  $V_{out} > 2.0\text{V}$ ).
- 8  $CM_L$  is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (ie  $V_{out} < 0.8\text{V}$ )

**FIG.1 SWITCHING TEST CIRCUIT**



**FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS**

