AVR1324: XMEGA ADC Selection Guide

Features

The Atmel® AVR® XMEGA® A family

- **Pipelined architecture**
- **Up to 2M samples per second**
- **Up to 12-bit resolution**
- **Signed and unsigned mode**
- **Selectable gain**
- **2MHz maximum ADC frequency**
- **Minimum single result propagation delay of 2.5µs (8-bit resolution)**
- **Minimum single result propagation delay of 3.5µs (12-bit resolution)**
- **Up to 4 virtual channels**
- **Result comparator**
- **Automatic calibration**
- **Internal connection to DAC output**
- **Optional DMA transfer of conversion results**

The Atmel AVR XMEGA B and D families

- **Cyclic architecture**
- **Up to 200.000 samples per second**
- **Up to 12-bit resolution**
- **Signed and unsigned mode**
- **Selectable gain**
- **1.4MHz maximum ADC frequency**
- **Minimum single result propagation delay of 3.57µs (8-bit resolution)**
- **Minimum single result propagation delay of 5.0µs (12-bit resolution)**
- **Optional DMA transfer of conversion results (for device with a DMA)**

1 Introduction

Atmel AVR XMEGA devices are grouped into several families offering comparable features. For example, the analog-to-digital converters (ADCs) on all A-family XMEGA devices are identical.

Depending on the selected family, AVR XMEGA devices offer two ADC types. Both are flexible modules suitable for a wide range of applications, such as data acquisition, embedded control, and general signal processing.

This application note describes these two ADC types and helps users to select the most suitable ADC for their application.

8-bit Atmel Microcontrollers

Application Note

Rev. 8378A-AVR-10/2011

2 AVR XMEGA ADC Summary

The main differences between the Atmel AVR XMEGA ADCs are described in Table 2-1. This table provides a summary of ADC features. For more details, please refer to individual product datasheets and manuals.

Table 2-1. ADC features

	AVR XMEGA A specific		
	AVR XMEGA B specific		
	AVR XMEGA A	**AVR XMEGA B**	**AVR XMEGA D**
ADCA	Yes	Yes	Yes
ADCB	Yes	Yes	_
Channel 0	Yes	Yes	Yes
Channel 1	Yes	_	_
Channel 2	Yes	_	_
Channel 3	Yes	_	_
Architecture	Pipelined	Cyclic	Cyclic
Max ADC frequency	2MHz	1.4MHz	1.4MHz
Single propagation ADC cycles number (12 bits)	7	7	7
Single propagation ADC cycles number (8 bits)	5	5	5
Max sample per second (12 bits)	2Msps	200ksps	200ksps
ADC result to DMA	Yes	Yes	_
SWEEP mode (channel sweep)	Yes	_	_
Number of Internal inputs	4	3	3
Internal inputs	Temperature VCC/10 Bandgap DAC	Temperature VCC/10 Bandgap -	Temperature VCC/10 Bandgap -
x 0.5 Gain	_	Yes	_
Voltage reference = INTVCC/2	_	Yes	_

3 ADC Selection guide

The following list of questions is intended to help provide guidance in finding the appropriate Atmel AVR XMEGA ADC.

Table 3-1. ADC selection guide

	Explanation	AVR XMEGA
What is the number of ADC channels needed?	All AVR XMEGA ADCs offer 16 ADC channels.	A, B, D
Are one or two external references required?	All AVR XMEGA ADCs offer two external references, even if only one ADC is available.	A, B, D
What is the propagation delay needed?	If propagation delay >200ksps: AVR XMEGA A offers 2Msps ADC.	A
	If propagation delay ≤200ksps: AVR XMEGA B and D offer 200ksps ADC.	B, D
Are one or two ADCs needed?	If simultaneous conversions are required on different channels, two ADCs are needed. AVR XMEGA A and B offer two ADCs	A, B
	If conversions on different channels are consecutive, only one ADC is needed. AVR XMEGA D offers one ADC.	D
Is the DAC output needed as internal input?	Only AVR XMEGA A features this link between DAC and ADC.	A
Is rail-to-rail conversion needed?	Rail-to-rail conversion requires accurate measurements around the ± voltage reference value. AVR XMEGA B offers x0.5 gain to optimize rail-to-rail conversion.	B
Is sweep mode required?	Sweep mode allows selecting the number of channels used to trigger the event controller. Only AVR XMEGA A offers sweep mode.	A

4 ADC Architecture Overview

The Atmel AVR XMEGA A family offers a high-performance ADC capable of conversion rates of up to 2Msps with a resolution of 12 bits.

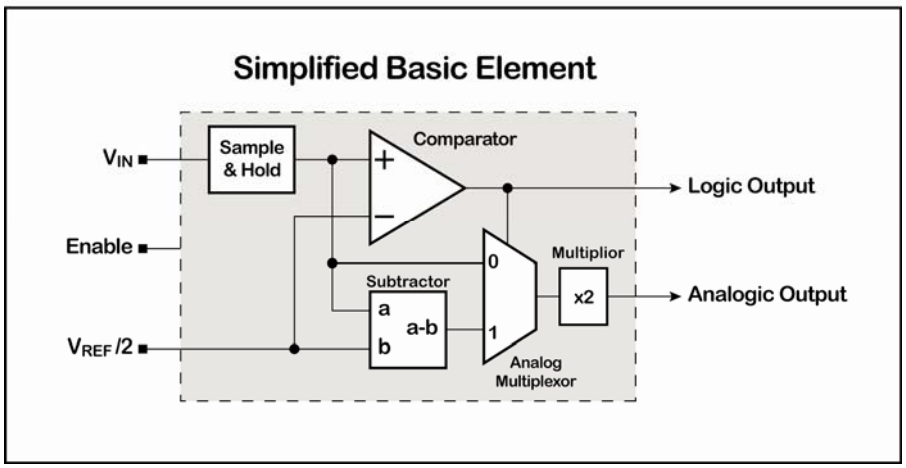
The Atmel AVR XMEGA B and D families offer a high-performance ADC capable of conversion rates up to 200ksps with a resolution of 12 bits.

This section provides an overview of the functionality and basic configuration options of the ADC.

4.1 Basic element

The basic element uses switched capacitor technology combined with an operational amplifier. Switched capacitor technology was chosen to reduce the power consumption (compared to a technology-based resistor).

Figure 4-1. Basic element description



The input voltage, V_{IN}, is compared to the voltage reference divided by two, $V_{REF}/2$.

If V_{IN} is smaller than $V_{REF}/2$, this voltage is kept for the next iteration.

The logic output is 0.

This is the value of the most-significant bit (MSB).

If V_{IN} is greater than $V_{REF}/2$, $V_{REF}/2$ is subtracted from V_{IN}.

The logic output is 1.

This is the value of the MSB.

The result is multiplied by two and becomes the input of another basic element to continue the conversion.

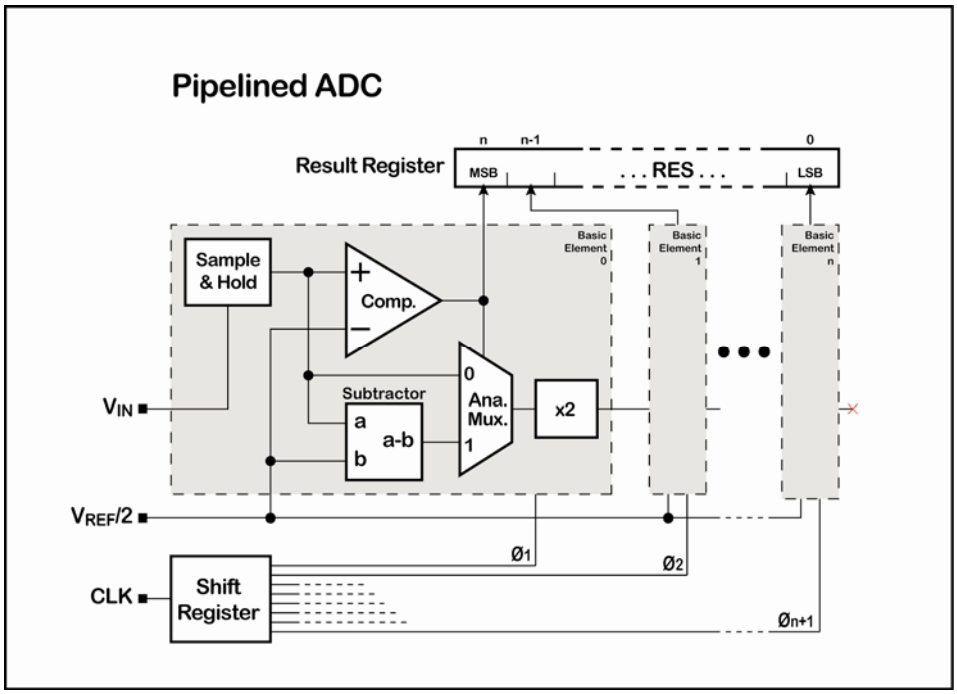
4.2 Pipelined structure

The Atmel AVR XMEGA A family uses a pipelined ADC with 12 identical basic elements. The first element will provide the MSB of the conversion, and the last one will provide the LSB. A series of basic elements allows creating a pipelined conversion.

When an element has finished its part of the conversion, it can then be re-used at CLK speed for another conversion channel.

The maximum number of channels corresponds to the number of basic elements used. The AVR XMEGA A family offers four levels (four ”virtual channels”) in the ADC, and offers four result registers.

Figure 4-2. Pipelined structure description



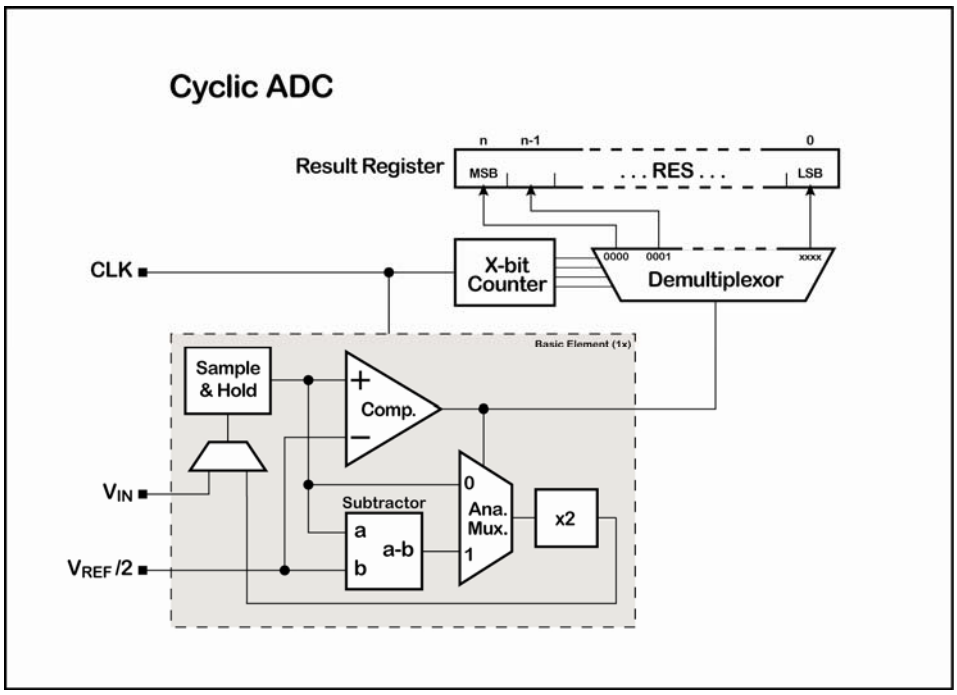
The even basic elements (0, 2 …) will be enabled during the high level of the ADC clock, and the odd basic elements (1, 3 …) will be enabled during the low level of the ADC clock. This speeds up (x2) the conversion time versus the ADC clock frequency.

For more details, the Atmel application note “AVR1300: Using the Atmel AVR XMEGA ADC” gives a complete description of the AVR XMEGA A.

4.3 Cyclic structure

The Atmel AVR XMEGA B and D families offer a cyclic ADC. Instead of using 12 distinct basic elements, a single basic element is used 12 times in series for the MSB to the LSB.

Figure 4-3. Cyclic structure description



In the cyclic ADC, the basic element has been modified slightly. It is made of two sets of switched capacitors associated to a unique operational amplifier. The first set will be enabled on the high level of the ADC clock, and the second one will be enabled on the low level of the ADC clock.

4.4 Differences between cyclic and pipelined structures

4.4.1 Cyclic propagation delay

With the cyclic structure, the minimum propagation delay corresponds to a conversion without gain (gain equal to 1).

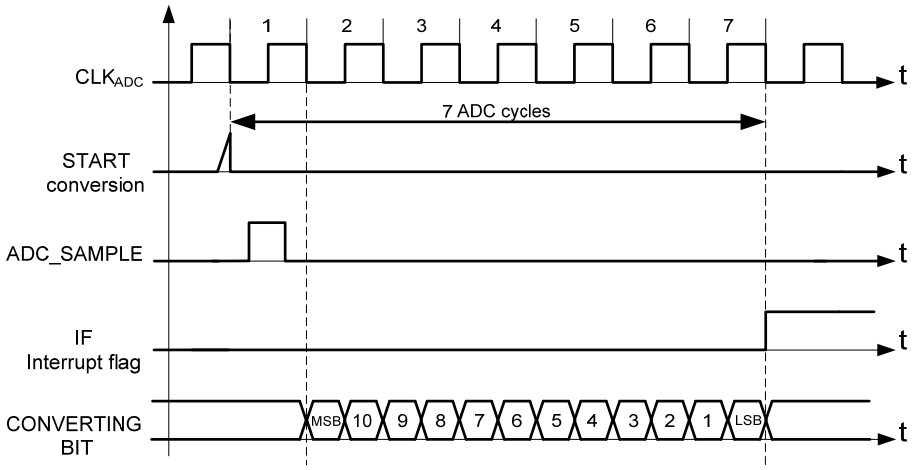
Depending on the gain value, several extra ADC cycles are added to the propagation delay.

A new conversion is started after the end of the first one.

The example shows a conversion with:

- One conversion channel: CH0
- Conversion without gain on CH0
- Conversion mode: Single-ended

Figure 4-4. Cyclic propagation delay



4.4.2 Pipelined propagation delay

With the pipelined structure, four basic elements are used at the same time. This number corresponds to the number of virtual channels (four virtual channels for the Atmel AVR XMEGA A).

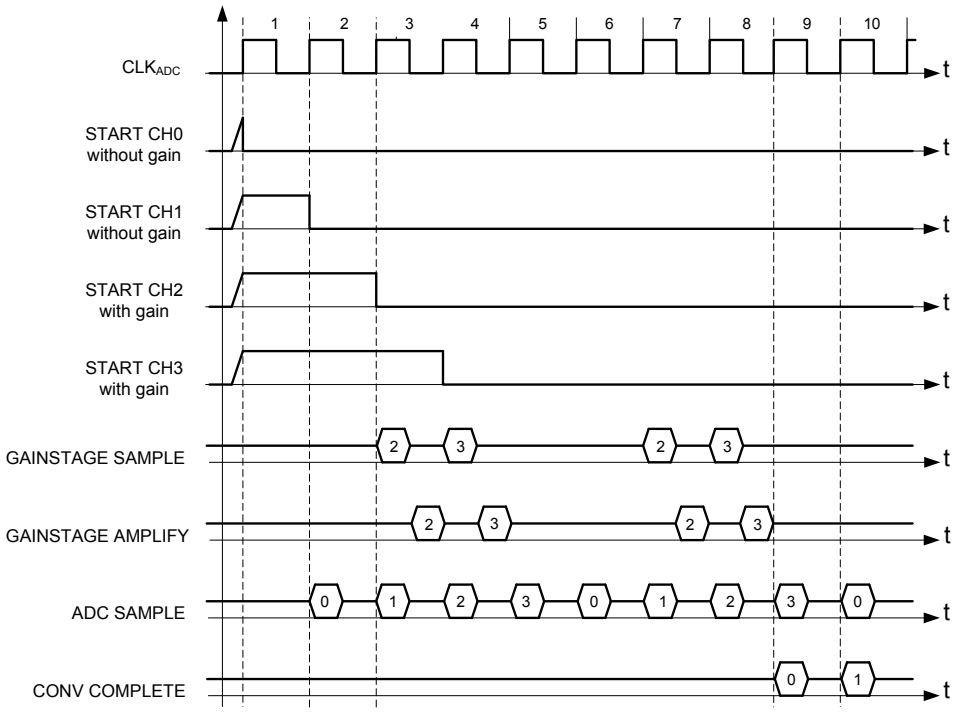
The result is that four basic elements are active during the same ADC cycle. After the end of the first conversion, a new end-of-conversion appears at each ADC cycle.

The pipelined structure is useful if several channels are converting at the same time.

The example (Figure 4-5) shows a conversion with:

- Four conversion channels: CH0, CH1, CH2, and CH3
- Two conversion channels without gain: CH0 and CH1
- Two conversion channels with gain: CH2 and CH3
- Conversion mode: Free-running

Figure 4-5. Pipelined propagation delay (with 4 channels used: 0, 1, 2, 3)



5 Software interface

5.1 Software description

The Atmel AVR XMEGA ADCs are developed with compatibility over a common architecture. Registers and bits follow the same rules.

The Atmel AVR XMEGA A ADC has more features than the AVR XMEGA B and D ADCs. Firmware developed for the Atmel AVR XMEGA B and D ADC can run on the AVR XMEGA A without any limitations. Firmware developed for the AVR XMEGA A ADC can run on the AVR XMEGA B and D provided it only uses the more limited features available on the AVR XMEGA B and D ADCs.

The AVR XMEGA ADC driver is available in the Atmel AVR Software Framework (ASF). This driver is common for all AVR XMEGA ADCs. There are two examples included in this framework, and they support both GCC and IAR™ toolchains:

- Using the internal temperature sensor
- Offset and gain calibration of the ADC

The ADC driver manages reserved bits and reserved registers. Firmware developed on the AVR XMEGA B and D targets don’t need to be modified to run on the AVR XMEGA A target.

Flags are defined within ASF to authorize only available registers when compiling.

5.2 Channel registers

All registers dedicated to a channel are listed in Table 5-1. If the ADC has four channels (AVR XMEGA A), four channel registers are available with the corresponding addresses:

- Channel 0: CTRL = 0x20, MUXCTRL = 0x21…
- Channel 1: CTRL = 0x28, MUXCTRL = 0x29…
- Channel 2: CTRL = 0x30, MUXCTRL = 0x31…
- Channel 3: CTRL = 0x38, MUXCTRL = 0x39…

Table 5-1. Channel registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	CTRL	START	_	_	GAIN[2:0]			INPUTMODE[1:0]	
0x01	MUXCTRL	_	_	MUXPOS[3:0]				MUXNEG[1:0]	
0x02	INTCTRL	_	_	_	_	INTMODE[1:0]		INTLVL[1:0]	
0x03	INTFLAG	_	_	_	_	_	_	_	IF
0x04	RESL	RES[7:0]							
0x05	RESH	RES[15:8]							

Only for channel 0:

0x06	SCAN	INPUTOFFSET[3:0]	INPUTSCAN[3:0]

5.3 ADC common registers

This section describes the register differences, and helps the user to check software compatibility between ADCs.

Table 5-2. ADC registers

	AVR XMEGA A specific
	AVR XMEGA B specific

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	CTRLA	DMASEL1	DMASEL0	CH3START	CH2START	CH1START	CH0START	FLUSH	ENABLE
0x01	CTRLB	_	_	_	CONVMODE	FREERUN	RESOLUTION1	RESOLUTION0	_
0x02	REFCTRL	_	REFSEL2	REFSEL1	REFSEL0	_	_	BANDGAP	TEMPREF
0x03	EVCTRL	SWEEP1	SWEEP0	EVSEL2	EVSEL1	EVSEL0	EVACT2	EVACT1	EVACT0
0x04	PRESCALER	_	_	_	_	_	PRESCALER2	PRESCALER1	PRESCALER0
0x06	INTFLAGS					CH3IF	CH2IF	CH1IF	CH0IF
0x07	TEMP	TEMP[7:0]							
0x0C	CALL	CAL[7:0]							
0x0D	CALH	_	_	_	_	CAL[11:8]			
0x10	CH0RESL	CH0RES[7:0]							
0x11	CH0RESH	CH0RES[15:8]							
0x12	CH1RESL	CH1RES[7:0]							
0x13	CH1RESH	CH1RES[15:8]							
0x14	CH2RESL	CH2RES[7:0]							
0x15	CH2RESH	CH2RES[15:8]							
0x16	CH3RESL	CH3RES[7:0]							
0x17	CH3RESH	CH3RES[15:8]							
0x18	CMPL	CMPL[7:0]							
0x19	CMPH	CMPH[15:8]							
0x20	CH0 Offset	Address of the first register dedicated to channel 0 is: 0x20							
0x28	CH1 Offset	Address of the first register dedicated to channel 0 is: 0x28							
0x30	CH2 Offset	Address of the first register dedicated to channel 0 is: 0x30							
0x38	CH3 Offset	Address of the first register dedicated to channel 0 is: 0x38							

If the device has two ADC modules (Atmel AVR XMEGA A and B), all registers in Table 2 1 are duplicated.

6 Conversion mode selection

6.1 Introduction

The Atmel AVR XMEGA A, B, and D ADCs offer four modes:

- Internal: Input sources are connected to internal analog signals (temperature, bandgap, etc.)
- Single-ended: The negative input is connected to ground. The input source is connected to positive input
- Differential without gain: The input signal is connected between positive and negative inputs
- Differential with gain: A selectable gain modifies the input signal level before ADC conversion.

6.2 Summary

Two bit fields are linked for conversion mode selection: INPUTMODE[1:0] and CONVMODE, respectively, in the CTRL and CTRLB registers.

Unsigned mode is available only if differential mode is not selected.

Table 6-1. Conversion modes

INPUTMODE[1:0]	Conversion mode	CONVMODE = 1	CONVMODE = 0
		Signed mode	Unsigned mode
00	*Internal*	Yes	Yes
01	*Single ended*	Yes	Yes
10	*Differential without gain*	Yes	_
11	*Differential with gain*	Yes	_

AVR XMEGA A, B, and D offer the same four conversion modes. Differences appear only on the available inputs/outputs (DAC, DMA, etc.).

6.3 Positive Input Pin

The ADC positive input pins are connected to analog input pins or internal analog pins. The value programmed in the MUXPOS[3:0] field (see MUXCTRL register) selects the input pin.

The list of available input pins depends on the Atmel AVR XMEGA family.

Table 6-2. Positive input pin selection

	AVR XMEGA A specific			
	AVR XMEGA B and D specific			
MUXPOS[3:0]	***Internal***		***Single-ended*** ***Differential without gain*** ***Differential with gain***	
	AVR XMEGA A	**AVR XMEGA B and D**	**AVR XMEGA A**	**AVR XMEGA B and D**
0000	Temperature reference	Temperature reference	ADC0	ADC0
0001	Bandgap voltage	Bandgap voltage	ADC1	ADC1
0010	VCC/10	VCC/10	ADC2	ADC2
0011	DAC output	_	ADC3	ADC3
0100	_	_	ADC4	ADC4
0101	_	_	ADC5	ADC5
0110	_	_	ADC6	ADC6
0111	_	_	ADC7	ADC7
1000	_	_	_	ADC8
1001	_	_	_	ADC9
1010	_	_	_	ADC10
1011	_	_	_	ADC11
1100	_	_	_	ADC12
1101	_	_	_	ADC13
1110	_	_	_	ADC14
1111	_	_	_	ADC15

6.4 Negative Input Pin

In differential mode with gain or without gain, the ADC negative inputs are not connected to the same analog input pins.

In single ended mode, the ADC negative input pin is always connected to ground.

If internal mode or single-ended mode are selected, the MUXNEG[1:0] fields are not used.

Table 6-3. Negative input pin selection

MUXNEG[1:0]	*Differential without gain*	*Differential with gain*	*Internal*	*Single Ended*
00	ADC0	ADC4	_	_
01	ADC1	ADC5	_	_
10	ADC2	ADC6	_	_
11	ADC3	ADC7	_	_

7 Conversion mode description

The Atmel AVR XMEGA A, B, and D ADCs offer the same conversion modes.

7.1 Unsigned Single-ended mode

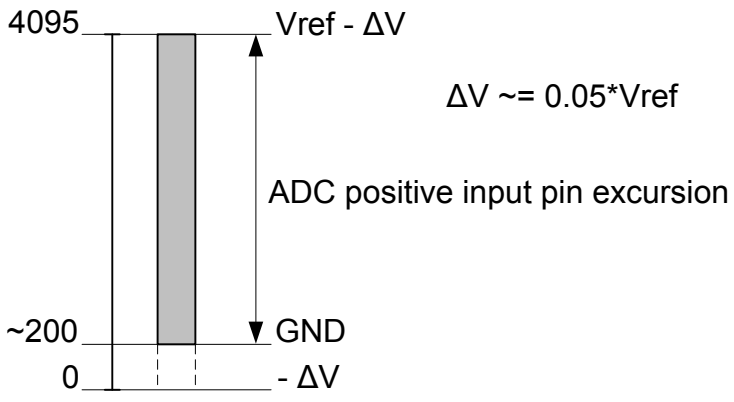
In unsigned mode, the conversion range is from ground to the reference voltage.

The resolution is 12 bits. The theoretical measurement step is Vref/4096.
A negative offset appears around ground measurement.

The approximate value corresponding to ground is around 200. This value corresponds to the digital result of ΔV (0.05 * 4096).

ΔV exists to allow zero-crossing detection.

Figure 7-1. Unsigned single-ended mode range



Advantage: This mode offers full resolution (12 bits) and zero-crossing detection.

Drawback: V_{REF} not reached (only V_{REF} - ΔV).

Domain: This mode allows using the device for Atmel QMatrix detection. Applications with limited excursions and maximum accuracy are the target (temperature sensor, battery supervision, multimeter).

7.2 Signed single-ended mode

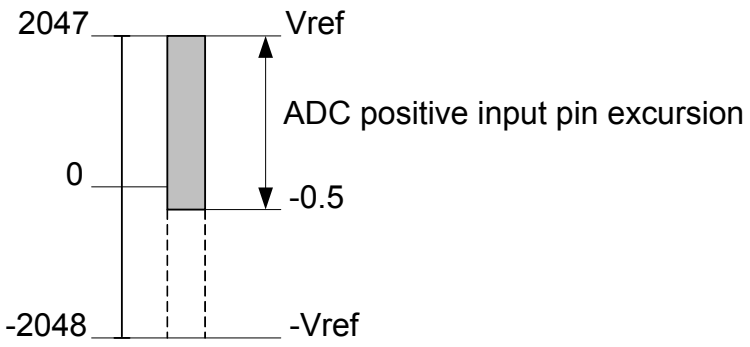
In signed mode, the conversion range is from Vref to -Vref.

The resolution is 11 bits. The theoretical measurement step is (2 * Vref)/4096.

The ADC negative input is connected to ground in this mode. The positive input voltage value is limited by the pad: $V_{IL\ min}$ (input low voltage).

In this mode, the full range is not reachable.

Figure 7-2. Signed single ended mode range



Advantage: This mode offers a full range from GND to V_{REF}.

Drawback: The mode resolution is 11 bits (plus sign). The negative voltage is limited by the microcontroller pad.

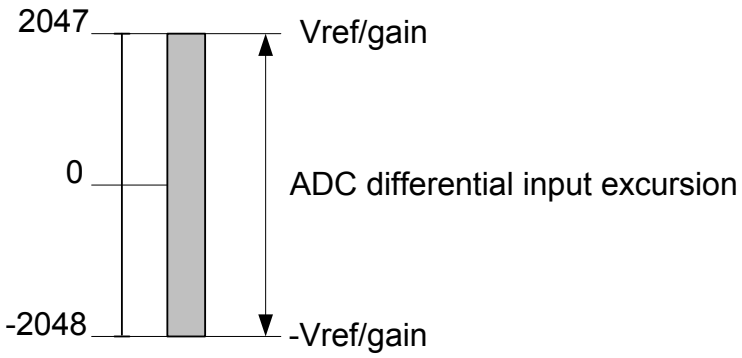
Domain: Applications needing full range and zero detection (for example, motor control).

7.3 Signed Differential Input (with x2 x4 x8 x16 x32 x64 gain/ without gain)

The input voltage is connected between positive and negative ADC inputs. The resolution is 11bits (plus sign).

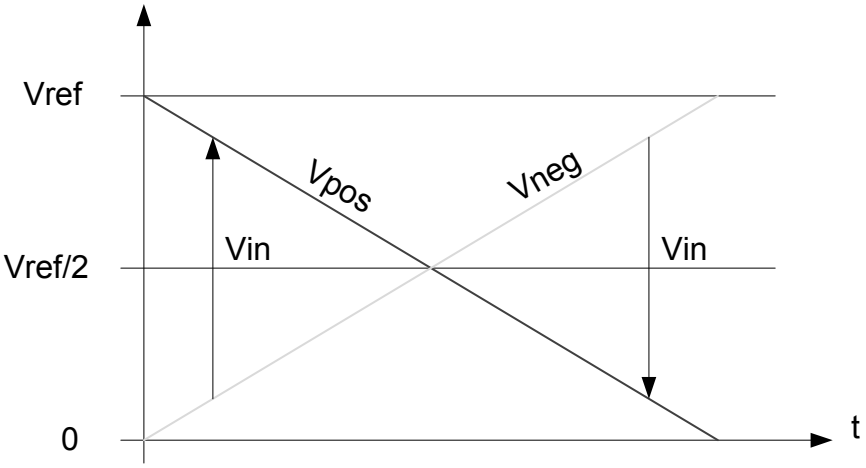
When the gain stage is used, the input signal is amplified before it reaches the ADC.

Figure 7-3. Signed differential mode range



When differential mode is selected, the input excursion on positive and negative inputs is as described in Figure 7-4.

Figure 7-4. Input voltage range



Advantage: Allows measurement of small amplitude signals with 11bits (plus sign) resolution. Differential input removes noise from the ground reference.

Drawback: Available only in differential mode.

Domain: Sensors with small signal amplitude, differential signals.

8 Conversion rate

The major difference between the Atmel AVR XMEGA A and the Atmel AVR XMEGA B and D is the conversion rate:

- 2Msps for AVR XMEGA A (pipelined ADC)
- 200ksps for AVR XMEGA B and D (cyclic ADC)

8.1 Cyclic ADC

This value corresponds to the max ADC frequency divided by the number of ADC cycles for a complete conversion:

$F_{ADC\ max}$ = 1.4MHz

Propagation delay for a 12-bit conversion = 7 ADC cycles => 200ksps

8.2 Pipelined ADC

The propagation delay for a single conversion is the same as that for a cyclic ADC. The main difference is that four channels can share the 12 basic elements. The maximum conversion rate is a complete conversion every ADC cycle.

$F_{ADC\ max}$ = 2MHz => Propagation delay = 2Msps

Propagation delay for a 12-bit conversion = 1 ADC cycle = 2Msps

9 Voltage references

Voltage references are identical on all Atmel AVR XMEGA devices.

The bandgap is a fixed and accurate voltage. This voltage allows monitoring V_{CC}.

The Atmel AVR XMEGA B offers an additional reference of $V_{CC}/2$. This voltage reference, combined with x0.5 gain, offers a rail-to-rail excursion from V_{CC} to $-V_{CC}$ (see Figure 10-1).

Table 9-1. Voltage references.

AVR XMEGA B AVR XMEGA D	**AVR XMEGA A**		
REFSEL[2:0]	REFSEL[1:0]	***Selection***	***Description***
000	00	INT1V	Internal 1V (Bandgap)
001	01	INTVCC	Internal $V_{CC}/1.6$
010	10	AREFA	External reference on AREF pin on PORTA
011	11	AREFB	External reference on AREF pin on PORTB
100	-	INTVCC/2	Internal $V_{CC}/2$

10 Additional features

10.1 Software Selectable Gain

Gain is only available in differential mode.

If gain is used, the propagation time increases.

This is for instance a complete channel sweep triggered by a single event, or an event re-synchronized conversion to achieve a very accurate timing for the conversion.

Table 10-1. Propagation delay

Gain	*Single Ended* *Differential without gain* *Differential with gain*	*Remark*
x0.5	+0.5	AVR XMEGA B specific
x1	0	
x2	+0.5	
x4	+1	
X8	+1.5	
x16	+2	
x32	+2.5	
X64	+3	

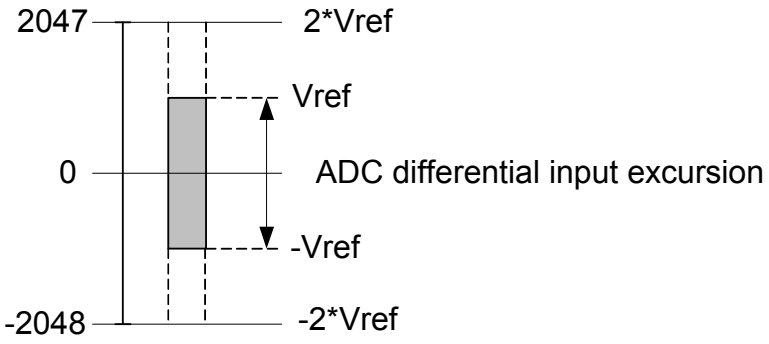
10.2 x0.5 Gain (only for AVR XMEGA B)

This gain is useful for rail-to-rail measurements in differential mode.

The x0.5 gain allows having a complete signal conversion from maximum value to minimum value.

This feature is important for measurements needing accuracy on the entire signal excursion.

Figure 10-1. x0.5 gain range



Advantage: Allows a rail to rail measurement without distortion around V_{REF} and $-V_{REF}$.

Drawback: Available only on AVR XMEGA B.

Domain: Sinusoidal signals, motor control.

10.3 DMA transfer

It is possible to use DMA to move the ADC results directly to memory or peripherals when conversions are done. The TRIGSRC[7:0] register selects which trigger source is used for triggering a transfer on the DMA channel.
ADCA or ADCB are proposed as DMA input for the Atmel AVR XMEGA A.
In addition to providing a DMA transfer request for each ADC channel, the ADC can be set up to provide a combined request for all channels. The combined request is decided according to the DMASEL value (see CTRLA register).

10.4 Scan mode

AVR XMEGA A, B and D ADCs offer a scan mode. This feature is only available on CH0. Scan mode is controlled by SCAN register.

Table 10-2. SCAN register

SCAN	INPUTOFFSET[3:0]	INPUTSCAN[3:0]

When INPUTSCAN is set to a value other than zero, the number of inputs scanned is (INPUTSCAN + 1). The next conversion is performed on input (INPUTOFFSET + MUXPOS) and INPUTOFFSET is incremented after each conversion.

The rate of conversion for CH0 is the same, regardless of the INPUTSCAN setting.

For example, if the initial values are INPUTOFFSET=0, INPUTSCAN=5 and MUXPOS=2, and then five conversions using START would be needed to cycle through input 2-7.

10.5 ADC Calibration

The production signature row offers several bytes for ADC calibration. The ADC is calibrated during production testing, and the calibration value must be loaded from the signature row into the ADC registers (CAL registers).

The calibration corrects the capacitor mismatch of the switched capacitor technology.

For the AVR XMEGA A, the calibration registers are composed of two 8-bit registers with 12 bits used for the calibration value. The 12-bit value is composed of three groups of 4 bits each. Each group corresponds to a basic element of the pipelined structure. Only the first three basic elements of the pipelined ADC are re-calibrated. The calibration value must be loaded from the signature row into the CALH and CAL ADC registers.

For the Atmel AVR XMEGA B and D, the calibration register is composed of one 8-bit register. The 8-bit value is composed of two groups of 4 bits each. Each group corresponds to a switch of the cyclic structure. The calibration value must be loaded from the signature row into the CAL ADC register.

The ADC driver available in Atmel AVR Software Framework (ASF) has an init function included for management of the calibration registers.

This is not a calibration for gain error and offset error.

Table 10-3. ADC calibration in production signature row

	AVR XMEGA A	AVR XMEGA B	AVR XMEGA D
ADCACAL0	Yes	Yes	Yes
ADCACAL1	Yes	_	_
ADCBCAL0	Yes	Yes	_
ADCBCAL1	Yes	Yes	_

10.6 Temperature sensor calibration

The signature row contains a 12-bit ADCA value from a temperature measurement done in production test. This measurement corresponds to 85°C.

This measurement can be used for temperature sensor calibration.

Table 10-4. Temperature sensor calibration in production signature row

	AVR XMEGA A	AVR XMEGA B	AVR XMEGA D
TEMPSENSE0	Yes	Yes	Yes
TEMPSENSE1	Yes	Yes	Yes

11 Conclusion

The following tables help in the selection of the ADC, depending on the application. A study of the application gives the ADC type to use (Table 11-2), after selection of conversion mode (Table 11-1).

Table 11-1. Conversion mode selection

	Unsigned Single-ended	***Signed Single-ended***	***Signed differential without gain***	***Signed differential with gain***
Resolution	12-bit	11-bit + sign	11-bit + sign	11-bit + sign
Advantage	Zero-crossing	No ΔV.	No external scaling system	No external scaling system Rail to rail conversion with x0.5 gain
Drawback	V_{REF} out of excursion. ΔV not fixed.	Negative voltage limited by pad	–	–
Application	QMatrix	Positive signals	Signal with excursion between Vref and -Vref	Signal with scaling needed

The major interest of XMEGA™ A comes from the pipelined structure to manage several conversions in parallel.

Table 11-2. ADC type selection

	A	***B***	***D***
What is the max propagation on each channel?	2Msps with 4 simultaneous channels	200ksps / Number of channels	200ksps / Number of channels
ADC result transferred with DMA	Yes	–	–
SWEEP mode	Automatic sweep	Manual sweep	Manual sweep
DAC output for ADC internal input	Yes	–	–
x0.5 gain	–	Yes	–

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