3 SHAMONINA, E., KALININ, V.A., RINGHOFER, K.H., and SOLYMAR, L.: 'Magnetoinductive waveguide', *Electron. Lett.*, 2002, **38**, pp. 371–373
4 SHAMONINA, E., KALININ, V.A., RINGHOFER, K.H., and SOLYMAR, L.: 'Magnetoinductive waves in one, two and three dimensions', *J. Appl. Phys.*, 2002, **92**, pp. 6252–6261

100 GHz dynamic frequency divider in SiGe bipolar technology

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A 100 GHz dynamic frequency divider and a 62 GHz static frequency divider are presented, both using a −3.8 V supply and designed in IBM's 0.12 μm SiGe technology with f_T of 207 GHz and f_{MAX} of 285 GHz. Static divider performance is compared to three other static dividers designed in IBM's 0.18 μm SiGe BiCMOS technology.

Introduction: Static and dynamic frequency divider performance is a standard benchmark used to qualify and compare high-speed technologies. To our knowledge, the fastest dynamic divider reported to date operates at 90 GHz [1] and uses InP/InGaAs HBTs. The fastest reported SiGe HBT dynamic divider operates at 82 GHz [2]. The record numbers for static dividers are 75 GHz for InAlAs/InGaAs HBT technology [3] and 71.8 GHz for SiGe [4]. We have designed and tested a dynamic and a static divider in IBM's 207 GHz f_T/285 GHz f_{MAX} 0.12 μm SiGe bipolar technology [5]. Additionally, we report and compare the performance and circuit topologies of three different static dividers designed in IBM's 120 GHz f_T/100 GHz f_{MAX} 0.18 μm SiGe BiCMOS technology.

Design: The dynamic divider uses a regenerative frequency division approach [6]. The schematic diagram of the divider core (without the input and output stages) is shown in Fig. 1. Both the dynamic and the static 0.12 μm SiGe dividers were designed for a −3.6 V nominal supply. This choice of power supply value was based on the use of the single emitter follower ECL logic in both designs. The static divider is a conventional two-latch toggle flip-flop. This same static divider was also implemented in a previous 0.18 μm generation of the SiGe bipolar technology. Comparing these two very similar circuits, one can determine the part of the performance increase which is due solely to the technology improvement. Two other variants of the static divider have also been designed and tested in 0.18 μm SiGe. One of them uses the same basic master-slave D-flip-flop circuit with addition of inductive peaking into the latch resistor loads. This approach trades-off chip area for a possible increase in performance, while using the same supply voltage and dissipating the same power. Another static divider variant employs a double emitter follower E^2CL logic family. The obvious disadvantage of the E^2CL approach is the need for a higher supply voltage (typically −5.2 V), and a higher transistor count, both resulting in a significant increase in power dissipation.

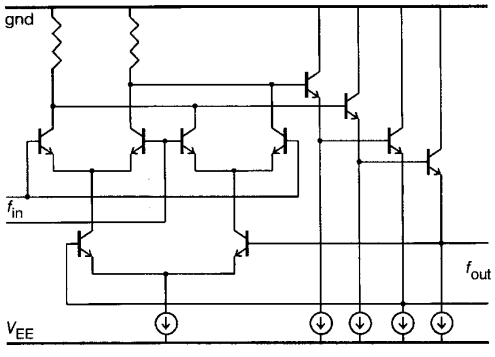

Fig. 1 *Dynamic divider circuit diagram*

Test results and discussion: Both static and dynamic 0.12 μm SiGe dividers were tested in packaged form, using a custom-made SHF module, at room temperature. From DC to 65 GHz input clock signal was generated by a commercially available synthesiser. From 66 GHz to 100 GHz a commercially available active frequency multiplier was used as a clock source. Fig. 2 shows the 50 GHz output of the dynamic divider, at 100 GHz input clock frequency. The output voltage swing is 260 mVpp (single ended). The exact value of the input power of the 100 GHz signal applied to the divider is not known, but we estimate it to be in the range between 0 and +4 dBm. At the input frequencies in the 30 to 50 GHz range the dynamic divider required only −7 dBm of input clock power and provided a 500 mVpp output (single ended). Above 60 GHz the minimum input power of the clock signal was in the 0 to +4 dBm range. In theory [6], the dynamic divider should not be operating correctly at frequencies below one third of the maximum frequency. However, applying 0 dBm of input clock power we have observed on the oscilloscope divided output signals for input frequencies down to 14 GHz. The 0.12 μm SiGe static divider was operational from 2 to 62 GHz (tested with a sinusoidal input signal). It required minimum −11 dBm of input clock power at 10 to 30 GHz, −20 dBm at 40 GHz and −6 dBm at 50 GHz, providing a 400 mVpp output signal (single ended). At least −1 dBm of input power was required for 62 GHz operation.

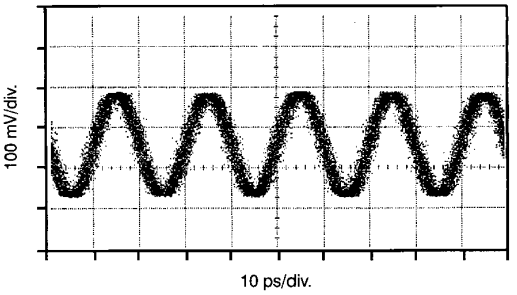

Fig. 2 *Output 50 GHz signal of dynamic divider at 100 GHz input*

All static 0.18 μm SiGe dividers were tested on wafer, at room temperature, using high-speed picoprobes. Table 1 summarises the measured performance parameters of the dividers (device with inductive peaking is marked as 'ECLi'). Two of the dividers reported in Table 1 were tested as a part of a larger chip. For these dividers, the current I_{EE} is only an estimate (marked with a superscript 2 in the Table) for the core of the device and it does not include the power dissipated in the input/output stages. Static dividers self-oscillate when no external clock signal is applied (floating inputs). The frequency of this oscillation is an important parameter (f_{SO} in the Table) and it is directly related to the maximum speed that can be achieved by a static divider.

Table 1: Divider performance summary

	0.12 μm SiGe		0.18 μm SiGe		
	Dynamic ECL	Static ECL	Static ECL	Static ECLi	Static E^2CL
V_{EE} (V)	−3.8	−3.8	−3.6	−3.6	−5.2
I_{EE} (*Ma*)	75[1]	68[1]	32[2]	80[1]	66[2]
f_{SO} (GHz)	none	24	9	18	19
f_{CLK} (GHz)	100	62	33	41	49

V_{EE}: power supply; I_{EE}: current (for dividers marked with '1' this is total number for whole chip, including input and output stages; for dividers marked with '2' it is an estimate for divider core only); f_{SO}: frequency of self-oscillation; f_{CLK}: maximum input clock frequency

Comparing the self-oscillation and maximum speed data for the 0.12 and 0.18 μm SiGe ECL static dividers, we observe approximately a 2× increase in performance, in a rough correspondence with a 2× increase in f_T and f_{MAX}. We also note that a significant increase in performance within the same technology can be gained by using E^2CL or ECL with inductive peaking, as opposed to plain ECL. It is not surprising therefore that all recent record numbers reported for SiGe static dividers used E^2CL topologies (see, e.g. [4]). At the same time, since double emitter follower performance is superior to the single emitter follower performance at higher speeds, it helps explain why the 0.12 μm dynamic divider is considerably faster than the static one. Indeed,

even though the design is formally ECL, the schematic diagram in Fig. 1 clearly shows double emitter followers in the feedback path. Using double emitter followers in a −3.6 V design became possible only due to the unusual nature of the dynamic design, where signals generated by the upper differential pair (they could be called 'data') are fed back into a lower differential pair (where 'clock' is normally applied).

Conclusion: We have designed and tested a 100 GHz dynamic frequency divider in a 207 GHz f_T/285 GHz f_{MAX} 0.12 μm SiGe bipolar technology. To our knowledge, this is the highest number ever reported for any transistor-based divider. We also report a 62 GHz, −3.8 V static ECL divider, designed in the same 0.12 μm SiGe bipolar technology. Compared to the previous generation 120 GHz f_T/100 GHz f_{MAX} 0.18 μm SiGe BiCMOS technology, this device shows approximately a 2× increase in performance. Comparing static divider data for both technologies we expect that 0.12 μm SiGe static divider performance will benefit significantly from using a double emitter follower E^2CL circuit topology.

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References

1 TSUNASHIMA, S., NAKAJIMA, H., SANO, E., IDA, M., KURISHIMA, K., WATANABE, N., ENOKI, T., and SUGAHARA, H.: '90 GHz operation of a novel dynamic frequency divider using InP/InGaAs HBTs'. Indium Phosphide and Related Materials Conf., 2002, pp. 43–46

2 WASHIO, K., OHUE, E., ODA, K., HAYAMI, R., TANABE, M., SHIMAMOTO, H., HARADA, T., and KONDO, M.: '82 GHz dynamic frequency divider in 5.5 ps ECL SiGe HBTs', *ISSCC Dig. Tech. Pap.-IEE Int. Solid-State Circuits Conf.*, 2000, pp. 210–211

3 MATHEW, T., KIM, H., JAGANATHAN, S., SCOTT, D., KRISHNAN, S., WEI, Y., URTEAGA, M., LONG, S., and RODWELL, M.: '75 GHz ECL static frequency divider using InAlAs/InGaAs HBTs', *Electron. Lett.*, 2001, **37**, pp. 667–668

4 WURZER, M., BOCK, J., KNAPP, H., AUFINGER, K., and MEISTER, T.: '71.8 GHz static frequency divider in a SiGe bipolar technology'. Proc. IEEE Bipolar/BiCMOS Circuits and Technology Mtg., Monterey, CA, USA, 2002, pp. 216–219

5 JAGANNATHAN, B., KHATER, M., PAGETTE, F., RIEH, J.-S., ANGELL, D., CHEN, H., FLORKEY, J., GOLAN, F., GREENBERG, D.R., GROVES, R., JENG, S., JOHNSON, J., MENGISTU, E., SCHONENBERG, K., SCHNABEL, C., SMITH, P., STRICKER, A., AHLGREN, D., and FREEMAN, G.: 'Self-aligned site NPN transistors with 285 GHz f/sub MAX/ and 207 GHz f/sub T/ in a manufacturable technology', *IEEE Electron Device Lett.*, 2002, **23**, pp. 258–260

6 KNAPP, H., MEISTER, T.F., WURZER, M., ZOSCHG, D., AUFINGER, K., and TREITLINGER, L.: 'A 79 GHz dynamic frequency divider in SiGe bipolar technology', *Dig. Tech. Pap.-IEE Int. Solid-State Circuits Conf.*, 2000, pp. 208–209

Class-F dual-fed distributed amplifier

K.W. Eccleston

The single-ended dual-fed distributed amplifier allows efficient combining of the output power of several FETs without multi-way power combiners. It is shown that this configuration can be operated under class-F operating conditions, thereby allowing high efficiencies.

Introduction: The conventional distributed amplifier offers broad bandwidth but has low efficiency since half of the FET output power is wasted in an idle termination, and only one of the FETs is fully utilised. Further, such amplifiers are normally operated in the class-A mode which has an inherently low efficiency. The single-ended dual-fed distributed amplifier (SE-DFDA) [1] allows all the FET output power to be utilised. The work of Moazzam and Aitchison [1] only considered single-FET SE-DFDAs. The SE-DFDA concept can be extended to N FETs, and if the FETs are spaced 180°, all FETs have identical loadlines, which can be chosen optimally [2]. The SE-DFDA therefore allows efficient power combining of FET output power without using bulky multi-way power combiners [2]. In the previous work on the power SE-DFDA, class-A [2] and class-B [3] operation was demonstrated. A class-F amplifier [4] can offer both high output power and high efficiency (up to 100% for ideal transistors). To date, the developments reported in the literature pertaining to class-F amplifiers have essentially only considered single transistor amplifiers. In this Letter we propose a class-F single-ended dual-fed distributed amplifier (SE-DFDA) configuration that combines several FETs. This proposal therefore partners the SE-DFDA power combining approach with the high efficiency of class-F operation.

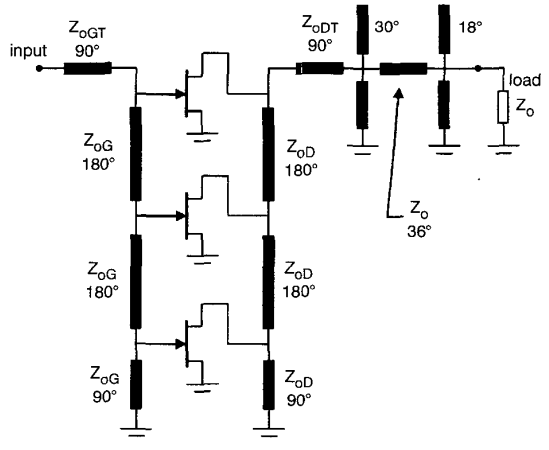

Fig. 1 *Circuit diagram of 3-FET class-F single-ended dual-fed distributed amplifier (electrical lengths specified at fundamental frequency)*

Class-F dual-fed distributed amplifier: In class-F operation, the input drive is established so that the drain current is a half-sinusoid waveform similar to that in class-B operation, and the drain voltage is a square waveform. High efficiency results as the drain voltage is low when the drain is conducting and vice-versa. To achieve a square drain voltage waveform, the load presented to the drain is resistive for the fundamental, short-circuit for the even harmonics and open-circuit for the odd harmonics. This can be achieved by coupling a parallel resonant load to the FET drain with a quarter-wave transformer. The resonator also suppresses harmonics at the output. For a square waveform to exist, odd harmonics must be present in the drain current and is achieved by appropriate choice of the FET gate bias voltage and input power so that the drain current waveform is not a pure half-sinusoid [4].

Fig. 1 shows the circuit topology of the proposed class-F single-ended dual-fed distributed amplifier and is based on the single-ended dual-fed distributed amplifier [2, 3]. Critical impedances and electrical lengths are indicated in Fig. 1. The dual-feeding of both the gate and drain lines is achieved by the short circuit terminations at the ends of the gate and drain lines farthest from the input and output ports, respectively. These short-circuit terminations allow DC bias voltages to be fed to the FETs and short-circuit the FET drains at even harmonics. The load for the SE-DFDA drain line consists of a quarter-wave transformer that is terminated by the external resistive load (Z_o) and a series of stubs, where Z_o is typically 50 Ω. The open-circuit stubs short-circuit the load at the third and fifth harmonics and the adjacent short-circuit stubs parallel resonate the open-circuit stubs at the fundamental frequency. Therefore, the quarter-wave transformer is