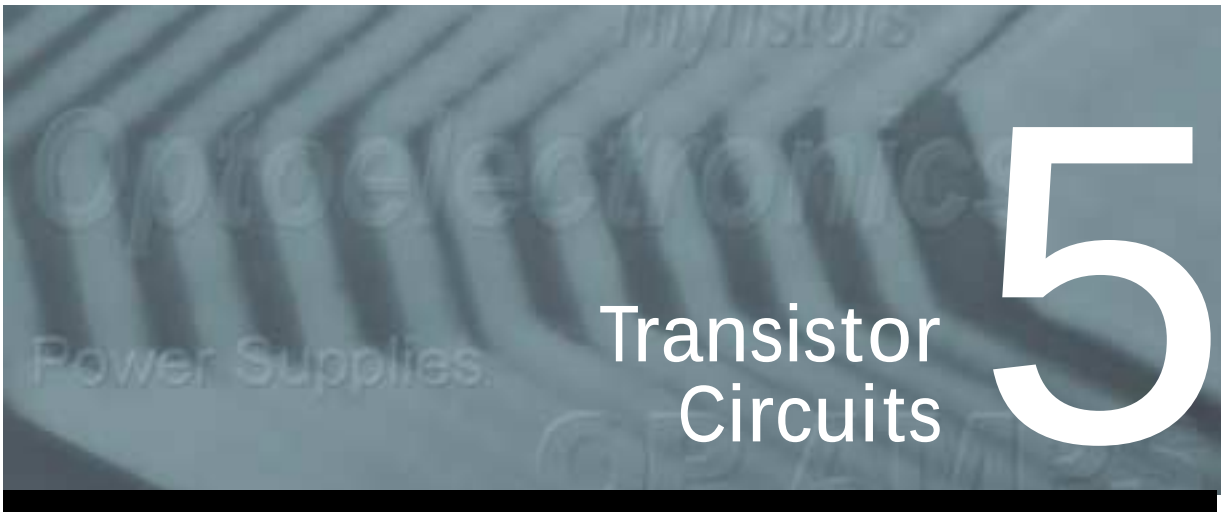

OBJECTIVES

After studying the material in this chapter, you will be able to describe and/or analyze:

- the need for biased and signal stabilizing circuitry,
- common-emitter amplifier circuits using voltage divider biasing,
- common-emitter amplifier circuits using emitter biasing,
- common-emitter amplifier circuits using voltage feedback biasing,
- RC coupled multistage amplifiers,
- direct coupled multistage amplifiers, and
- troubleshooting procedures for transistor circuits.

5.1 INTRODUCTION

In the previous chapter you studied the bipolar transistor and learned how to make a simple amplifier circuit. Our study was limited, however, in that we assumed an ideal transistor and considered only single-stage amplifiers. In this chapter, we will consider transistor limitations and multistage amplifier circuits.

Q-POINT INSTABILITY CAUSED BY BETA

Because manufacturers cannot produce transistors with a precise beta value and because beta also changes with environmental conditions, the exact value for beta is unknown. The typical beta, given on data sheets, is an approximation. The actual beta for the individual transistor can range from minus 50% to plus 100% of the typical beta given by the manufacturer. Example 5.1 shows how the acceptable range of beta is calculated.

EXAMPLE 5.1

If a transistor has a typical beta of 150, what is the acceptable range of beta for the transistor?

EXAMPLE 5.1 continued

Step 1. Calculate the minimum beta:

$$\beta_{min} = \beta_{typical} - (\beta_{typical} \times 50\%) = 150 - (150 \times 50\%) = 75$$

Step 2. Calculate the maximum beta:

$$\beta_{max} = \beta_{typical} + (\beta_{typical} \times 100\%) = 150 + (150 \times 100\%) = 300$$

A transistor with a typical beta of 150 is considered good if its actual beta is within the range of 75 to 300.

The beta of a transistor also varies with changes in temperature. Figure 5–1 shows a graph of beta versus temperature. For an operational temperature of 0ºC, the beta of the 2N3904 is 140, and at a temperature of 100ºC, the beta is 220.

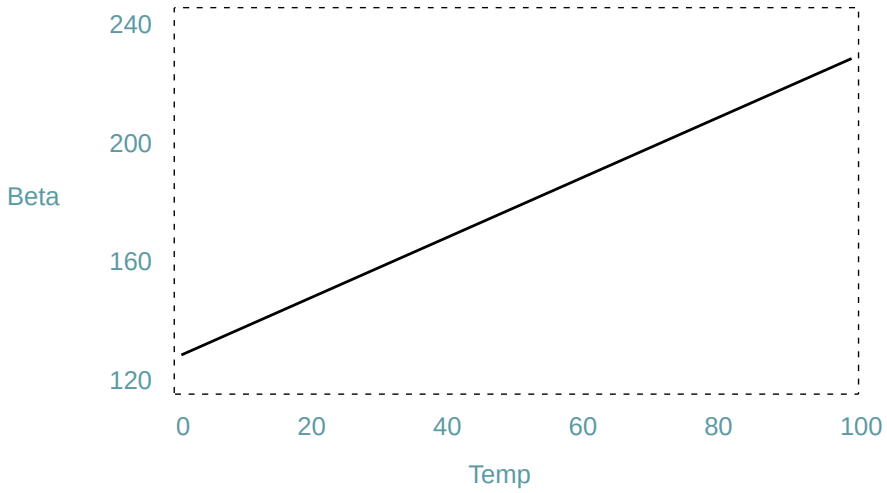

FIGURE 5–1 Beta versus temperature

In order for a transistor amplifier circuit to be useful, the circuit must be stable and predictable. With no signal applied to the amplifier circuit, the amplifier is in the quiescent state. At quiescence, the voltage across the transistor (V_{CE}) and the current through the transistor (I_C) should be constant. When the signal is applied to a class-A amplifier, the signal will cause variations around the quiescent point, also referred to as the Q-point. It is the function of the bias circuit to hold the circuit stable at the designed Q-point. Example 5.2 shows how the base-biased amplifier is not effective at holding the Q-point constant with changes in beta.

EXAMPLE 5.2

Calculate the values of I_c and V_{CE} for the transistor amplifier in Figure 5–2, assuming the transistor has a beta of (a) 100 and (b) 180.

Step 1. Calculate I_C and V_c for a beta equal to 100.

$$I_B = V_{Rb} / R_b = 9.3\text{ V}/930\text{ k}\Omega = 10\ \mu\text{A}$$

$$I_c = \beta I_b = 100 \times 10\ \mu\text{A} = 1\text{ mA}$$

$$V_{Rc} = I_c \times R_c = 1\text{ mA} \times 5\text{ k}\Omega = 5\text{ V}$$

$$V_c = V_{cc} - V_{Rc} = 10\text{ V} - 5\text{ V} = 5\text{ V}$$

EXAMPLE 5.2 continued

Step 2. Calculate I_C and V_c for a beta equal to 180.

$$I_B = V_{Rb}/R_b = 9.3\text{ V}/930\text{ k}\Omega = 10\ \mu\text{A}$$
$$I_c = \beta I_b = 180 \times 10\ \mu\text{A} = 1.8\text{ mA}$$
$$V_{Rc} = I_c \times R_c = 1.8\text{ mA} \times 5\text{ k}\Omega = 9\text{ V}$$
$$V_c = V_{cc} - V_{Rc} = 10\text{ V} - 9\text{ V} = 1\text{ V}$$

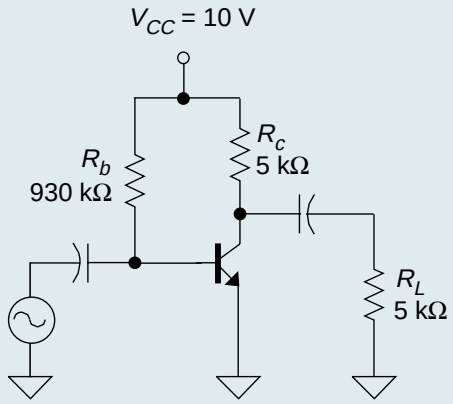

FIGURE 5–2 Base-biased amplifier

THE VOLTAGE DIVIDER

A simple voltage divider circuit can be used to provide reference voltage. Two resistors connected in series can provide any voltage level below the supply voltage at the junction of the two resistors by adjusting the ratio of the resistors. If the junction point is connected to other circuitry, the voltage at the junction may drop because of the loading effect of the added circuitry. However, if the resistance of the added circuitry is high compared to the resistors in the voltage divider, the voltage loading may be negligible. Example 5.3 illustrates how a lightly loaded voltage divider circuit can maintain a near constant output voltage.

EXAMPLE 5.3

Calculate the voltage at the junctions of R_1 and R_2 for both circuits shown in Figure 5–3 and determine the percentage of change in voltage caused by adding the load.

Step 1. Calculate the voltage at the test point for the circuit in Figure 5–3(a). The circuit is an unloaded voltage divider, and the voltage at the test point can be calculated by using the voltage divider formula.

$$V_{\text{out}} = V_{\text{in}} \times R_2/(R_1 + R_2) = 12\text{ V} \times 2\text{ k}\Omega/\text{xü0 k}\Omega + 2\text{ k}\Omega) = 2\text{ V}$$

Step 2. Calculate the voltage at the test point for the circuit in Figure 5–3(b). The parallel equivalent resistance (R_{EQ}) of R_2 and the load resistor must first be calculated before the voltage divider formula can be used.

$$R_{EQ} = R_2 \parallel R_L = 2\text{ k}\Omega \parallel 20\text{ k}\Omega = 1.82\text{ k}\Omega$$
$$V_{\text{out}} = V_{\text{in}} \times R_{EQ}/(R_1 + R_{EQ})$$
$$V_{\text{out}} = 12\text{ V} \times 1.82\text{ k}\Omega/(10\text{ k}\Omega + 1.82\text{ k}\Omega) = 1.85\text{ V}$$

EXAMPLE 5.3 continued

Step 3. Calculate the percent of change in voltage caused by loading the voltage divider circuit.

$$\%\Delta = \Delta V/V \times 100\%$$
$$\Delta V = 2\text{ V} - 1.85\text{ V} = 0.15\text{ V}$$
$$\%\Delta = 0.15\text{ V}/2\text{ V} \times 100\% = 7.5\%$$

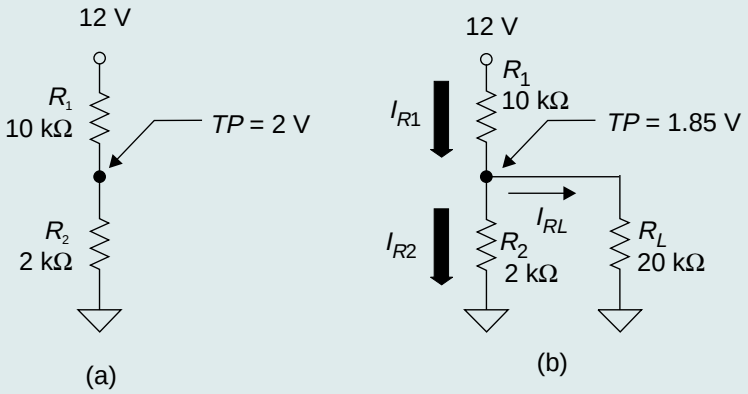

FIGURE 5–3 Voltage divider circuit

The voltage divider circuit in Figure 5–3(b) can be considered a lightly loaded voltage divider because the load resistor is ten times the resistance of R_2. The load causes the voltage at the junction of the voltage divider to drop by 7.5%. Loads with higher resistance will cause a smaller drop in voltage, and loads with lower resistance will cause a greater drop. A good rule of thumb is to consider the voltage divider lightly loaded if the load is ten times or greater the value of the parallel resistor (R_2 in this case). For lightly loaded voltage dividers, the voltage at the junction of the divider can be approximated using the simple voltage divider formula.

Figure 5–3(b) shows that the conventional current through R_1 divides, and a portion of the current flows through R_2 while the remainder flows through the load resistor. If the voltage divider is lightly loaded, most of the current will flow through R_2, and less than 10% of the current will flow through the load.

5.2 VOLTAGE DIVIDER BIASING

The amplifier circuit shown in Figure 5–4(a) uses voltage divider biasing. This method of biasing has proven to be a popular way to design bipolar transistor amplifiers. The circuit counteracts the effects of the uncertainty of beta. For DC bias analysis, the circuit can be simplified as shown in Figure 5–4(b) because the capacitors are considered open to the DC bias currents.

The name *voltage divider* comes from the fact that the base voltage is provided by a voltage divider formed by R_{b1} and R_{b2}. The voltage at the junction of R_{b1} and R_{b2} holds the base voltage constant. The circuit is always designed so the base current (I_B) is less than 10% of the current flowing through R_{b2}. Therefore, the voltage divider is essentially not loaded by the base current flow.

Since the voltage divider formed by R_{b1} and R_{b2} is lightly loaded, the base voltage (V_B) can be easily calculated by using the simple voltage divider formula. The base/emitter junction is forward-biased. Therefore, the emitter voltage (V_E) will be one junction drop different than the

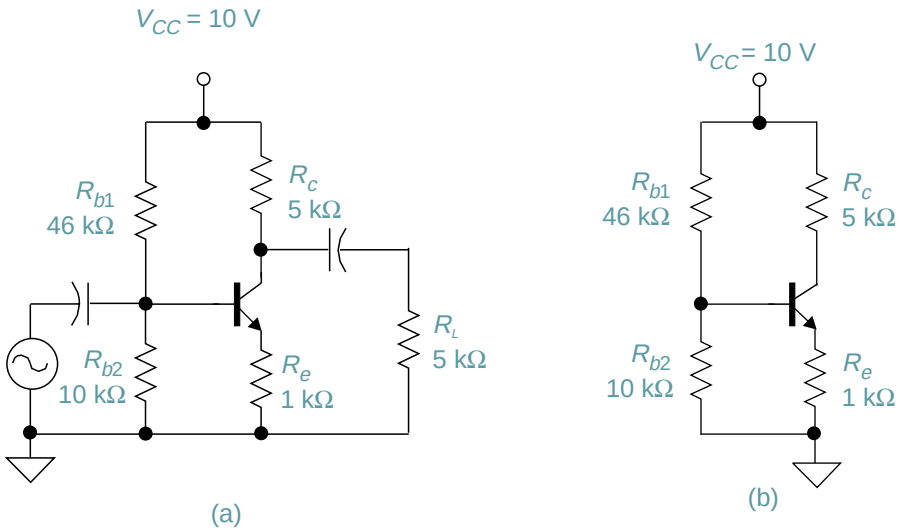

FIGURE 5–4 Voltage divider biasing

base voltage. Once the voltage on the emitter is known, the emitter current (I_E) can be easily calculated using Ohm's law, since R_e is connected between the emitter and ground. The collector current (I_C) can be approximated, since it is almost the same as the emitter current. With the collector current known, the collector voltage (V_C) can be calculated.

The preceding paragraph gave the procedures for calculating all of the bias voltages and currents for a voltage divider biased amplifier. Note that the calculations were completely independent of the beta of the transistor. This means the voltage divider biased amplifier will maintain a constant Q-point (I_C will be constant) even with large changes in beta. The circuit design does depend on a minimum beta, but we can be sure the engineer designed the circuit for the minimum beta of the transistor. Example 5.4 will show you how easy it is to calculate the bias voltages and currents for a voltage divider biased amplifier circuit.

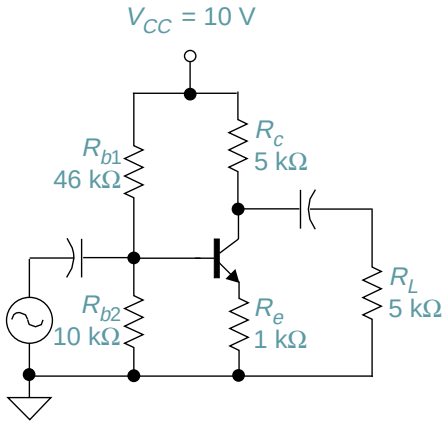

FIGURE 5–5 Voltage divider biased amplifier circuit

EXAMPLE 5.4

Calculate V_B, V_E, I_E, I_C, V_C, and V_{CE} for the amplifier circuit in Figure 5–5.

Step 1. Calculate the base voltage (V_B). Since the base voltage divider is lightly loaded, we can use the simple voltage divider formula.

EXAMPLE 5.4 continued

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2})$$
$$V_B = 10\text{ V} \times 10\text{ k}\Omega/(46\text{ k}\Omega + 10\text{ k}\Omega) = 1.8\text{ V}$$

Step 2. Calculate the emitter voltage (V_E). The base/emitter junction is forward-biased. The circuit is using a silicon NPN transistor, so the base must be 0.7 V more positive than the emitter.

$$V_E = V_B - V_{BE}$$
$$V_E = 1.8\text{ V} - 0.7\text{ V} = 1.1\text{ V}$$

Step 3. Calculate the emitter current (I_E) and collector current (I_C). Ohm's law can be used to calculate the emitter current, since $R_{E(\text{total})}$ is connected between the emitter and ground.

$$I_E = V_E / R_{E(\text{total})}\ (R_{E(\text{total})} = R_e \text{ in this case.})$$
$$I_E = 1.1\text{ V}/1\text{ k}\Omega = 1.1\text{ mA}$$
$$I_E \approx I_C\ (\text{Base current is small; therefore, } I_E \text{ is approximately equal to } I_C.)$$
$$I_C \approx 1.1\text{ mA}$$

Step 4. Calculate the collector voltage. With the collector current known, the voltage drop across R_c can be calculated. If the voltage across R_c is subtracted from the supply voltage (V_{CC}), the voltage on the collector can be found.

$$V_{Rc} = I_c \times R_c = 1.1\text{ mA} \times 5\text{ k}\Omega = 5.5\text{ V}$$
$$V_c = V_{cc} - V_{Rc} = 10\text{ V} - 5.5\text{ V} = 4.5\text{ V}$$

Step 5. Calculate the collector to emitter voltage (V_{CE}). The voltage across the transistor can be calculated by finding the difference in voltage between the collector and the emitter.

$$V_{CE} = V_C - V_E$$
$$V_{CE} = 4.5\text{ V} - 1.1\text{ V} = 3.4\text{ V}$$

Voltage divider biasing uses current-mode feedback to stabilize the circuit. The current flowing through the emitter resistor causes negative feedback and stabilizes the circuit. Voltage divider biasing is a practical way to make the bias circuitry independent of beta. This approach is not the only means of stabilization, but it is one of the most popular.

5.3 SIGNAL PARAMETERS IN VOLTAGE DIVIDER CIRCUITS

The price paid for independence from beta is a decrease in signal voltage gain. Fortunately, these lower voltage gains are predictable. The input impedance is also affected, but it increases, and in most cases this is a plus. We will discuss each of these parameters and then look at some examples.

The size and the type of resistance in the emitter leg has a great effect on the operation of the voltage divider amplifier. There are five types of resistances in the emitter leg, each of which is defined in the following list. As you continue with the chapter, use this list to make sure you understand the type of emitter resistance being discussed.

r'e is the internal signal resistance of the base/emitter junction ($r'_e = 25\text{ mV}/I_E$).

Re is an external emitter resistor that opposes signal current (AC) and bias current (DC).

RE is an external emitter resistor that only opposes bias current (DC).

$\boldsymbol{r_e}$ is the total signal (AC) resistance in the emitter leg and is equal to r'_e plus R_e.
$\boldsymbol{R_{E(total)}}$ is the total bias (DC) resistance in the emitter leg and is equal to R_E plus R_e.

INPUT IMPEDANCE

The general formula for input impedance is $z_{in} = r_b \parallel \beta r_e$. Resistance r_b is the equivalent signal resistance to ground on the base leg, and r_e is the equivalent signal resistance to ground on the emitter leg. Figure 5–6(a) shows a voltage divider biased amplifier circuit. From the perspective of the signal generator, resistors R_{B1} and R_{B2} appear in parallel as shown in Figure 5–6(b). Remember the power supply bus is at signal ground. This parallel combination is shown as r_b in Figure 5–6(c).

The path through the reverse-biased base/collector junction is considered an open. Figure 5–6(b) shows that the values of r'_e and R_e are seen through the forward-biased base/emitter junction. The resistance r_e is the series equivalent of r'_e and R_e as shown in Figure 5–6(c). The signal resistance (r_e) in the emitter leg must be multiplied by the value of beta as shown in Figure 5–6(c). Example 5.5 shows how input impedance of a voltage divider biased amplifier can be calculated using circuit values.

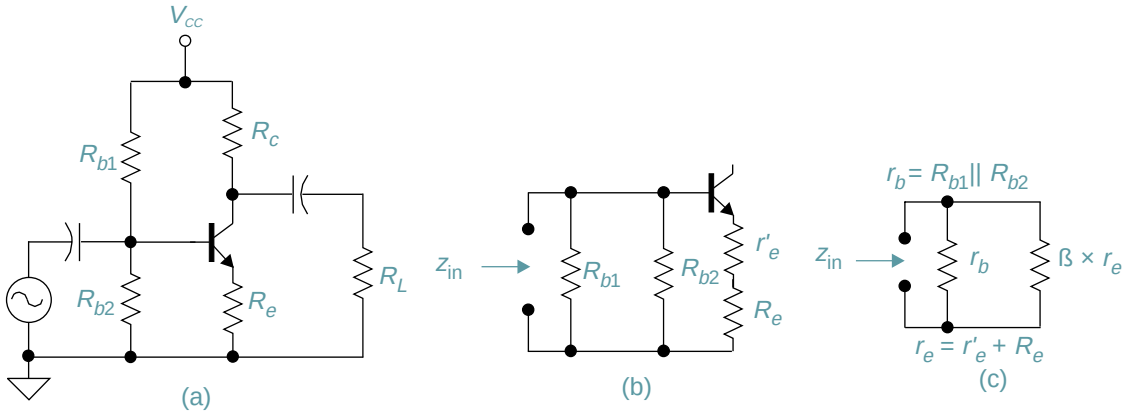

FIGURE 5–6 Input impedance of the voltage divider circuit

EXAMPLE 5.5

Assume a beta of 100 and calculate the input impedance of the circuit in Figure 5–7.

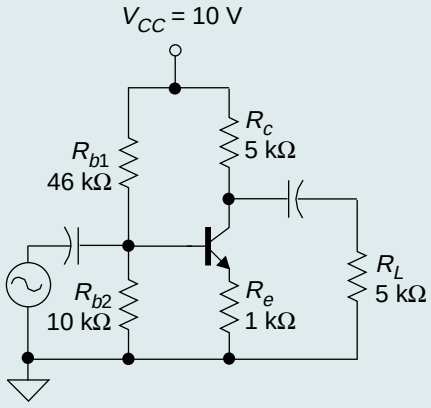

FIGURE 5–7 Voltage divider biased amplifier circuit

EXAMPLE 5.5 continued

Step 1. Calculate the biased emitter current. The biased emitter current is needed to calculate the value of r'_e.

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2})$$

$$V_B = 10\text{ V} \times 10\text{ k}\Omega/(46\text{ k}\Omega + 10\text{ k}\Omega) = 1.8\text{ V}$$

$$V_E = V_B - V_{BE}$$

$$V_E = 1.8\text{ V} - 0.7\text{ V} = 1.1\text{ V}$$

$$I_E = V_E/R_{E(\text{total})}\ (R_{E(\text{total})} = R_e \text{ in this case.})$$

$$I_E = 1.1\text{ V}/1\text{ k}\Omega = 1.1\text{ mA}$$

Step 2. Calculate the signal resistance of the base/emitter junction.

$$r'_e = 25\text{ mV}/I_E = 25\text{ mV}/1.1\text{ mA} = 23\ \Omega$$

Step 3. Draw an equivalent circuit showing how R_{b1}, R_{b2}, R_e, and r'_e appear from the perspective of the signal generator. The equivalent circuit is shown in Figure 5–8.

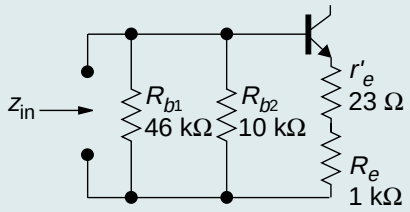

FIGURE 5–8 Input impedance equivalent circuit

Step 4. Calculate the signal resistance in the base leg (r_b).

$$r_b = R_{b1} \parallel R_{b2} = 46\text{ k} \parallel 10\text{ k}\Omega = 8.2\text{ k}\Omega$$

Step 5. Calculate the signal resistance in the emitter leg (r_e).

$$r_e = r'_e + R_e = 23 + 1\text{ k}\Omega = 1023\ \Omega$$

Step 6. Multiply the emitter leg signal resistance times beta. (Assume beta equals 100.)

$$\beta \times r_e = 100 \times 1023 = 102.3\text{ k}\Omega$$

Step 7. Draw the simplified equivalent circuit showing the base signal resistance in parallel with the emitter path signal resistance. The equivalent circuit is shown in Figure 5–9.

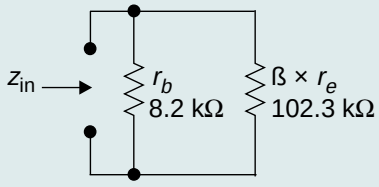

FIGURE 5–9 Simplified equivalent circuit

Step 8. Calculate the circuit input impedance by finding the parallel equivalent of the signal base resistance and the signal emitter path resistance.

$$z_{in} = r_b \parallel \beta r_e = 8.2\text{ k}\Omega \parallel 102.3\text{ k}\Omega = 7.6\text{ k}\Omega$$

Two points should be noted. First, if the value of R_e is large in comparison to the value of r'_e, then r'_e can be dropped from the calculation. Second, note that beta is still in the equation, but by examining Example 5.5, you can see that the signal base resistance (r_b) is the main influence on input impedance. Because of this, changes in beta do not have a dramatic effect.

VOLTAGE GAIN OF THE VOLTAGE DIVIDER BIASED AMPLIFIER

The general formula for the voltage gain of the common emitter amplifier is $A_v = r_c/r_e$, where r_e is the signal resistance in the emitter leg and r_c is the signal resistance in the collector leg. In the base biased circuit, the only signal resistance in the emitter leg is r'_e. In the voltage divider circuit, the signal resistance in the emitter leg (r_e) is equal to r'_e plus R_e, where R_e is equal to the unbypassed resistance in the emitter leg. The signal resistance in the collector leg r_c is equal to R_c in parallel with R_L. Example 5.6 shows how the voltage gain of a circuit can be calculated from circuit component values.

EXAMPLE 5.6

Calculate the voltage gain of the circuit in Figure 5–10.

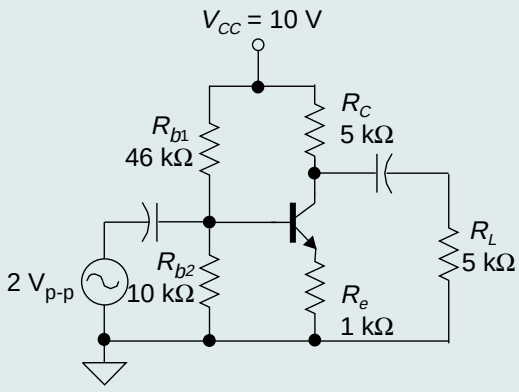

FIGURE 5–10 Voltage divider biased amplifier

Step 1. Calculate the signal resistance in the collector leg.

$$r_c = R_c \parallel R_L = 5\ \text{k}\Omega \parallel 5\ \text{k}\Omega = 2.5\ \text{k}\Omega$$

Step 2. Calculate the signal resistance of the base/emitter junction.

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2})$$

$$V_B = 10\ \text{V} \times 10\ \text{k}\Omega/(46\ \text{k}\Omega + 10\ \text{k}\Omega) = 1.8\ \text{V}$$

$$V_E = V_B - V_{BE}$$

$$V_E = 1.8\ \text{V} - 0.7\ \text{V} = 1.1\ \text{V}$$

$$I_E = V_E/R_{E(\text{total})} \quad (R_{E(\text{total})} = R_e \text{ in this case.})$$

$$I_E = 1.1\ \text{V}/1\ \text{k}\Omega = 1.1\ \text{mA}$$

$$r'_e = 25\ \text{mV}/I_E = 25\ \text{mV}/1.1\ \text{mA} = 23\ \Omega$$

Step 3. Calculate the signal resistance in the emitter leg.

$$r_e = r'_e + R_e = 23\ \Omega + 1000\ \Omega = 1023\ \Omega \text{ or } 1.023\ \text{k}\Omega$$

Step 4. Calculate the voltage gain (A_v).

$$A_v = r_c/r_e = 2.5\ \text{k}\Omega/1.023\ \text{k}\Omega = 2.44$$

The value of r'_e has little affect on the voltage gain of the circuit as long as R_e is much larger than r'_e. The voltage gain is greatly reduced, but the gain is predictable because it is independent of r'_e. In the following sections you will learn techniques to regain some of the lost gain and still have circuit stability.

Once the voltage gain of an amplifier is known, the output signal can be easily calculated by multiplying the input signal by the voltage gain. It should be noted that the output signal swing is limited by the power supply voltage and the Q-point. A good rule of thumb to follow for estimating the maximum peak-to-peak signal swing is to calculate the voltage across the transistor at quiescence (V_{CE}) and multiply this value by two. If the calculated output signal exceeds this value, clipping will occur on the peaks of the output signal. Example 5.7 shows how to calculate the output signal and the maximum output swing.

EXAMPLE 5.7

Calculate the output signal and the maximum output swing for the circuit in Figure 5–10.

Step 1. Calculate the output signal.

$$V_{out} = V_{in} \times A_v = 2\ V_{p\text{-}p} \times 2.44 = 4.88\ V_{p\text{-}p}$$

Step 2. Calculate V_{CE}. The value of V_E was calculated in Example 5.5 and equals 1.1 V. The value of V_c needs to be calculated.

$$V_{Rc} = I_c \times R_c = 1.1\ mA \times 5\ k\Omega = 5.5\ V\ (I_E \approx I_c \text{ was calculated in Example 5.5.})$$

$$V_c = V_{cc} - V_{Rc} = 10\ V - 5.5\ V = 4.5\ V$$

$$V_{CE} = V_c - V_E = 4.5\ V - 1.1\ V = 3.4\ V$$

Step 3. Calculate the maximum output swing.

$$\text{maximum } V_{out\ p\text{-}p} = 2 \times V_{CE} = 2 \times 3.4\ V = 6.8\ V_{p\text{-}p}$$

Since the output signal (4.88 $V_{p\text{-}p}$) is less than the calculated maximum output swing (6.8 $V_{p\text{-}p}$), the output signal will not be clipped.

5.4 VARIATIONS OF VOLTAGE DIVIDER BIASED AMPLIFIERS

There are three variations of the voltage divider biased amplifier: the unbypassed, the fully bypassed, and the split emitter. The bias circuitry on all three variations functions the same. The difference is in the signal parameters. We will examine each variation and work an example of each.

UNBYPASSED VOLTAGE DIVIDER BIASED AMPLIFIER

The circuit in Figure 5–11 is the unbypassed voltage divider biased amplifier. This is the same circuit we have studied in the previous sections. Making two assumptions will simplify the circuit calculations. First, no value is given for the beta of the transistor in the circuit. Rather than wasting time looking it up, let us assume beta equals 100. One hundred is a reasonable guess of beta for low and medium power transistors. Second, the unbypassed resistor in the emitter (R_e) is large compared to r'_e, so r'_e will be negligible. These assumptions permit us to use a practical approach to calculate the bias and signal parameters of the voltage divider amplifier circuit using component values. The answers may not be precise because of the

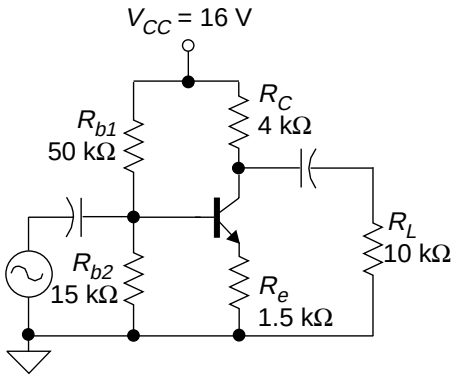

FIGURE 5–11 Unbypassed voltage divider biased amplifier

assumptions made, but they will be close enough to use in troubleshooting. Example 5.8 demonstrates this approach.

EXAMPLE 5.8

Analyze the circuit in Figure 5–11. Calculate (a) the DC bias voltages for V_B, V_E, V_c, and V_{CE}, and (b) the signal voltage gain (A_v), input impedance (z_{in}), output impedance (z_{out}), and the approximate maximum signal output voltage swing.

Step 1. Calculate the DC biased voltages and currents.

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2})$$

$$V_B = 16\text{ V} \times 15\text{ k}\Omega/(50\text{ k}\Omega + 15\text{ k}\Omega) = 3.7\text{ V}$$

$$V_E = V_B - V_{BE} = 3.7\text{ V} - 0.7\text{ V} = 3\text{ V}$$

$$I_E = V_E/R_{E(total)} = 3\text{ V}/1.5\text{ k}\Omega = 2\text{ mA} \quad (R_{E(total)} = R_e \text{ in this case.})$$

$$I_C \approx I_e = 2\text{ mA}$$

$$V_{RC} = I_C \times R_c = 2\text{ mA} \times 4\text{ k}\Omega = 8\text{ V}$$

$$V_c = V_{cc} - V_{RC} = 16\text{ V} - 8\text{ V} = 8\text{ V}$$

$$V_{CE} = V_c - V_E = 8\text{ V} - 3\text{ V} = 5\text{ V}$$

Step 2. Calculate the signal input impedance.

$$R_b = R_{b1} \parallel R_{b2} = 15\text{ k}\Omega \parallel 50\text{ k}\Omega = 11.5\text{ k}\Omega$$

$$r_e \approx R_e = 1.5\text{ k}\Omega \quad (R_e \text{ is large compared to } r'_e.)$$

$$z_{in} = r_b \parallel \beta r_e$$

$$z_{in} = 11.5\text{ k}\Omega \parallel 100 \times 1.5\text{ k}\Omega$$

$$z_{in} = 10.7\text{ k}\Omega$$

Step 3. Calculate the output impedance.

$$z_{out} = R_c = 4\text{ k}\Omega$$

Step 4. Calculate the voltage gain.

$$r_c = R_c \parallel R_L = 4\text{ k}\Omega \parallel 10\text{ k}\Omega = 2.86\text{ k}\Omega$$

$$A_v = r_c/r_e$$

$$A_v = 2.86\text{ k}\Omega/1.5\text{ k}\Omega = 1.9$$

Step 5. Calculate the maximum output signal swing. An approximation of the output peak-to-peak signal swing equals $2 \times V_{CE}$.

$$V_{CE} = 5\text{ V}$$

Therefore:

$$\text{Maximum output swing} = 2 \times 5\text{ V} = 10\text{ V}_{p\text{-}p}$$

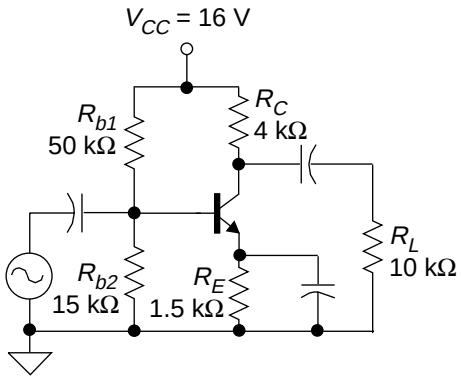

FIGURE 5–12 Bypassed voltage divider amplifier

THE FULLY BYPASSED AMPLIFIER

The voltage divider biased amplifier using an unbypassed emitter resistor (R_e) is stable and predictable but has a greatly reduced voltage gain when compared to the base biased amplifier. The voltage gain of the base biased amplifier is in the range of 50 to 500, but the voltage gain of the unbypassed voltage divider biased circuit is in the range of 2 to 10. In this section we will examine a circuit that retains the bias stability but has high voltage gain.

The circuit in Figure 5–12 is identical to the circuit in Figure 5–11, except that a capacitor has been added that bypasses the emitter resistor (R_E). The capacitor is an open for DC bias, hence, the biased currents and voltages are unchanged by the addition of the bypass capacitor. The circuit retains good Q-point stability, but the voltage gain is greatly increased.

Note the bypassed emitter resistor is called R_E with a capital "E" subscript. This denotes that the resistor will exist for the DC biased current but will appear as a short for the signal current. An unbypassed emitter resistor will be denoted as R_e and will exist for both biased currents (DC) and signal currents (AC).

The voltage gain is equal to the ratio of signal resistance in the collector leg to signal resistance in the emitter leg ($A_v = r_c/r_e$). In the unbypassed circuit, the signal resistance in the emitter leg is equal to r'_e plus the signal emitter resistor. The bypass capacitor shorts out the emitter resistor for the signal, leaving the signal resistance in the emitter leg equal to r'_e. With only the value of r'_e in the emitter leg, the voltage gain returns to the high voltage gain obtained with the base biased circuit.

The addition of the bypass capacitor will cause a decrease in input impedance. The output impedance will not be affected. Example 5.9 illustrates how signal values can be calculated for the fully bypassed amplifier.

EXAMPLE 5.9

Calculate the input impedance, output impedance, and the voltage gain for the circuit in Figure 5–12.

Step 1. Calculate r'_e.

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2})$$

$$V_B = 16\text{ V} \times 15\text{ k}\Omega/(50\text{ k}\Omega + 15\text{ k}\Omega) = 3.7\text{ V}$$

$$V_E = V_B - V_{BE} = 3.7\text{ V} - 0.7\text{ V} = 3\text{ V}$$

$$I_E = V_E/R_{E(\text{total})} = 3\text{ V}/1.5\text{ k}\Omega = 2\text{ mA} \quad (R_{E(\text{total})} = R_E \text{ in this case.})$$

$$I_C \approx I_e = 2\text{ mA}$$

$$r'_e = 25\text{ mV}/I_E = 25\text{ mV}/2\text{ mA} = 12.5\ \Omega$$

EXAMPLE 5.9 continued

Step 2. Calculate the input impedance.

$$r_b = R_{b1} \parallel R_{b2} = 50\ \text{k}\Omega \parallel 15\ \text{k}\Omega = 11.5\ \text{k}\Omega$$

$$r_e = r'_e = 12.5\ \Omega\ (R_E \text{ is bypassed.})$$

$$z_{in} = r_b \parallel \beta r_e = 11.5\ \text{k}\Omega \parallel (100 \times 12.5\ \Omega) = 1.13\ \text{k}\Omega$$

Step 3. Calculate the output impedance.

$$z_{out} = R_c = 4\ \text{k}\Omega$$

Step 4. Calculate the voltage gain.

$$r_c = R_c \parallel R_L = 4\ \text{k}\Omega \parallel 10\ \text{k}\Omega = 2.9\ \text{k}\Omega$$

$$A_v = r_c / r_e = 2.9\ \text{k}\Omega / 12.5\ \Omega = 232$$

The circuits in Examples 5.8 and 5.9 are identical except for the addition of the bypass capacitor. The addition of the bypass capacitor makes a dramatic change to the voltage gain and input impedance. The voltage gain goes up from 1.9 to 232, and the input impedance goes down from 10.7 kΩ to 1.13 kΩ. The increase in voltage gain is generally considered a plus that would probably outweigh the disadvantages of lowering the input impedance. However, the voltage gain is now dependent on r'_e, which makes it less predictable. The input impedance is not only lower but now is dependent on r'_e and β, which makes it less predictable than it was in the unbypassed circuit. Signal distortion is another disadvantage of the fully bypassed circuit. Figure 5–13 shows an example of signal distortion that is easily seen when the output signal has a large swing. The distortion is caused by fluctuations in r'_e and directly affects the voltage gain of the amplifier. The fluctuations in r'_e are caused by the wide variations in emitter current. On the positive swing of the input, the emitter current increases, causing r'_e to decrease and the voltage gain to increase. On the negative swing of the input, the emitter current decreases, causing r'_e to increase and the voltage gain to decrease.

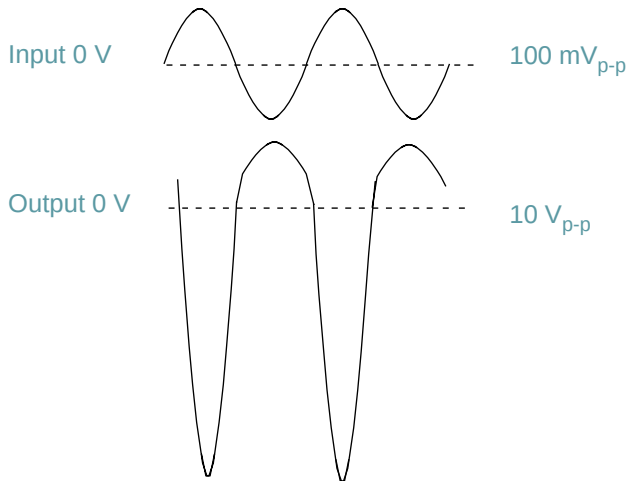

FIGURE 5–13 Signal distortion

The fully bypassed circuit is used in low cost circuitry where the high voltage gain reduces the number of stages needed, therefore, cutting cost. The price paid for this lower cost is distortion, unpredictable voltage gains, and input impedances that fluctuate with changes in environmental conditions and device parameters.

THE SPLIT-EMITTER AMPLIFIER

The split-emitter amplifier is a compromise between the fully bypassed and the unbypassed voltage divider amplifier. Figure 5–14 shows a split-emitter amplifier. The resistor in the emitter leg has been split into two parts: R_e and R_E. Resistor R_E is bypassed with a capacitor and is considered to be zero ohms when calculating signal parameters. Resistor R_e is unbypassed and must be considered when calculating signal parameters. The total value of the DC resistance ($R_e + R_E$) in the emitter leg is the same as it was in the circuits in Figures 5–11 and 5–12, and the DC currents and voltages are also the same. Example 5.10 will show the differences in signal parameters.

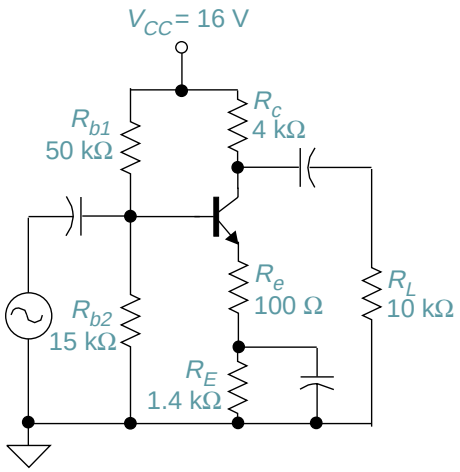

FIGURE 5–14 Split-emitter voltage divider amplifier

EXAMPLE 5.10

Calculate the input impedance, output impedance, and voltage gain for the circuit in Figure 5–14.

Step 1. Calculate r'_e.

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2})$$

$$V_B = 16\text{ V} \times 15\text{ k}\Omega/(50\text{ k}\Omega + 15\text{ k}\Omega) = 3.7\text{ V}$$

$$V_E = V_b - V_{be} = 3.7\text{ V} - 0.7\text{ V} = 3\text{ V}$$

$$I_E = V_E/R_{E(\text{total})} = 3\text{ V}/1.5\text{ k}\Omega = 2\text{ mA} \quad (R_{E(\text{total})} = R_e + R_E.)$$

$$I_C \approx I_e = 2\text{ mA}$$

$$r'_e = 25\text{ mV}/I_E = 25\text{ mV}/2\text{ mA} = 12.5\ \Omega$$

Step 2. Calculate the input impedance.

$$r_b = R_{b1} \parallel R_{b2} = 50\text{ k}\Omega \parallel 15\text{ k}\Omega = 11.5\text{ k}\Omega$$

$$r_e = r'_e + R_e = 12.5\ \Omega + 100 = 112.5\ \Omega$$

$$z_{\text{in}} = r_b \parallel \beta r_e = 11.5\text{ k}\Omega \parallel (100 \times 112.5\ \Omega) = 5.7\text{ k}\Omega$$

Step 3. Calculate the output impedance.

$$z_{\text{out}} = r_c = 4\text{ k}\Omega$$

Step 4. Calculate the voltage gain.

$$r_c = R_c \parallel R_L = 4\text{ k}\Omega \parallel 10\text{ k}\Omega = 2.9\text{ k}\Omega$$

$$A_v = r_c/r_e = 2.9\text{ k}\Omega/112.5\ \Omega = 26$$

The split-emitter amplifier has values of voltage gain and input impedance between those of the fully bypassed and the unbypassed circuits. The predictability of the signal parameters is also between the other two circuits. The amount of the emitter resistor left unbypassed determines the voltage gain and predictability of the circuit. Because the designer has the ability to control voltage gain and signal parameter predictability, the split-emitter voltage divider circuit has become a popular circuit in electronic systems.

SUMMARY OF VOLTAGE DIVIDER BIASING

In order for the transistor amplifier to be a practical circuit, it is necessary to use a biasing circuit that will stabilize the Q-point. In order to make the Q-point stable, the DC collector current must be independent of beta. This can be accomplished by using voltage divider biasing. There are three variations of voltage divider biasing circuits: the unbypassed circuit with voltage gains in the range of 2 to 10 but with excellent signal parameter predictability, the fully bypassed circuit with voltage gains in the range of 50 to 500 but with unpredictable signal parameters, and the split-emitter circuit with voltage gains in the range of 5 to 50 with good signal parameter predictability.

5.5 EMITTER BIASED AMPLIFIER

Figure 5–15 shows circuits using emitter bias for stabilization. The base is connected to ground through a relatively low resistance (R_b). The base/emitter is forward biased by a negative power supply (V_{EE}) connected to the emitter resistor (R_e). Since the base current is small, the voltage drop across the base resistor (R_b) is negligible, and the base is considered to be at zero volts. The forward-biased base/emitter junction drops to 0.7 V, so the emitter is at –0.7 V. This means the current through the emitter is determined by the value of the negative supply and the value of the emitter resistor. Since the emitter current is independent from changes in beta, the circuit obtains stability. One disadvantage of the emitter biased amplifier is the need for an emitter supply voltage (V_{EE}). Example 5.11 shows how the DC voltage of the emitter biased amplifier can be calculated.

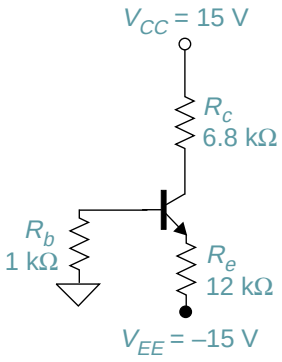

FIGURE 5–15 Emitter biased amplifier

EXAMPLE 5.11

Calculate the DC voltage V_B, V_E, and V_C of the circuit shown in Figure 5–15.

Step 1. Determine the base voltage. The base is at zero voltage because the current through R_b is considered negligible.

$$V_B = 0 \text{ V}$$

EXAMPLE 5.11 continued

Step 2. Determine the emitter voltage. The base/emitter of the NPN transistor is forward biased, so the emitter must be 0.7 V negative with respect to the base.

$$V_E = -0.7 \text{ V}$$

Step 3. Calculate the collector current.

$$I_E = (V_{EE} - V_{BE})/R_e = (-15 \text{ V} - (-0.7 \text{ V}))/12 \text{ k}\Omega = -1.2 \text{ mA}$$

(The negative sign can be dropped.)

$$I_C \approx I_E = 1.2 \text{ mA}$$

Step 4. Calculate the collector voltage.

$$V_{Rc} = I_C \times R_c = 1.2 \text{ mA} \times 6.8 \text{ k}\Omega = 8.2 \text{ V}$$

$$V_c = V_{cc} - V_{Rc} = 15 \text{ V} - 8.2 \text{ V} = 6.8 \text{ V}$$

Figure 5–16 shows the same emitter biased amplifier with an input signal and a load connected. The signal parameters are calculated using the same procedure as the voltage divider amplifier. The emitter can be fully bypassed for high voltage gain or partly bypassed, which reduces the gain but improves predictability and reduces distortion. Example 5.12 shows how the signal parameters can be calculated.

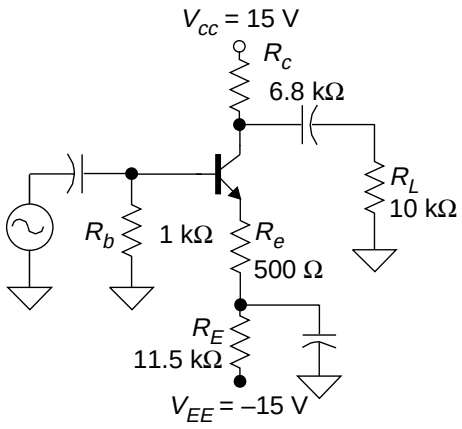

FIGURE 5–16 Emitter biased amplifier with split emitter

EXAMPLE 5.12

Calculate the input impedance, output impedance, and voltage gain for the circuit in Figure 5–16.

Step 1. Calculate r'_e.

$$I_E = 1.2 \text{ mA (Calculated in Example 5.11.)}$$

$$r'_e = 25 \text{ mV}/I_E = 25 \text{ mV}/1.2 \text{ mA} = 20.8 \ \Omega$$

Step 2. Calculate the input impedance.

$$r_b = R_b = 1 \text{ k}\Omega$$

$$r_e = r'_e + R_e = 20.8 \ \Omega + 500 = 520.8 \ \Omega \quad (r'_e \text{ is small and may be disregarded.})$$

$$z_{in} = r_b \parallel \beta r_e = 1 \text{ k}\Omega \parallel (100 \times 521 \ \Omega) = 981 \ \Omega$$

EXAMPLE 5.12 continued

Step 3. Calculate the output impedance.

$$z_{out} = R_c = 6.8\ \text{k}\Omega$$

Step 4. Calculate the voltage gain.

$$r_c = R_c \parallel R_L = 6.8\ \text{k}\Omega \parallel 10\ \text{k}\Omega = 4\ \text{k}\Omega$$

$$A_v = r_c / r_e = 4\ \text{k}\Omega / 521\ \Omega = 7.7$$

5.6 VOLTAGE-MODE FEEDBACK BIASED AMPLIFIER

Figure 5–17 shows circuits using voltage feedback for stabilization. Note that there is not a resistor in the emitter leg. Voltage divider biasing using current-mode feedback is normally preferred over voltage-mode feedback. However, for low voltage power supplies or when maximum output voltage swings are necessary, voltage-mode feedback may be preferred.

Figure 5–17(a) shows a circuit operating from a 4 V supply. A resistor (R_b) is connected between the collector and base. The base current is controlled by the voltage dropped across R_b, which is equal to the collector-to-base voltage. If the collector current increases, the voltage on the collector will decrease, reducing the voltage across R_b. A reduced voltage across R_b causes less base current, which then causes the collector current to decrease. The opposite is also true. A decrease in collector current causes the collector voltage to increase, which increases the base current and causes the collector current to rise. The voltage across the transistor (V_{CE}) stabilizes at approximately 2 V, and the remaining supply voltage is dropped across R_c. The voltage gain of the amplifier is the same as the fully bypassed voltage divider circuit and can be calculated using the formula $A_v = r_c / r_e$. Since there is no emitter resistor in the circuit, $r_e = r'_e$ causing the voltage gain to be high. The input impedance is equal to R_b divided by the voltage gain plus one in parallel with r'_e times beta [$z_{in} = (R_b / A_v + 1) \parallel (r'_e \beta)$] . The reason R_b appears to be much smaller than its actual size is because as the voltage goes up on the base end of R_b, the voltage is forced down on the collector end of R_b. Miller's theorem states that the effective impedance of a component in the negative feedback loop of an amplifier is equal to the actual impedance of the component divided by the voltage gain plus one. The main advantage of the circuit in Figure 5–17(a) is its ability to operate with a low supply voltage.

The circuit in Figure 5–17(b) uses voltage-mode feedback. The second resistor in the base circuit (R_{b2}) permits a portion of the current flowing through R_{b1} to bypass the base. This permits the circuit

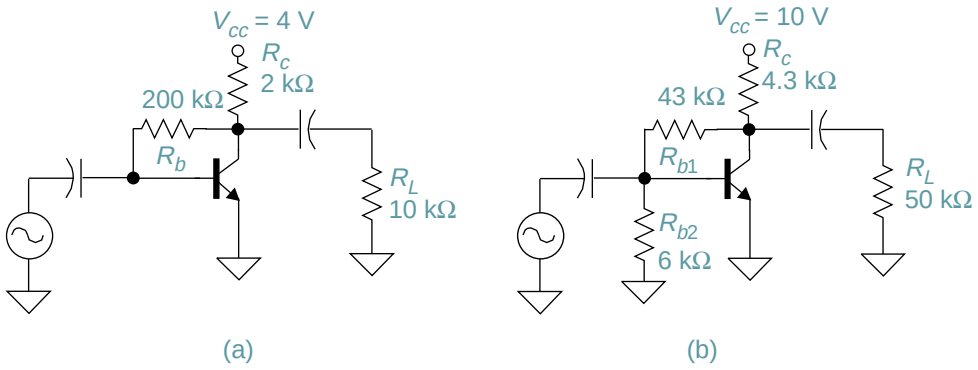

FIGURE 5–17 Voltage-mode feedback amplifiers

to operate with a higher value of collector-to-emitter voltage (V_{CE}). The circuit can be designed for ideal midpoint biasing, permitting maximum output signal swings. This type of voltage-mode feedback is often used to drive power amplifier stages when maximum swing is of utmost importance.

5.7 MULTISTAGE RC COUPLED AMPLIFIERS

In order to obtain the gain an electronic system needs, it is often necessary to connect amplifiers in series. When amplifiers are connected in series, they are said to be cascaded. Figure 5–18 shows a two-stage cascaded amplifier circuit. The two stages are both voltage divider biased amplifiers.

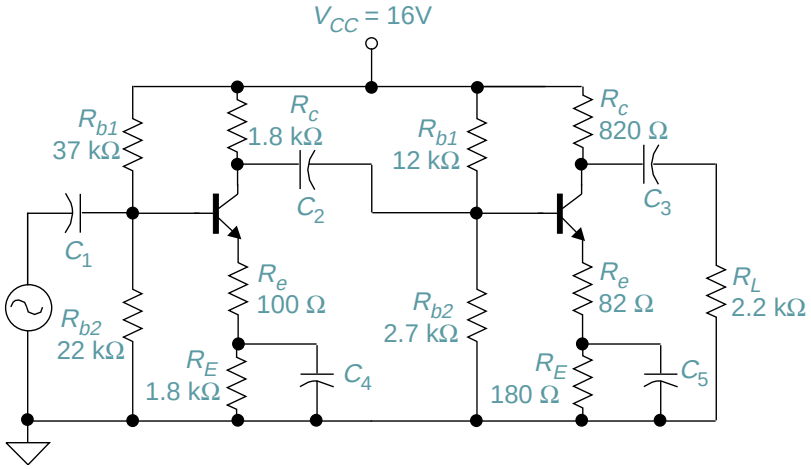

FIGURE 5–18 RC coupled amplifier

One method for coupling transistor stages together is by using coupling capacitors between stages. This method of coupling is called RC, or resistance-capacitor, coupling. Coupling capacitors act like an open for biased currents but are a short for signal currents. Because of this, the biased circuitry in each stage is independent. The biased currents and voltages can be calculated in the same manner used for a single-stage amplifier. You simply consider each stage individually.

The signal parameters of a multistage amplifier are easy to calculate if you remember the following facts. The input impedance of the total circuit is equal to the input impedance of the first stage. The output impedance of the total circuit is equal to the output impedance of the final stage of the system. The voltage gain of the total circuit is equal to the product of the individual stages. The output signal from the first stage will see the input impedance of the second stage as its load resistance.

EXAMPLE 5.13

Analyze the circuit in Figure 5–18.

Step 1. Analyze each stage independently for the biased voltages.

First stage:

$$V_B = V_{cc} \times R_{b2}/(R_{b1}+R_{b2}) = 16\text{ V} \times 22\text{ k}\Omega/(37\text{ k}\Omega + 22\text{ k}\Omega) = 6\text{ V}$$

$$V_E = V_B - V_{BE} = 6\text{ V} - 0.7\text{ V} = 5.3\text{ V}$$

$$I_E = V_E/R_{E(\text{total})} = 5.3\text{ V}/1.9\text{ k}\Omega = 2.8\text{ mA}$$

EXAMPLE 5.13 continued

$$V_{RC} = I_C \times R_c = 1.8\ \text{k}\Omega \times 2.8\ \text{mA} = 5\ \text{V}$$
$$V_C = V_{CC} - V_{RC} = 16\ \text{V} - 5\ \text{V} = 11\ \text{V}$$
$$V_{CE} = V_C - V_E = 11\ \text{V} - 5.3\ \text{V} = 5.7\ \text{V}$$

Second stage:

$$V_B = V_{cc} \times R_{b2}/(R_{b1} + R_{b2}) = 16\ \text{V} \times 2.7\ \text{k}\Omega/(12\ \text{k}\Omega + 2.7\ \text{k}\Omega) = 2.9\ \text{V}$$
$$V_E = V_B - V_{BE} = 2.9\ \text{V} - 0.7\ \text{V} = 2.2\ \text{V}$$
$$I_E = V_E/R_{E(\text{total})} = 2.2\ \text{V}/262\ \Omega = 8.4\ \text{mA}$$
$$V_{RC} = I_C \times R_c = 820\ \Omega \times 8.4\ \text{mA} = 6.9\ \text{V}$$
$$V_C = V_{CC} - V_{RC} = 16\ \text{V} - 6.9\ \text{V} = 9.1\ \text{V}$$
$$V_{CE} = V_C - V_E = 9.1\ \text{V} - 2.2\ \text{V} = 6.9\ \text{V}$$

Step 2. Calculate the input impedance and output impedance of each stage. Assume beta to equal 100 for both transistors.

First stage:

$$r_b = R_{b1} \parallel R_{b2} = 37\ \text{k}\Omega \parallel 22\ \text{k}\Omega = 13.8\ \text{k}\Omega$$
$$r'_e = 25\ \text{mV}/I_E = 25\ \text{mV}/2.8\ \text{mA} = 9\ \Omega$$
$$r_e = r'_e + R_e = 9\ \Omega + 100\ \Omega = 109\ \Omega$$
$$z_{\text{in}} = r_b \parallel \beta r_e = 13.8\ \text{k}\Omega \parallel (100 \times 109\ \Omega) = 6\ \text{k}\Omega$$
$$z_{\text{out}} = R_c = 1.8\ \text{k}\Omega$$

Second stage:

$$r_b = R_{b1} \parallel R_{b2} = 12\ \text{k}\Omega \parallel 2.7\ \text{k}\Omega = 2.2\ \text{k}\Omega$$
$$r'_e = 25\ \text{mV}/I_E = 25\ \text{mV}/8.4\ \text{mA} = 3\ \Omega$$
$$r_e = r'_e + R_e = 3\ \Omega + 82\ \Omega = 85\ \Omega$$
$$z_{\text{in}} = r_b \parallel \beta r_e = 2.2\ \text{k}\Omega \parallel (100 \times 85\ \Omega) = 1.7\ \text{k}\Omega$$
$$z_{\text{out}} = R_c = 820\ \Omega$$

Step 3. Calculate the voltage gain of each stage.

First stage:

$$r_c = R_c \parallel R_L = 1.8\ \text{k}\Omega \parallel 1.7\ \text{k}\Omega = 874\ \Omega\ (R_L = z_{\text{in}}\ \text{of next stage.})$$
$$A_v = r_c/r_e = 874\ \Omega/109\ \Omega = 8$$

Second stage:

$$r_c = R_c \parallel R_L = 820\ \Omega \parallel 2.2\ \text{k}\Omega = 597\ \Omega$$
$$A_v = r_c/r_e = 597\ \Omega/85\ \Omega = 7$$

Step 4. Calculate the input impedance, output impedance, and voltage gain of the total amplifier circuit.

$$z_{\text{in}} = z_{\text{in}}\ \text{of first stage} = 6\ \text{k}\Omega$$
$$z_{\text{out}} = z_{\text{out}}\ \text{of last stage} = 820\ \Omega$$
$$A_{v(\text{total})} = A_{V1} \times A_{V2} = 8 \times 7 = 56$$

5.8 COUPLING AND BYPASS CAPACITORS

Up to this point we have assumed the capacitors in the circuits to have zero impedance (X_c) for signal currents and infinite impedance for biased currents. The impedance of a capacitor is

dependent on its capacitance and the frequency of the signal and is expressed as $X_c = 1/(2\pi F_c)$. Any size capacitor will exhibit some ohms of impedance at any frequency. Engineers design circuits so X_c is relatively small at the lowest operating frequency. Normally, technicians will not have to calculate the size of the capacitors, but it is helpful to have a rule of thumb to determine the approximate size. As a rule, X_c, at the lowest frequency, should be equal to one-tenth or less of the series impedance being driven by the signal passing through the capacitor.

The signal passing through the input coupling capacitor is driving z_{in} of the first stage of the circuit, and the impedance of the coupling capacitor should be one-tenth of z_{in}. The coupling capacitor between stages should have an impedance of one-tenth of z_{in} of the stage being driven. The output coupling capacitor should have an impedance of one-tenth of R_L.

The purpose of the emitter capacitor is to bypass signal currents to ground. The parallel combination of R_E and the bypass capacitor should be one-tenth of r'_e for the fully bypassed circuit or one-tenth of r_e ($r'_e + R_e$) for the split-emitter circuit. Example 5.14 will demonstrate how this rule of thumb can be used to calculate the size of coupling and bypass capacitors. It should be emphasized that the procedure to be used in Example 5.14 will result in estimated values that permit the technician to select capacitors for experimental circuits. Engineers use other calculation methods that result in smaller capacitor values that save money on commercially produced circuits.

EXAMPLE 5.14

Calculate the size of the coupling and bypass capacitors needed in the circuit in Figure 5–18 if the lowest signal frequency to be amplified is 300 Hz.

Step 1. Determine the series resistance being driven by each capacitor. In Example 5.13, the input impedance and the value of signal resistance in the emitter leg (r_e) was calculated for each stage. These values are listed as the driven resistance in Table 5–1.

TABLE 5–1

Capacitor	Driven resistance	$X_{C(max)}$	Capacitor value
C_1	6 kΩ (z_{in} Q_1)	600 Ω	0.9 µF
C_2	1.7 kΩ (z_{in} Q_2)	170 Ω	3.1 µF
C_3	2.2 kΩ (R_L)	220 Ω	2.4 µF
C_4	109 Ω (r_e Q_1)	10.9 Ω	49 µF
C_5	85 Ω (r_e Q_2)	8.5 Ω	63 µF

Step 2. Calculate the maximum impedance of the capacitor by assuming the capacitive reactance (X_c) to equal one-tenth of the driven resistance value shown in Table 5–1.

Step 3. Using 300 Hz, calculate the value of each capacitor using the following formula. The calculation for the first capacitor is shown. Table 5–1 shows the calculated values for all capacitors for the circuit shown in Figure 5–18.

$$C_1 = 1/(2\pi\ X_c\ F) = 1/(2\pi \times 600\ \Omega \times 300\ \text{Hz}) = 0.9\ \mu\text{F}$$

The results in Table 5–1 show the minimum size capacitor using our rule of thumb for calculation. The next larger standard size capacitor can be used to construct the circuit. Since

coupling and bypass capacitors with larger capacitance values will function fine, often circuits will use the same value for all coupling capacitors.

5.9 DIRECT COUPLED AMPLIFIERS

Capacitor coupled (RC coupled) amplifiers are popular because each stage has its own independently biased circuit. Fluctuations in the DC operating point in one stage is not amplified by the next stage. Occasionally, however, it is necessary to have an amplifier that is capable of amplifying DC currents and voltages. In order to couple a DC signal from one stage to the next, it is necessary to remove the coupling capacitor and connect the output of one stage directly to the input of the next. Emitter-bypass capacitors are removed; thus, the DC signal gain will be the same as the dynamic signal gain.

Figure 5–19 shows a two-stage direct coupled amplifier. The first stage uses emitter biasing. With no input signal, the 4.3 kΩ emitter resistor connected to the negative 5 V supply sets the emitter and collector current of Q_1 to 1 mA. The 1 mA of collector current flowing through Q_1 causes a 15 V drop across the 15 kΩ collector resistor setting the collector voltage at 5 V. The second stage uses a PNP transistor, and the bias voltage on the base is held constant at 5 V by the output of the first stage. The emitter of Q_2 is connected to a 10 V supply through a 4.3 kΩ emitter resistor. Since 4.3 V will be dropped across the emitter, the emitter current and collector current of Q_2 will equal 1 mA. The 1 mA of collector current flows through the 20 kΩ collector resistor of Q_2, dropping 20 V. This causes the output to be zero volts at quiescence.

One advantage of DC coupling is the high input impedance of the second stage. The high input impedance is a result of the absence of base resistors at the input of the second stage. This reduces loading on the first stage and permits a higher voltage gain. Example 5.15 shows how the direct coupled amplifier can be analyzed.

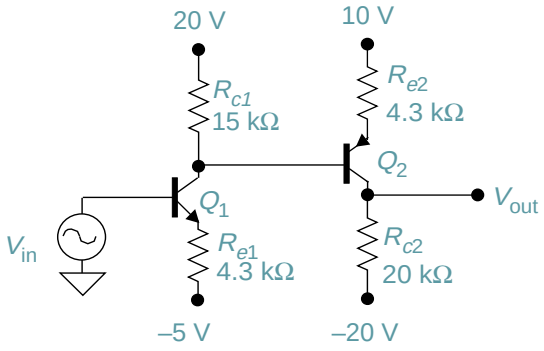

FIGURE 5–19 Direct coupled amplifier

EXAMPLE 5.15

For the circuit in Figure 5–19, calculate V_B, V_E, V_C, V_{CE}, z_{in}, z_{out}, and A_v for each transistor. Then calculate z_{in}, z_{out}, and A_v for the total circuit.

Step 1. Calculate the DC voltage for the first stage.

$$V_B = 0 \text{ V (Assume the input signal has zero DC offset.)}$$

$$V_E = V_B - V_{BE} = 0 \text{ V} - 0.7 \text{ V} = -0.7 \text{ V}$$

EXAMPLE 5.15 continued

$$I_E = (-5\text{ V} - (-0.7\text{ V}))/4.3\text{ k}\Omega = -1\text{ mA}$$
$$I_E \approx I_C$$
$$V_{Rc} = I_c \times R_{c1} = 1\text{ mA} \times 15\text{ k}\Omega = 15\text{ V}$$
$$V_C = V_{CC} - V_{Rc} = 20\text{ V} - 15\text{ V} = 5\text{ V}$$
$$V_{CE} = V_C - V_E = 5\text{ V} - (-0.7)\text{ V} = 5.7\text{ V}$$

Step 2. Calculate the DC voltage for the second stage.

$$V_B = V_C \text{ of first stage} = 5\text{ V}$$
$$V_E = V_B + V_{BE} = 5\text{ V} + 0.7\text{ V} = 5.7\text{ V} \quad \text{(PNP transistor } V_{BE} \text{ is added.)}$$
$$I_E = (10\text{ V} - 5.7\text{ V})/4.3\text{ k}\Omega = 1\text{ mA}$$
$$I_E \approx I_C$$
$$V_{Rc} = I_c \times R_c = 1\text{ mA} \times 20\text{ k}\Omega = 20\text{ V}$$
$$V_C = V_{CC} - V_{Rc} = -20\text{ V} - (-20\text{ V}) = 0\text{ V}$$
$$V_{CE} = V_C - V_E = 0\text{ V} - 5.7\text{ V} = -5.7\text{ V}$$

Step 3. Calculate the input impedance and output impedance for each stage. Assume beta to equal 100 for both transistors.

First stage:

$$r'_e = 25\text{ mV}/I_E = 25\text{ mV}/1\text{ mA} = 25\ \Omega$$
$$r_e = r'_e + R_e = 25\ \Omega + 4.3\text{ k}\Omega = 4.3\text{ k}\Omega \ (r'_e \text{ is too small to consider.})$$
$$z_{in} = \beta \times r_e = 100 \times 4.3\text{ k}\Omega = 430\text{ k}\Omega$$
$$z_{out} = R_c = 15\text{ k}\Omega$$

Second stage:

$$r'_e = 25\text{ mV}/I_E = 25\text{ mV}/1\text{ mA} = 25\ \Omega$$
$$r_e = r'_e + R_e = 25\ \Omega + 4.3\text{ k}\Omega \approx 4.3\text{ k}\Omega \ (r'_e \text{ is too small to consider.})$$
$$z_{in} = \beta \times r_e = 100 \times 4.3\text{ k}\Omega = 430\text{ k}\Omega$$
$$z_{out} = R_c = 20\text{ k}\Omega$$

Step 4. Calculate the voltage gain of each stage.

First stage:

$$r_c = R_c \parallel R_L = 15\text{ k}\Omega \parallel 430\text{ k}\Omega = 14.5\text{ k}\Omega \ (R_L = z_{in} \text{ of second stage (430 k}\Omega\text{).})$$
$$A_v = r_c/r_e = 14.5\text{ k}\Omega/4.3\text{ k}\Omega = 3.37$$

Second stage:

$$r_c = R_c = 20\text{ k}\Omega \ \text{(No load resistance connected.)}$$
$$A_v = r_c/r_e = 20\text{ k}\Omega/4.3\text{ k}\Omega = 4.65$$

Step 5. Calculate z_{in}, z_{out}, and $A_{V(total)}$ for the total amplifier circuit.

$$z_{in} = z_{in} \text{ first stage} = 430\text{ k}\Omega$$
$$z_{out} = z_{out} \text{ last stage} = 20\text{ k}\Omega$$
$$A_{V(total)} = A_{V1} \times A_{V2} = 3.37 \times 4.65 = 15.7$$

Direct coupled amplifiers have the advantage of being able to amplify DC voltages. However, in order to amplify DC, coupling capacitors and bypass capacitors must be removed. The removal of coupling capacitors means that stages cannot be individually biased, and any Q-point drift in one stage will be amplified by the next stage. The removal of the bypass capacitor causes the gain of each stage to be low. The system will require more stages to obtain the needed gain. Even

though direct coupled amplifiers have these disadvantages, they still are used in high quality circuits where low frequency and DC amplification are required.

Another way to obtain DC and low frequency amplification is to use a capacitor coupled amplifier and chop (turning the signal off and on at a high frequency) the DC and low frequency signals so that they can be passed by the coupling capacitors. Chopper circuits will be discussed in a future chapter.

5.10 TROUBLESHOOTING TRANSISTOR CIRCUITS

Troubleshooting transistor circuits can be divided into two areas: troubleshooting the circuit for correct bias voltages, and troubleshooting the circuit for correct signal responses.

BIAS TROUBLESHOOTING

If the stages are capacitor coupled, the procedure used in troubleshooting single-stage circuits can be applied. Each stage in a capacitor coupled amplifier is biased independently, and therefore, troubleshooting the biased circuitry is done one stage at a time. In direct coupled amplifiers, the biased voltage on the base is the collector voltage of the previous stage. Troubleshooting the biased circuit becomes a multistage problem.

SIGNAL TROUBLESHOOTING

Signal troubleshooting is performed by inserting a signal from a signal generator through a capacitor into the circuit, and then tracing the signal through the system. In multistage amplifiers, remember, the load on one stage is the input impedance of the next. So when the gain of a stage is not as estimated, it may be because the next stage is loading it down. This can be checked by disconnecting the next stage and replacing it with a resistor equal to its input impedance. Open capacitors can cause signal problems while not affecting the biased voltages. The bypass capacitor in the emitter leg, if it is open, will cause the voltage gain of the stage to go down. Open coupling capacitors can be detected by noting that the signal is not being coupled from one stage to the next. One of the best ways to check for open capacitors is to bypass these capacitors with a known good capacitor. If the circuit returns to proper working order, the capacitor needs replacing.

PRE-LAB 5.1

Voltage Divider Biased Amplifiers

1. Calculate and record V_B, V_E, V_C, z_{in}, z_{out}, A_v, and maximum output voltage swings without distortion for each circuit in Figure 5–20.

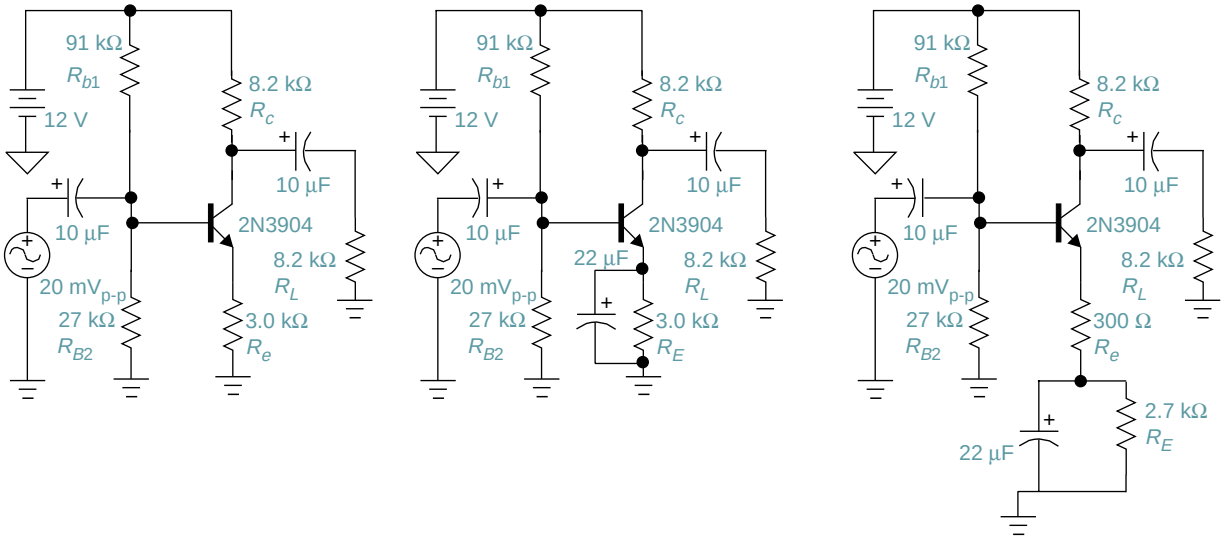

FIGURE 5–20

Circuit a:

V_B = _____ V_E = _____ V_C = _____

z_{in} = _____ z_{out} = _____ A_v = _____

Maximum output voltage swing = _____

Circuit b:

V_B = _____ V_E = _____ V_C = _____

z_{in} = _____ z_{out} = _____ A_v = _____

Maximum output voltage swing = _____

Circuit c:

V_B = _____ V_E = _____ V_C = _____

z_{in} = _____ z_{out} = _____ A_v = _____

Maximum output voltage swing = _____

2. For a minimum frequency of 1 kHz, calculate the minimum capacitor size for each capacitor in the circuit in Figure 5–20.

C_1 = _____ C_2 = _____ C_3 = _____ C_4 = _____

C_5 = _____ C_6 = _____ C_7 = _____ C_8 = _____

3. Simulate and record V_B, V_E, V_C, z_{in}, z_{out}, A_v, and maximum output voltage swings without distortion for each circuit in Figure 5–20.

Circuit a:

V_B = _____ V_E = _____ V_C = _____

z_{in} = _____ z_{out} = _____ A_v = _____

Maximum output voltage swing = _____

Circuit b:

V_B = _____ V_E = _____ V_C = _____

z_{in} = _____ z_{out} = _____ A_v = _____

Maximum output voltage swing = _____

Circuit c:

V_B = _____ V_E = _____ V_C = _____

z_{in} = _____ z_{out} = _____ A_v = _____

Maximum output voltage swing = _____

LAB 5.1

Voltage Divider Biased Amplifiers

I. Objective

To analyze and construct three variations of voltage divider biased amplifiers.

II. Test Equipment

(1) sine wave generator
(1) dual trace oscilloscope
(1) 12 V power supply

III. Components

Resistors: (1) 200 Ω, (1) 620 Ω, (1) 820 Ω, (1) 3.9 kΩ, (1) 5.6 kΩ, (1) 8.2 kΩ, (1) 39 kΩ
Capacitors: (2) 10 µF and (1) 22 µF
Transistors: (1) 2N3904

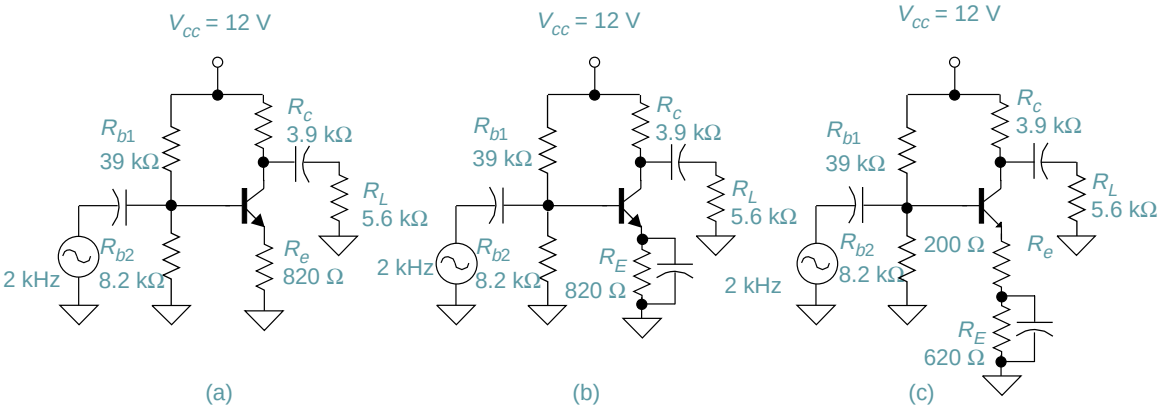

FIGURE 5–21

IV. Procedure

1. Calculate and record V_B, V_E, V_C, z_{in}, z_{out}, A_v, and maximum output voltage swing without distortion for each circuit in Figure 5–21.

Circuit a:

V_B = _____ V_E = _____ V_C = _____
z_{in} = _____ z_{out} = _____ A_v = _____
Maximum output voltage swing = _____

Circuit b:

V_B = _____ V_E = _____ V_C = _____
z_{in} = _____ z_{out} = _____ A_v = _____
Maximum output voltage swing = _____

Circuit c:

V_B = _____ V_E = _____ V_C = _____
z_{in} = _____ z_{out} = _____ A_v = _____
Maximum output voltage swing = _____

2. Construct each circuit in Figure 5–21 and measure the values of V_B, V_E, V_C, z_{in}, z_{out}, A_v, and maximum output voltage swing without distortion. Set the input signal frequency to 2 kHz and the signal magnitude as needed.

   Circuit a:

   V_B = _____ V_E = _____ V_C = _____

   z_{in} = _____ z_{out} = _____ A_v = _____

   Maximum output voltage swing = _____

   Circuit b:

   V_B = _____ V_E = _____ V_C = _____

   z_{in} = _____ z_{out} = _____ A_v = _____

   Maximum output voltage swing = _____

   Circuit c:

   V_B = _____ V_E = _____ V_C = _____

   z_{in} = _____ z_{out} = _____ A_v = _____

   Maximum output voltage swing = _____

V. Points to Discuss

1. Analyze and discuss the percent of difference in calculated and measured values.

2. Explain the difference in voltage gain (A_v) among the three circuits.

3. Explain the difference in input impedance (z_{in}) among the three circuits.

4. Why were z_{out} and the DC voltage readings approximately the same for all three circuits?

PRE-LAB 5.2

Multistage Amplifier

1. Calculate and record all values listed below for the amplifier circuit in Figure 5–22.

Stage 1:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Stage 2:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Total Circuit:

A_v = _____ z_{in} = _____ z_{out} = _____

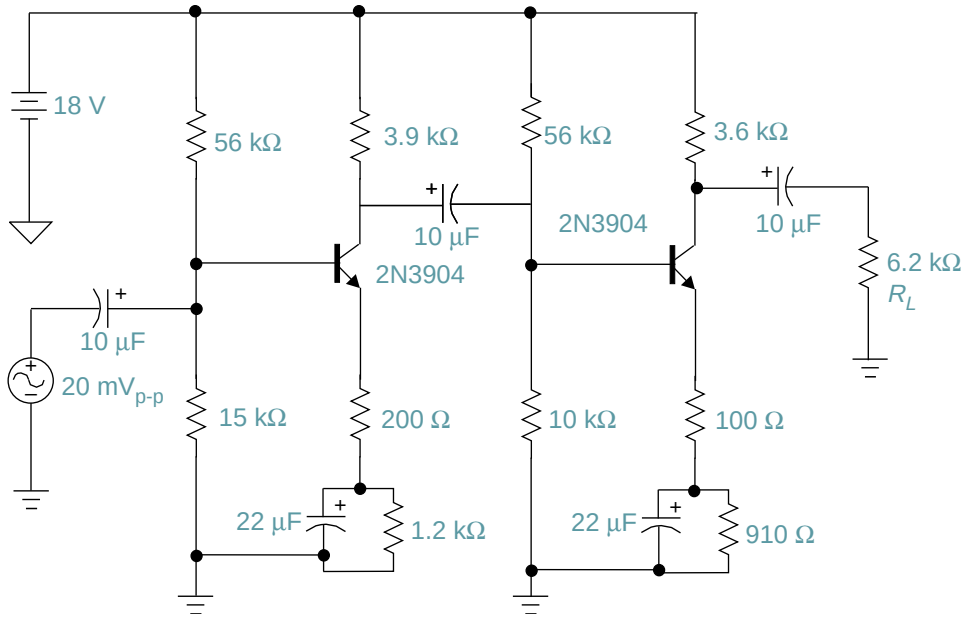

FIGURE 5–22

2. For a minimum frequency of 1 kHz, calculate the minimum capacitor size for each capacitor in the circuit in Figure 5–22.

C_1 = _____ C_2 = _____ C_3 = _____ C_4 = _____

C_5 = _____

3. Simulate and record V_B, V_E, V_C, A_v, z_{in}, and z_{out}, for the amplifier circuit in Figure 5–22.

Stage 1:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Stage 2:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Total Circuit:

A_v = _____ z_{in} = _____ z_{out} = _____

LAB 5.2

Multistage Amplifier

I. Objective

To analyze a multistage amplifier to determine the bias and signal values at test points.

II. Test Equipment

(1) sine wave generator
(1) dual-trace oscilloscope
(1) 12 V power supply

III. Components

Resistors: (1) 100 Ω, (1) 180 Ω, (1) 680 Ω, (1) 820 Ω, (2) 3.9 kΩ, (3) 8.2 kΩ, (2) 39 kΩ
Capacitors: (3) 2.2 µF and (2) 10 µF
Transistors: (2) 2N3904

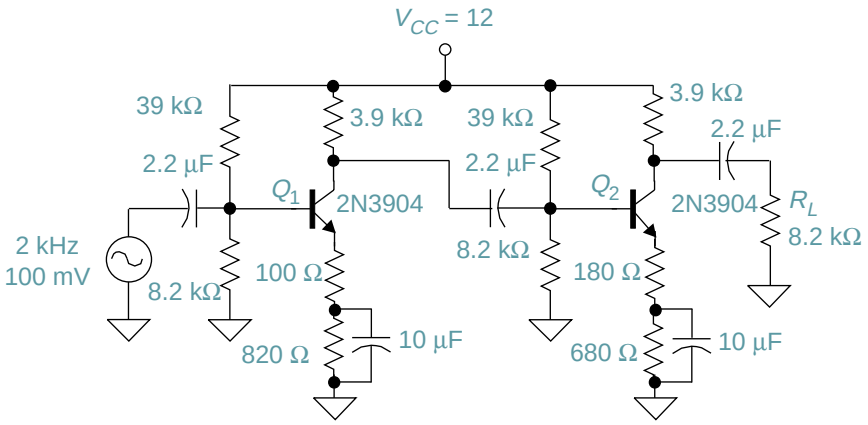

FIGURE 5–23

IV. Procedure

1. Calculate and record all values listed below for the amplifier circuit in Figure 5–23.

Stage 1:

V_B = _____ V_E = _____ V_C = _____
A_v = _____ z_{in} = _____ z_{out} = _____

Stage 2:

V_B = _____ V_E = _____ V_C = _____
A_v = _____ z_{in} = _____ z_{out} = _____

Total Circuit:

A_v = _____ z_{in} = _____ z_{out} = _____

2. Construct the circuit in Figure 5–23 and measure the values listed below for the amplifier circuit.

Stage 1:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Stage 2:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Total Circuit:

A_v = _____ z_{in} = _____ z_{out} = _____

V. Points to Discuss

1. Explain any differences between calculated and measured values.

2. Explain why z_{in} of the first stage equals z_{in} of the total circuit.

3. Explain why z_{out} of the last stage equals z_{out} of the total circuit.

4. Explain why input impedance of the second stage affected the voltage gain of the first stage.

5. The total voltage gain of this circuit could be obtained by using a single-stage amplifier. Explain the advantages of using two stages.

QUESTIONS

5.1 Introduction

____ 1. Why is it necessary to stabilize the bipolar transistor amplifier against changes in beta?
   a. Beta changes with temperature.
   b. Beta changes with changes in coupling capacitors.
   c. Beta is different among transistors of the same type.
   d. Both a and c.

____ 2. The typical beta of a transistor should be considered to be _____.
   a. +50% and –50%
   b. +50% and –100%
   c. +100% and –50%
   d. +100% and –100%

____ 3. If beta changes, how will the lack of bias stability show up in an amplifier circuit?
   a. The collector voltage will change.
   b. The collector current will change.
   c. The emitter current will change.
   d. All of the above.

5.2 Voltage Divider Biasing

____ 4. In voltage divider biasing, why is the voltage at the junction of R_{b1} and R_{b2} considered to be independent of the transistor base current?
   a. The base current does not flow through R_{b1} or R_{b2}.
   b. The base current is small in comparison to the bleeder current through R_{b1} and R_{b2}.
   c. Only the emitter current has an effect on the current flow through R_{b1} and R_{b2}.
   d. The coupling capacitor blocks base current through the voltage divider.

____ 5. In voltage divider biased amplifiers, the difference in voltage between the emitter and base is always _____.
   a. 0 V
   b. 0.2 V
   c. 0.7 V
   d. 2 V

____ 6. In voltage divider biased amplifiers, once the DC emitter voltage is calculated, the quiescence collector current can be approximated by dividing the emitter voltage by _____ .
   a. the resistance in the base leg
   b. the resistance in the emitter leg
   c. the resistance in the collector leg
   d. the resistance of the load

____ 7. In voltage divider biased amplifiers, the collector voltage is calculated by _____.
   a. multiplying the collector current times the collector resistor
   b. multiplying the collector current times the load resistor
   c. adding the base voltage and the emitter voltage
   d. subtracting the voltage dropped across the collector resistor from the supply voltage

5.3 Signal Parameters in Voltage Divider Circuits

____ 8. Voltage divider biased amplifiers are beta independent, but what is the price paid for this independence?
   a. loss of stability
   b. low output impedance
   c. loss of voltage gain
   d. both a and c

____ 9. When calculating input impedance, the two base resistors (R_{b1} and R_{b2}) appear in _____ with each other.
   a. series
   b. series/parallel
   c. parallel
   d. opposing series

____ 10. The dynamic resistance of the base/emitter junction is in _____.
   a. series with the signal resistance in the base leg
   b. parallel with the signal resistance in the base leg
   c. parallel with the signal resistance in the emitter leg
   d. series with the signal resistance in the emitter leg

____ 11. The output impedance of the common emitter amplifier is equal to _____.
   a. the collector resistor
   b. the load resistance
   c. the collector resistor in parallel with the load resistance
   d. the collector resistor times beta

5.4 Variations of Voltage Divider Biased Amplifiers

____ 12. Which type of voltage divider biased amplifier has the highest input impedance?
   a. fully bypassed
   b. split-emitter
   c. unbypassed
   d. all the same

____ 13. Which type of voltage divider biased amplifier has the highest output impedance?
   a. fully bypassed
   b. split-emitter
   c. unbypassed
   d. all the same

____ 14. Which type of voltage divider biased amplifier has the highest voltage gain?
a. fully bypassed
b. split-emitter
c. unbypassed
d. all the same

____ 15. Which type of voltage divider biased amplifier has the least distortion?
a. fully bypassed
b. split-emitter
c. unbypassed
d. all the same

5.5 Emitter Biased Amplifier

____ 16. The quiescent base voltage of the emitter biased amplifier is normally _____.
a. 0 V
b. 0.7 V
c. 2 V
d. V_{cc}

____ 17. A disadvantage of the emitter biased amplifier when compared to the voltage divider biased amplifier is the emitter biased amplifier requires _____.
a. transistors with higher beta
b. two power supply voltages
c. higher value of V_{cc}
d. none of the above

____ 18. The voltage gain of the emitter biased amplifier is _____.
a. dependent on beta
b. calculated using the same general formula as that used for the voltage divider biased amplifier
c. equal to $\beta \times r_c$
d. always higher than that of the voltage divider biased amplifier

5.6 Voltage-Mode Feedback Biased Amplifier

____ 19. Voltage-mode feedback biased amplifiers are particularly suitable for operations with _____.
a. high frequency signals
b. low voltage power supplies
c. circuits requiring an exceedingly high input impedance
d. circuits requiring an exceedingly low output impedance

____ 20. The input impedance of a voltage-mode feedback biased amplifier is affected by the _____.
a. wattage value of the collector resistor
b. amplifier voltage gain
c. resistance of the feedback resistor
d. both b and c

5.7 Multistage RC Coupled Amplifiers

____ 21. Why is it important to know the input impedances of each stage in a multistage amplifier?
a. The total input impedance is the product of each stage's input impedance.
b. The voltage gain of a stage is affected by the input impedance of the next stage.
c. The input impedance of a stage is the load resistance on the previous stage.
d. Both b and c.

____ 22. What is one of the main advantages of using coupling capacitors between stages?
a. They permit the multistage amplifier to pass DC signals.
b. They permit the bias circuitry in each stage to be independent.
c. They bypass the emitter resistor and increase the gain.
d. Both b and c.

____ 23. The total voltage gain of a multistage amplifier is equal to the _____.
a. sum of each stage's voltage gain
b. product of each stage's voltage gain
c. first stage voltage gain
d. last stage voltage gain

____ 24. The input impedance of the total multistage amplifier is equal to the _____.
a. sum of each stage's input impedance
b. product of each stage's input impedance
c. first stage input impedance
d. last stage input impedance

____ 25. The output impedance of the total multistage amplifier is equal to the _____.
a. sum of each stage's output impedance
b. product of each stage's output impedance
c. first stage output impedance
d. last stage output impedance

5.8 Coupling and Bypass Capacitors

____ 26. The size of coupling and bypass capacitors is one of the main factors determining _____.
a. low frequency cutoff
b. voltage gain
c. current gain
d. high frequency cutoff

____ 27. If the input impedance of the second stage is 1 kΩ, the coupling capacitor connecting the first stage to the second stage should have an X_C of approximately _____ for the lowest frequency to be amplified.
a. 1 Ω
b. 10 Ω
c. 100 Ω
d. 1 kΩ
e. 10 kΩ

5.9 Direct Coupled Amplifiers

____ 28. Direct coupled amplifiers have an advantage over RC coupled amplifiers in that they can amplify _____.

a. larger signals
b. high frequency signals
c. smaller signals
d. low frequency signals

____ 29. Direct coupled amplifiers are particularly susceptible to _____ problems.

a. gain
b. saturation
c. DC drift
d. impedance

5.10 Troubleshooting Transistor Circuits

____ 30. The collector of Q_1 in Figure 5–24 measures approximately 20 V DC.

a. The circuit is functioning correctly.
b. Capacitor C_2 is shorted.
c. Capacitor C_2 is open.
d. Resistor R_1 is open.

____ 31. The collector of Q_2 in Figure 5–24 measures 13.8 V DC.

a. The circuit is functioning correctly.
b. Transistor Q_2 is open between the collector and the emitter.
c. Capacitor C_5 is shorted.
d. Resistor R_8 is shorted.

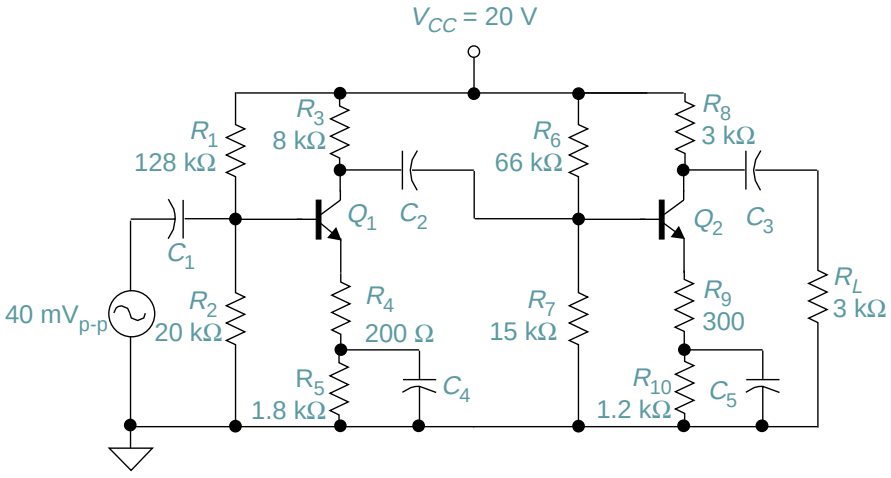

FIGURE 5–24

____ 32. The DC voltage at the junction of resistors R_4 and R_5 in Figure 5–24 is zero volts.

a. The circuit is functioning correctly.
b. Transistor Q_1 has a collector to emitter short.

c. Capacitor C_4 is open.
d. Resistor R_2 is shorted.

____ 33. The signal voltage gain of Q_2 in Figure 5–24 is approximately two times the calculated gain.
a. The circuit is functioning correctly.
b. Capacitor C_3 is open.
c. Capacitor C_3 is shorted.
d. Capacitor C_5 is open.

____ 34. The signal voltage gain of Q_1 is approximately three.
a. The circuit is functioning correctly.
b. Capacitor C_4 is open.
c. Capacitor C_4 is shorted.
d. Capacitor C_2 is open.

PROBLEMS

1. For the circuit in Figure 5–25, find:

V_c = _____ V_B = _____ V_E = _____ A_v = _____
V_{CE} = _____ z_{in} = _____ z_{out} = _____ V_{out} = _____

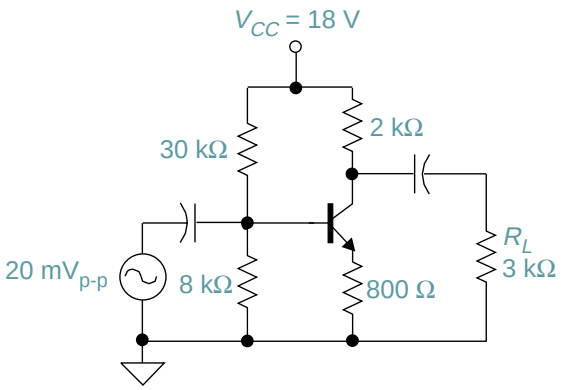

FIGURE 5–25

2. For the circuit in Figure 5–26, find:

V_c = _____ V_B = _____ V_E = _____ A_v = _____
V_{CE} = _____ z_{in} = _____ z_{out} = _____ V_{out} = _____

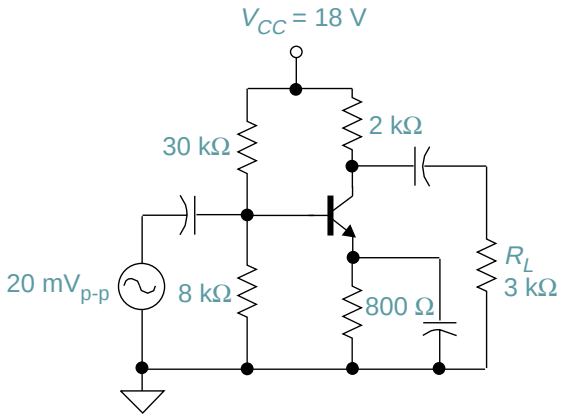

FIGURE 5–26

3. For the circuit in Figure 5–27, find:

   V_c = _____ V_B = _____ V_E = _____ A_v = _____

   V_{CE} = _____ z_{in} = _____ z_{out} = _____ V_{out} = _____

4. What is the largest signal that can be accommodated at the input of the circuit in Figure 5–27 before the output begins to clip?

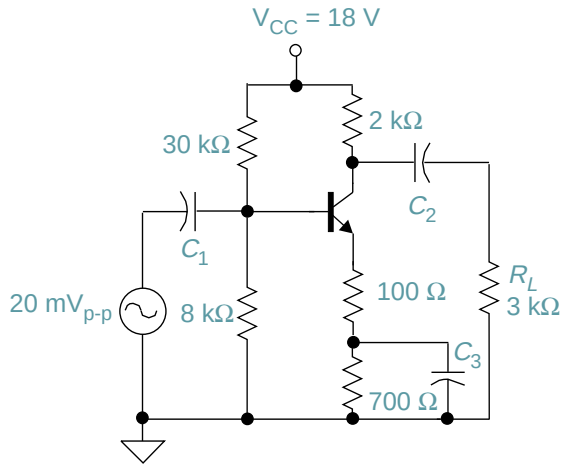

FIGURE 5–27

5. If the lowest frequency of operation is to be 100 Hz, select a value for C_1, C_2, and C_3 in the circuit in Figure 5–27.

   C_1 = _____ C_2 = _____ C_3 = _____

6. For the circuit in Figure 5–28, find:

   V_c = _____ V_B = _____ V_E = _____ A_v = _____

   V_{CE} = _____ z_{in} = _____ z_{out} = _____ V_{out} = _____

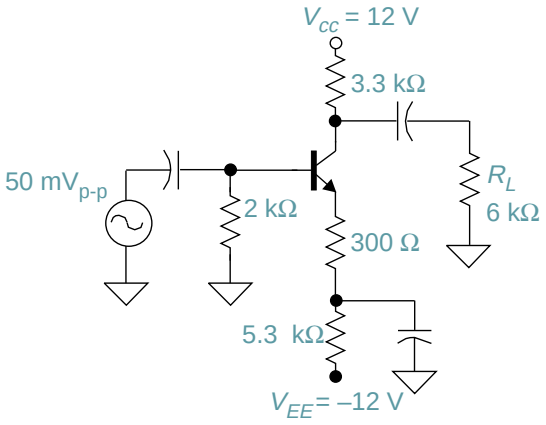

FIGURE 5–28

7. Find the values requested below for the circuit in Figure 5–29.

Stage 1:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Stage 2:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Total Circuit:

A_v = _____ z_{in} = _____ z_{out} = _____

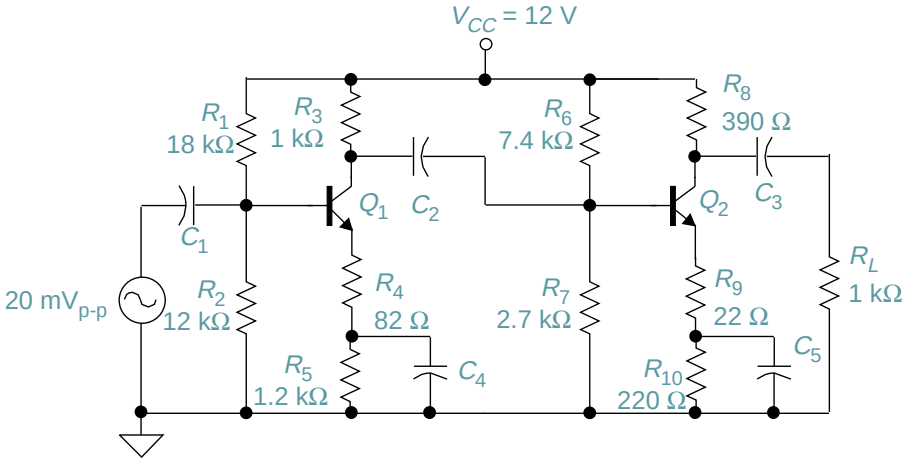

FIGURE 5–29

8. If the lowest frequency of operation is to be 1 kHz, select a value for C_1, C_2, C_3, C_4, and C_5 in the circuit in Figure 5–29.

C_1 = _____ C_2 = _____ C_3 = _____

C_4 = _____ C_5 = _____

9. Find the values requested below for the circuit in Figure 5–30.

Stage 1:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Stage 2:

V_B = _____ V_E = _____ V_C = _____

A_v = _____ z_{in} = _____ z_{out} = _____

Total Circuit:

z_{in} = _____ z_{out} = _____ A_v = _____

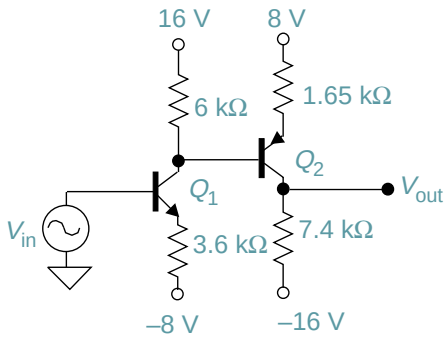

FIGURE 5–30