Application Note AN4107

Design of Power Factor Correction Using FAN7527

1. Introduction

The FAN7527 is an active power factor correction(PFC) controller for boost PFC application which operates in the critical conduction mode. It turns on MOSFET when the inductor current reaches zero and turns off MOSFET when the inductor current meets the desired input current reference voltage as shown in Fig. 1. In this way, the input current waveform follows that of the input voltage, therefore a good power factor is obtained.

1-1. Internal Block Diagram

It contains following blocks.

- Error amplifier (E/A)
- Zero current detection (Idet)
- Switch current sensing (CS)
- Input voltage sensing (MULT)
- Switch drive (OUT)

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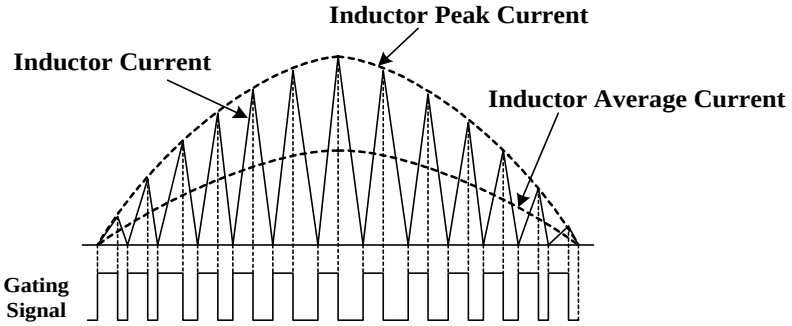

Figure 1. Inductor Current Waveform

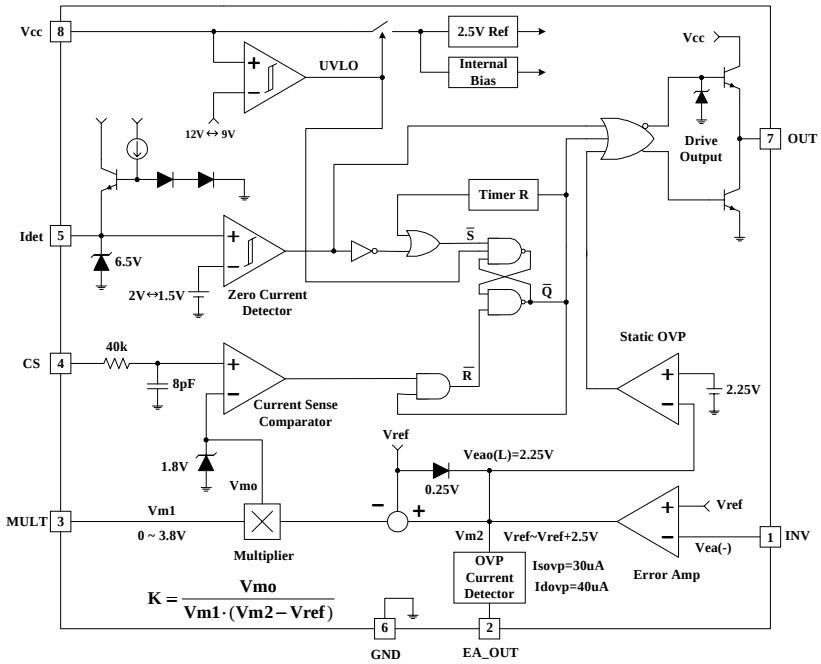

Figure 2. Block diagram of the FAN7527

2. Device Block Description

2-1. Error Amplifier and Over Voltage Protection Block

The sensed and divided output voltage is fedback to the error amplifier inverting input(INV) to regulate the output voltage. The non-inverting input is internally biased at 2.5V. The error amp output(EA_OUT) is internally connected to the multiplier and is pinned out for the loop compensation. Generally, the control loop bandwidth of PFC converter is set below 20Hz to get a good power factor. In this application, a capacitor is connected between INV and EA_OUT. However, in case of over voltage condition, the E/A must be saturated low as soon as possible, but the narrow E/A bandwidth slows down the response. To make the over voltage protection fast, the soft OVP and dynamic OVP is added. The FAN7527 monitors the current flowing into the EA_OUT pin. If the monitored current reaches about 30uA, the output of multiplier is forced to be decreased, thus reducing the input current drawn from the mains(soft OVP). If the monitored current exceeds 40uA, the OVP protection is triggered(dynamic OVP), then the external power transistor is switched off until the current falls below about 10uA. In this case, it disables some internal blocks reducing the quiescent current of the chip to 2mA. However, if the over voltage lasts so long that the output of E/A goes below 2.25V, then the protection is activated(static OVP) keeping the output stage and the external power switch turned off. The operation of the device is re-enabled as the E/A output goes back into its linear region.

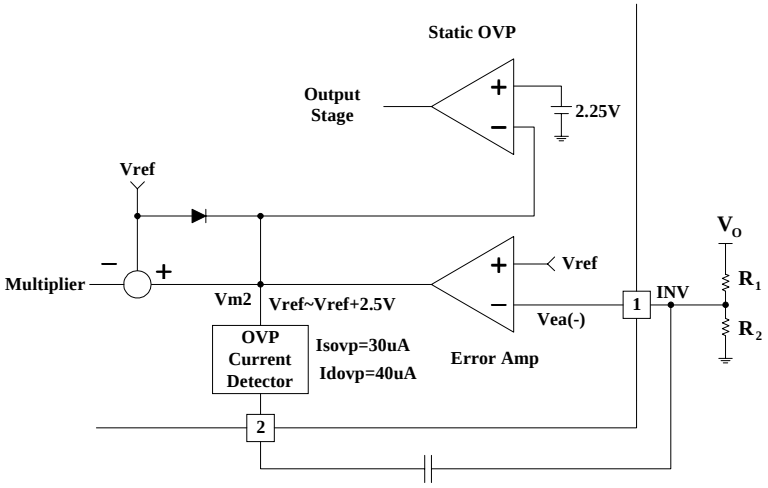

Figure 3. Error Amplifier and OVP Block

2-2. Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to get power factor correction. One input of multiplier(Pin 3) is connected to an external resistor divider which monitors the rectified ac line voltage. The other input is internally driven by a DC voltage which is the difference between error amplifier output (Pin 2) and reference voltage, Vref. The multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0V to 3.8V for Pin 3, and 2.25V to 6V for error amplifier output under all line and load conditions.

The multiplier output controls the current sense comparator threshold voltage as the ac voltage traverses sinusoidally from zero to peak line. This allows the inductor peak current to follow the ac line thus forcing the average input current to be sinusoidal. In other words, this has the effect of forcing the MOSFET on-time to track the input line voltage, resulting in a fixed drive output on-time, thus making the pre-converter load appear to be resistive to the ac line.

The equation below describes the relationship between multiplier output and its inputs.

$Vmo = K \times Vm1 \times (Vm2 - Vref)$

K : Multiplier gain

Vm1: Voltage at Pin 3

Vm2: Error amp output voltage

Vmo: Multiplier output voltage

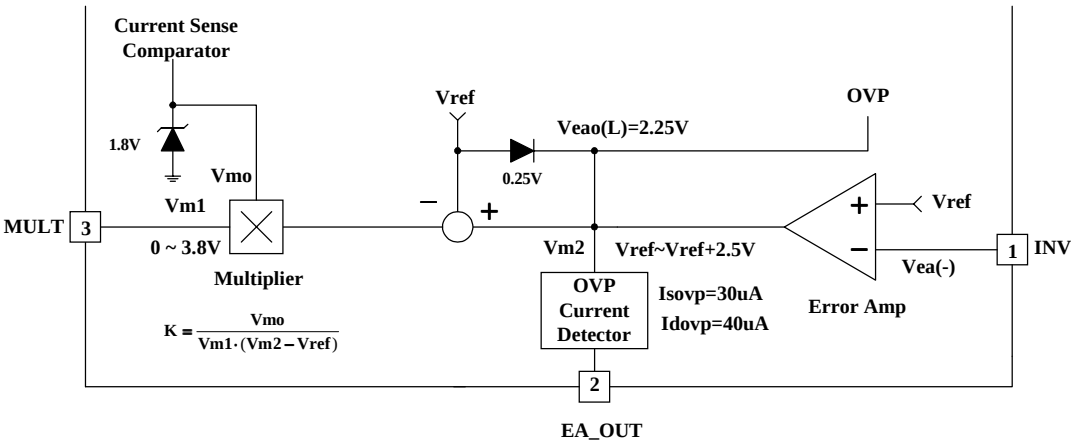

Figure 4. Multiplier block

2-3. Current Sense Comparator

The current sense comparator adopts the RS latch configuration to ensure that only a single pulse appears at the drive output during a given cycle. MOSFET drain current is sensed using an external sense resistor in series with the external MOSFET. When the sensed voltage exceeds the threshold set by the multiplier output, the current sense comparator turns off the MOSFET and resets the PWM latch. The latch insures that the output remains in a low state after the MOSFET drain current falls back to zero.

The peak inductor current under the normal operating condition is controlled by the multiplier output, Vmo. The abnormal operating condition occurs during pre-converter start-up at extremely high line or as output voltage sensing is lost. Under these conditions, the multiplier output and current sense threshold will be internally clamped to 1.8V. Therefore, the maximum peak switch current is limited to:

Ipk(max) = 1.8V / Rsense

In the FAN7527, an internal R/C filter has been included to attenuate any high frequency noise that may be present on the current waveform. This circuit block eliminates the need for an external R/C filter otherwise required for proper operation of the circuit.

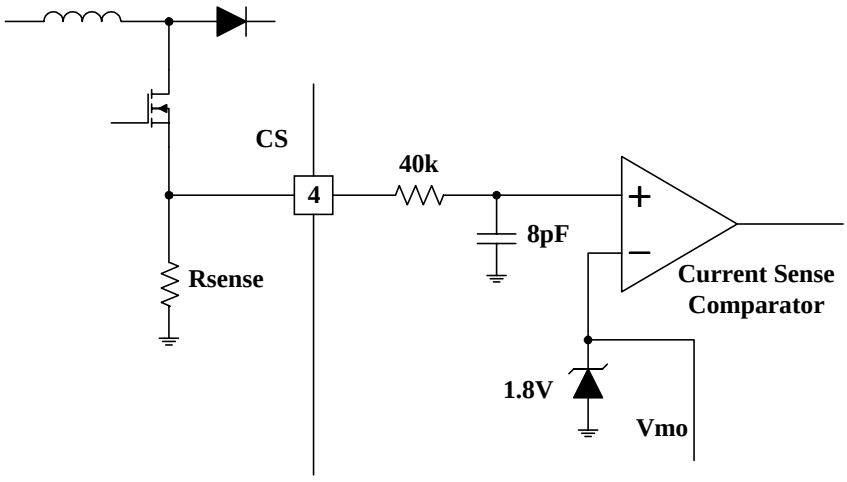

Figure 5. Current Sense Circuit

2-4. Zero Current Detector

FAN7527 operates as a critical conduction current mode controller. The zero current detector switches on the external MOSFET as the voltage across the boost inductor reverses, just after the current through the boost inductor has gone to zero. The slope of the inductor current is indirectly detected by monitoring the voltage across an auxiliary winding and connecting it to the zero current detector Pin 5.
Once the inductor current reaches ground level, the polarity of the voltage across the winding is reversed. When the Idet input falls below 1.5V, the comparator output is triggered to the low state. To prevent false tripping, 0.5V hysteresis is provided. The zero current detector input is protected internally by two clamps. The upper 6.5V clamp prevents input over voltage breakdown while the lower 0.75V clamp prevents substrate injection. An internal current limit resistor protects the lower clamp transistor in case the Idet pin is shorted to ground accidentally. A watchdog timer function is added to the IC to eliminate the need for an external oscillator when used in stand-alone applications. The timer provides a means to start or restart the pre-converter automatically if the drive output has been off for more than 500us after the inductor current reached zero.

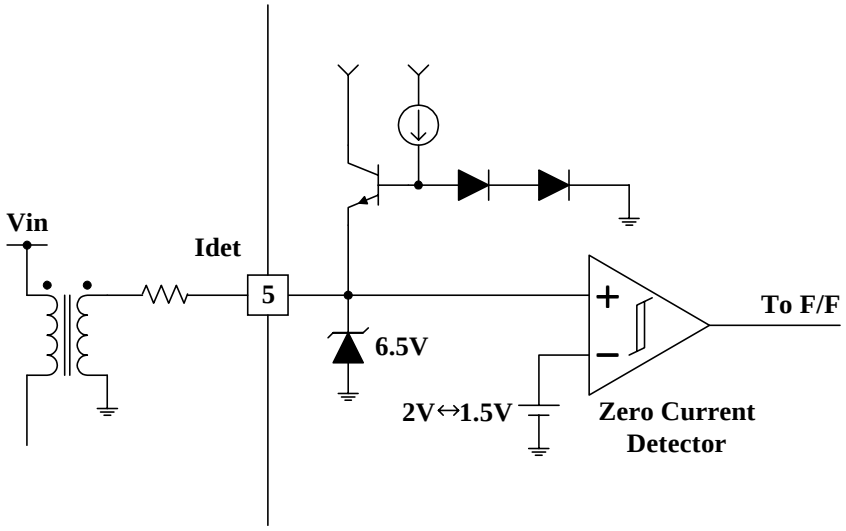

Figure 6. Zero Current Detector Block

2-5. Output Drive

The FAN7527 contains a single totem-pole output stage designed specifically for a direct drive of power MOSFET. The drive output is capable of up to 500mA peak current with a typical rise and fall time of 130ns, 50ns respectively with a 1.0nF load. Additional circuitry has been added to keep the drive output in a sinking mode whenever the UVLO is active. This characteristic eliminates the need for an external gate pull-down resistor. Internal voltage clamping ensures that the output driver is always lower than 14V when supply voltage exceeds the rated Vgs of the external MOSFET. This eliminates an external zener diode and extra power dissipation associated with it that otherwise is required for the reliable circuit operation.

3. Circuit Components Design

3-1. Power stage design

1) Boost inductor design

The boost inductor value is determined by the minimum switching frequency limitation. The minimum switching frequency has to be above the audio frequency.
The switching period is maximum when the input voltage is highest at maximum load condition. $T_{S(max)}$ is a function of $V_{in(peak)}$ and V_O. It can have maximum value at highest line or at lowest line according to V_O. Check $T_{S(max)}$ at $V_{in(peak\_min)}$ and $V_{in(peak\_max)}$, then take the higher value for the maximum switching period. The boost inductor value can be obtained by (5)

$$t_{on} = L\frac{I_{L(peak)}(t)}{V_{in(peak)}\sin(\omega t)} = L\frac{2I_{in(peak)}\sin(\omega t)}{V_{in(peak)}\sin(\omega t)} \quad (1)$$

$$= L\frac{2I_{in(peak)}}{V_{in(peak)}}$$

$$t_{off} = L\frac{I_{L(peak)}(t)}{V_O - \sin(\omega t)} = L\frac{2I_{in(peak)}\sin(\omega t)}{V_O - V_{in(peak)}\sin(\omega t)} \quad (2)$$

$$I_{in(peak)} = \frac{2V_O I_O}{\eta \cdot V_{in(peak)}} \quad (3)$$

$$T_S = t_{on} + t_{off}$$

$$= 2LI_{in(peak)}\left(\frac{1}{V_{in(peak)}} + \frac{\sin(\omega t)}{V_O - V_{in(peak)}\sin(\omega t)}\right) \quad (4)$$

$$= \frac{4LV_O I_{O(max)}}{\eta}\left(\frac{1}{V^2_{in(peak)}} + \frac{1}{V_{in(peak)}(V_O - V_{in(peak)})}\right)$$

$$T_{S(max)} = \frac{4LV_O I_{O(max)}}{\eta}\left(\frac{1}{V^2_{in(peak)}} + \frac{1}{V_{in(peak)}(V_O - V_{in(peak)})}\right) \quad (5)$$

$$L = \frac{\eta}{4f_{sw(min)}V_O I_{O(max)}\left(\frac{1}{V^2_{in(peak)}} + \frac{1}{V_{in(peak)}(V_O - V_{in(peak)})}\right)} \quad (6)$$

2) Auxiliary winding design

The auxiliary winding voltage is lowest at the highest line. So the number of auxiliary winding can be obtained by (7). A small resistor is connected to the auxiliary winding to suppress the high frequency ringing voltage.

$$N_{aux} = \frac{V_{CC} \cdot N_P}{\left(V_O - \frac{2\sqrt{2}}{\pi}V_{in(HL)}\right)} \quad (7)$$

3) Input capacitor design

The voltage ripple of the input capacitor is maximum when the line is lowest and the load is heaviest. If $f_{sw(min)} >> f_{ac}$, the input current can be assumed to be constant during a switching period.

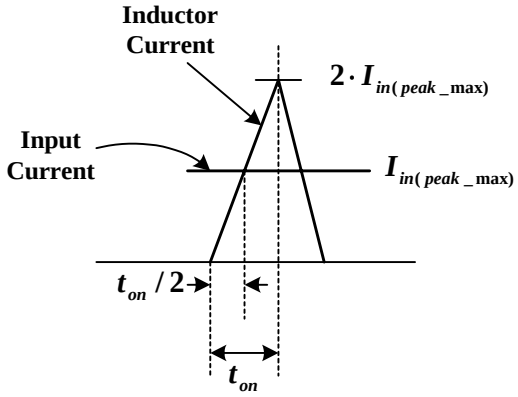

Figure 7. Input Current and Inductor Current Waveform during a Switching Cycle

$$C_{in} \geq \frac{2}{\Delta V_{in(max)}} \cdot \int_0^{\frac{ton}{2}} \left(I_{in(peak\_max)} - \frac{2 \cdot I_{in(peak\_max)}}{t_{on}}t\right)dt$$

$$\geq \frac{t_{on} \cdot I_{in(peak\_max)}}{2 \cdot \Delta V_{in(max)}} \quad (8)$$

$$\geq \frac{L \cdot I^2_{O(max)} \cdot V^2_O}{\Delta V_{in(max)} \cdot V^3_{in(peak\_max)}}$$

The input capacitor must be larger than the value calculated by (8). And the maximum input capacitance is limited by the input displacement factor(IDF), defined as IDF≡cosθ . Therefore the input capacitor must be smaller than $C_{in(max)}$ calculated by (12).

$$V_a = V_A = V_{in(peak)}\cos(\omega t) \quad (9)$$

$$i_a = I_a\cos(\omega t)$$

$$i_A = i_a + i_c = I_a\cos(\omega t) - \omega C_{in}V_{in(peak)}\sin(\omega t) \quad (10)$$

$$\theta = \tan^{-1}\frac{\omega C_{in}V_{in(peak)}}{I_a} \quad (11)$$

$$C_{in(max)} = \frac{I_a}{\omega V_{in(peak)}}\tan(\cos^{-1}(IDF))$$

$$= \frac{2V_O I_O}{\omega V^2_{in(peak\_max)}}\tan(\cos^{-1}(IDF)) \quad (12)$$

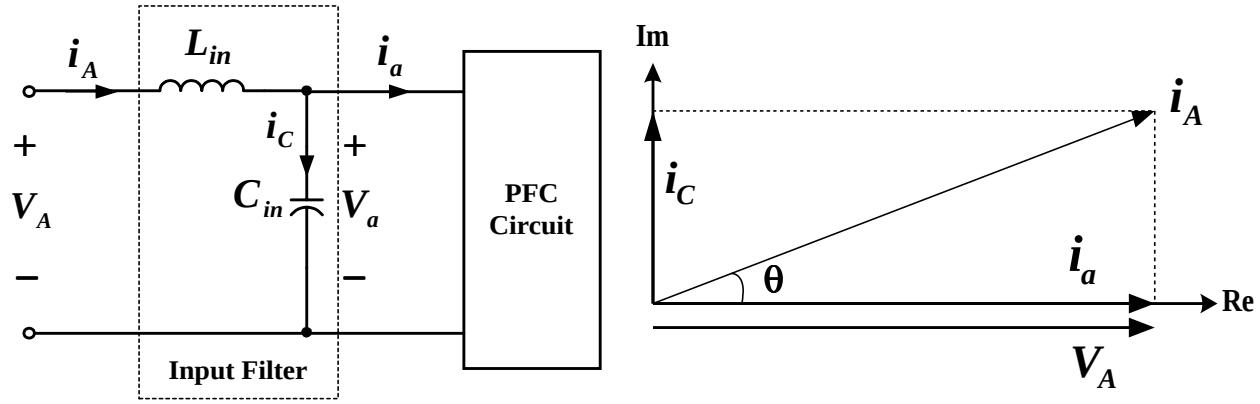

Figure 8. Input voltage and current displacement due to input filter capacitance

4) Output capacitor design

The output capacitor is determined by the relation between the input power and the output power. As shown in Fig. 10, the minimum output capacitance is determined by (14).

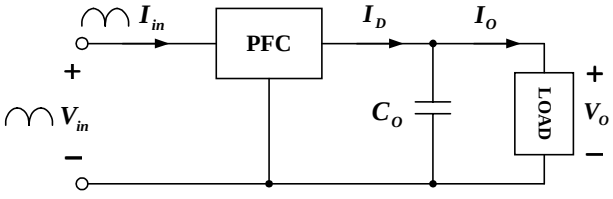

Figure 9. PFC configuration

$$P_{in} = I_{in(rms)}V_{in(rms)}(1-\cos(2\omega t)) = I_D V_O$$

$$I_D = \frac{I_{in(rms)}V_{in(rms)}}{V_O}(1-\cos(2\omega t)) = I_O(1-\cos(2\omega t)) \qquad (13)$$

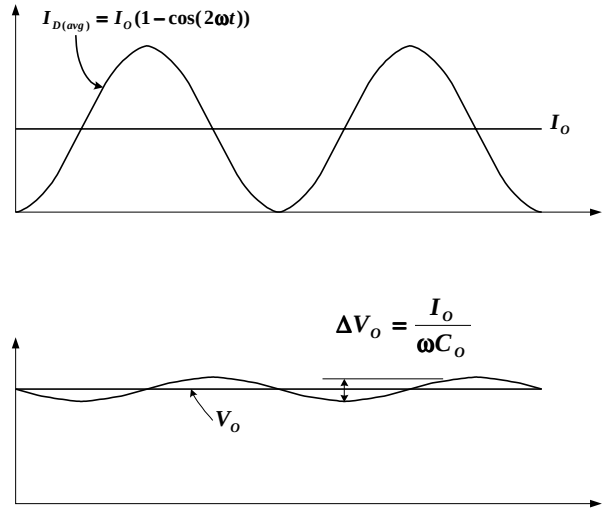

Figure 10. Diode current and output voltage waveform

$$C_{O(min)} \geq \frac{I_{O(max)}}{2\pi f_{ac} \cdot \Delta V_{O(max)}} \qquad (14)$$

5) MOSFET and diode selection

Maximum MOSFET rms current is obtained by (15) and the conduction loss of the MOSFET is calculated by (16). When MOSFET turns on the MOSFET current rises slowly so the turn on loss is negligible. MOSFET turn off loss and MOSFET discharge loss are obtained by (17) and (18) respectively. The switching frequency of the critical conduction mode boost PFC converter varies according to the line condition and load condition. Therefore the switching frequency is the average value during a line period. The total MOSFET loss can be calculate by (19) and then a MOSFET can be selected considering MOSFET thermal characteristic.

$$I_{Qrms} = I_{L(peak\_max)}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}V_{in(LL)}}{9\pi V_O}}$$

$$= \frac{2\sqrt{2}\cdot V_O I_{O(max)}}{\eta V_{in(LL)}}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}V_{in(LL)}}{9\pi V_O}} \qquad (15)$$

$$P_{on} = I^2_{Qrms}\cdot R_{DSon} \qquad (16)$$

$$P_{turn-off} = \frac{1}{6}V_O I_{L(peak\_max)}\cdot t_f \cdot f_{sw}$$

$$= \frac{\sqrt{2}}{3}\frac{V^2_O \cdot I_{O(max)}}{\eta V_{in(LL)}}\cdot t_f \cdot f_{sw} \qquad (17)$$

$$P_{discharge} = \frac{4}{3}C_{oss.Vo}\cdot V^2_O \cdot f_{sw} \qquad (18)$$

$$P_{MOSFET} = P_{on} + P_{turn\text{-}off} + P_{discharge} \qquad (19)$$

And the MOSFET gate drive resistor is determined by (20).

$$R_g > \frac{V_{Omax}}{I_{Omax}} = \frac{16V}{500mA} = 32\Omega \qquad (20)$$

Diode average current can be calculated by (21). The total diode loss can be calculated by (22) and then a diode can be selected considering diode thermal characteristic.

$$I_{Davg} = I_{O(max)} \quad (21)$$

$$P_{Diode} = V_f I_{Davg} \quad (22)$$

3-2. Control circuit design

1) Output voltage sensing resistor and feedback loop design
R_1 is determined by the maximum output over voltage, ΔV_{ovp} and R_2 is determined by (23).

$$\frac{R_1}{R_2} = \frac{V_O - 2.5}{2.5}, R_1 = \frac{\Delta V_{OVP}}{40\mu A}$$

$$, R_2 = \frac{2.5 R_1}{V_O - 2.5} \quad (23)$$

The feedback loop bandwidth must be narrower than 20Hz for the PFC application. Therefore a capacitor is connected between INV and EA_OUT to eliminate the 120Hz ripple voltage by 40dB. The error amp compensation capacitor can be calculated by (24). To improve the power factor, C_{comp} must be increased than the calculated value. And to improve the system response, C_{comp} must be lowered than the calculated value.

$$C_{comp} = \frac{1}{0.01 \cdot 2\pi \cdot 120Hz \cdot R_1} \quad (24)$$

2) Zero current detection resistor design
Idet current should be less than 3mA, therefore zero current detection resistor is determined by (25).

$$R_{idet} > \frac{N_{aux} \cdot V_O}{N_P \cdot 3mA}$$

3) Start-up circuit design
To start up the FAN7527, the start-up current must be supplied through a start-up resistor. The resistor value is calculated by (26) and (27). The start-up capacitor must supply IC operating current before the auxiliary winding supplies IC operating current maintaining Vcc voltage higher than the UVLO voltage. Therefore the start up capacitor is designed by (28).

$$R_{ST} \le \frac{V_{in(peak\_min)} - V_{th(st)max}}{I_{STmax}} \quad (26)$$

$$P_{Rst} = \frac{V^2_{in(rms\_max)}}{R_{ST}} \le 0.5W \quad (27)$$

$$C_{ST} \ge \frac{I_{dcc}}{2\pi \cdot f_{ac} \cdot HY_{(ST)min}} \quad (28)$$

4) Line voltage sense resistor and current sense resistor design
The maximum line voltage sensing gain is determined by (29) at the highest line.

$$V_{PIN3} = V_{in(peak\_max)} \cdot \frac{R_{in2}}{R_{in1} + R_{in2}}$$

$$= V_{in(peak\_max)} \cdot G_{in(max)} < 3.8V \quad (29)$$

Calculate the pin 3 voltage at the lowest line using $G_{in(max)}$ by (30). Then the current sense resistor is determined by (31), (32) and (34). Once the current sense resistor is determined, then the minimum line voltage sensing gain, $G_{in(max)}$ is determined by (31).

$$V_{O(m)} = K \cdot V_{in(peak\_min)} \cdot \frac{R_{in2}}{R_{in1} + R_{in2}} \Delta Vm2(max) \quad (30)$$

$$R_{semse} < \frac{V_{O(m)}}{I_{L(peak\_max)}} = K \cdot V_{in(peak\_min)} \cdot \frac{R_{in2}}{R_{in1} + R_{in2}} \cdot 2.5V \cdot \frac{\eta V_{in(peak\_min)}}{4 \cdot V_O I_{O(max)}} \quad (31)$$

$$R_{sense} < \frac{1.8V}{I_{L(peak\_max)}} = 1.8V \frac{\eta V_{in(peak\_min)}}{4 \cdot V_O I_{O(max)}} \quad (32)$$

$$P_{Rsense} = 2 \cdot \left(\frac{V_O I_{O(max)}}{\eta V_{in(peak\_min)}} \right)^2 \cdot R_{sense} < 1W \quad (33)$$

$$R_{sense} < \frac{1W}{2} \cdot \left(\frac{\eta V_{in(peak\_min)}}{V_O I_{O(max)}} \right)^2 \quad (34)$$

And attach 1nF capacitor in parallel with R2 to reduce the switching ripple voltage.

4. Design Example

A 100W converter is designed to illustrate the design procedure. The system parameters are as follows.

- Maximum output power : 100W
- Input voltage range : 85Vrms~265Vrms
- Output voltage : 400V
- AC line frequency : 60Hz
- PFC efficiency : 90%
- Minimum switching frequency : 34kHz
- Input displacement factor(IDF) : 0.98
- Input capacitor ripple voltage : 24V
- Output voltage ripple : 8V
- OVP set voltage : 450V

4-1. Inductor design

The boost inductor is determined by (6). Calculate it at both the lowest line and the highest line and choose the lower value. The calculated value is 586uH. To get the calculate inductor value, EI3026 core is used and the primary winding is 62 turns. The air gap is 0.586mm at both legs of the EI core. The auxiliary winding is determined by (7) and the auxiliary winding is 5 turns.

4-2. Input capacitor design

The minimum input capacitance is determined by the input voltage ripple specification. The calculated minimum input

capacitor value is 0.56uF. And the maximum input capacitance is restricted by IDF. The calculated value is 0.76uF. The selected value is 0.67uF for the input capacitor(sum of all capacitors connected to the input).

4-3. Output capacitor design

The minimum output capacitor is determined by (14) and the calculated value is 83uF. The selected value is 100uF capacitor.

4-4. MOSFET and diode selection

By (15)~(19), 500V/6A MOSFET FQP6N50 is selected and by (21)~(23), and 1000V/1A diode BYV26E is selected by (21)~(22).

4-5. Output voltage sense resistor and feedback loop design

The upper output voltage sense resistor is 1.2MΩ and the bottom output voltage sense resistor is 7kΩ plus 10kΩ variable resistor. A variable resistor is used to adjust the output voltage. The error amp compensation capacitance must be larger than 0.11uF by (24). Therefore 0.33uF capacitor is used.

4-6. Zero current detection resistor design

The calculate value is 430Ω and the selected value is 22kΩ.

4-7. Start-up circuit design

The maximum start-up resistor is 1 MΩ and the minimum is 140kΩ by (26)~(27). Our selection is 150kΩ. And the start-up capacitance must be larger than 10.6uF by (28). The selected value is 47uF.

4-8. Line voltage sense resistor and current sense resistor design

The maximum input voltage sensing gain is determined by (29). Using the calculated value, the current sense resistance is determined by (31), (32) and (34). The maximum current sense resistance is 0.48Ω and the selected value is 0.2Ω. Then the minimum input voltage sensing gain is determined by (30). If we choose the input voltage sense bottom resistor to be 18kΩ then the maximum input voltage sense upper resistance and the minimum input voltage sense upper resistance can be obtained from $G_{in(min)}$ and $G_{in(max)}$.
The selected value is 2.7MΩ.
Fig. 11 shows the designed application circuit diagram and table 1 shows the 100W demo board components list.

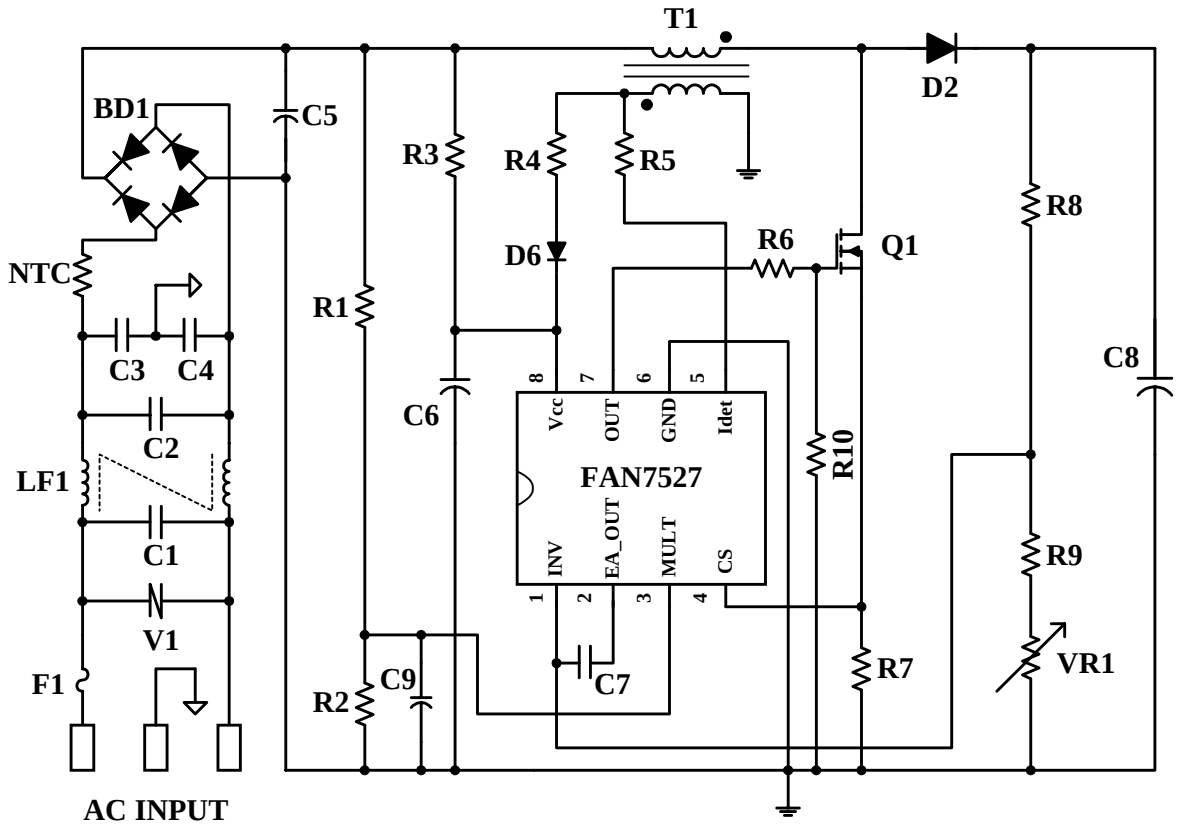

Figure 11. Application circuit diagram

Table 1: 100W demo board part list

Part#	Value	Note	Part#	Value	Note
Fuse			Capacitor		
F1	250V/3A	-	C1	47nF	275Vac
Varistor			C2	150nF	275Vac
V1	471	-	C3,C4	2200pF	3000V
NTC			C5	0.47nF	630V
RT1	10D-9	-	C6	47nF	35V
Resistor			C7	0.33nF	MLCC
R1	2.7MΩ	1/4W	C8	100nF	450V
R2	18kΩ	1/4W	C9	102	Ceramic
R3	150kΩ	1W	**Diode**		
R4	100Ω	1/4W	BD1	660(600V/6A)	Bridge Diode
R5	22kΩ	1/4W	D1	1N4148	-
R6	47Ω	1/4W	D2	BYV26E	1000V/1A
R7	0.2Ω	1W	**Line Filter**		
R8	1.2MΩ	1/4W	LF1	45mH	-
R9	7kΩ	1/4W	**Inductor**		
R10	500kΩ	1/4W	T1	590uH(62T : 5T)	EI3026
VR1	103	-	**MOSFET**		
IC			Q1	FQPF6N50	500V/6A
IC1	FAN7527	-	-	-	-

Table 2: 150W demo board part list

Part#	Value	Note	Part#	Value	Note
Fuse			Capacitor		
F1	250V/3A	-	C1	330nF	275Vac
Varistor			C2	330nF	275Vac
V1	471	-	C3,C4	2200pF	3000V
NTC			C5	0.68nF	630V
RT1	10D-9	-	C6	47nF	35V
Resistor			C7	1nF	MLCC
R1	2.2MΩ	1/4W	C8	150nF	450V
R2	20kΩ	1/4W	C9	102	Ceramic
R3	150kΩ	1W	**Diode**		
R4	100Ω	1/4W	BD1	660(600V/6A)	Bridge Diode
R5	22kΩ	1/4W	D1	1N4148	-
R6	47Ω	1/4W	D2	SUF15J	600V/1.5A
R7	0.2Ω	1W	**Line Filter**		
R8	1.2MΩ	1/4W	LF1	45mH	-
R9	7kΩ	1/4W	**Inductor**		
R10	500kΩ	1/4W	T1	500uH(83T:5T)	MPP Core
VR1	103	-	**MOSFET**		
IC			Q1	FQA9N50	500V/9A
IC1	FAN7527	-	-	-	-

Table 3: 200W demo board part list

Part#	Value	Note	Part#	Value	Note
Fuse			Capacitor		
F1	250V/3A	-	C1	330nF	275Vac
Varistor			C2	330nF	275Vac
V1	471	-	C3,C4	2200pF	3000V
NTC			C5	0.68nF	630V
RT1	10D-9	-	C6	47nF	35V
Resistor			C7	1nF	MLCC
R1	2.2MΩ	1/4W	C8	220nF	450V
R2	22kΩ	1/4W	C9	102	Ceramic
R3	150kΩ	1W	**Diode**		
R4	100Ω	1/4W	BD1	660(600V/6A)	Bridge Diode
R5	22kΩ	1/4W	D1	1N4148	-
R6	47Ω	1/4W	D2	SUF15J	600V/1.5A
R7	0.1Ω	1W	**Line Filter**		
R8	1.2MΩ	1/4W	LF1	45mH	-
R9	7kΩ	1/4W	**Inductor**		
R10	500kΩ	1/4W	T1	400uH(74T:5T)	MPP Core
VR1	103	-	**MOSFET**		
IC			Q1	FQA13N50	500V/13A
IC1	FAN7527	-	-	-	-

Nomenclature

$I_{L(peak)}$ (t) : inductor current peak value during one switching cycle

$I_{L(peak)}$: inductor current peak value during one AC line cycle

$I_{L(peak\_max)}$: maximum inductor current peak value

I_L (t) : inductor current

I_D : boost diode current

I_{in} (t) : input current

$I_{in\ (peak)}$: input current peak value

$I_{in\ (peak\_max)}$: maximum of the input current peak value

$I_{in\ (rms)}$: input current RMS value

I_{Qrms} : MOSFET rms current

I_{Drms} : diode rms current

I_{Davg} : diode average current

I_O : output current

$I_{O\ (max)}$: maximum output current

V_{in} (t) : input voltage

$\Delta V_{in\ (max)}$: maximum input voltage ripple

$V_{in\ (peak)}$: input voltage peak value

$V_{in\ (peak\_max)}$: maximum input voltage peak value

$V_{in\ (peak\_min)}$: minimum input voltage peak value

$V_{in\ (rms)}$: input voltage RMS value

$V_{in\ (rms\_max)}$: maximum input voltage RMS value

$V_{in\ (rms\_min)}$: minimum input voltage RMS value

$V_{in\ (LL)}$: low line rms input voltage

$V_{in\ (HL)}$: high line rms input voltage

V_O : output voltage

$\Delta V_{O\ (max)}$: maximum output voltage ripple

ΔV_{OVP} : maximum output over voltage

P_O : output power

$P_{O(max)}$: maximum output power

P_{in} : input power

η : converter efficiency

t_{on} : switch on time

t_{off} : switch off time

t_f : MOSFET current falling time

T_S : switching period

f_{ac} : AC line frequency

ω : AC line angular frequency

f_{SW} : switching frequency

$f_{SW(max)}$: maximum switching frequency

$f_{SW(min)}$: minimum switching frequency

L : boost inductance

C_O : output capacitance

C_{in} : input capacitance

η : converter efficiency

N_{aux} : auxiliary winding turn number

N_P : boost inductor turn number

C_{comp} : compensation capacitance

R_{idet} : zero current detection resistance

R_{ST} : start up resistance

R_1 : output voltage divider top resistance

R_2 : output voltage divider bottom resistance

R_{in1} : input voltage divider top resistance

R_{in2} : input voltage divider bottom resistance

R_{sense} : current sense resistance

I_{STmax} : maximum start up supply current

C_{ST} : start up capacitance

$HY_{(ST)min}$: minimum UVLO hysteresis

K : multiplier gain

$G_{in\ (min)}$: minimum input voltage sense gain

$G_{in\ (max)}$: maximum input voltage sense gain