Latch-Up Protection For MOSFET Drivers

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INTRODUCTION

Most CMOS ICs, given proper conditions, can "latch" (like an SCR), creating a short circuit from the positive supply voltage to ground. This application note explains how this occurs and what can be done to prevent it for MOSFET drivers.

CONSTRUCTION OF CMOS ICs

In fabricating CMOS ICs, parasitic bipolar transistors are formed as a by-product of the CMOS process (see Figure 1). These transistors are inherent in the CMOS structure and can't be eliminated. The P-channel device has a parasitic PNP and the N-channel has a parasitic NPN. Through internal connections, the two parasitics form a four-layer SCR structure (see Figure 1 and Figure 2).

The parasitic SCR can be turned on if the P+ of the P-channel drain is raised above V_S+. This action will bias the drain P+ of parasitic Q_1 (Q_1's emitter), back through Q_1's base and return to V_S+ through bulk resistance R_1. A similar situation can occur if the drain of the N-channel MOSFET (emitter of Q_2) is taken below the V_S- supply.
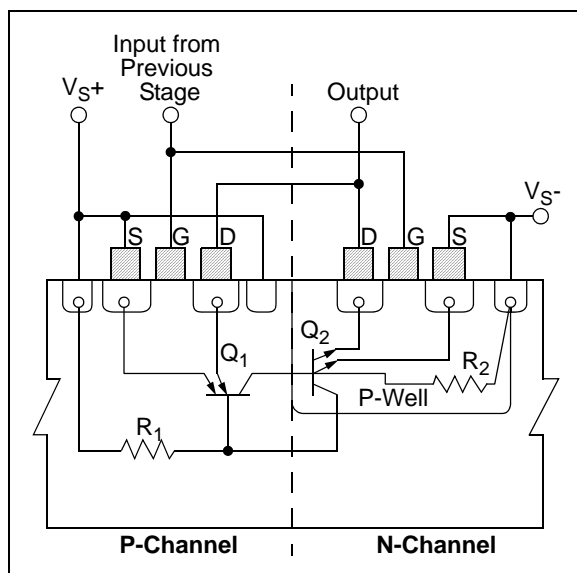
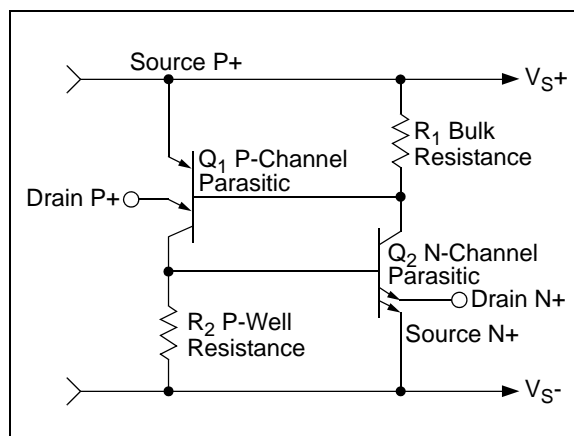

FIGURE 1:   Output Stage IC Layout.

FIGURE 2:   Equivalent SCR Circuit.

This emitter base junction of the parasitic bipolar is the parasitic diode that is also found in power MOSFETs. One of these diodes exists in every CMOS structure for both N- and P-channel devices. This corresponds with the fact that there exists a parasitic bipolar for every MOSFET in the IC, including the input transistors. Turn any one of them on and the SCR action will occur.

In most applications, the triggering of the parasitic SCR results in the destruction of the IC. The only time destruction does not occur is when the supply current to the device is limited. In this case, the device will resume normal operation when the parasitic SCR is unlatched by cycling the supply current through zero.

PREVENTING SCR TRIGGERING

Grounds

Clean grounds are important in any system, but they are especially important in analog and power processing circuits, becoming even more critical when CMOS ICs are used.

Poor ground practice can result in device latching. An example of this is shown in Figure 3. In this example, the PWM source sends the TC426 a "low" signal which causes the power MOSFET to turn "on". If the ground return resistance (R_1) is sufficiently high, the ground voltage of the TC426 will rise above that of the PWM source, resulting in the input of the TC426 being negatively biased and will cause the TC426 to latch.

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A similar condition can be caused by circuit inductance. Referring to Figure 3, assume R_1 is replaced by an inductor. When the MOSFET turns "on", current in the source lead builds up very rapidly. Typical rise times would be about 30 nsec to 60 nsec.

For our example, assume that the MOSFET is switching 5A and the circuit inductance is 10 nH. From V = L di/dt, we can generate voltage shifts of 0.83V to 1.66V, depending upon the rise time, which is more than enough to trigger the parasitic SCR.

Troubleshooting this type of problem can be facilitated by placing a series resistor, typically 100Ω, between the TC426 and the MOSFET gate. This slows the MOSFET's transition and the circuit can be observed in operation without anything being destroyed. Be sure to take into account the increased dissipation in the MOSFET when using this technique.
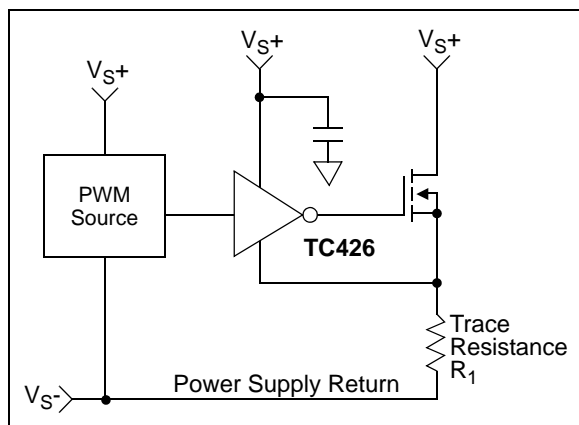

FIGURE 3:   *Improper Ground.*

Figure 7 and Figure 9 show a proper "star" ground that will prevent latching. Notice all grounds meet only at one point. On a PC board, this means all traces must meet at one point, not that they are all connected to the same trace (Figure 3 and Figure 9 show this mistake).
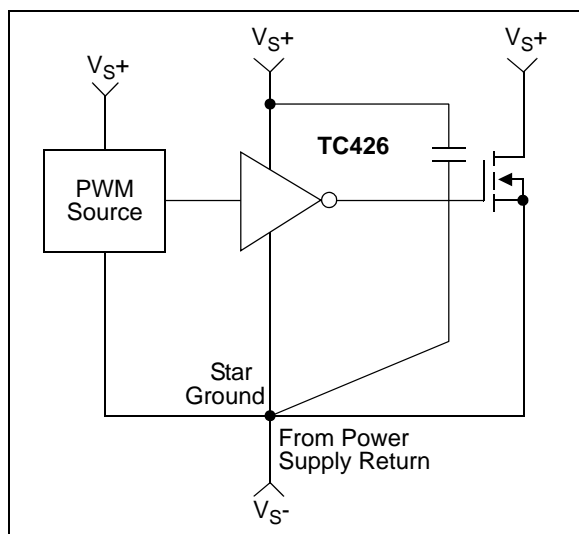

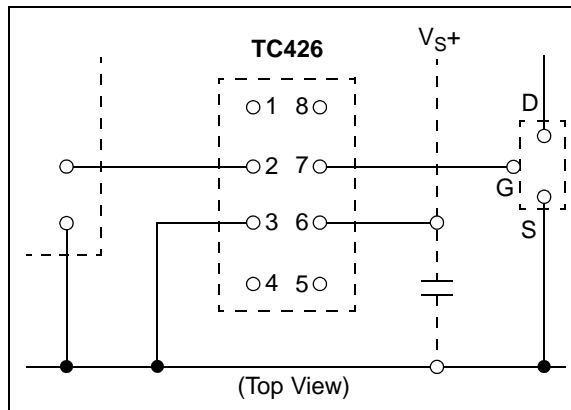
FIGURE 4:   *Proper Ground.*

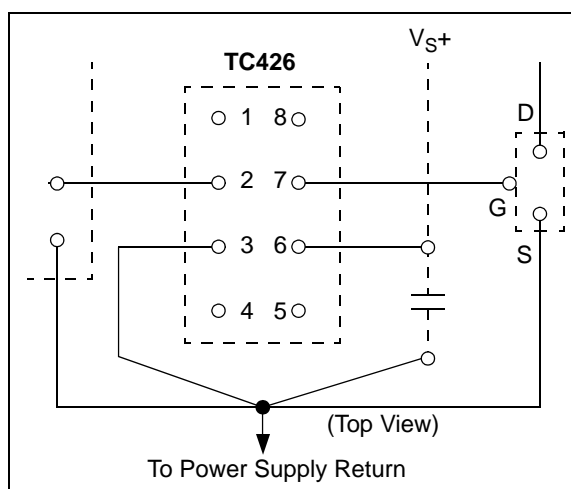**FIGURE 5:**   *Improper PC Layout.*

FIGURE 6:   *Proper PC Layout.*

DECOUPLING

Ripple and noise on the power supply voltage is another source of latch-up problems. V_S+ may be properly decoupled at the power supply, but at the supply pins of the IC, voltage transients occur. These transients are generated by the combination of the fast peak currents being drawn by the IC and the parasitic inductances and resistances of the power supply conductors (see Figure 7 and Figure 8).

This problem can be very pronounced with ICs driving large loads, as is the case of a TC426 or TC429 driving a power MOSFET. Upon switching, the TC429 can draw several amperes of current from the V_S+ supply, causing large transients in the local supply voltage. If the TC429's input is very close to the system supply voltage, as it can be when being driven by CMOS logic, the local V_S+ supply can drop significantly below the input, triggering the parasitic SCR. The parasitic SCR is very fast and this transition need last only a few nanoseconds for latching to occur.
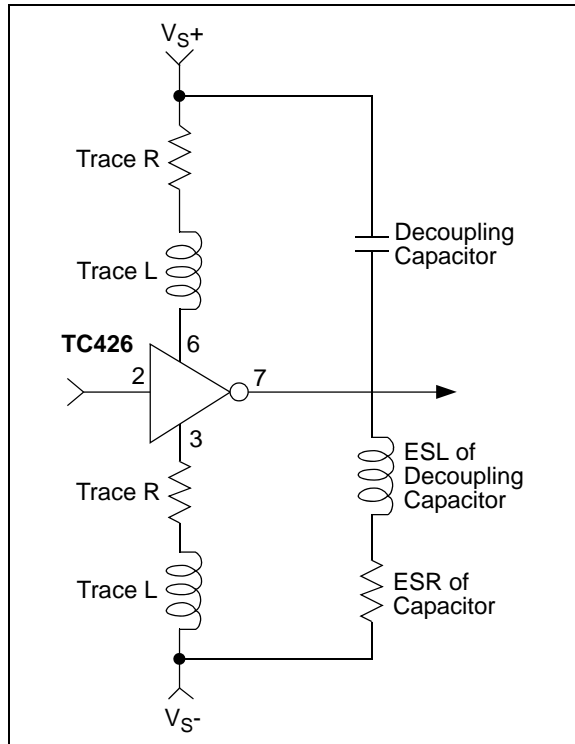
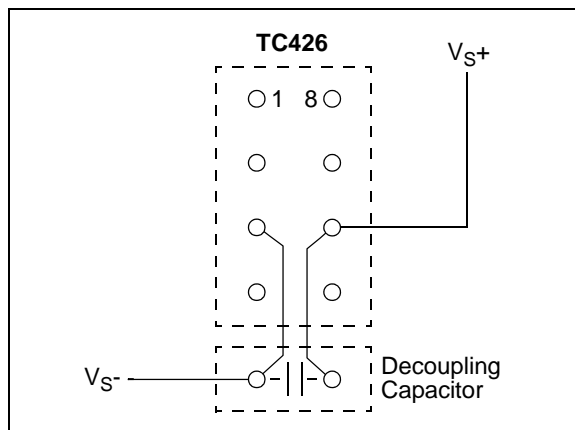**FIGURE 7:** *TC426 Fed by two PC Traces (Equivalent Circuit).*

FIGURE 8: *Typical PC Layout (TC426).*

Aggravating this is the temperature dependence of the parasitic transistors. Their base emitter voltage decreases ≈ 2.2 mV/°C as temperature increases, making them increasingly more sensitive to transients as the chip temperature rises. Many times a system, which performed admirably on the bench, begins to experience problems at high temperatures because the local decoupling was marginal. The obvious solution is to properly decouple the supply bus so that V_S+ can't drop below the value of the input signal. A second, less obvious, solution is to reduce the logic level applied to the input of the device.

Although lowering the input voltage will help the spikes that occur, they can cause other ICs on the same power supply to suffer noise immunity problems from the noise generated by the driver IC.

In some applications, such as portable instrumentation, it is desirable to keep the total power consumption at a minimum and designers will commonly shut off power to unused portions of the system to conserve battery life.

This can cause problems when an input signal is always present even though the V_S+ line is turned "off". In this case, a resistor in series with the CMOS device's input will limit the injected current to a value below that listed in the device data sheet as "the maximum current into any pin". When V_S+ is subsequently switched "on", the SCR action will be prevented.

DIODES

A very reliable method for preventing parasitic SCR action is to guard all the susceptible IC pins with steering diodes. This is most commonly done when a MOSFET driver is driving an inductive load, such as a long length of wire or a pulse transformer.

Placing a reverse-biased diode between each supply rail and the input/output pins (as shown in Figure 9 and Figure 10) limits the applied voltage swing to no more than the supply voltage plus the forward voltage drop of the clamping diode. For this reason, Schottky diodes are usually the best choice for this technique, as their forward voltage drop is less than the parasitic SCR's base emitter drop at any temperature. A Philips®/Mullard™/Amperex® BYV10-30, for example, will work well for higher-power applications, such as MOSFET drivers. A BAT54 dual diode works well for surface-mount applications and with lower power ICs, such as operational amplifiers and A/D converters.
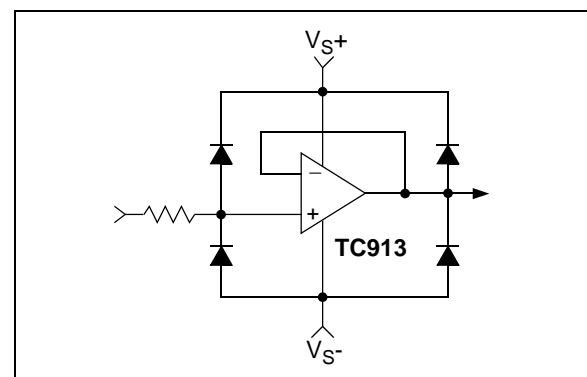

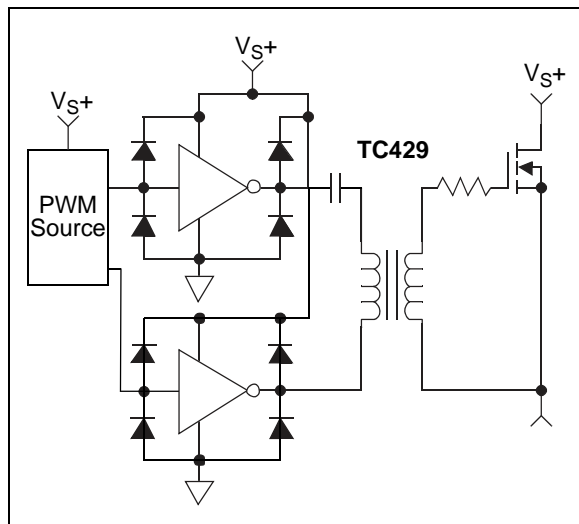**FIGURE 9:** *TC913 with Diode Clamps.*

FIGURE 10: *TC429's Driving Pulse Transformer.*

Germanium diodes, such as a 1N270, will work well also, but may be too leaky for some applications. Standard signal diodes, the 1N4148 or 1N914, for example, are frequently used. Their larger junctions having a lower effective forward drop than the parasitic junctions in the IC work effectively as over/under voltage clamps.

In some instances where standard junction diodes are too leaky (such as might be the case in Figure 10), a very low leakage junction FET (JFET) acting as a diode will do the trick. These devices can have leakage as low as a few picoamps and are very quick in responding. For these applications, contact Microchip Technology Inc.

RESISTORS

In applications where triggering of the parasitic SCR is not a concern and protecting the IC from destruction is the only issue, adding a resistor in series with the power supply pin will prevent device destruction. Once the SCR has been triggered, the supply voltage will have to be brought momentarily to zero to reset the SCR, but no damage will have been done to the IC unless the series resistor was not large enough to limit the fault current to a safe value. This is the lowest cost solution to prevent device damage.

Using the resistor has limitations, however. The resistor will limit the current allowed for the decoupling capacitor, which limits the frequency that the circuit can be driven at due to the R x C value.

This method works very well in DC op amp circuits, as op-amps draw very little peak current and the circuit is only amplifying DC; no AC component – no R x C problems.

CONCLUSION

Latch-up in CMOS ICs is preventable. Simple circuit techniques and attention to system design details will ensure that the CMOS' full potential can be realized in all operating environments. Designers can also look forward to the day, in the not too distant future, when even these few simple precautions will no longer be necessary.

Synopsis

To prevent latch-up:

1. Properly decouple IC.
2. Clamp outputs with diodes when driving inductive loads.
3. Clamp inputs with diodes if input signal exceeds the negative or positive rails of the power supply.
4. Use star grounds, if at all possible, in high-current applications.

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