

Third Harmonic Filtered 13.56 MHz Push-Pull Class-E Power Amplifier

Thomas Gerrits, Jorge L. Duarte and Marcel A.M. Hendrix
Eindhoven University of Technology
Email: t.gerrits@tue.nl

Abstract—A novel energy efficient power amplifier designed to drive an inductive load is presented in this paper. In this power amplifier the standard Class-E topology is extended towards a Push-Pull configuration with frequency tripling. By tuning the load network to the third harmonic of the switching frequency, gate driving losses have been decreased. Opportunities and restrictions related to the fundamental change in operation of the amplifier are clarified. Calculations and simulation results are shown as well as experimental results. Furthermore a circuit is presented to further reduce the required power of the gate drive circuit.

I. INTRODUCTION

The Class-E amplifier is a resonant converter that becomes increasingly valuable as a high frequency solid state power converter in both its dc-to-ac (inverter), and dc-to-dc (voltage converter) configuration. This is due to its simple design and high efficiency. In this framework a Class-E Power Amplifier (PA) embedded in a Push-Pull (PP) configuration is designed, aiming to provide 300 Watts of power to an inductively coupled lamp bulb. Around the output frequency (f_o) of 13.56 MHz, the lamp bulb electric equivalent circuit consists of a series connection of an inductor ($L_{load} = 2.2 \mu H$), and a resistor ($R_{load} = 11 \Omega$).

The Class-E switching mode tuned PA was first introduced in [1], the PP configuration of the Class-E PA was first mentioned in [2]. A variation on this design was previously presented [3] to reduce the higher harmonic content in the load compared to the conventional Class-E. A symmetrical load network arrangement of one inductor and one capacitor, thereby further reducing the total number of used components, was proposed in [3].

Previously implemented Class-E PAs, of comparable output power and with the same output frequency (f_o) of 13.56 MHz, can be found in [4], [5] and [6]. In [4] a 400 Watt PA is presented which has an efficiency (η) of 84% and a peak voltage across the MOSFET (\hat{v}_{ds}) of 362 Volt. For this design an input power of 22 Watts is needed to drive the gate of the MOSFET. In [5] and [6], a 1 KW PA is implemented with an η of 85 and 86% respectively. When delivering 300 Watts of power these PAs have an η of 85 and 95% respectively. The remark that needs to be made here is that all three amplifiers were designed for a 50 Ω load impedance, which is substantially higher than the 11 Ω required in this application, resulting in lower currents and therefore a higher η . Moreover, the design in [6] excludes the required power to drive the gate

in the η calculation, thereby resulting in a very high η (95%) at low power levels. In [5] the required gate driving power is 45 Watts. This high number is due to the combination of a large gate capacitance, 15 V gate voltage and the high switching frequency (f_{sw}). To avoid losses of this magnitude in the gate driver, this paper proposes a combination of two solutions i.e. third harmonic filtering and resonant gate driving.

Intentionally filtering out one higher harmonic of f_{sw} in the load network has not yet been tried in a conventional Class-E PA. Looking at the design assumptions stated in [1], this is because the Radio Frequency Choke (RFC) feed inductor is chosen sufficiently large to act as a source of substantially constant current. In the Class-D topology this principle has been used before [7]; but no power loss reduction in comparison to base harmonic operation is stated.

Various resonant gate driving circuits have been presented in the last decade [8]–[11]. All these circuits aim to completely recover the energy stored in the input capacitance (C_{iss}) when turning the MOSFET off. Ideally it is possible to operate the resonant gate driver circuit without losses i.e. with a balanced energy exchange mechanism between the gate of the MOSFET and a passive circuit. Main differences between the reported gate drive topologies are the number of active components, their switching sequences, and the way in which the recovered energy is managed.

The design of the proposed PA has been changed significantly in comparison to the conventional Class-E. This PA delivers a High Frequency (HF) voltage to the load and it does this with the switches operated at one-third of the resonant load frequency, i.e. 4.52 MHz (f_{sw}), to reduce the switching losses. An extra feature to further reduce the power consumption of the amplifier is the charge exchange mechanism with which the gates of the MOSFETs are driven. The opportunities and restrictions in comparison with conventional Class-E amplifiers will be explained and experimental results are presented.

II. CONVERTER DESIGN

In order to find the optimal converter for this specific application, other resonant converter topologies (Class-D [12], F [13], and E/F [14]) were also investigated. To be able to determine which topology is most suitable, the filtering capability, or Quality factor (Q) of the load itself must be clarified first. For the given combination of L_{load} and R_{load} ,

Q can be calculated with:

$$Q = \frac{P_{stored}}{P_{dissipated}} = \frac{I^2 X}{I^2 R} = \frac{2\pi f_o L_{load}}{R_{load}} = 17. \quad (1)$$

From (1) the conclusion can be drawn that this load circuit has excellent filtering properties. The Class-E configuration is thought to be the best solution for the given load specification, as a result of that. The motivations for this choice will be explained in the following.

The Class-E tuning approach has been designed as a time-domain technique with the active device treated as an ideal switch: assume an open circuit during the off state and a perfect short during the on state. The basic Single Stage (SS) Class-E topology and its optimal waveforms are depicted in Fig. 1a. To make a time-domain analysis of the circuit possible,

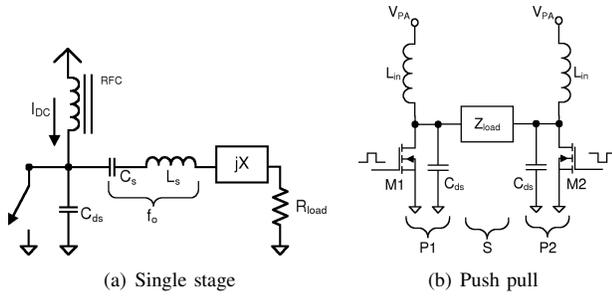


Fig. 1. Class-E amplifier topologies.

restrictions on the waveforms have to be made according to [1]. An amplifier with a switch and a resonant load network which meets these criteria is called *Optimum Class-E*. The cited criteria can be translated to a set of equations:

$$v_{ds}(t) |_{t=kT} = 0, \quad (2)$$

$$\frac{dv_{ds}(t)}{dt} |_{t=kT} = 0. \quad (3)$$

Where $T = 1/f_{sw}$ is the duration of one period, k is an integer, and $v_{ds}(t)$ is the drain to source voltage across the switch. The second term (3) ensures that the drain current, $i_d(t)$ is equal to zero at switch on since the drain source capacitance (C_{ds} , Fig. 1) has been fully discharged by then. Analysis of the Class-E PA based on this set of assumptions is done in many papers, e.g., [2], [15]–[17] and has been expanded for analysis considering a finite input inductor [18], [19]. Main problem using these design procedures is that they are only valid for base harmonic tuning because of (3). If e.g. the optimum Class-E PA of [18] is switched at 1/3 of the designated frequency, the voltage across the ideal switch starts to resonate at f_o (Fig. 1) depending on the combination of components in the load circuit. This leads to negative voltages across the switch, which is not possible when a MOSFET is used. As a result of this, the PA cannot operate in optimal mode, and is therefore called *Suboptimal Class-E*.

A. The Push-Pull Configuration

The PP configuration (Fig. 1b) is chosen for this application for multiple reasons from which filtering is the most important one. By switching the legs of the PA alternating with a duty-ratio $D = 0.5$ and a phase difference between the two legs (ϕ) of π , all the even harmonics of (f_{sw}) generated by M1 will be canceled out by the same signal generated in M2 due to its anti-phase. MOSFET conduction loss, and the resulting thermal stress problems are the second reason to choose for PP. The desired output power of 300 W in combination with an aimed efficiency around 90% means 33 W of loss in total. Given a passive cooling mechanism, distributing losses over more than one switch is desirable.

In the PP circuit there are three resonant circuits that determine the behaviour of the circuit, namely the parallel resonances in the two legs (P1 and P2) and the series load resonance (S), as indicated in Fig. 1b. An extra difficulty is the non linear output capacitance of the MOSFETs in P1 and P2. Therefore the total C_{ds} is first determined using an ideal switch, and will be replaced with a MOSFET model and fixed value capacitors to minimize the non linearity influence.

To make third harmonic tuning possible, a few changes to the general Class-E have to be made. The first change is that the input inductors (L_{in} , Fig. 1b) must allow the current from the DC-supply to contain the base harmonic and especially the third harmonic of f_{sw} . Another parameter that needs to be accurately determined is the shunt capacitor (C_{ds}), which has to resonate with L_{in} and the load network at f_o during the off state. Finally, in order to guarantee subresonant operation, L_x should represent a substantial part of L_{load} . At the same time a suitable value for C_{ds} and L_f is required to maximize the third harmonic content, to reduce the peak voltage across the MOSFET (\hat{v}_{ds}), to maximize η , and to minimize the non linear effect of the output capacitance of the MOSFET (C_{oss}). In the following simulations an optimum for these arguments is found and the final PP amplifier is tested.

B. Model Analysis and Simulations

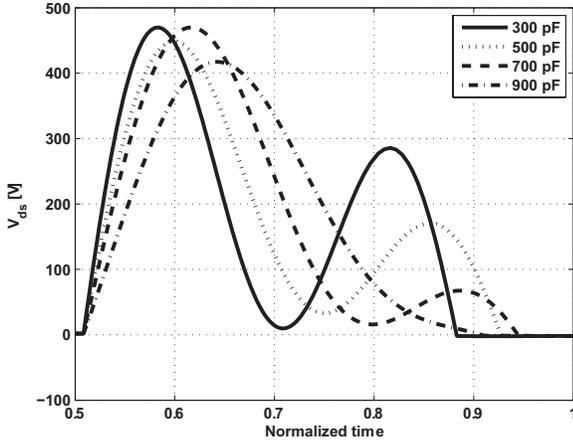
To determine the optimal component combination, first an ideal switch (on resistance, $R_{ds(on)} = 100 \text{ m}\Omega$) with a fixed capacitance in parallel and a diode anti-parallel (forward voltage, $v_{fwd} = 1 \text{ V}$) to it are used. To ensure a sufficiently high lifetime of the MOSFET, the maximum allowed peak voltage across the switch is set to 75% of the maximum voltage across the MOSFET ($\hat{v}_{ds} = 450 \text{ V}$ for a 600 V device). During the simulations a variable supply voltage (V_{pa} , Fig. 3) is used as indicated in Tab. I. Various combinations of L_{in} , C_{ds} and L_x are used, to determine which combination results in the maximum efficiency. Because of the already high Q of the load network (1), the series capacitance (C_s) is increased and the inductance ($L_{load} = L_s + L_x$ Fig. 1a) is kept constant. This gives the same result as using an additional inductor L_x , i.e. a subresonant load network.

The optimum combinations of L_{in} , C_{ds} and C_s when using an ideal switch are depicted in Tab. I, the simulated gate drive

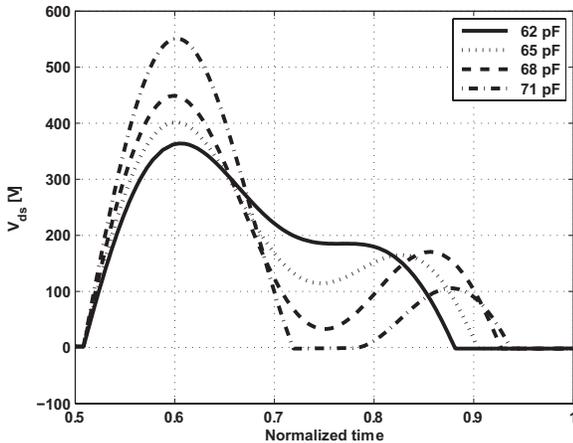
losses (Sec. III, 3.4 W in total) are taken into account here. Simulations using higher values for L_{in} are also carried out to reduce the input currents (i_1 & i_2 , Fig. 3) but this resulted in too high values for \hat{v}_{ds} . The results shown in Tab. I are obtained without the ESR losses of the various components, these are added in Sec. II-D.

TABLE I
EFFICIENCY AS FUNCTION OF BEST COMPONENT COMBINATIONS

L_{in} [nH]	C_{ds} [pF]	C_s [pF]	V_{pa} [V]	\hat{V}_{ds} [V]	η [%]
550	500	65	90	443	96
550	700	65	99	450	96.3
550	500	68	80	440	96.3
550	700	68	75	450	97



(a) $L_{in} = 550$ nH and $C_s = 68$ pF, C_{ds} as indicated



(b) $L_{in} = 550$ nH and $C_{ds} = 500$ pF, C_s as indicated

Fig. 2. Waveforms of v_{ds} for indicated values of L_{in} , C_{ds} and C_s .

In Fig. 2, V_{pa} is fixed to 80 V to illustrate the difference in response and peak voltage. From Fig. 2a it becomes clear that only for a high C_{ds} the derivative of the voltage goes to

zero, which is an optimal Class-E demand. A disadvantage is that the third harmonic of the switching frequency is relatively small in this situation, resulting in a lower efficiency than a waveform which does not satisfy this demand. From this it can be concluded that this requirement is incompatible when tuning for frequency tripling. The high Q of the load network is clearly visible in figure 2b, a small difference in C_s results in a different response.

From table I it can be concluded that for this situation the combination of $L_{in} = 550$ nH $C_{ds} = 700$ pF and $C_s = 68$ pF is the most efficient solution satisfying all demands.

C. Component Selection

Due to the strict requirements, an extensive selection for all components is carried out. For the MOSFET, the most important are the channel resistance ($R_{ds(on)}$), the C_{iss} and with it the dynamic characteristics, and the already mentioned \hat{v}_{ds} . Furthermore should the C_{oss} be as low as possible, but certainly smaller than the required total C_{ds} . The capacitors used are mainly selected on HF losses (ESR), low capacitance variation between devices and as a function of temperature due its COG dielectric, and allowed terminal voltage. To spread the current and reduce the ESR, each of these capacitors are build up out of paralleled capacitors. Due to the high voltage across C_s and v_{ds} , also multiple devices are placed in series. For the additional buffer capacitor (C_{PA} Fig. 3) the ESR at f_o is crucial, as well as the allowed voltage. The inductor requirements are explained in Sec. IV An overview of the selected components is shown in Tab. II, and correspond to Fig. 3. The mentioned ESR is the actually measured resistance at f_o of the full set of components representing the corresponding device. Now that all the passive components are set and a suitable MOSFET has been chosen, the behaviour of the circuit can be compared to the ideal switch situation.

TABLE II
PA COMPONENT KEY PARAMETERS

Component	Type nr.	Key parameters
M_1, M_2	ST26NM60 [20]	$C_{oss} = 165$ pF, $R_{ds(on)} = 125$ m Ω
C_s	Murata ERB	500 V ESR = 140 m Ω
$C_{ds(fix)}$	Murata ERB	500 V ESR = 30 m Ω
C_{PA}	Yageo Class1 NPO	100 V 18 nF, 6 parallel ESR = 10 m Ω

D. Topology Efficiency Comparison

The total setup of the PP amplifier is simulated to verify if the circuit works as intended. A model with all the loss mechanisms is made to determine the efficiency of the full converter. The total schematic with all components and their ESRs is depicted in Fig. 3. In this research a first order intrinsic MOSFET model with non linear capacitors is used. A MOS tool [21] is used to model the device for simulations. From first simulations with the selected MOSFET and passive components, \hat{v}_{ds} exceeded the demand, and C_{ds} is therefore lowered to 600 pF. From its data sheet [20] it can be found that the C_{oss} of the device is approximately 165 pF for

$\bar{v}_{ds} = V_{pa}/(1 - D) = 154$ V during the off state. With an optimal total C_{ds} of 600 pF, the additional fixed capacitance ($C_{ds(fix)}$) must be 435 pF. Small variations in $C_{ds(fix)1,2}$ are required to compensate the variations of the build inductors L_{in1} and L_{in2} (Sec. IV), their values are $C_{ds(fix)1} = 445$ pF and $C_{ds(fix)2} = 439$ pF. The efficiency and absolute losses of the proposed solution are summarized and compared to base harmonic tuned Class-E in Tab. III. From these results it can be

TABLE III
POWER LOSS COMPARISON WITH BUILD 13.56 MHz BASE HARMONIC TUNING CONFIGURATIONS

Section	Proposed solution	Davis <i>et al.</i> [4]	Vania [5]
Loss	$P_o = 300$ W $R_{load} = 11 \Omega$	$P_o = 400$ W $R_{load} = 50 \Omega$	$P_o = 1$ kW $R_{load} = 50 \Omega$
Gate Driver	5 W, Sec. V	22 W	45 W
percentage	13 %	28 %	20 %
MOS conduction	10 W	30 W	65 W
percentage	26 %	39 %	28 %
MOS switching	8 W	14 W	112 W
percentage	21 %	18 %	49 %
ESR	15 W	12 W	8 W
percentage	40 %	15 %	3 %
Absolute loss	38 W	78 W	230 W
Efficiency	89 %	84 %	81 %

concluded that the proposed solution has an overall increased efficiency, which is mainly due to the lower gate driver and MOS switching losses. The main disadvantage is the increase in ESR losses due to the use of high voltage components, in combination with a higher relative RMS input current.

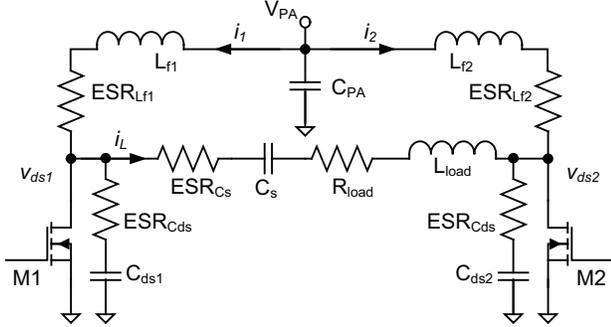


Fig. 3. Total PP Class-E PA with ESR of passive components.

The waveforms of the simulated PA are shown in Fig. 4. The voltage across MOSFET M_1 (v_{ds1}) shows a small deviation from the ideal switch simulations, which is due to the non linear behaviour, and delays by the dynamic properties of the device. The current through the load (i_L) demonstrates clearly that f_o is present in the output, the RMS value of i_L (I_L) is 5.2 A. The simulated RMS input currents ($I_1 = I_2$) are 6.7 A each in this setup, which is relatively high considering that $V_{PA} = 80$ V and $P_o = 300$ W. This value is used to determine the loss of L_{in} in Sec. IV. In Sec. V, these results will be compared to the measurement on the build PA.

III. RESONANT GATE DRIVER

In order to reach the maximum efficiency in a PA, every part of the circuit has to be designed for this purpose. The

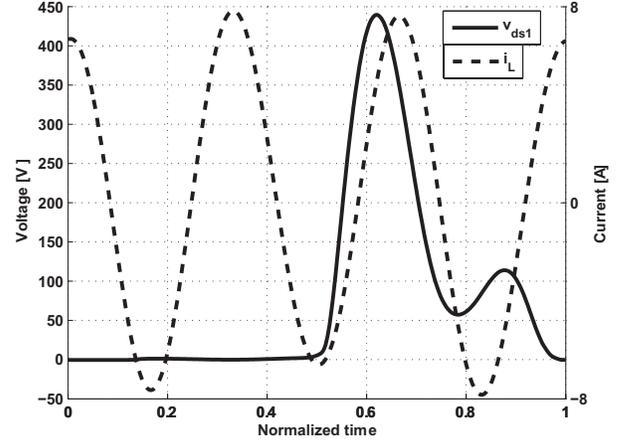


Fig. 4. Waveforms of v_{ds1} across M_1 , and i_L through the load.

power loss generated by the gate drivers can be a significant part of the overall power losses in a PA [5], especially at high frequencies and in case of high input capacitance (C_{iss}) MOSFETs. The Voltage Source Driver (VSD) circuit is popular for its simplicity and low cost. Downside of the circuit is that it is hard switched and that the energy stored in C_{iss} is lost when the device is switched off. The loss mechanisms of in a VSD can be divided in three parts [9]; the hard switching losses of the HB, the losses in the gates M_1 and M_2 and the largest part, the main MOSFET gate losses.

The power loss in the gate the main MOSFET when using a VSD is equal to the product of the gate charge, the gate-drive voltage and the switching frequency as given by

$$P_{gate} = Q_g V_{dc} f_{sw} = C_{iss} V_{dc}^2 f_{sw}. \quad (4)$$

This results in a calculated loss of 3.3 W per MOSFET, using a 26NM50 from ST [20] with a drive voltage (V_{dc}) of 10 V and a gate charge of 73nC (Tab. IV).

The additional power loss due to hard switching is caused by the dissipation of the energy stored in the output capacitances (C_{oss}) of the HB. These losses can be determined using:

$$P_{C_{oss}HB} = 2C_{oss} V_{dc}^2 f_{sw}. \quad (5)$$

The third loss component is caused by the conduction losses through the HB MOSFETs. These losses can be calculated with:

$$P_{R_{ds(on)}HB} = R_{ds(on)M1} I_{dM1}^2 + R_{ds(on)M2} I_{dM2}^2. \quad (6)$$

Resonant gate drivers are a efficient alternative to a conventional VSD to drive power MOSFETs, if properly operated.

In [8] the first effort was made to come up with a so called Resonant Transitions (RT) circuit and in [9] an extensive analysis of the same circuit was performed. The circuit consists of a current source with a HB (Fig. 5a) to switch the direction of the current. The resonant circuit L_{gate} , C_{iss} , is formed only during transitions i.e. when both M_1 and M_2 are off, clarifying the name of the circuit. When the gate is fully charged to V_{dc} ,

M_1 is turned on to provide a low impedance path from the gate to V_{dc} (Fig. 5b). Provided that C_{buf} is large enough, the steady state voltage across $V_{C_{buf}} \approx DV_{dc}$ with an ac ripple depending on the value of C_{buf} and the power drawn per cycle. A disadvantage of this topology is that during $T - 2T_d$ one of

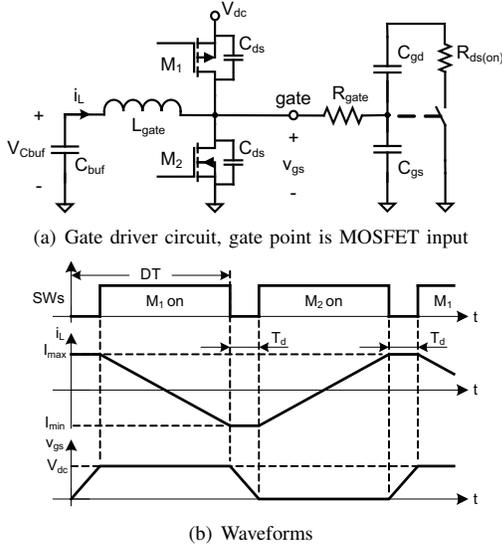


Fig. 5. Resonant transition gate driver [8].

the HB MOSFETs is conducting, decreasing the efficiency. The required inductance to drive the main MOSFET (Tab. IV) can be determined with:

$$L_{gateRT} = \frac{D(1-D)T_d}{2C_{iss}f_{sw}} = 316nH, \quad (7)$$

where the dead time (T_d) has been set to 15% of T to avoid cross conduction through the HB. The maximum current through the inductor (I_{max}) can subsequently be determined using:

$$I_{max} = \frac{D(1-D)V_{dc}T_d}{2L_{gateRT}} = 873mA. \quad (8)$$

In [10] a Passive Clamping Resonant (PCR) gate driving configuration is introduced. The circuit consists of a HB, an inductor as resonant element, and a set of free running anti-parallel diodes. Main difference with the RT circuit is that here the MOSFETs are only turned on for a short period of time to change v_{gs} . The diodes provide a return path for i_L when C_{iss} is charged. Downside of the topology is that the value of the resonant inductance depends on the required rise time for v_{gs} and the gate capacitance of the upper MOSFET (M_1). This results in a low inductance for this application due to the high value of f_{sw} , and with that high RMS losses. The required resonant inductance $L_{gatePCR}$ can be calculated as:

$$L_{gatePCR} = \left(\frac{2T_d}{\pi}\right)^2 \frac{1}{C_{iss}} = 154nH. \quad (9)$$

Simulations on the RT and PCR gate driving topology are carried out to determine the most suitable topology. The key parameters of the used components can be found in Tab. IV.

TABLE IV
RESONANT GATE DRIVER COMPONENT KEY PARAMETERS

Component	Type nr.	Key parameters
Main MOSFET	ST26NM60	$Q_g = 73nC, R_{ds(on)} = 125m\Omega$
P-MOS M_1	Si4532DY-P	$C_{oss} = 180pF, R_{ds(on)} = 62m\Omega$
N-MOS M_2	Si4532DY-N	$C_{oss} = 110pF, R_{ds(on)} = 44m\Omega$
$D_{1,2}$ (PCR)	PMEG2020A	$V_F = 380mV@1A_{pk}$
L_{gateRT}	3615uH33-K	$R_{dc} = 50m\Omega, L = 330nH \pm 10\%$
$L_{gatePCR}$	3615uH15-K	$R_{dc} = 30m\Omega, L = 150nH \pm 10\%$

The RT gate driver circuit with a 330 nH inductor has high Hard Switching (HS) losses due to the slow transitions between V_{dc} and ground. Simulations with lower inductance values for L_{gateRT} , are carried out to find an optimum combination of the lowest RMS and HS losses. The results of this simulation sequence can be found in Tab. V, where also the losses of a VSD are added for comparison. Based on these results a 150 nH inductor should be chosen. The falling edge however, has a discontinuity around the threshold level of the main MOSFET, which could result in duty cycle variation (Fig. 6). The 100 nH inductor is therefore chosen as the best solution. The resistance R_{dc} in Tab. V represents the ESR of that specific inductor. The waveforms of v_{gs} for different inductance values can be found in Fig. 6. The rise (t_{rise}) and fall time (t_{fall}) of v_{gs} with the 100 nH inductor RT gate driver is approximately 16 ns. PCR simulations show 3.8 W of losses when achieving the same t_{rise} & t_{fall} times, due to a $L_{gatePCR}$ of 35 nH. The RT circuit is therefore chosen as the gate driver for this application.

TABLE V
RT GATE DRIVER LOSSES

Inductance [nH]	I_{max} [A]	R_{dc} [mΩ]	P_{loss} [W]
VSD	4.4	0	3.4
50	6.1	14	4.1
80	3.6	20	2.4
100	2.7	27	1.7
150	1.7	30	1.4
220	1.1	35	1.7
330	0.8	50	2.1

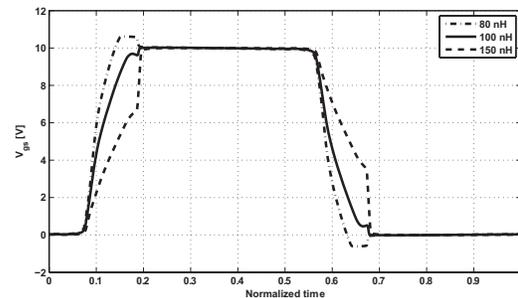


Fig. 6. Waveforms of v_{gs} for L_{gateRT} is 80, 100, 150 nH respectively.

IV. INDUCTOR DESIGN

With efficiency being the most important application requirement, an input inductor has to be developed that contributes

to this goal. The RMS current flowing through the inductors ($I_{1,2}$) is 6.7 A, and has a main frequency component of f_{sw} . Therefore a coil needs to be designed with a low ESR at this frequency. Important choices that have to be made is the type of conductor, whether magnetic material will be used and the shape of the coil and coil-former. The main problems faced when developing a inductor for the designated frequency range are the skin and the proximity-effect.

As can be concluded from the previous, an input inductor must be designed which meets the following demands, sorted by importance for this application:

- 1) The inductance must be 550nH, $\pm 5\%$ allowed deviation.
- 2) The overall loss of the coil must be as low as possible.
- 3) The coil should be as compact as possible.

In order to minimize the skin effect, copper strip of $35\mu\text{m}$ thick and 6.35 mm wide is used. Downside of copper strip is that its very wide so a clever way of winding it must be found, which is presented in [22].

As can be found in [23], a solenoid uses the least space for a coil with a given inductance. But a solenoid does not encapsulate the magnetic field it generates, thus it would have to be placed further away from the rest of the circuit, resulting in extra effective space for the inductor. Another disadvantage is that the two inductors would interfere with each other causing a change in their inductance. To be able to comply with the given demands 1 and 3, a toroid shape is chosen for this application.

Once the shape of the coil is known, the size of the required inductor core should be determined. The basic idea is to comply with demand 3, which means that the maximum outer diameter (d_o) of the coil is 50 mm. The minimum inner diameter (d_i) is set to be 20 mm, to maximize the enclosed surface. The value of d_i is limited by the width of the copper strip in combination with the number of windings (N). The number of windings is set to 7.

The required height for the core can be determined according to [22] with :

$$h = \frac{\pi}{N^2 \ln\left(\frac{d_o}{d_i}\right)} \left[\frac{2L}{\mu_0} - \frac{(d_i + d_o)}{2} \left[\ln\left(8 \frac{d_o + d_i}{d_o - d_i}\right) - 2 \right] \right] \\ = 59\text{mm} \quad (10)$$

where μ_0 is the permeability of free space, and L the required inductance. Two test inductors were first build to verify (10), and from this a compensation factor of 0.712 is calculated. The resulting height of the inductor is 42mm.

The strip length (l_{strip}) resulting from the calculated parameters is 794 mm. The skin depth in copper at f_{sw} is equal to 31 μm , therefore the skin effect can be neglected in this 35 μm thick conductor. The calculated ESR of the strip ($R_{strip/m}$) is equal to 77 $\text{m}\Omega/\text{m}$, the resulting (R_{strip}) for the given l_{strip} should therefore be 61 $\text{m}\Omega$. The measured ESR of a straight piece of copper strip (1 meter) is equal to 173 $\text{m}\Omega$.

The large difference can be a result of impurities in the copper or a deviant thickness, increasing its electrical resistivity. The measured value of R_{strip} is used in the loss comparison of Tab. VI.

Since demand 1 can be satisfied with both a magnetic or air core inductor, a theoretical comparison is made between an air core inductor and two configurations of magnetic material. The aim was to verify which suits demand 2 best and whether the decrease in wire length is sufficient to compensate for the core loss. The magnetic cores used are the T175-2, and T157-6 (Micrometals). The peak AC flux density is denoted by \hat{B}_{ac}

TABLE VI
INDUCTOR LOSS COMPARISON

Core type	L [nH]	N [#]	\hat{B}_{ac} [mT]	P_{core} [W]	l_{strip} [mm]	P_{Cu} [W]	P_{total} [W]
Air	550	7	0.6	-	794	6.2	6.2
T175-2	540	6	6.4	4.6	293	2.3	6.9
T157-6	564	7	7.2	4.3	307	2.4	6.7

and l_{strip} is the length of strip needed to wind the core N times. From Tab. VI it can be concluded that for this combination of parameters an air core coil is the most efficient solution.

To verify the presented theory in practice the inductors are build. To minimize the radiated magnetic field of the inductors one is wound CW and the other CCW. The material used for the toroid coil-former is Delrin, a polymer grade which can withstand temperatures up to 200 °C. A comparison between the theory and the two actually manufactured inductors can be found in Tab. VII. The tested frequency range (Δf) used is that from 3 MHz till 15 MHz. From Tab. VII it can be concluded

TABLE VII
INDUCTOR IN THEORY AND PRACTICE

Inductor	L [nH]	ESR [mΩ]	Q	ΔL [%]	ΔESR [%]	$\frac{\Delta L}{\Delta f}$ [$\frac{\text{pH}}{\text{MHz}}$]	$\frac{\Delta ESR}{\Delta f}$ [$\frac{\text{m}\Omega}{\text{MHz}}$]
Theory	550	139	112				
Inductor I	538	141	108	-2.2	1.4	-125	5.1
Inductor II	545	139	111	-0.9	0	-75	5

that the theoretically determined height (10) results in two inductors with an inductance well within the 5% tolerance stated in demand 1 if the compensation factor is used.

V. EXPERIMENTAL RESULTS

The 13.56 MHz Class-E Push-Pull amplifier is build, Fig. 7 shows the implemented amplifier. The PCB that has been designed is clearly visible as is the passive cooling element on which it is mounted. To be able to adequately cool the main MOSFETs, a window is milled out of the PCB for each of them. The crystal oscillator and dead time control circuitry are placed on the lower left side of the PCB, the PA part including the input inductors designed in Sec. IV can be found in the upper right corner.

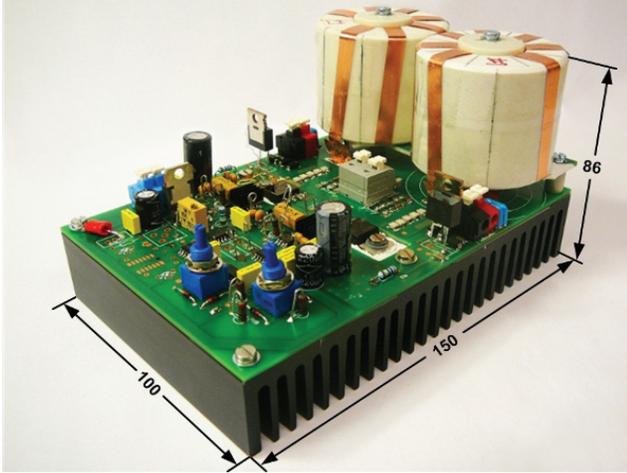


Fig. 7. Implemented power amplifier, dimensions in mm.

A. Resonant Transitions Gate Driver

To verify whether the gate driver operates as intended in Sec. III, measurements are carried out. A picture of v_{gs} of both the RT gate driver waveforms of M_1 (v_{gs1}) and M_2 (v_{gs2}) can be found in Fig. 10. When comparing these waveforms to the simulations it can be concluded that t_{rise} and t_{fall} are approximately 20 ns each, being slightly higher than the predicted value. The voltage however, is not clamped to the supply voltage (V_{dc}) or ground level, this is due to the inductance formed by the piece of PCB track from the HB to the gate of the main MOSFET. The duty cycle of v_{gs1} and v_{gs2} is 46%, being slightly less than intended. To verify if the proposed circuit reaches the calculated power loss reduction of 50%, additional measurements are carried out. The power loss of the RT gate driver is measured over a long period of time (30 min.) to ensure thermal stability. The resulting power needed to drive the main MOSFET is 2.6 W, which is significantly higher than the calculated 1.7 W. To clarify the large difference, the frequency response of the 100nH inductor was measured to verify the data stated in its data sheet. The measured inductance and ESR of the inductor at f_{sw} are 90 nH and 90 m Ω respectively. The decrease in inductance as well as the larger ESR results in a higher RMS current and with it losses in the circuit. With these values an additional simulation was done which resulted in 2.3 W of loss. The additional difference is due to small variations in the gate drive signals of M_1 and M_2 (Fig. 5a). The loss of the VSD is also measured for comparison, with 3.4 W this was the same as the calculated value. The final reduction in power required to drive the ST26NM60, is 24% with the circuit presented here.

B. Power Amplifier

Measurements on the PP PA are carried out. To avoid breakdown of the main MOSFETs during the measurements, a supply voltage (V_{pa}) of 50 V was used during the first measurements. The resulting optimal $C_{ds(fix)1} = 370$ and $C_{ds(fix)2} = 364$ pF were used. The resulting waveforms of

v_{ds1} and v_{ds2} are depicted in Fig. 8, the current through the load network is also shown here, with a RMS value (I_L) of 2.6 A.

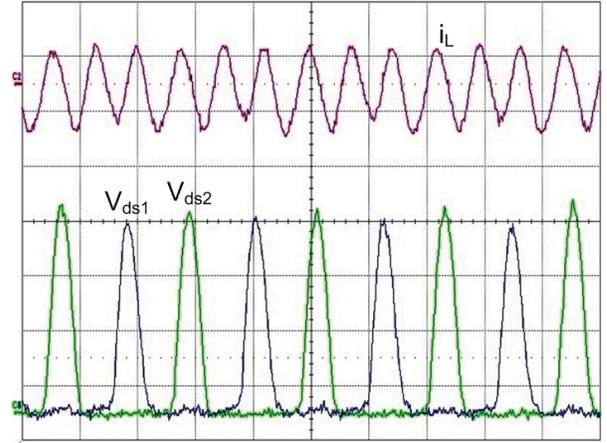


Fig. 8. i_L , v_{ds1} and v_{ds2} , $t = 100\text{ns/div}$, $I = 5 \text{ A/div}$, $V = 100\text{V/div}$.

From Fig. 8 it can be concluded that v_{ds1} and v_{ds2} do not have the required shape. The simulated peak voltage across the MOSFET (\hat{v}_{ds}) should be approximately 280 V in this configuration. In order to get the required power into the load network, the waveforms should have a lower \hat{v}_{ds} with a constant average voltage across the switch i.e. the second peak should be present. Several possible solutions to this problem have been examined. The first idea was to vary $C_{ds(fix)1,2}$ because of the very non linear behaviour of C_{oss} . The second idea was to use a different type of MOSFET, with an even lower C_{oss} in order to decrease its influence. The final idea was to measure and compare the impedance of the two parallel resonance loops (P1 and P2, Fig. 1b). The impedance of the loops was tuned by making small changes in the fixed capacitor values ($C_{ds(fix)1,2}$) and repositioning the input inductors ($L_{in(1,2)}$). The difference in measured frequency sweep impedance response between P1 and P2 before and after the tuning can be found in Fig. 9a and b respectively. The normalized frequency in Fig. 9 is determined by measuring the total parallel impedance response of P1 and P2 together. The frequency corresponding to the maximum impedance point was chosen as the unity frequency.

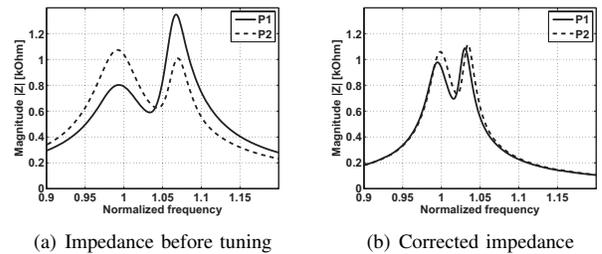


Fig. 9. Impedance of P1 and P2 dependent of the frequency.

The final measurements were carried out using a new type of MOSFET and the improved parallel resonance loops. The MOSFETs used in the final setup were two ST20NM50 devices

with a very low C_{oss} , especially at low v_{ds} values ($C_{oss} \approx 3$ nF at $v_{ds} = 0$ V). These devices have a V_{dss} of 500 V and are therefore only suitable for testing purposes. The used values for $C_{ds(fix)1,2}$ in this setup were 395 and 370 pF respectively, and $V_{pa} = 50$ V. The resulting waveform of v_{ds2} has the intended shape and \hat{v}_{ds} , but v_{ds1} does not (Fig. 10). This is due to a small phase angle error between v_{gs1} and v_{gs2} causing an unbalanced energy distribution in the circuit. No total efficiency measurement was done because the PA did not fully function as intended.

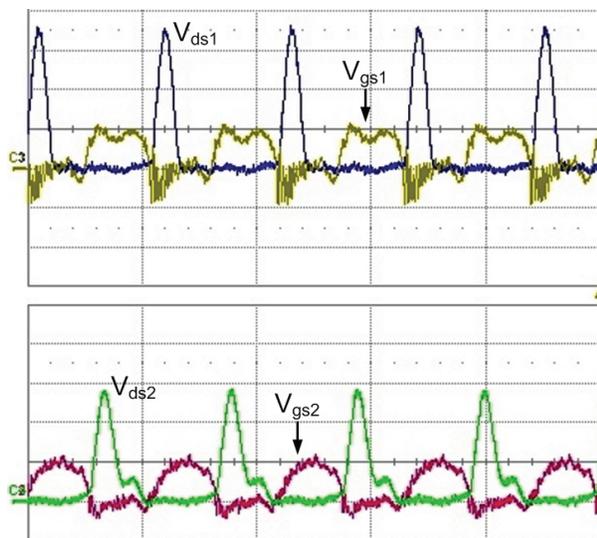


Fig. 10. Waveforms of v_{ds} and v_{gs} of M_1 and M_2 , $t = 200\text{ns/div}$, $v_{gs} = 10$ V/div, $v_{ds} = 100\text{V/div}$.

VI. CONCLUSIONS

In this paper a novel approach for driving a Class-E PA is presented. Simulations on the proposed circuit were performed, and showed that an efficient energy conversion to a high frequency load network is possible. The measurements on the build PA however, show that there are a lot of essential parameters that need to be very accurate and stable. The maximum efficiency bottlenecks in this circuit are mainly the ESR of the air core inductors and C_s . The most critical parameter of the MOSFET is the output capacitance, which is limited by the ideal total drain source capacitor value $C_{ds(fix)}$. The simulated maximum efficiency of 89% is an evident improvement opposing [4]–[6]. The proposed circuit proves to be an efficient solution for HF power conversion, which can be beneficial in future Class-E designs. Less demanding component requirements would moderate the design procedure.

An efficient gate drive circuit is presented. The measured losses are somewhat higher than simulated, but still a significant improvement is shown when compared to [4], [5].

A trustworthy method is presented to design inductors for the low inductance range, aimed to have an as low as possible overall loss. Thicker copper strip should be used to decrease the ESR of the input inductors to an acceptable level.

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