Useful Circuit Theorems

Impedance of a Two-Terminal RC Network

Consider any two-terminal RC network. If the impedance at dc is not infinite, the impedance can be written

$$Z = R_{dc}\frac{1+\tau_z s}{1+\tau_p s}$$

where R_{dc} is the dc resistance of the circuit, τ_o is its open-circuit time constant, and τ_z is its short-circuit time constant.

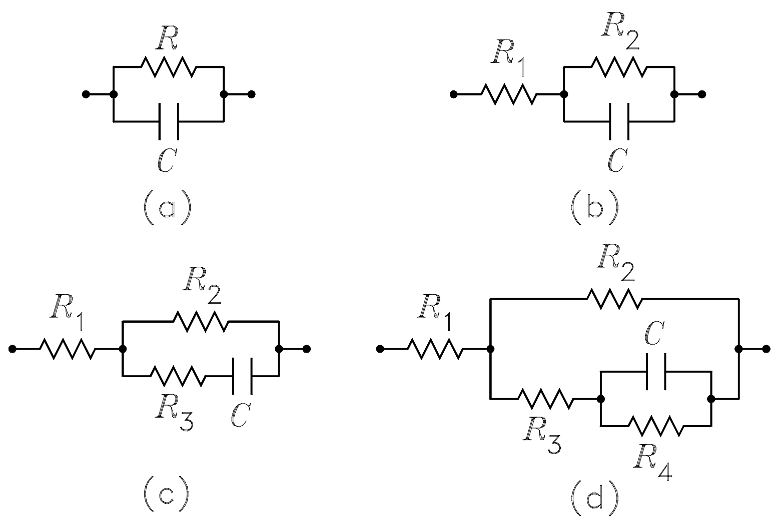

Figure 1: Example two-terminal circuits.

For example applications of the theorem, consider the circuits shown in Fig. 1. In order from (a) to (d), the impedances are given by

$$Z = R\frac{1}{1+RCs}$$

$$Z = (R_1 + R_2)\,\frac{1+R_1\|R_2Cs}{1+R_2Cs}$$

$$Z = (R_1 + R_2)\,\frac{1+(R_1\|R_3+R_2)\,Cs}{1+(R_2+R_3)\,Cs}$$

$$Z = [R_1 + R_2\|\,(R_3+R_4)]\,\frac{1+(R_1\|R_2+R_3)\,\|R_4Cs}{1+(R_2+R_3)\,\|R_4Cs}$$

Although the theorem is strictly valid for circuits containing only one capacitor, it can be applied to circuits containing more than one capacitor if the adjacent poles and zeroes in the transfer function are well removed, preferable by a decade or more. Consider the circuit shown in Fig. 2. Let us assume that C_2 and C_3 are open circuits in the frequency range in which C_1 is active, C_1 is a short circuit and C_3 is an open circuit in the frequency range in which C_2 is active, and C_1 and C_2 are short circuits in the frequency range in which C_3 becomes active.

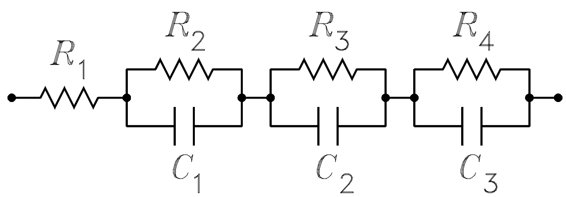

Figure 2: Example circuit containing more than one capaictor.

With the above information, the impedance in the range where C_2 and C_3 are open circuits is given by

$$\begin{aligned} Z_1 &= (R_1 + R_2 + R_3 + R_4)\,\frac{1 + R_2 \| (R_1 + R_3 + R_4)\, C_1 s}{1 + R_2 C_1 s} \\ &= (R_1 + R_2 + R_3 + R_4)\,\frac{1 + s/\omega_2}{1 + s/\omega_1} \end{aligned}$$

where

$$\omega_1 = \frac{1}{R_2 C_1} \qquad \omega_2 = \frac{1}{1 + R_2 \| (R_1 + R_3 + R_4)\, C_1}$$

At low frequencies, Z_1 starts at the value $R_1 + R_2 + R_3 + R_4$ and shelves at high frequencies at the value $R_1 + R_3 + R_4$. The impedance in the range where C_1 is a short circuit and C_3 is an open circuit is given by

$$\begin{aligned} Z_2 &= (R_1 + R_3 + R_4)\,\frac{1 + R_3 \| (R_1 + R_4)\, C_2 s}{1 + R_3 C_2 s} \\ &= (R_1 + R_3 + R_4)\,\frac{1 + s/\omega_4}{1 + s/\omega_3} \end{aligned}$$

where

$$\omega_3 = \frac{1}{R_3 C_2} \qquad \omega_4 = \frac{1}{R_3 \| (R_1 + R_4)\, C_2}$$

At low frequencies, Z_2 starts at the value $R_1 + R_3 + R_4$ and shelves at high frequencies at the value $R_1 + R_4$. The impedance in the range where C_1 and C_2 are short circuits is given by

$$\begin{aligned} Z_3 &= (R_1 + R_4)\,\frac{1 + R_4 \| R_1 C_3 s}{1 + R_4 C_3 s} \\ &= (R_1 + R_4)\,\frac{1 + s/\omega_6}{1 + s/\omega_5} \end{aligned}$$

where

$$\omega_5 = \frac{1}{R_4 C_3} \qquad \omega_6 = \frac{1}{R_4 \| R_1 C_3}$$

At low frequencies, Z_3 starts at the value $R_1 + R_4$ and shelves at high frequencies at the value R_1.

The three impedances can be "pieced" together to obtain the overall impedance to obtain

$$Z = (R_1 + R_2 + R_3 + R_4)\,\frac{(1 + s/\omega_2)\,(1 + s/\omega_4)\,(1 + s/\omega_6)}{(1 + s/\omega_1)\,(1 + s/\omega_3)\,(1 + s/\omega_5)}$$

This expression is strictly if

$$\omega_1 \ll \omega_2 \ll \omega_3 \ll \omega_4 \ll \omega_5 \ll \omega_6$$

The straight-line approximation to the Bode magnitude plot for the impedance is shown in Fig. 3.

The impedance theorem can be used to write by inspection the transfer function of an inverting op-amp circuit where the input and feedback impedances contain no more than one capacitor each. Consider the circuit shown in Figure 4. The voltage gain can be written by inspection to obtain

$$\begin{aligned} \frac{V_2}{V_1} &= -\frac{R_3}{1 + R_3 C_2 s} \div \left[(R_1 + R_2)\,\frac{1 + R_1 \| R_2 C_1 s}{1 + R_2 C_2 s} \right] \\ &= -\frac{R_3}{R_1 + R_2}\,\frac{1 + R_2 C_2 s}{(1 + R_1 \| R_2 C_1 s)\,(1 + R_3 C_2 s)} \end{aligned}$$

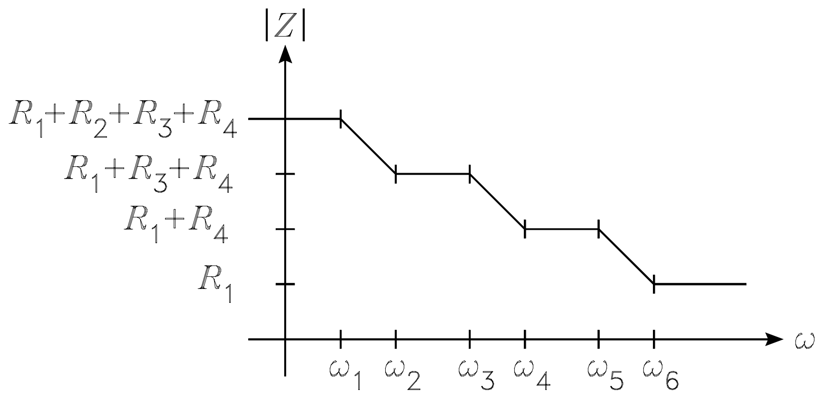

Figure 3: Bode magnitude plot for the impedance Z.

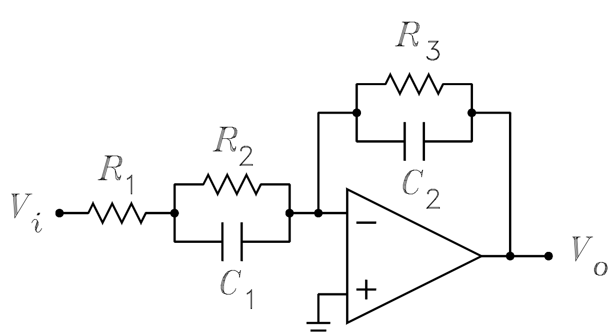

Figure 4: Inverting op-amp example.

Impedance of an RC Voltage-Divider Network

Case 1 – Capacitor in Shunt Arm

Consider the voltage-divider network shown in Fig. 5(a). Let the impedance Z_2 contain one capacitor and satisfies the condition for the two-terminal impedance theorem. By voltage division, the gain of the network is given by

$$\frac{V_2}{V_1} = \frac{Z_2}{R_1 + Z_2} = \frac{Z_2}{Z_3}$$

where $Z_3 = R_1 + Z_2$. The impedance Z_2 can be written

$$Z_2 = R_2 \frac{1 + \tau_{2s} s}{1 + \tau_{2o} s}$$

where τ_{2o} is the open-circuit time constant for Z_2 and τ_{2s} is its short-circuit time constant. The impedance Z_3 can be written

$$Z_3 = (R_1 + R_2) \frac{1 + \tau_{3s} s}{1 + \tau_{3o} s}$$

where τ_{3o} is the open-circuit time constant for Z_3 and τ_{3s} is its short-circuit time constant.

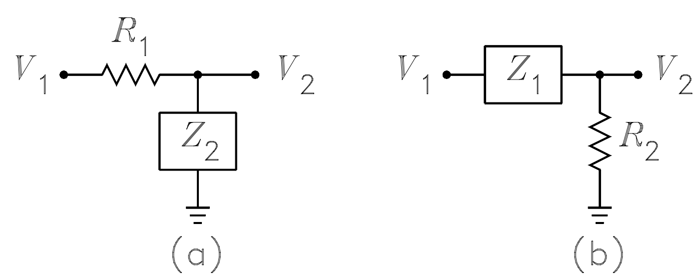

Figure 5: Voltage divider networks containing only one capacitor.

But the open-circuit time constants for Z_2 and Z_3 are the same. Let this be denoted by $\tau_o = \tau_{2o} = \tau_{3o}$. thus the two impedances can be written

$$Z_2 = R_2 \frac{1 + \tau_{2s} s}{1 + \tau_o s}$$

and

$$Z_3 = (R_1 + R_2) \frac{1 + \tau_{3s} s}{1 + \tau_o s}$$

It follows that the gain of the voltage divider is given by

$$\frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2} \frac{1 + \tau_{2s} s}{1 + \tau_{3s} s}$$

Notice that the term $1 + \tau_o s$ is canceled. Note also that the gain constant is the circuit gain at dc, the pole time constant τ_{3s} is the time constant calculated with $V_i = 0$, and the zero time constant τ_{2s} is the time constant with $V_o = 0$.

Case 2 – Capacitor in Series Arm

Now consider the case shown in Fig. 5(b) where Z_1 contains one capacitor and satisfies the condition for the two-terminal impedance theorem. By voltage division, the gain of the network is given by

$$\frac{V_2}{V_1} = \frac{R_2}{Z_1 + R_2} = \frac{R_2}{Z_3}$$

where $Z_3 = Z_1 + R_2$. The impedance Z_3 can be written

$$Z_3 = (R_1 + R_2) \frac{1 + \tau_{3s} s}{1 + \tau_{3o} s}$$

where τ_{3o} is the open-circuit time constant for Z_3 and τ_{3s} is its short-circuit time constant.

It follows that the gain of the voltage divider is given by

$$\frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2} \frac{1 + \tau_{3o} s}{1 + \tau_{3s} s}$$

But the open-circuit time constant for Z_3 is equal to the open-circuit time constant for Z_1, i.e. $\tau_{3o} = \tau_{1o}$. Thus the gain of the circuit can be written

$$\frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2} \frac{1 + \tau_{1o} s}{1 + \tau_{3s} s}$$

Note that the gain constant is the circuit gain at dc, the pole time constant τ_{3s} is the time constant calculated with $V_i = 0$, and the zero time constant τ_{1s} is the time constant with the V_i node floating, i.e. open circuited.

Combined Theorem

We seek to combine the two theorems into one which gives the correct answer for both cases. In the second case, the time constant τ_{1o} is the same as the time constant calculated with $V_o = 0$. Thus it follows that the two theorems can be combined to obtain the general solution

$$\frac{V_2}{V_1} = k_{dc} \frac{1 + \tau_2 s}{1 + \tau_1 s}$$

where k_{dc} is the dc gain, τ_1 is the time constant with $V_1 = 0$, and τ_2 is the time constant with $V_2 = 0$.

As an example, consider the circuit shown in Fig. 6(a). By inspection, the voltage gain can be written

$$\frac{V_2}{V_1} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \frac{1 + (R_2 \| R_3 + R_4)\, Cs}{1 + [(R_1 + R_2) \| R_3 + R_4]\, Cs}$$

The Bode magnitude plot is that of a low-pass shelving function.

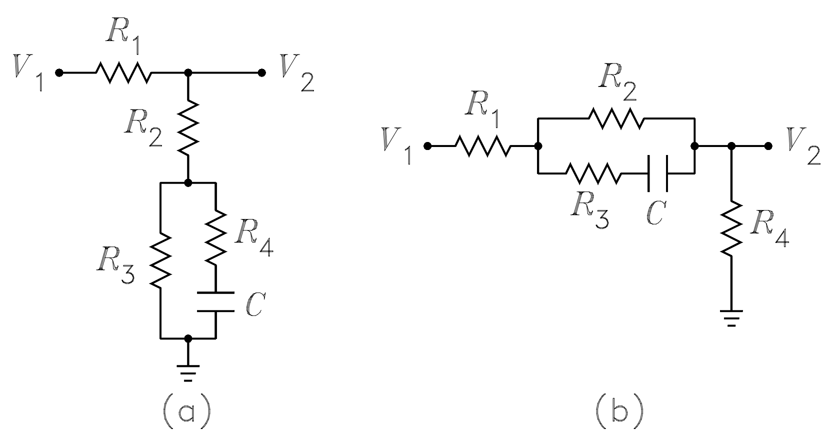

Figure 6: Example circuits for the voltage-divider theorem.

The voltage gain of the circuit in Fig. 6(b) is given by

$$\frac{V_2}{V_1} = \frac{R_4}{R_1 + R_2 + R_4} \frac{1 + (R_2 + R_3)\, Cs}{1 + [(R_1 + R_4) \| R_2 + R_3]\, Cs}$$

The Bode magnitude plot is that of a high-pass shelving function.

The voltage-divider theorem can be used to write the voltage gain expression for a non-inverting op-amp circuit. Consider the circuit shown in Fig. 7. The voltage divider network in Fig. 6(a) is shown connected between the output of the op amp and its inverting input. Because the op amp has negative feedback, there is a virtual short between its + and − inputs. Thus the voltage output of the voltage divider is $V_2 = V_i$ and its voltage input is $V_1 = V_o$. It follows that the voltage gain of the circuit is given by

$$\frac{V_o}{V_i} = \frac{V_1}{V_2} = \left(\frac{V_2}{V_1}\right)^{-1} = \frac{R_1 + R_2 + R_4}{R_4} \frac{1 + [(R_1 + R_4) \| R_2 + R_3] \, Cs}{1 + (R_2 + R_3) \, Cs}$$

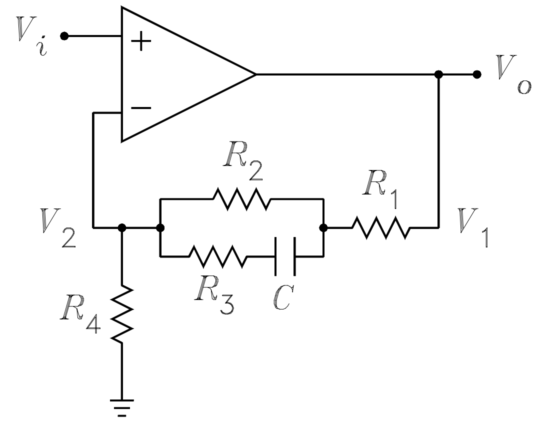

Figure 7: Non-inverting op-amp example.