Design Trade-offs for Switch-Mode Battery Chargers

Jose Formenti and Robert Martinez

ABSTRACT

The design of switching converters as a standalone block is a well-known topic. However, very specific challenges arise when a DC/DC converter is used to charge a battery pack. Understanding the impact of using a battery as a load, and other charger-related system-level details up-front, is a requirement when designing a DC/DC converter targeted at battery-pack charging. Up-front consideration of those issues will enable the designer to incorporate features and functions during the design phase that are not present in common DC/DC converters but that should be included in DC/DC converters targeted at battery charging. This article discusses the most common benefits and challenges faced when using switching converter topologies to charge battery packs, including specific challenges and design tradeoffs faced when using the battery pack as a load.

I. INTRODUCTION

Methods for designing stand-alone switching converters are well-known. However, specific challenges arise when a DC/DC converter is used to charge a battery pack. Understanding up-front the impact of using a battery as a load and other charger-related system-level details enables the designer to incorporate features and functions not present in common DC/DC converters.

This paper discusses the most common benefits and challenges of using switching-converter topologies to charge battery packs. A comparison of distinct switching topologies identifies when each is most advantageous. Subsequent sections focus on buck switching charger design; synchronous versus nonsynchronous operation; power dissipation and switching frequency; the impact of AC adapter voltage range on converter design; MOSFET selection; loop-compensation requirements for battery-pack loads; and safety and fault-protection circuits.

II. CONVERTER TOPOLOGY

A. Overview

There are currently two major topologies used to implement buck converters targeted at battery-pack-charging applications: synchronous and nonsynchronous rectification. These topologies can be implemented with integrated or discrete switching MOSFET devices. The switching devices can be NMOS, PMOS, or a combination of both.

The selection of a specific topology will be dictated by the design boundaries set by the following system requirements:

- Charge-current level
- AC adapter voltage range
- Ambient temperature range
- Converter switching frequency
- Target PCB area
- Availability of system resources dedicated to power-management functions

Sections B and C discuss the most common synchronous and nonsynchronous topologies.

B. Basic Buck-Converter Topologies and High-Side FET Selection

Nonsynchronous buck converters represent one of the earliest implementations of switching regulators; a simplified circuit for a nonsynchronous buck converter is shown in Fig. 1. A single switch (S1) is

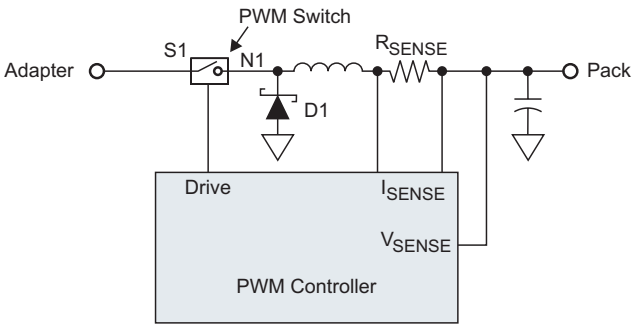

Fig. 1. Simplified nonsynchronous topology.

closed during a time (t_{ON}) connecting the AC adapter voltage to the inductor. When the switch opens during the off time (t_{OFF}), a free-wheeling diode (D1) holds the voltage at a node (N1) while providing a path for inductor (charge) current. The duty cycle is set by internal control circuits and regulation loops that monitor the pack voltage and pack charge current.

The control loops are configured to limit either the charge current or the charge voltage to a programmed value. This scheme enables control of the charge current when the battery voltage is below the target charge voltage, or control of the charge voltage when the battery voltage reaches the regulation voltage (see Fig. 2).

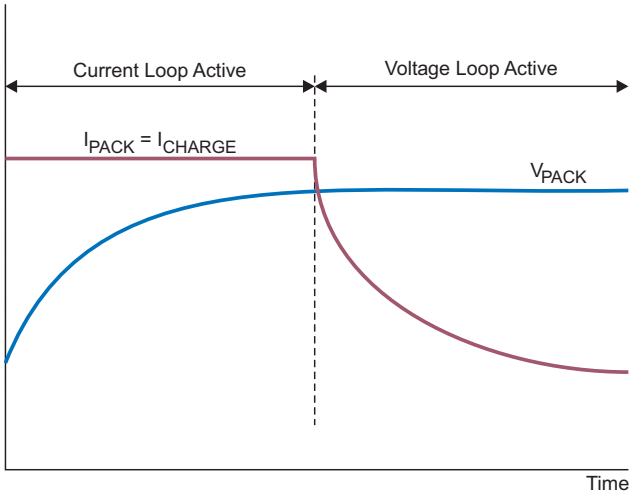

Fig. 2. Typical charge cycle.

The high-side power MOSFET selection will influence and sometimes dictate key charging parameters such as the maximum possible charge current, maximum frequency, minimum number of output filter components, and cost. The two obvious choices are either NMOS or PMOS FETs (see Fig. 3). Each has its own advantages, disadvantages, and proper application.

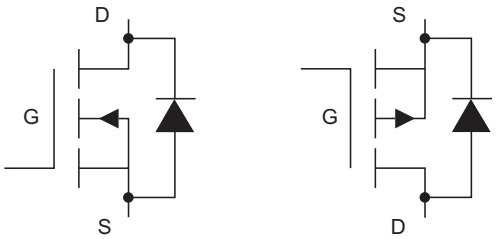

Fig. 3. NMOS FET (left) and PMOS FET.

Typically the NMOS devices have the advantage of a lower $R_{DS(ON)}$ for the same package; thus either more load current can be used or the cost can be lower. Another way to look at it is that, for the same $R_{DS(ON)}$, the die size can be smaller; thus the total gate charge of a discrete NMOS typically can be lower than that of a discrete PMOS. The lower gate charge lowers the switching losses, allowing a higher switching frequency and lowering the output filter inductor and capacitor requirements. The disadvantage of an NMOS on the high side is that turning it on requires a method to drive the gate with a voltage higher than the input voltage. The voltage also must be maintained below the maximum gate-to-source voltage rating of the device. For PMOS high-side FETs, turn-on of the FETs is simplified because the gate voltage needs to be lower than the input voltage by at least 5 V instead of higher. Devices with a lower voltage rating can be used, and the only requirement is that the lower voltage rail be provided.

For most implementations where the power MOSFETS are discrete parts external to the control IC, the preferred MOSFET to use is the NMOS to lower system cost and to have high performance with high efficiency.

For implementations where the power MOSFETs are integrated within the control IC, the PMOS is usually preferred over the NMOS because of its ease of implementation and also because the PMOS/NMOS area trade-off favors the PMOS in integrated MOSFETs (see Fig. 4). Discrete devices typically have a 2:1 trade-off,

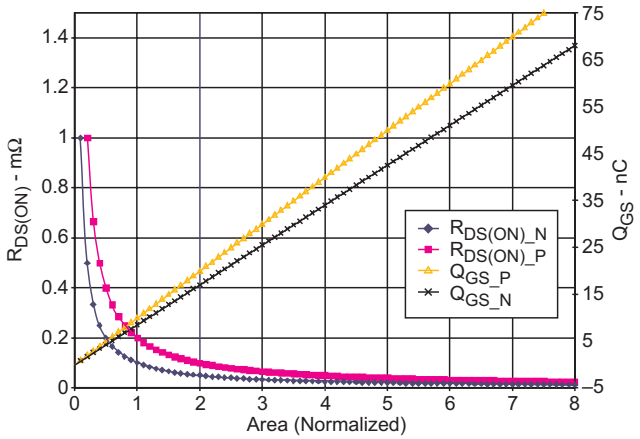

Fig. 4. $R_{DS(ON)}$ and Q_{GS} versus area for NMOS and PMOS FETs.

whereas integrated lateral devices may have a 1.4:1 trade-off. This is typically offset by the gate-drive requirements of the NMOS implementation. Total gate charge also is typically much smaller in an integrated lateral device, allowing the increase in gate charge for the larger-area PMOS implementation with little effect on total power losses.

C. Nonsynchronous and Synchronous Topologies

Nonsynchronous Topologies

Nonsynchronous topologies enable designs that simplify controller architecture and system-side power-management functions. To minimize system cost, less complex controllers designed to drive external PMOS devices are the preferred choice for nonsynchronous buck-charger stages. The selection of PMOS switching devices enables the use of a very simple driver architecture for the power stage on the controller, switching gate-voltage levels between adapter voltage and ground. More sophisticated designs that require higher efficiency or operation at higher voltages have dedicated circuits to clamp the gate-driver low level to a fixed value as shown in Fig. 5, minimizing switching losses and preventing MOSFET device damage from gate-oxide breakdown. The clamp circuit is usually a low-accuracy regulator that uses an external tank capacitor to handle the current peak pulses that occur during MOSFET switching. Another advantage of the PMOS is that the duty cycle can be kept indefinitely at 100%.

The use of a free-wheeling diode implements a topology that intrinsically has no problems with cross-conduction on the power stage during switching; it also eliminates any stray paths from battery pack to ground when the high-side switch is off (see Fig. 6). As a result there is no need for the complex system power-management functions usually required when cross-conduction and battery-pack leakage paths are present.

The downside of nonsynchronous topologies is their power dissipation. With proper PCB thermal design and proper selection of PWM power-stage components, nonsynchronous topologies typically can be used to charge battery packs with maximum

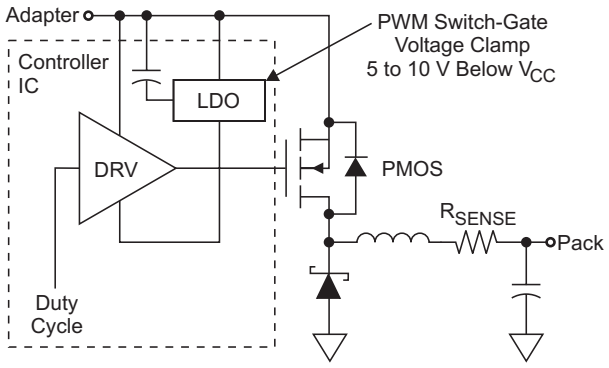

Fig. 5. High-side-driver voltage clamp.

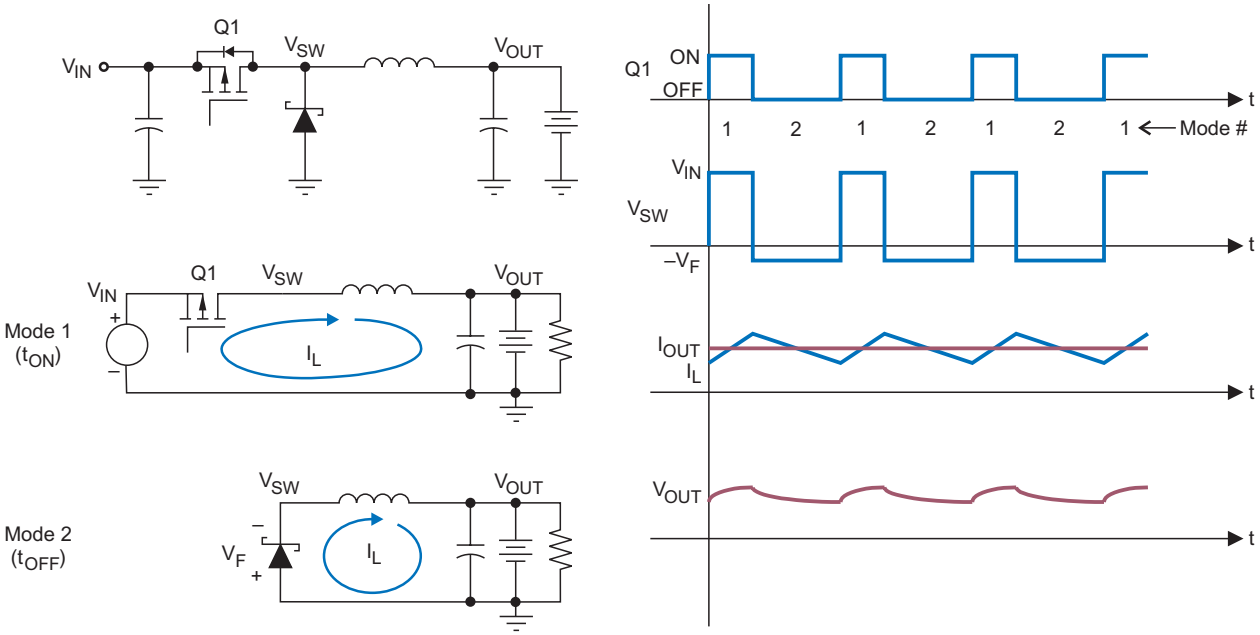

Fig. 6. Modes of operation and waveforms for an nonsynchronous buck converter.

charge-current rates in the 3- to 4-A range. The power dissipation for nonsynchronous topologies occurs in the switching device, the free-wheeling diode, and the driver. Power losses on the free-wheeling diode effectively limit the maximum charge current to values significantly lower than those in synchronous topologies.

Synchronous Topologies

Synchronous DC/DC converters are a logical choice for application conditions where the nonsynchronous topologies do not meet power dissipation and efficiency requirements. Synchronous converters typically cost more because additional components are required and the controller is more complex. There are two basic topologies commonly used for synchronous DC/DC converters; both of them use a low-side NMOS switch to minimize losses on the free-wheeling diode. The high-side switch can be either PMOS or NMOS.

Fig. 7 shows a simplified diagram for a synchronous converter with a PMOS high-side switch. This configuration improves the overall efficiency as compared to the nonsynchronous solution, while still enabling use of a simple gate driver for the high-side switch.

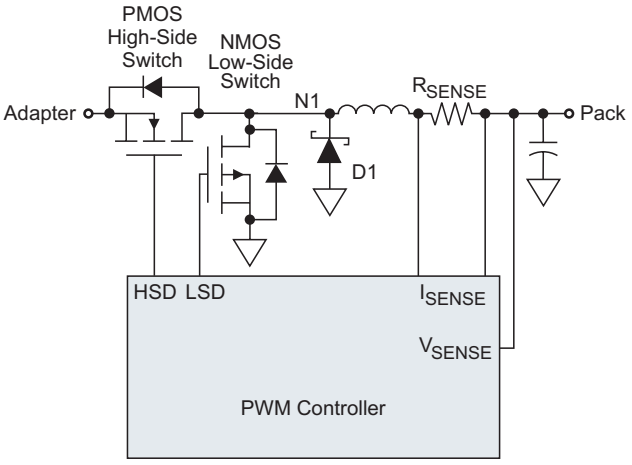

Fig. 7. Synchronous topology with a PMOS high-side switch.

The synchronous operation of the high/low-side switches impacts controller complexity. To avoid shoot-through currents during switching, a break-before-make logic function must be added to ensure that the switches are never on at the same time. Usually a dead time is built in to guarantee that no cross-conduction happens; a Schottky free-wheeling diode is required to hold the node N1 voltage during the dead time (see Fig. 8).

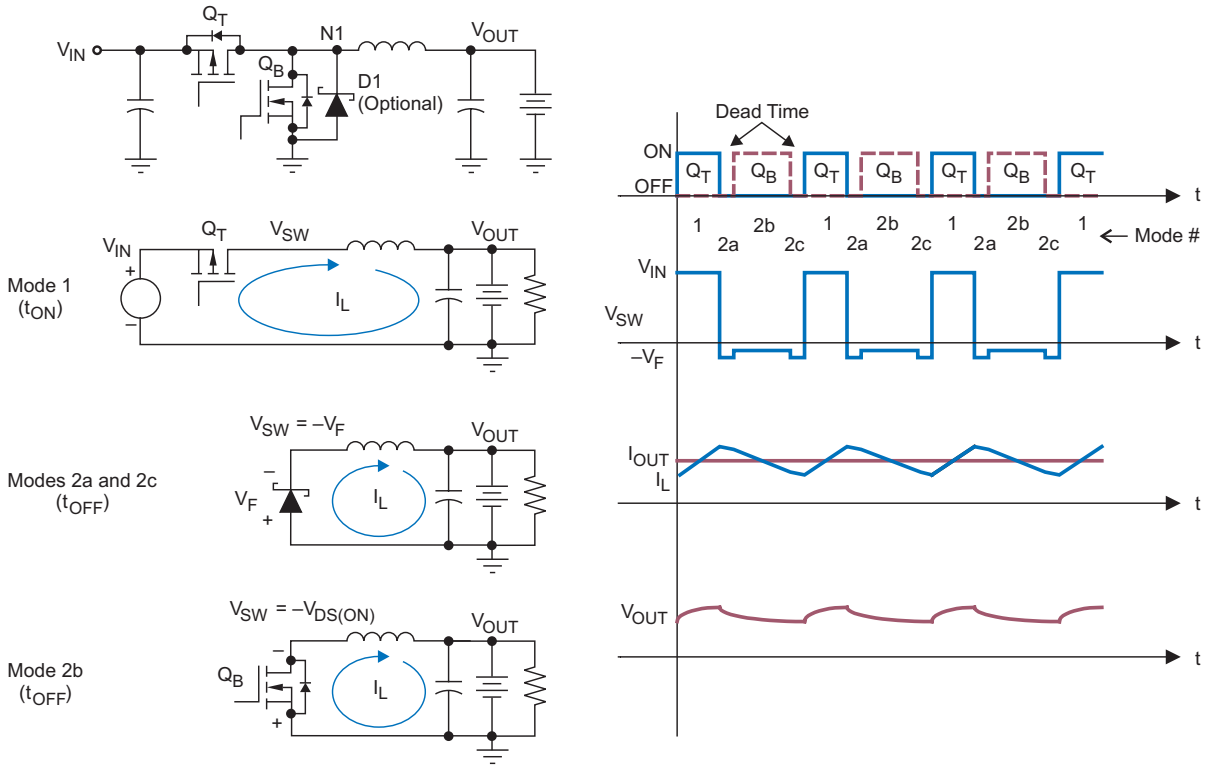

Fig. 8. Modes of operation and waveforms for a synchronous buck converter.

The main impact of implementing a synchronous topology is that additional functionality must be added to the PWM controller. In addition to the break-before-make circuit, a new gate driver for the low-side switch is needed; this in turn requires a new LDO and tank capacitor to enable operation of the low-side switch driver at high voltages with minimal switching losses (see Fig. 9).

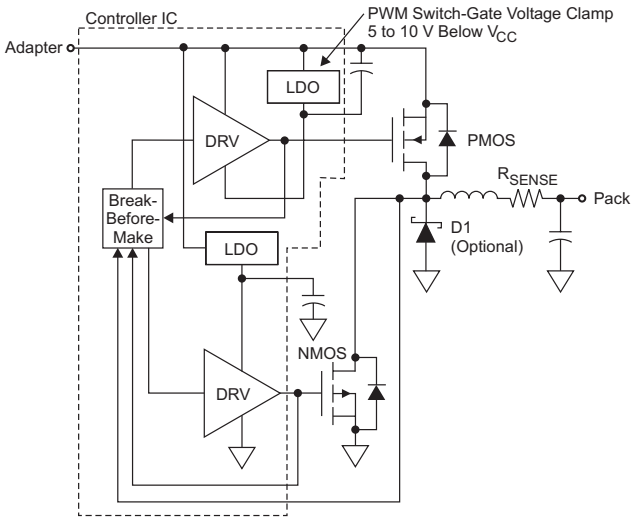

Fig. 9. Driver topology for synchronous PMOS/NMOS topology.

To avoid shoot-through currents during PMOS switch activation (the PMOS drain goes from ground to adapter voltage), the low-side driver must be dimensioned to hold the low-side switch gate close to ground while the drain/gate capacitor for the low-side switch is being charged. This can be accomplished by designing the low-side switch driver so that the off-state $R_{DS(ON)}$ is lower than the high-side switch on-state $R_{DS(ON)}$.

Even though the PMOS/NMOS synchronous topology represents an improvement over the nonsynchronous topology, a few limitations still are present. The most important is that the synchronous PWM can't be run at very high frequencies due to the typically high gate-charge values for PMOS devices and the power-dissipation constraints on the PWM controller IC. This prevents the use of a smaller inductor. Also note that PMOS switches cost more than NMOS switches with the same voltage/current ratings.

This limitation can be overcome by using an NMOS/NMOS topology. Similar to the non-synchronous/synchronous transition previously discussed, new circuitry must be added to the controller because an NMOS/NMOS synchronous converter requires driving the high-side switch gate to voltage levels above the adapter voltage. This can be done in any of three ways:

1. Use a separate, external gate-drive supply rail that is higher than the input voltage rail by at least 5 V.
2. Use a charge pump to generate the higher gate-drive supply rail. This requires three capacitors and four high-frequency switching FETs, or two high-frequency switching FETs and two Schottky diodes.
3. Use a bootstrap circuit to provide the required gate-drive voltage from a 5-V external rail every cycle. This requires the 5-V supply, a Schottky diode, and a capacitor.

The preferred method is usually the bootstrap circuit because it does not require a higher voltage rail and is usually the simplest to implement. The disadvantage is that it requires extra components, and they need to be rated at higher voltage than the input voltage. Another disadvantage is that the bootstrap capacitor needs to replenish its charge loss due to switching and leakage currents within the IC and the Schottky diode. This prevents leaving the high-side FET fully on at a 100% duty cycle for long periods of time. A periodic recharge pulse providing a 99.9x% duty cycle is required.

The other two methods, using a higher voltage rail or a charge pump, do allow an indefinite 100% duty cycle to be maintained; but in most cases, durations of < 1% are not required when traded off with the expense of more complex circuitry, more components, bigger size, and more internal noise.

A simplified schematic for an NMOS/NMOS topology is shown in Fig. 10. This commonly used solution implements a bootstrap circuit with an external capacitor and a regulated voltage generated by the controller IC.

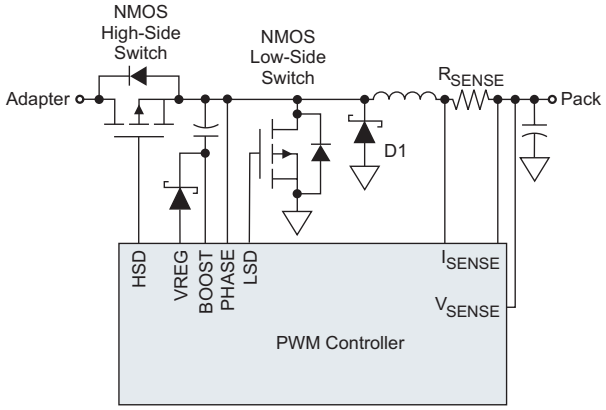

Fig. 10. NMOS/NMOS synchronous topology.

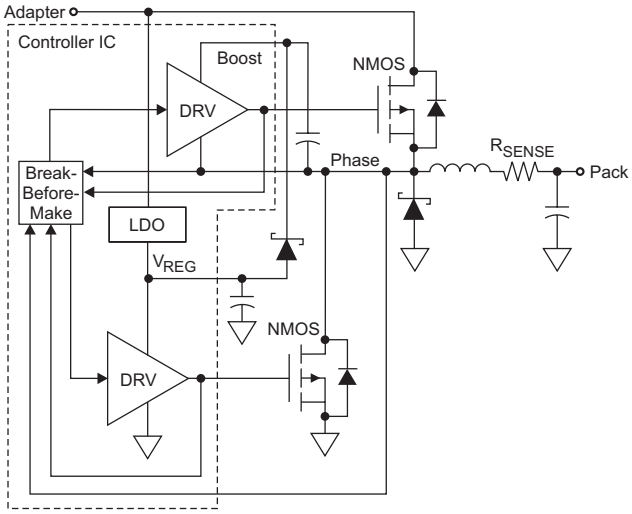

Fig. 11. Driver topology for synchronous NMOS/NMOS topology.

The controller drivers also have to be modified to enable use of an NMOS/NMOS topology; Fig. 11 is a simplified diagram of commonly used driver topologies. Note that in this configuration the high-side switch driver is driven between boost and phase nodes; the bootstrap capacitor is recharged with the low-side driver supply regulator to optimize controller design. The break-before-make circuit also needs to be modified to sense the high-side voltage gate levels accordingly.

III. Power Dissipation and Size versus Switching Frequency

For most chargers the input supply is off the AC adapter; thus low-load efficiency as a battery input supply is not a key concern. Instead, high current efficiency is important for lower thermal dissipation and to obtain maximum charge current. With this in mind, it is common to target an increase in switching frequency to decrease the output inductor and output capacitor values and sizes. The output inductor and output capacitor can be calculated from the following equation:

$$L = \frac{V_L \bullet \Delta t_{ON}}{\Delta I_L} = \frac{\left(V_{IN} - V_{OUT}\right) \bullet \left(\frac{V_{OUT}}{V_{IN} \bullet f_S}\right)}{\Delta I_L}$$

where ΔI_L is the inductor current ripple. This is plotted in Fig. 12 for a one-cell Li-ion battery charger (V_{OUT} = 4.2 V) with a 2-A charge current, an input voltage of 10 V and 20 V, ΔI_L = 600 mA, and sweeping switching frequency from 100 kHz to 1.5 MHz.

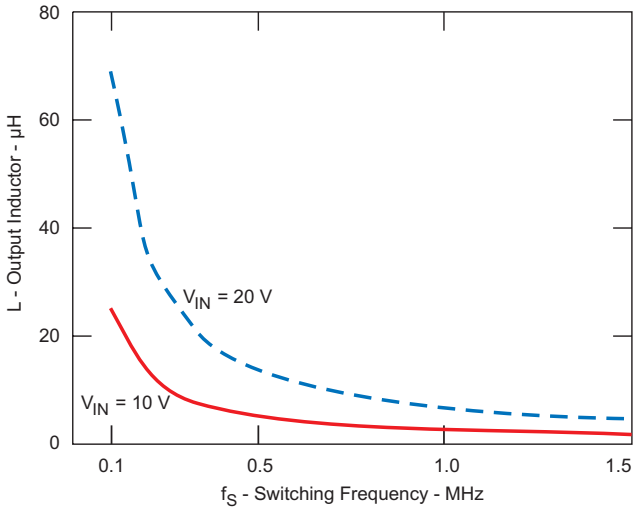

Fig. 12. Output inductor versus switching frequency at V_{IN} = 10 V and V_{IN} = 20 V.

The output capacitor is determined with the following formula:

$$C = \frac{\Delta I_L \bullet \left(\frac{V_{OUT}}{V_{IN} \bullet f_S}\right)}{\Delta V_C}$$

where ΔV_C is the capacitor output voltage ripple. This is plotted in Fig. 13 for a one-cell Li-ion battery charger (V_{OUT} = 4.2 V) with a 2-A charge current, an input voltage of 10 V and 20 V, ΔI_L = 600 mA, and ΔV_C = 0.5% of V_{OUT} = 21 mV.

The formula for C also shows that a higher switching frequency can decrease the ripple current and voltage proportionately for the same output inductor and capacitor. If the frequency is kept constant and the output inductor or capacitor

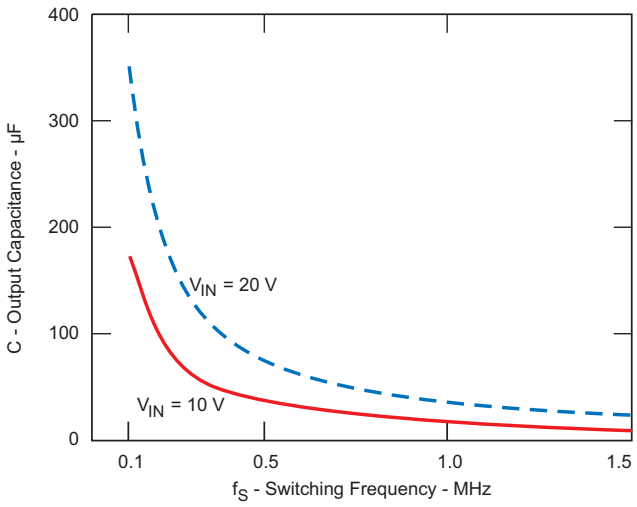

Fig. 13. Output capacitor versus switching frequency at V_{IN} = 10 V and V_{IN} = 20 V.

is decreased, the output ripple current and voltage will proportionately increase.

The simplified first-order power-loss equations are composed of conduction-loss components and switching-loss components.

Total power losses are

$$P_{TOT} = P_{CON} + P_{SW}$$

The conduction losses are composed of five main contributors. Conduction losses are

$$P_{CON} = P_{ON\_T} + P_{ON\_B} + P_{R_{SENSE}} + P_L + P_C$$

given by

$$P_{ON\_T} = R_{DS(ON)\_T} \bullet \left(\sqrt{D} \bullet I_{OUT}\right)^2$$

where $R_{DS(ON)\_T}$ is for the *top* control MOSFET.

$$P_{ON\_B} = R_{DS(ON)\_B} \bullet \left\{\sqrt{(1-D) - \left[f_S \bullet \left(t_{d1} + t_{d2}\right)\right]} \bullet I_{OUT}\right\}^2$$

where $R_{DS(ON)\_B}$ is for the *bottom* synchronous MOSFET, and t_{d1} and t_{d2} are the dead times.

$$P_{R_{SENSE}} = R_{R_{SENSE}} \bullet {I_{OUT}}^2$$

where R_{SENSE} is the current sense resistor.

P_L inductor power loss, excluding AC losses, is

$$P_L = R_{DCR} \bullet {I_{OUT}}^2$$

where R_{DCR} is the series resistance of the output inductor.

P_C capacitor power loss is

$$P_C = R_{ESR} \times \left(\sqrt{D} \bullet I_{OUT}\right)^2$$

where R_{ESR} is the equivalent series resistance (ESR) of the input capacitor.

The switching losses are primarily dependent on the gate charge of the power FETs and the dead time. Switching losses are

$$P_{SW} = P_{SW\_T} + P_{SW\_B} + P_{SCH} + P_{GD}$$

The top high-side power FET switching losses are

$$P_{SW\_T} = \frac{Q_{GSI\_T} + Q_{GD\_T}}{I_G} \bullet \frac{V_{IN} \bullet I_{OUT}}{2} \bullet f_S$$

where Q_{GSI} is the gate-to-source charge, and Q_{GD} is the gate-to-drain Miller gate charge of the *top* control MOSFET.

$$P_{SW\_B} = \left[\left(Q_{RR\_B} \bullet V_{IN}\right) + \frac{C_{OSS} \bullet {V_{IN}}^2}{2}\right] \bullet f_S$$

including the reverse recovery, Q_{RR}, losses and output capacitance, C_{OSS}, of the lower synchronous MOSFET.

$$P_{SCH} = V_F \bullet I_{OUT} \bullet \left(t_{d1} + t_{d2}\right) \bullet f_S$$

where V_F is the forward voltage of the Schottky diode in parallel with the low-side synchronous FET, and t_{d1} and t_{d2} are the dead times.

$$P_{GD} = V_{IN} \bullet (Q_{GSTOT\_T} + Q_{GSTOT\_B}) \bullet f_S$$

where Q_{GSTOT_T} and Q_{GSTOT_B} are the total gate charge at the gate drive regulator voltage for the top and bottom FETs, respectively.

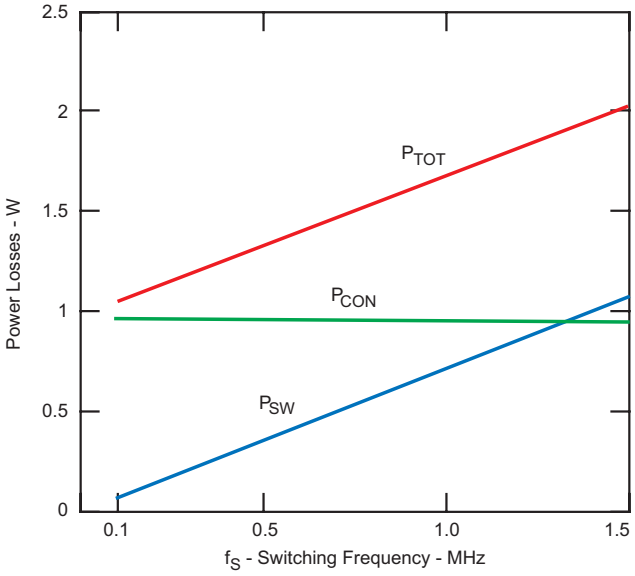

Fig. 14. Total power losses, switching losses, and conduction losses for a typical single-cell, Li-ion battery charger.

As shown in Fig. 14, the total power dissipation is dependent on the switching frequency; however, the values of the output inductor and capacitor are inversely proportional to the switching frequency. For battery chargers, this trade-off is usually optimized to minimize the size and cost of the components while keeping the system power dissipation below the thermal limit. Thus switching frequency is increased primarily to improve the power density (size) of the charger until a thermal limit is reached. Also keep in mind that off-the-shelf capacitors and inductors are available in only a handful of values and sizes; thus they must change as a step function instead of linearly with frequency.

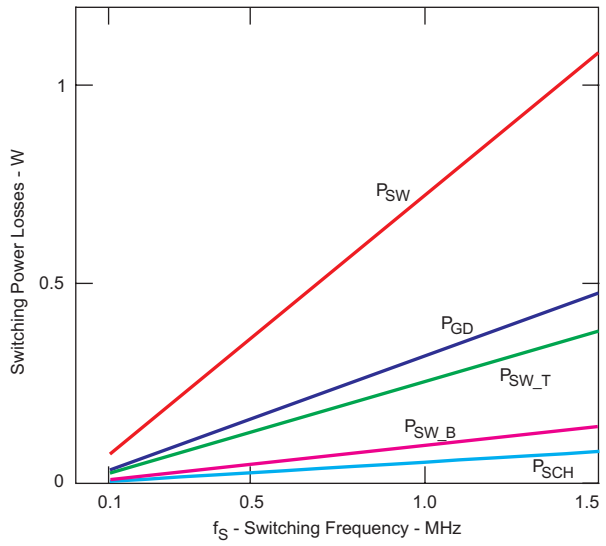

Fig. 15. Switching losses during dead time for the single-cell, Li-ion battery charger: Total, gate drive, top FET, bottom FET, and Schottky.

The total input gate charge of the power MOSFETs contributes to gate-drive losses that dissipate within the control IC and raise its temperature. As shown in Fig. 15, the gate-drive losses could be significant. This needs to be considered when the charger ICs are operated at higher switching frequencies such as 500 kHz for high-current applications, or 1 MHz for lower-current applications. The junction temperature should be calculated to ensure that the data sheet specification is not being exceeded. To reduce the temperature, the designer can either decrease the switching frequency or select power MOSFETs with lower gate charge. Some charger control ICs have an integrated thermal-limit comparator that automatically shuts off if the junction temperature exceeds a maximum threshold. The maximum power loss for a package can be calculated from the maximum junction temperature of the silicon ($T_{J(max)}$), the ambient temperature (T_A), and the package thermal junction-to-ambient resistance ($R_{\theta JA}$).

$$P_{LOSS(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

IV. Switching Regulator Trade-offs for Battery-Charging Applications

A. Can Standard Converters Be Used in a Battery-Charging Environment?

The standard topologies discussed in section II can be implemented with a wide array of DC/DC controllers available on the market today. However, using standard controllers for a synchronous conversion potentially can cause various problems when a battery load is used, unless additional circuits are designed into the overall solution.

Traditional stand-alone controllers are designed to handle loads that have only sink capability; a battery load can both source and sink currents. Using traditional converters can lead to premature battery discharge; pack protector activation; or converter malfunction.

Following are a few problems that can happen:

- The pack is shorted to the AC adapter output if the pack is above the adapter voltage.
- The PWM converter does not start when the charger is enabled and a pack is connected.
- Battery reverse current flows through the low-side switch during the charge-current taper phase.
- The bootstrap circuit can't be recharged when the adapter voltage is too close to the battery-pack voltage.

The discussion up to this point has focused on the major topologies used in synchronous converters targeted at battery-pack-charging applications. For the sake of simplicity, only the trade-offs related to controller complexity, cost, and power dissipation have been covered. The next section provides an overview of common challenges that arise when those topologies are used in a battery-pack-charging environment and practical solutions that can be used to implement a robust design.

B. Avoiding Undesirable Reverse Discharge

A battery is a two-quadrant device in that it has a positive voltage but could allow both positive and negative current to flow. When the current is positive, the battery sources the current; when the current is negative, it sinks the current (see Fig. 16). Because of this, battery chargers need to avoid reverse discharge, which can drain the battery and reduce expected run-time capacity. There are two probable paths for reverse discharge within a synchronous buck regulator: from battery to input and from battery to power ground.

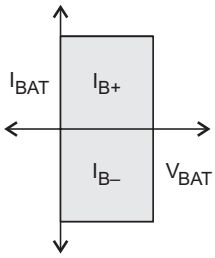

Fig. 16. A battery is a two-quadrant device that sources and sinks current.

The first path is from the battery, through the output inductor, and through the back diode of the high-side power MOSFET to the input (see Fig. 17). This occurs when the battery is higher than the input voltage. Connecting a series Schottky diode at the input with the cathode connected to the drain of the high-side power FET prevents the reverse-discharge current (see Fig. 18). This protection is the simplest to implement for discrete solutions. The penalty of using the Schottky diode, however, is that the added forward voltage drop, V_F, increases conduction power losses and the size of the diode as the charge current increases. A power MOSFET can be used instead of the Schottky diode to reduce the conduction losses and the area as shown in Fig. 19. A gate signal needs to be generated in which the FET is kept on only during charging. Also, the input voltage and battery voltage must be monitored during charging to ensure that the blocking FET is turned off quickly if the input voltage ever falls below the battery voltage. This is easier to implement with integrated solutions. Keep in mind that both Schottky-diode and FET reverse-blocking implementation still have reverse leakage currents to consider. Schottky diodes typically have higher leakage current (up to the milliamps), especially at high junction temperatures; whereas the MOSFET leakage is typically in the microamps.

The second path for reverse discharge within a synchronous buck regulator is from the battery, through the output inductor, and through the low-side FET to ground, as shown in Fig. 20. This occurs through the channel of the FET when the power MOSFET is on and the current reverses

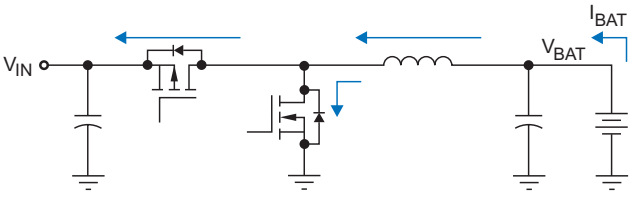

Fig. 17. Reverse battery leakage path from battery to input when $V_{IN} < V_{BAT}$.

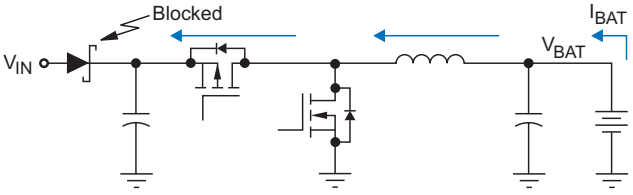

Fig. 18. Protecting reverse leakage from battery to input with a Schottky diode.

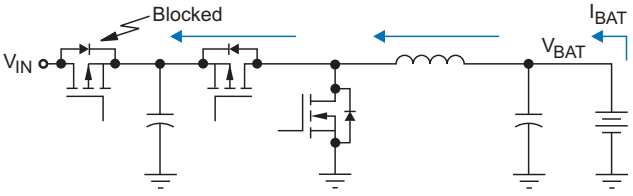

Fig. 19. Protecting reverse leakage from battery to input with a synchronous PMOS FET.

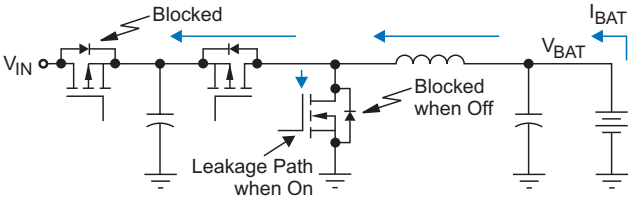

Fig. 20. The NMOS low-side FET provides a leakage path to ground when on but blocks reverse conduction when off. A circuit that detects a near-zero current is needed to shut off the FET before the current reverses.

through the inductor. To prevent this, the inductor current or low-side MOSFET current must be monitored, and the low-side power MOSFET must be turned off before the inductor current reverses (goes negative). It is better to turn off the low-side FET before the current reverses than to let even a small current reverse. If the inductor current is allowed to reverse and then the low-side FET is turned off, the inductor will try to force current through the high-side power MOSFET into the input supply. If there is an input reverse-blocking Schottky diode or MOSFET, it will avalanche and possibly could be damaged if the energy is high enough. Thus it is always preferable to avoid reverse conduction of synchronous buck chargers. Keep the low-side FET off when the circuit is not charging; turn on the low-side FET when the circuit is charging and the inductor current is positive; and then turn off the FET before the inductor current reverses. This is very important, especially during power-up or whenever the duty cycle is very low, during which the low-side FET will attempt to be on most of the time.

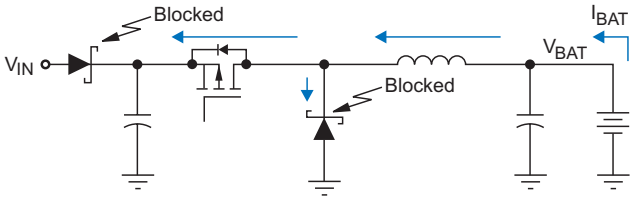

Fig. 21. A nonsynchronous buck regulator blocks large reverse-discharge currents to ground, but it also has higher conduction losses.

Nonsynchronous buck regulators use the Schottky diode instead of a power MOSFET to prevent reverse discharge (see Fig. 21). The diode prevents reverse conduction at the expense of increased forward-conduction power dissipation and size. Again, keep in mind that there will be some reverse leakage current for both the Schottky diode and the power MOSFET. The leakage of a Schottky diode is usually a magnitude higher than that for a power NMOS FET. Both Schottky diodes and NMOS FETs have a higher leakage as their junction temperature increases.

Preventing reverse discharge to ground is also important when a charger is started up with a battery connected at the output. If the converter is allowed to conduct negative current through the low-side FET, the current will go negative and will not be able to charge the inductor with positive current, either indefinitely or for a significant amount of time. Fig. 22 shows an oscilloscope plot of a charger with no reverse-current protection. The current is allowed to go to –1.5 A. Fig. 23 shows the same charger with the reverse-current protection enabled. The NMOS low-side FET is turned off before the current is allowed to reverse and discharge to ground. There is no negative current, and the charger more quickly powers up the output.

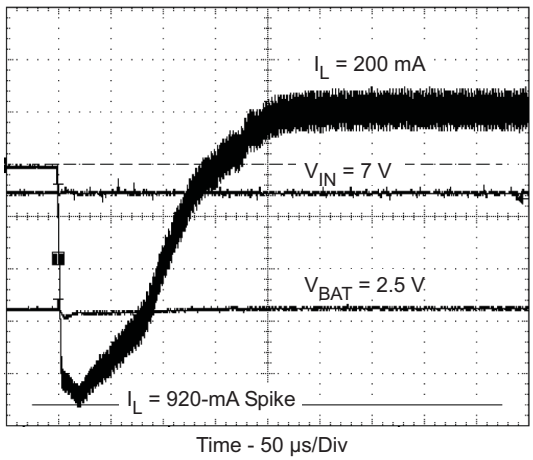

Fig. 22. Inductor current during startup with no reverse-current protection, causing large 920-mA discharge-current spikes. Inductor current goes negative and settles to a charge current of 200 mA.

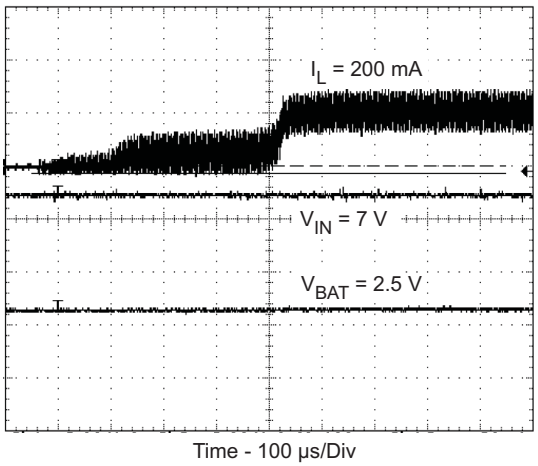

Fig. 23. Inductor current during startup with reverse-current protection enabled so there are no discharge-current spikes. The low-side FET is turned off before the inductor current reverses and goes discontinuous, which then settles to a charge current of 200 mA.

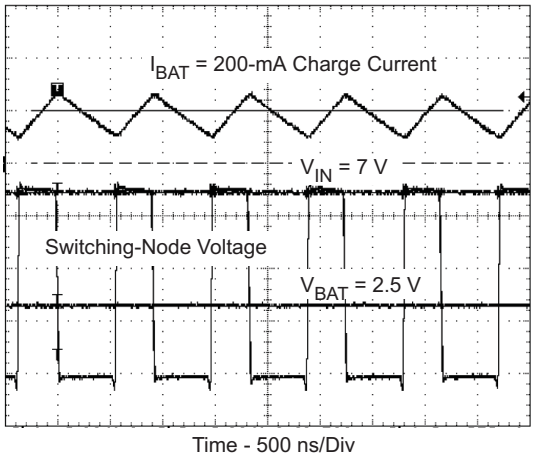

Fig. 24. Switching-node voltage with continuous inductor-current conduction when current is always positive.

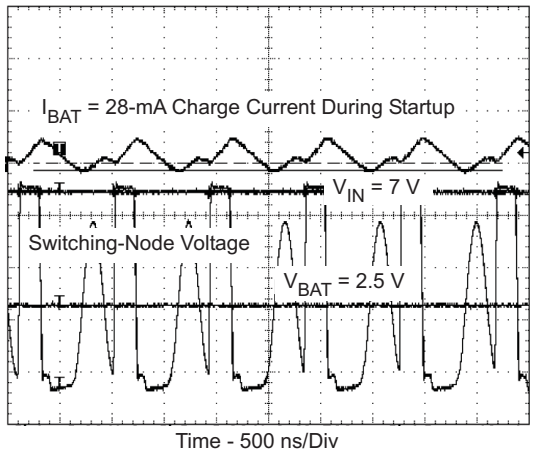

Fig. 25. Switching-node voltage with discontinuous inductor-current conduction to prevent reverse conduction.

C. Unique-Load Behavior

Battery chargers have a few unique requirements that stand-alone voltage converters don't. Besides regulating the output voltage, battery chargers have the additional task of regulating output current when the battery voltage is below the voltage-regulation value. Another difference with battery chargers is that the loads are not always the same as in a simple voltage converter. Voltage converters typically have a resistive load, or a constant power load with very low input impedance. For a constant output voltage, the load could be simplified to a constant current source. Expected loads for a typical stand-alone voltage converter are shown in Fig. 26. Constant power loads are usually due to any combination of linear and switching regulators that distribute the power to the various blocks of the application. Constant power loads can be represented by a voltage-dependent current source.

Battery chargers, on the other hand, are expected to have various load combinations depending on the application. Cradle chargers usually have only a battery load (see Fig. 27). If the battery is removed, the cradle charger is expected to detect removal and then stop charger operation.

For embedded-charger applications, the charger could have a battery load and a constant-power system load at the same time (see Fig. 28). The combined load behaves more like a constant-power operation than a constant-current operation

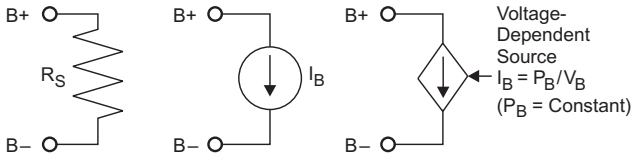

Fig. 26. Expected loads for a typical stand-alone voltage converter.

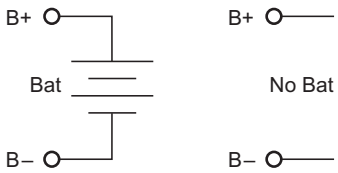

Fig. 27. Expected loads for a cradle battery charger.

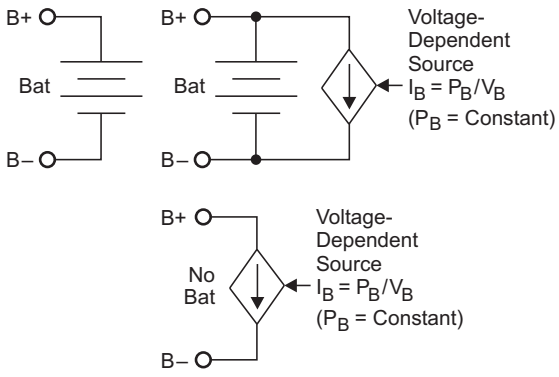

Fig. 28. Expected loads for an embedded battery charger.

when the battery voltage is below the voltage-regulation threshold. In some embedded applications, the charger is also expected to regulate the main system rail if the battery is removed or is being changed. Dual-pack embedded applications require power-management handling to switch from one pack to another.

Special attention should be paid to compensation when a battery is connected as a load. The battery behaves as an energy source or an energy sink, since current can flow in both directions. The battery protection described earlier can take care of the reverse-discharge concerns; however, it introduces a discontinuous-current mode when the current is low. The converter needs to ensure stable operation for both continuous- and discontinuous-current modes. Chargers go discontinuous when in precharge and during tapering when nearing charge termination. Fast charge is typically in continuous-current mode. Operation in continuous-current mode has a double pole due to the output inductor and capacitor. During discontinuous-current mode, the poles split and the dominant pole frequency is a function of the load.

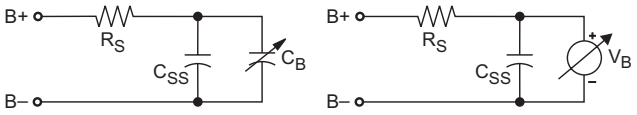

Fig. 29. Large-signal model of a battery.

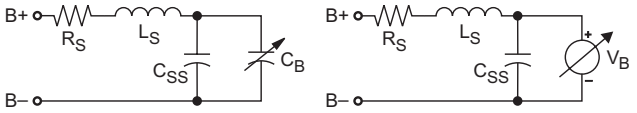

Fig. 30. Small-signal model of a battery.

Another requirement is that the battery behave as a unique load whose small-signal behavior is not always taken into consideration. As shown in Fig. 29, the battery looks like a very large capacitor that plays a key role in large-signal behavior; but, contrary to intuition, the small-signal behavior is different in that it is dominated by the series inductance and resistance of the pack (see Fig. 30). The large capacitor is modeled as an ideal voltage source during the small-signal analysis and plays a minor role in the response. The voltage on the ideal (large-capacitance) voltage source may vary depending on its state, but the series resistance and inductor are relatively constant. This inductive behavior needs to be accounted for in compensation design, as it has a tendency to improve phase margin but reduce gain margin as the output behaves more like a current source. The low gain margin can allow excessive ringing at frequencies above the crossover frequency.

As in voltage converters, the output capacitor and its associated ESR need to be considered in battery chargers. A key goal in portable equipment is to reduce the size of converters by increasing the switching frequency, which enables small ceramic capacitors to be used at the input and the output. The result is that the converter could have large swings in resonant frequency due to the wide capacitance tolerance over temperature. Ceramic capacitors also have very low ESR values that push out the zero frequency to a value too high to assist in canceling a pole. ESR zeros for ceramics are typically at or above the switching frequency.

D. Control Scheme Affecting Frequency

Various control schemes can be used to regulate the converter current and voltage. Control schemes can be divided into two groups: one that maintains constant switching frequency and another that varies the switching frequency. In all control schemes the output is regulated by varying the duty cycle, which is equal to the on time divided by the period.

$$D = \frac{t_{ON}}{T_S} \approx \frac{V_{OUT}}{V_{IN}}$$

The constant-frequency control schemes regulate the duty cycle by varying the on time while keeping the frequency constant (f_{S_Fixed}).

The variable-frequency control schemes can be divided into three types: constant on time, constant off time, and hysteretic. Following are the equations for the first-order frequency of each:

- The constant-on-time method keeps the on time constant and varies the off time to get the necessary duty cycle, thus varying the frequency.

$$f_{S\_t_{ON}} = \frac{D}{t_{ON}}$$

- The constant-off-time method keeps the off time constant and varies the on time to get the necessary duty cycle, thus varying the frequency.

$$f_{S\_t_{OFF}} = \frac{1-D}{t_{OFF}}$$

- The hysteretic method varies both on time and off time, thus varying the frequency.

$$f_{S\_HYS} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{L \bullet \Delta I_C \bullet \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{OUT}} \right)}$$

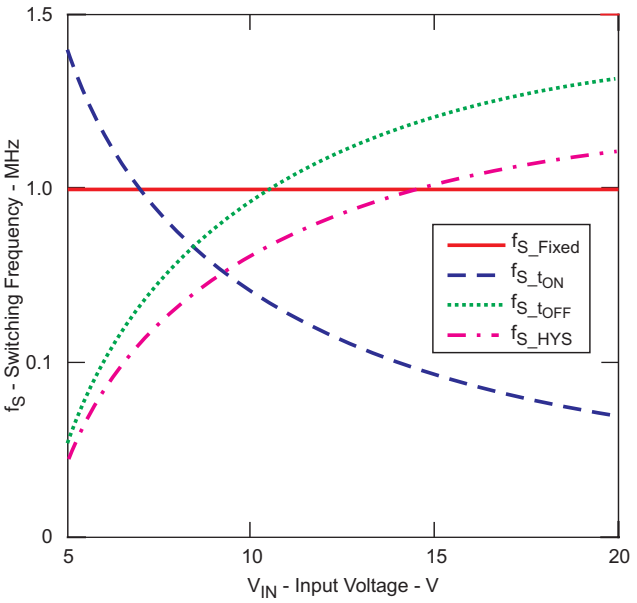

Fig. 31. Frequency variation versus input voltage of converters with fixed-frequency, constant-on-time, constant-off-time, and hysteretic control schemes.

The possible frequency variations for a 4.2-V, single-cell output charger with a 10-µH inductor, a 100-µF output capacitor, and an input varying from 5 to 20 V are plotted in Fig. 31. A 1-MHz constant-frequency converter is compared to a 500-ns constant-on-time converter, a 500-ns constant-off-time converter, and a 15% current ripple hysteretic converter.

Constant-frequency control schemes have the benefit of keeping the frequency above critical frequency bands such as the audible noise region (300 Hz to 3 kHz) or the ADSL carrier frequency (900 kHz), which are important design constraints in many portable applications. Lower efficiency due to higher switching frequency is not an issue for chargers as long as the thermal limits are not reached.

Variable-frequency schemes have the disadvantage that the frequency could vary depending on the adapter input voltage, output (battery) voltage, and load-current (charge) conditions. The frequency could drop into or below a critical frequency range, causing noise issues; or it could go up so high that the switching losses are excessive, causing thermal concerns.

Also, worst-case minimum frequencies could occur at minimum load (charge) current, such as when the charge cycle is tapering and nearing termination. This is due to the slow rate at which the output capacitor is discharged. Frequencies could easily fall into the audible frequency range. Sometimes a "dummy" load is required to bleed the minimum-current limit and avoid falling into low-frequency operation. Care must be taken, as this "bleed" resistor is a leakage source that drains the battery when it is not being charged.

V. Overall System-Design Considerations

A. Preventing AC-Adapter-Induced Failure Modes

The use of an AC adapter to power a converter requires consideration of the following items:

- The DC/DC controller must survive an adapter hot-plug event.
- The DC/DC converter application circuit must not affect AC adapter insertion/removal detection.

An adapter hot-plug event can have catastrophic results for the controller IC, depending on the input capacitor used on the system. When an already powered adapter is connected to the system, the input voltage at the adapter connector terminal rises very fast; the adapter cable inductance and series resistance interact with the input filter capacitor and generate an overshoot pulse. For small input-capacitor values, it is not uncommon to see overshoots in excess of 50% of the adapter regulation voltage, as shown in Fig. 32. Increasing

the input capacitor to large values to obtain an underdamped response is not a viable solution, as cost will increase and sparks on the adapter system connector will occur upon connector insertion, causing long-term reliability effects.

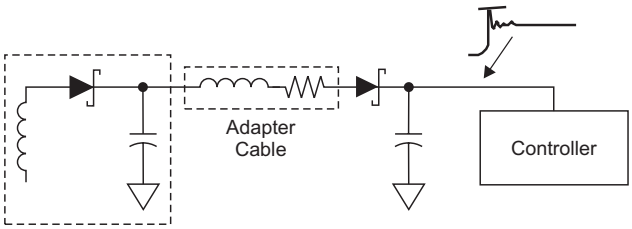

Fig. 32. Supply-line overshoot upon adapter hot-plug insertion.

The only practical solution is to dimension the input capacitor to limit the pulse to reasonable values, below the converter maximum ratings for input voltage. Selecting controllers with high input-voltage ratings will minimize system cost while still enabling design of a robust system.

The simplified topologies shown in section II have the potential problem of biasing the adapter terminal with the battery-pack voltage through the high-side switch back-gate diode when the battery voltage exceeds the adapter voltage. This situation can occur during adapter removal or when DC voltages lower than the pack voltage are used to bias the end equipment (such as car battery lines, airline adapters, etc.).

This parasitic path can hold the voltage at the adapter terminal above the threshold for AC adapter detection, preventing the detection of AC adapter removal and creating the potential for unexpected system behavior.

The condition that has the highest damage potential, however, occurs when one of the simplified circuits in section II is used on systems where the positive terminal of the adapter connector is mechanically shorted to ground upon adapter removal. This will generate a hard short from battery to ground with the current path being provided by the high-side switch back-gate diode, potentially damaging the high-side switch.

The solution discussed in section IV to prevent reverse conduction from the battery to the adapter also takes care of these additional issues.

B. AC Adapter Power Considerations

Most end equipment must maintain normal operation while charging a battery pack. Usually the cost of the AC adapter is directly proportional to the rms current supplied to the system. One of the design targets for the system is to lower the power dissipation of the AC adapter; to do that, usually the adapter voltage is kept as close as possible to the target charge voltage. This approach has an adverse impact on the rms current, as the converter duty cycle will increase as the battery-pack voltage increases. To harmonize these requirements, a new topology was developed with the addition of a third dynamic-power-management (DPM) loop to the standard converter (see Fig. 33). This third loop effectively reduces the charge current when the adapter current limit is reached, effectively adapting the charge-current value to the system load conditions and AC-adapter limits

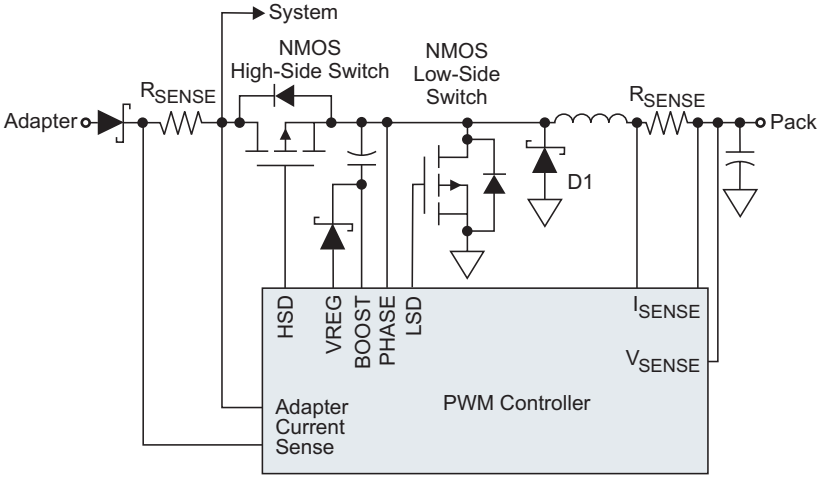

Fig 33. Additional DPM loop.

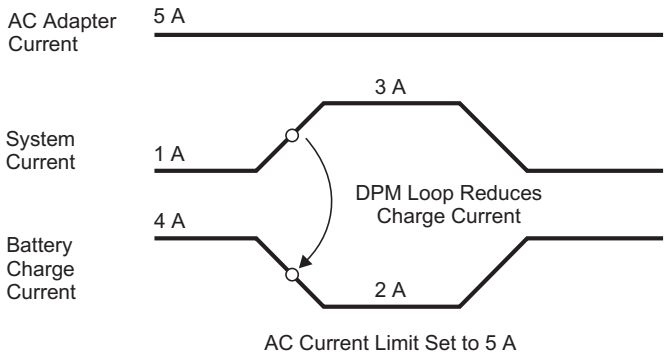

Fig 34. Example of charge-current reduction to accommodate a system load increase.

(see Fig. 34). As a result, the AC adapter cost can be reduced, and simultaneous pack charging and system operation can be achieved.

C. Additional Charger-Startup Issues

Upon initial startup, the error signal generated by the error amplifiers will try to increase the ramp voltage. Some amount of overshoot for the charge current or charge voltage can be expected during power-up if the ramp voltage increases faster than the feedback loop response. To avoid overshoot conditions, a soft-start circuit is usually implemented to decrease the slew rate for the error signal used by the PWM ramp comparator. This methodology guarantees an orderly startup for the system and avoids undesirable ringing or overshoots (see Fig. 35).

The most common topologies use an external capacitor that is charged by a current source; the voltage at the capacitor clamps the PWM ramp-comparator input if it is below the desired regulation point. When the error voltage reaches the regulation point, the soft-start circuit is disabled.

As a general rule, to guarantee that the soft-start circuit is always active when the converter is initially enabled, all the soft-start capacitors must be discharged by a fast-discharge circuit when the converter is disabled.

Another soft-start method is to step up the internal voltage reference that the charge-current regulation loop uses to set the battery charge current.

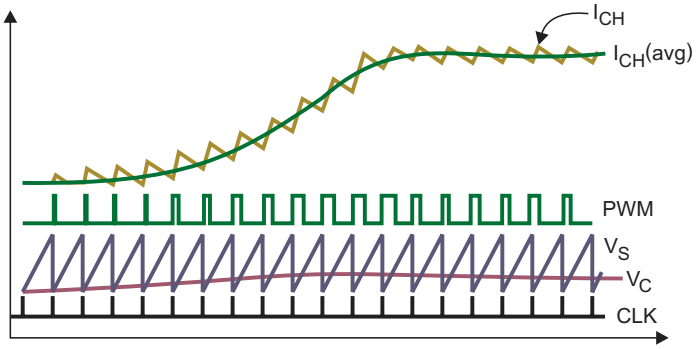

Fig. 35. Soft start ramping up the charge current.

D. Preventing Other Battery-Charger Failure Mechanisms

Failure mechanisms are of special concern when Li-ion packs are being charged. Li-ion packs have internal safety devices to protect against overcurrent and overvoltage conditions; however, it is a recommended practice to include secondary fault-protection functions in Li-ion charging systems for increased reliability and safety. Those functions should end the charge if abnormal conditions are detected; and they can be implemented on either the charge controller or in a power-management IC that monitors the charge process (see Table 1).

TABLE 1. FAULT-PROTECTION FUNCTIONS IN LI-ION CHARGING SYSTEMS

Event	Detection/Action
Charge time exceeds normal charging time	Monitor converter on time; End charge
Battery-pack temperature is out of range	Monitor pack thermistor; End charge
Converter-IC temperature exceeds safe operating range	Monitor converter-IC junction temperature (thermal shutdown); End charge
Charge current exceeds target value while pack is connected	Monitor charge current; End charge
Voltage overshoot occurs at pack removal when charger is on (due to loop delay)	Detect pack removal; End charge
Pack cell or pack terminal is short-circuited; or pack opens, resulting in low pack visible voltage	None; Design PWM loop with ground-compatible common-mode range
High-side switch is damaged due to thermal overload and shorts adapter to pack	Monitor charge current; Add additional on/off switch in series with high-side device to isolate pack from adapter
Overvoltage condition occurs	Detect output voltage above target voltage; End charge

MUST HAVE **OPTIONAL**

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265