PIC16F/LF1824/1828 Family Silicon Errata and Data Sheet Clarification

The PIC16F/LF1824/1828 family devices that you have received conform functionally to the current Device Data Sheet (DS41419**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F/LF1824/1828 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16F/LF1824/1828 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
PIC16F1824	10 0111 010x xxxx	1
PIC16LF1824	10 1000 010x xxxx	1
PIC16F1828	10 0111 110x xxxx	1
PIC16LF1828	10 1000 110x xxxx	1

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC16F/LF182X/PIC12F/LF1822 Memory Programming Specification"* (DS41390) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]
				A1
ADC	ADC Conversion	1.1	ADC Conversion may not complete.	X
Oscillator	HS Oscillator	2.1	HS Oscillator min. V_{DD}.	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	3.1	PWM 0% duty cycle direction change.	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	3.2	PWM 0% duty cycle port steering.	X
Timer1	T1 Gate Toggle mode	4.1	T1 Gate Flip-Flop does not clear.	X
ADC	Error Parameters	5.1	Differential and gain error.	X
In-Circuit Serial Programming™ (ICSP™)	Low-Voltage Programming	6.1	Bulk Erase not available with LVP.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: ADC

1.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/$\overline{\text{DONE}}$ bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

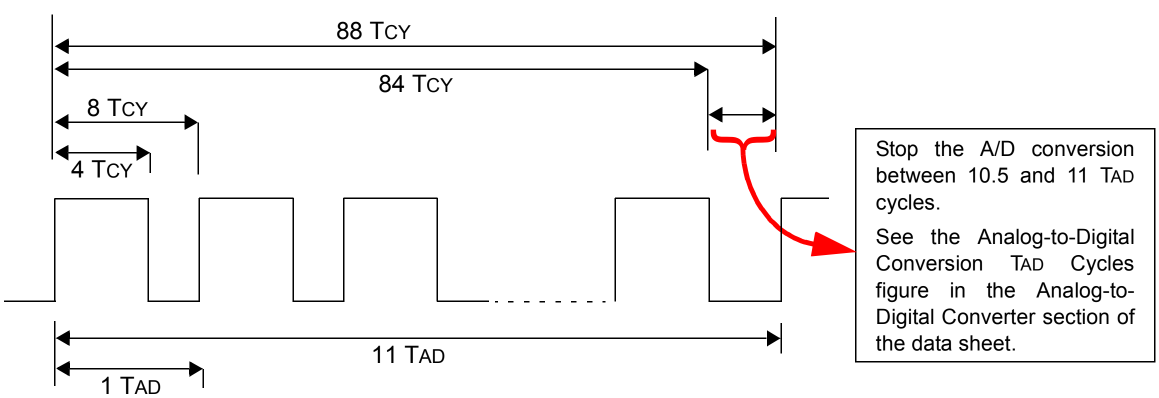
Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/$\overline{\text{DONE}}$ bit in software. The GO/$\overline{\text{DONE}}$ bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note:	The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO   ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, ADGO   ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A1							
X							

2. Module: Oscillator

2.1 HS Oscillator

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

Work around

None.

Affected Silicon Revisions

A1							
X							

3. Module: Enhanced Capture Compare PWM (ECCP)

3.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A1							
X							

3.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A1							
X							

4. Module: Timer1

4.1 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A1							
X							

5. Module: ADC

5.1 ADC Differential and Gain Error Parameters

The differential and gain error parameters are as follows:

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
AD03	EDL	Differential Error	—	—	±1.5	LSb	VREF = 3.0V
AD05	EGN	Gain Error	—	—	±2	LSb	VREF = 3.0V

Work around

None.

Affected Silicon Revisions

A1							
X							

6. Module: In-Circuit Serial Programming™ (ICSP™)

6.1 Bulk Erase Feature not available with Low-Voltage Programming mode

A bulk erase of the program Flash memory or data memory cannot be executed in Low-Voltage Programming mode.

Work around

Method 1: If ICSP Low-Voltage Programming mode is required, use row erases to erase the program memory, as described in the Program/Verify mode section of the Programming Specification. Data memory must be over-written with the desired values.

Method 2: Use ICSP High-Voltage Programming mode if a bulk erase is required.

Note:	Only the bulk erase feature will erase program or data memory if code or data protection is enabled. Method 2 must be used if code or data protection is enabled.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41419**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (06/2010)

Initial release of this document.

Rev B Document (07/2010)

Revised Module 1.1; Added Module 6.1; Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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