June 14, 2011

National Semiconductor

LMV7271/LMV7275/LMV7272

Single & Dual, 1.8V Low Power Comparators with Rail-to-Rail Input

General Description

The LMV727X are rail-to-rail input low power comparators, which are characterized at supply voltage 1.8V, 2.7V and 5.0V. They consume only 9uA supply current per channel while achieving a 800ns propagation delay.

The LMV7271/LMV7275 (single) are available in SC70 and SOT23 packages. The LMV7272 (dual) is available in micro SMD package. With these tiny packages, the PC board area can be significantly reduced. They are ideal for low voltage, low power and space critical designs.

The LMV7271/LMV7272 both feature a push-pull output stage which allows operation with minimum power consumption when driving a load. The LMV7275 features an open drain output stage that allows for wired-OR configurations. The open drain output also offers the advantage of allowing the output to be pulled to any voltage up to 5.5V, regardless of the supply voltage of the LMV7275.

The LMV727X are built with National Semiconductor's advance submicron silicon-gate BiCMOS process. They all have bipolar inputs for improved noise performance and CMOS outputs for rail-to-rail output swing.

Features

(V_S = 1.8V, T_A = 25°C, Typical values unless specified).

- Single or Dual Supplies
- Ultra low supply current 9µA per channel
- Low input bias current 10nA
- Low input offset current 200pA
- Low guaranteed V_{OS} 4mV
- Propagation delay 880ns (20mV overdrive)
- Input common mode voltage range 0.1V beyond rails
- LMV7272 is available in micro SMD package

Applications

- Mobile communications
- Laptops and PDA's
- Battery powered electronics
- General purpose low voltage applications

Typical Circuit

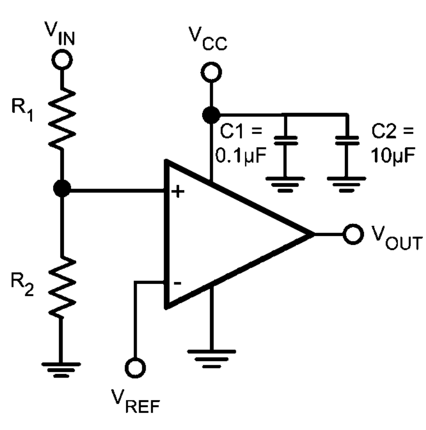


FIGURE 1. Threshold Detector

Part Number	Single/Dual	Package	Output
LMV7271	Single	SC70, SOT23	Push/Pull
LMV7272	Dual	micro SMD	Push/Pull
LMV7275	Single	SC70, SOT23	Open Drain

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2)
	200V (Note 6)
V_{IN} Differential	±Supply Voltage
Supply Voltage (V^+ - V^-)	6V
Voltage at Input/Output pins	V^+ +0.1V, V^- −0.1V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C

Operating Ratings (Note 1)

Supply Voltage Range	1.8V to 5.5V
Temperature Range (Note 3)	−40°C to +85°C
Package Thermal Resistance (Note 3)	
SOT23-5	325°C/W
SC-70	265°C/W
8-Bump Thin micro SMD	220°C/W

1.8V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 0.9V (Note 7)		20		uV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7271/LMV7275		9	12 **14**	µA
		LMV7272		18	25 **28**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0.9V (LMV7271/LMV7272 only)	3.5	6		mA
		Sinking, V_O = 0.9V	4	6		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5mA	1.7	1.74		V
		I_O = 1.5mA	1.47	1.63		
V_{OL}	Output Voltage Low	I_O = −0.5mA		52	100	mV
		I_O = −1.5mA		166	220	
V_{CM}	Input Common Mode Voltage Range	CMRR > 45 dB			1.9	V
			−0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 1.8V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8V (LMV7275 only)		2		pA

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		880		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		570		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		800		ns

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 1.35V (Note 7)		20		μV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input offset Current			200		pA
I_S	Supply Current	LMV7271/LMV7275		9	13 **15**	μA
		LMV7272		18	25 **28**	μA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 1.35V (LMV7271/LMV7272 only)	10	15		mA
		Sinking, V_O = 1.35V	10	15		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5mA	2.63	2.66		V
		I_O = 2.0mA	2.48	2.55		
V_{OL}	Output Voltage Low	I_O = −0.5mA		50	70	mV
		I_O = −2mA		155	220	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			2.8	V
			−0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 2.7V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7V (LMV7275 only)		2		pA

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		1200		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		810		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1300		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		860		ns

5.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 2.5V (Note 7)		20		μV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_S	Supply Current	LMV7271/LMV7275		10	14 **16**	μA
		LMV7272		20	27 **30**	μA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 2.5V (LMV7271/LMV7272 only)	18	34		mA
		Sinking, V_O = 2.5V	18	34		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5mA	4.93	4.96		V
		I_O = 4.0mA	4.675	4.77		
V_{OL}	Output Voltage Low	I_O = −0.5mA		27	70	mV
		I_O = −4.0mA		225	315	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			5.1	V
			−0.1			
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 5.0V	46	78		dB
PRSS	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5V (LMV7275 only)		2		pA

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = 0.5V, V_O = $V^+/2$ and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		2100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1380		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1800		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1100		ns

Note 1: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

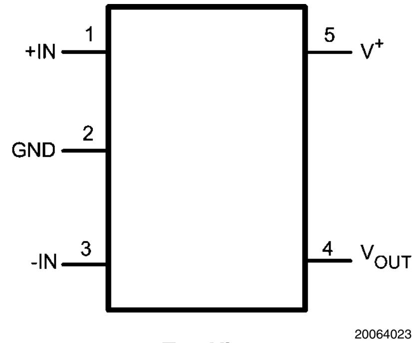
Note 6: Machine Model, 0Ω in series with 200pF.

Note 7: Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 8: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

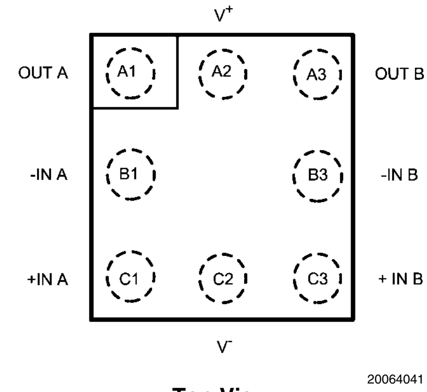
Connection Diagrams

5-Pin SOT23/SC70 (LMV7271/LMV7275)



Top View

8-Bump micro SMD (LMV7272)



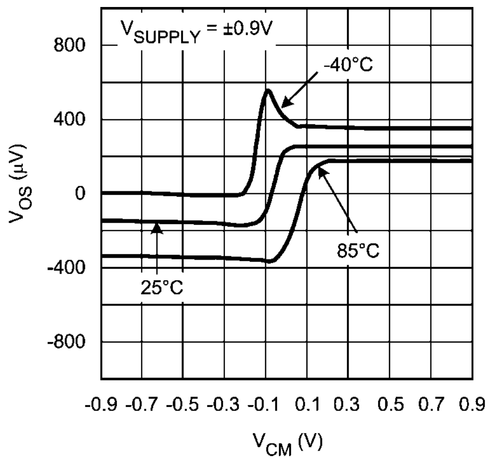
Top View
(bump side down)

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT23	LMV7271MF	C25A	1k Units Tape and Reel	MF05A
	LMV7271MFX		3k Units Tape and Reel	
	LMV7275MF	C26A	1k Units Tape and Reel	
	LMV7275MFX		3k Units Tape and Reel	
5-Pin SC70	LMV7271MG	C34	1k Units Tape and Reel	MAA05A
	LMV7271MGX		3k Units Tape and Reel	
	LMV7275MG	C35	1k Units Tape and Reel	
	LMV7275MGX		3k Units Tape and Reel	
8-Bump micro SMD	LMV7272TL	I 01	250 Units Tape and Reel	TLA08AAA
	LMV7272TLX		3k Units Tape and Reel	

Typical Performance Characteristics
(T_A = 25°C, Unless otherwise specified).

V_{OS} vs. V_{CM}



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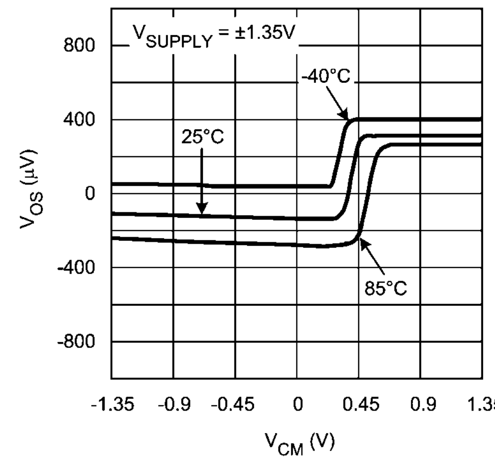
V_{OS} vs. V_{CM}



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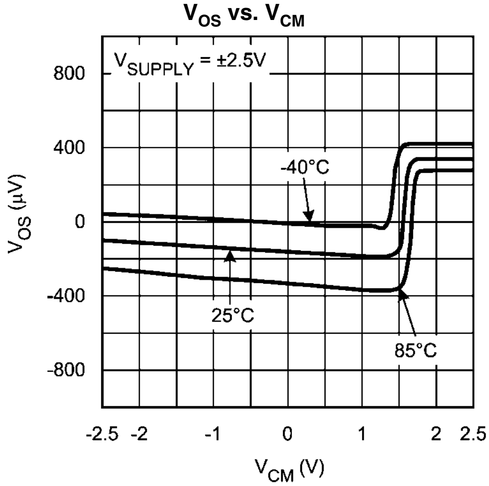
V_{OS} vs. V_{CM}



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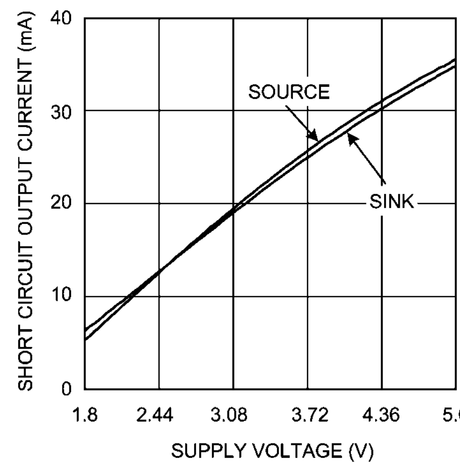
Short Circuit vs. Supply Voltage



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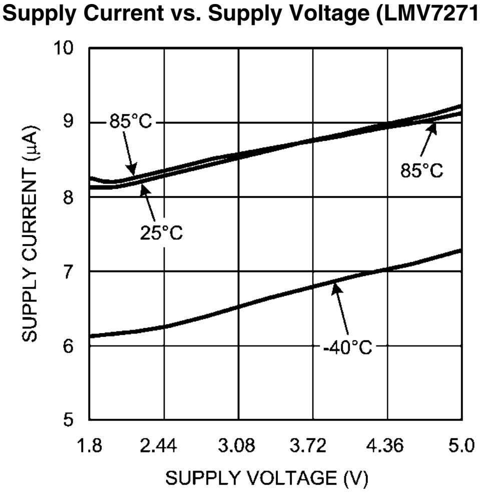
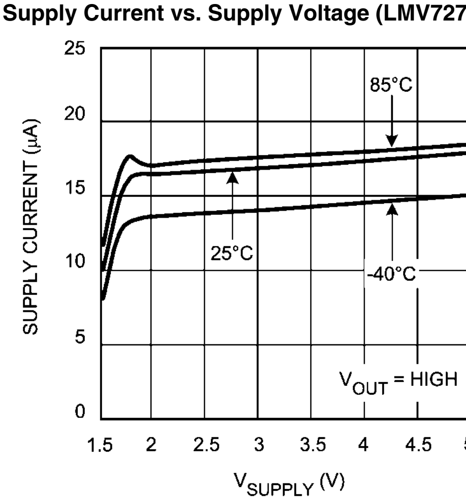
Supply Current vs. Supply Voltage (LMV7271)



20064002

Supply Current vs. Supply Voltage (LMV7272)



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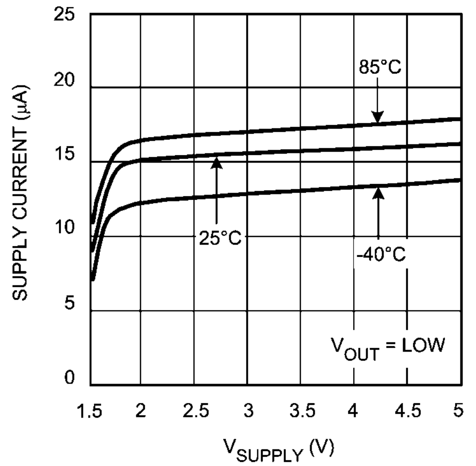
Supply Current vs. Supply Voltage (LMV7272)



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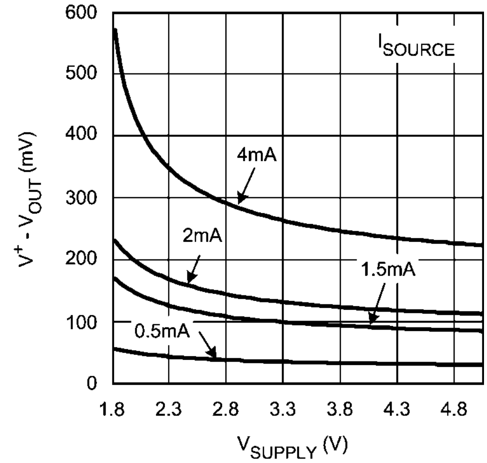
Output Positive Swing vs. V_{SUPPLY}



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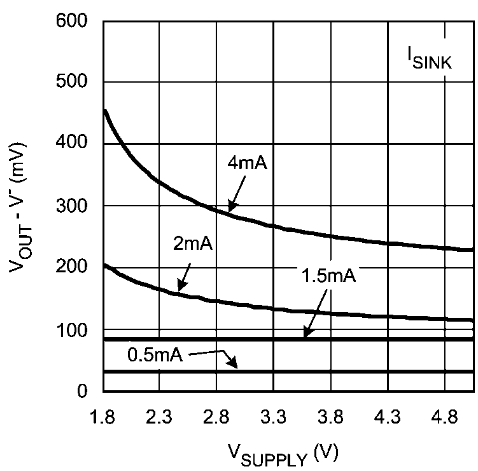
Output Negative Swing vs. V_{SUPPLY}



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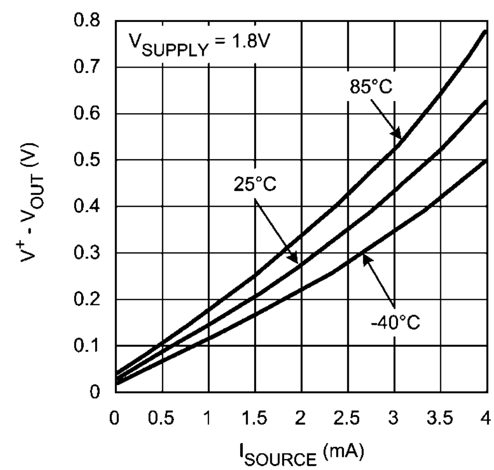
Output Positive Swing vs. I_{SOURCE}



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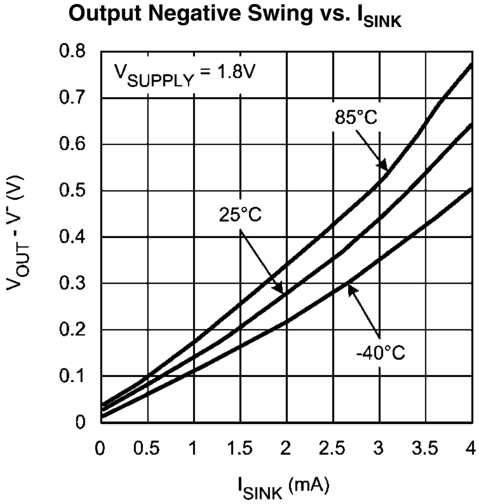
Output Negative Swing vs. I_{SINK}



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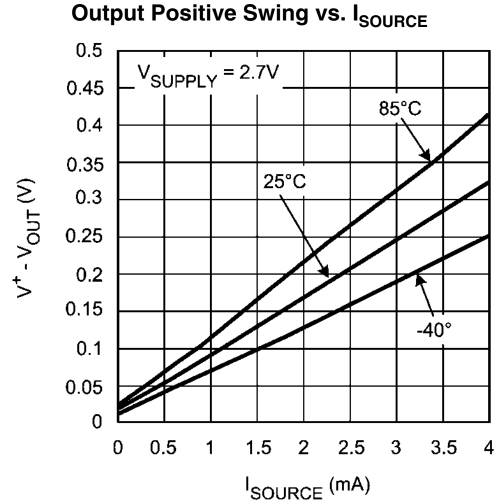
Output Positive Swing vs. I_{SOURCE}



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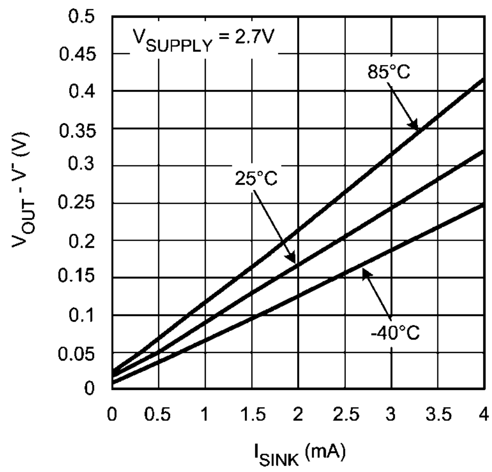
Output Negative Swing vs. I_{SINK}



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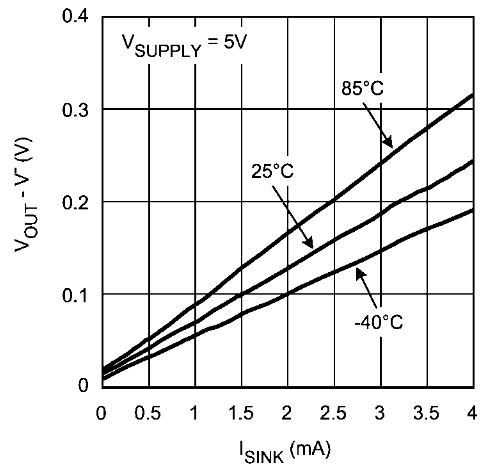
Output Negative Swing vs. I_{SINK}



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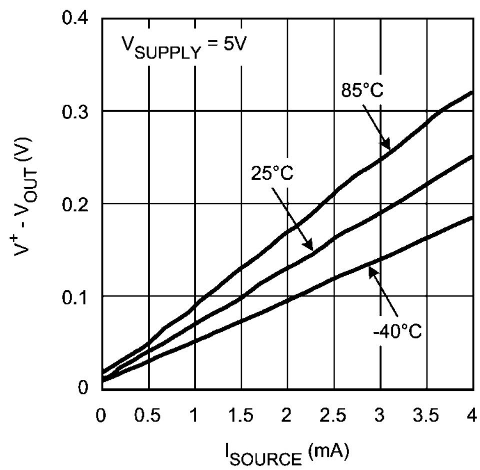
Output Positive Swing vs. I_{SOURCE}



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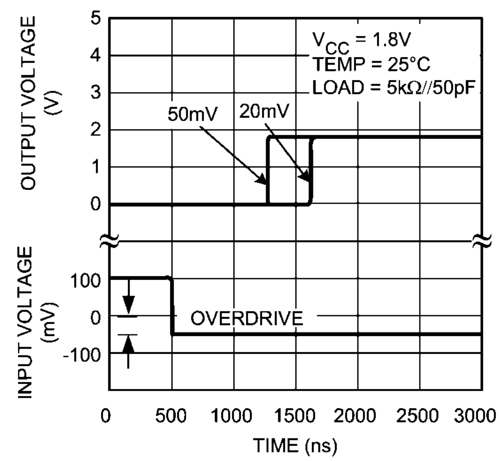
Propagation Delay (t_{PLH})



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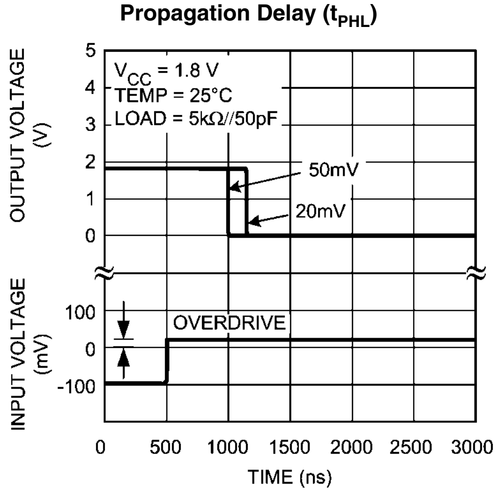
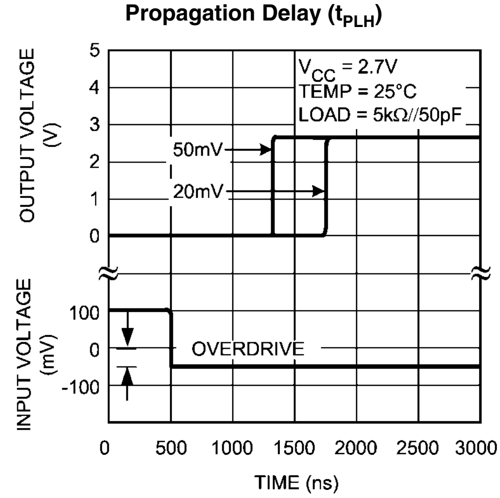
Propagation Delay (t_{PHL})



20064018

Propagation Delay (t_{PLH})



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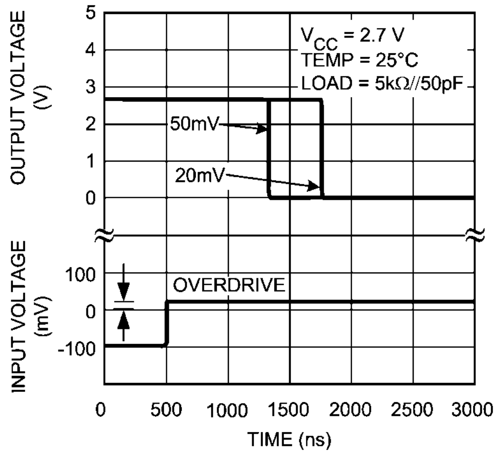
Propagation Delay (t_{PHL})



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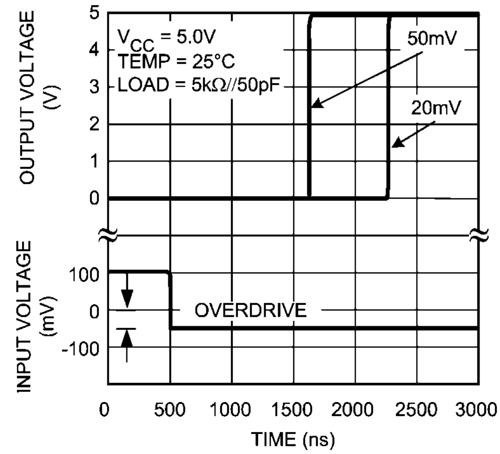
Propagation Delay (t_{PLH})



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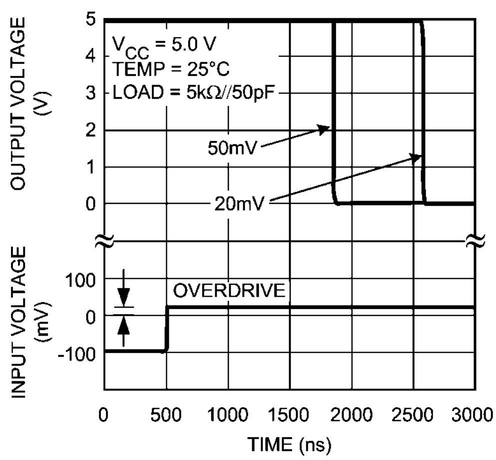
Propagation Delay (t_{PHL})



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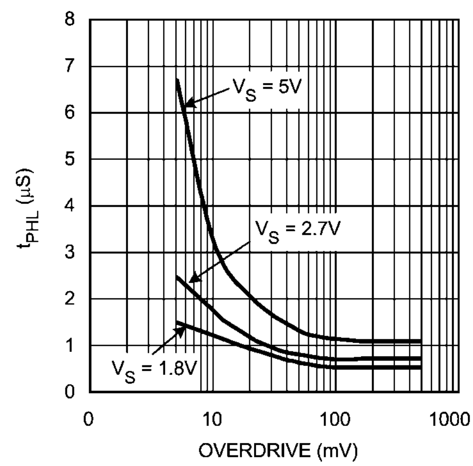
t_{PHL} vs. Overdrive



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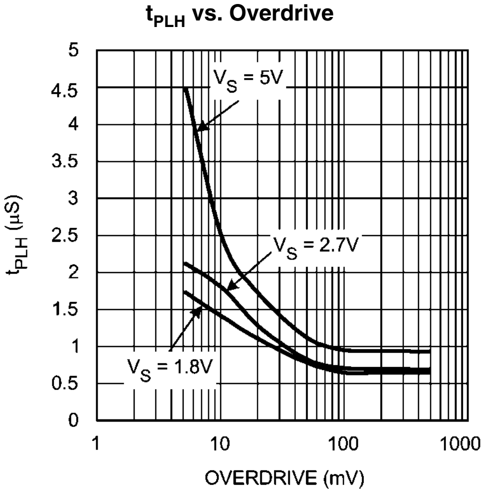
t_{PLH} vs. Overdrive



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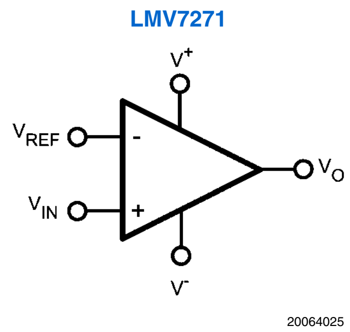
Application Notes

BASIC COMPARATOR

A comparator is often used to convert an analog signal to a digital signal. As shown in *Figure 2*, the comparator compares an input voltage (V_{IN}) to a reference voltage (V_{REF}). If V_{IN} is less than V_{REF}, the output (V_O) is low. However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high.



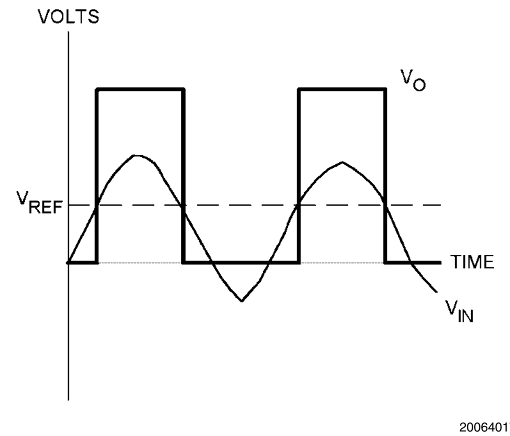


FIGURE 2. LMV7271 Basic Comparator

RAIL-TO-RAIL INPUT STAGE

The LMV727X has an input common mode voltage range (V_{CM}) of –0.1V below the V– to 0.1V above V+. This is achieved by using paralleled PNP and NPN differential input pairs. When the V_{CM} is near V+, the NPN pair is on and the PNP pair is off. When the V_{CM} is near V–, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from V+. Since each input stage has its own offset voltage (V_{OS}), the V_{OS} of the comparator becomes a function of the V_{CM}. See curves for V_{OS} vs. V_{CM} in Typical Performance Characteristics section. In application design, it is recommended to keep the V_{CM} away from the crossover point to avoid problems. The wide input voltage range makes LMV727X ideal in power supply monitoring circuits, where the comparators are used to sense signals close to ground and power supplies.

OUTPUT STAGE

The LMV7271 and LMV7272 have a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum. The only current consumed is the low supply current and the current going directly into the load. When the output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between V+ and V– through output transistors. The result is a short spike of current (shoot-through current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See section for supply bypassing in the Application Notes for details.

HYSTERESIS

It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier of its own noise.

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V_{CC} of the comparator (*Figure 3*). When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1||R_3$ in series with R_2. The lower input trip voltage V_{A1} is defined as

$$V_{A1} = \frac{V_{CC}\,R_2}{(R_1||R_3) + R_2}$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low and very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{A2} is defined as

$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)}$$

The total hysteresis provided by the network is defined as

$$\Delta V_A = V_{A1} - V_{A2}$$

A good typical value of ΔV_A would be in the range of 5 to 50mV. This is easily obtained by choosing R_3 as 1000 to 100 times ($R_1||R_2$) for 5V operation, or as 300 to 30 times ($R_1||R_2$) for 1.8V operation.

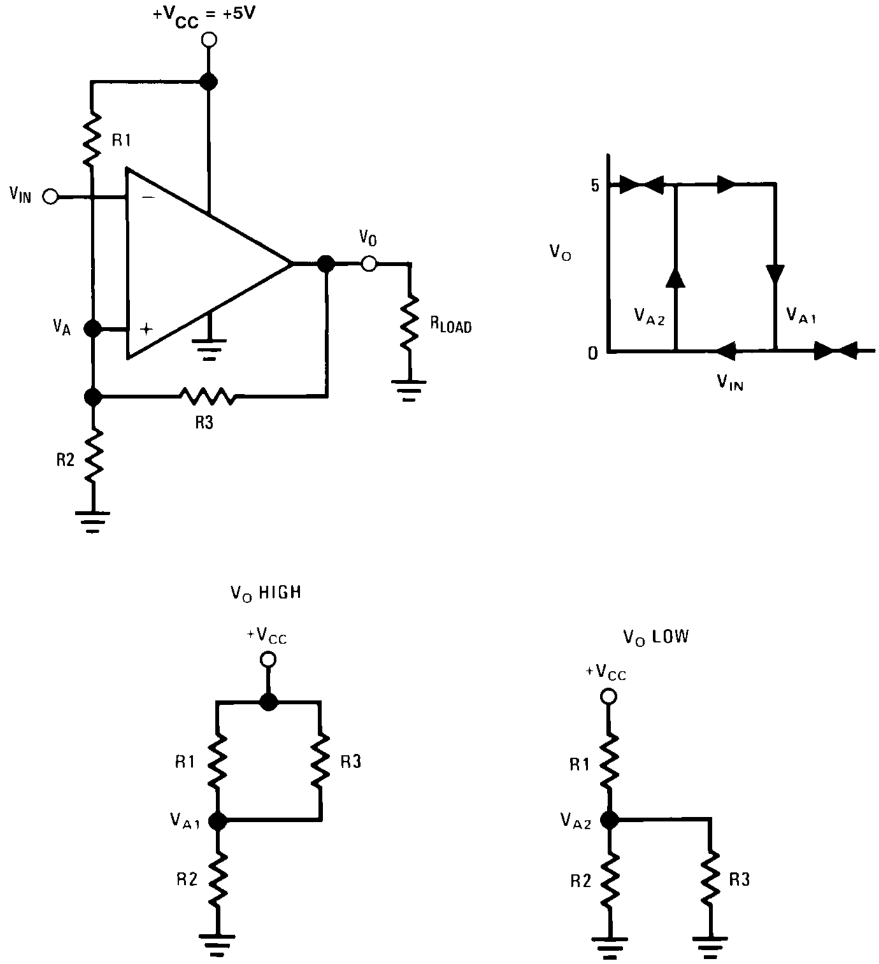


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FIGURE 3. Inverting Comparator with Hysteresis

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input (*Figure 4*). When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}, where V_{IN1} is calculated by

$$V_{in1} = \frac{V_{ref}\,(R_1 + R_2)}{R_2}$$

When V_{IN} is high, the output is also high. To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN} can be calculated by:

$$V_{in2} = \frac{V_{ref}\,(R_1 + R_2) - V_{CC}\,R_1}{R_2}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC}R_1/R_2$$

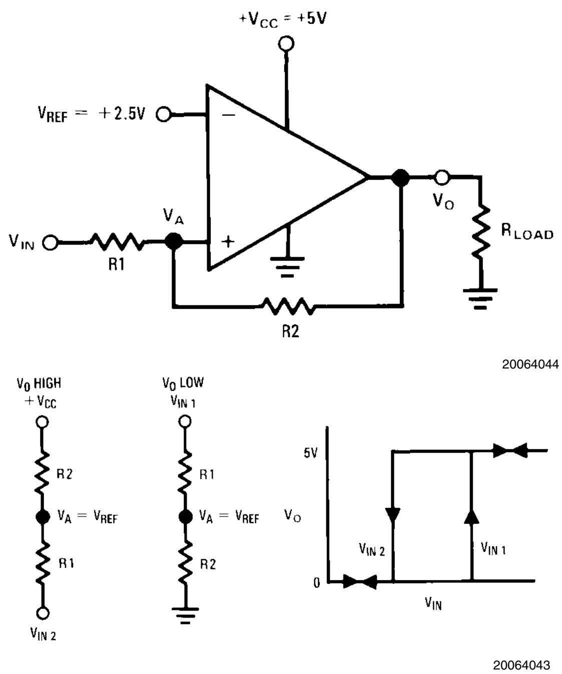


FIGURE 4. Non-Inverting Comparator with Hysteresis

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to misoperate. To avoid problems, a small bypass capacitor, such as 0.1uF ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8µF or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In dual supply application, a 0.1µF capacitor is recommended to be placed across V+ and V− pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed circuit board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard. This can be achieved by running a topside ground plane between the output and inputs. A typical PCB layout is shown in *Figure 5*.

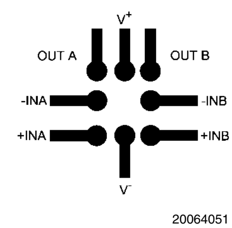


FIGURE 5. Typical PCB Layout

5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.
6. All pins of any unused comparators should be tied to the negative supply.

micro SMD LIGHT SENSITIVITY

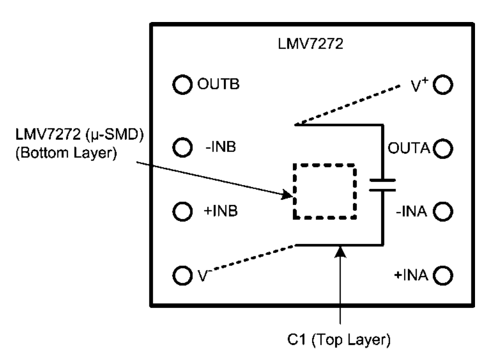
Exposing the micro SMD device to direct sunlight will cause mis-operation of the device. Light sources such as Halogen lamps can also affect electrical performance if brought near to the device. The wavelengths, which have the most detrimental effect, are reds and infrareds.

micro SMD MOUNTING

The micro SMD package requires specific mounting techniques, which are detailed in National Semiconductor Application Note AN-1112.

LMV7272 micro SMD to DIP Conversion Board

To facilitate characterization and testing, a micro SMD to DIP conversion board, LMV7272TLCONV, is available. It is a 2-layer board, with the LMV7272 mounted on the bottom layer, and a capacitor (C1, between the positive and negative supplies) added to the top layer.



LMV7272TLCONV Diagram

Typical Applications

UNIVERSAL LOGIC LEVEL SHIFTER

The output of LMV7275 is an unconnected drain of an NMOS device, which can be pulled up, through a resistor, to any desired output level within the permitted power supply range. Hence, the following simple circuit works as a universal logic level shifter, pulling up the signal to the desired level.

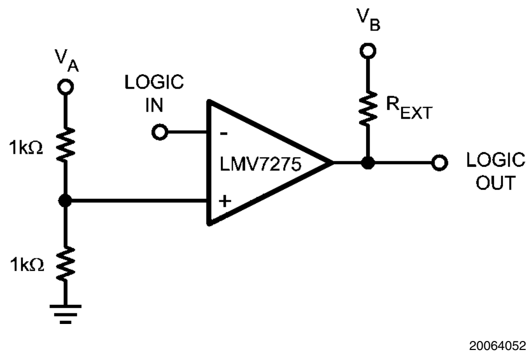


FIGURE 6. Logic Level Shifter

POSITIVE PEAK DETECTOR

A positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to maintain the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the pull-up resistor, and a 1MΩ resistor added in parallel to the capacitor to provide a high impedance discharge path. When the input V_{IN} increases, the inverting input of the comparator follows it, thus charging the capacitor. When it decreases, the cap discharges through the 1MΩ resistor. The decay time can be modified by changing the resistor. The output should be accessed through a follower circuit to prevent loading.

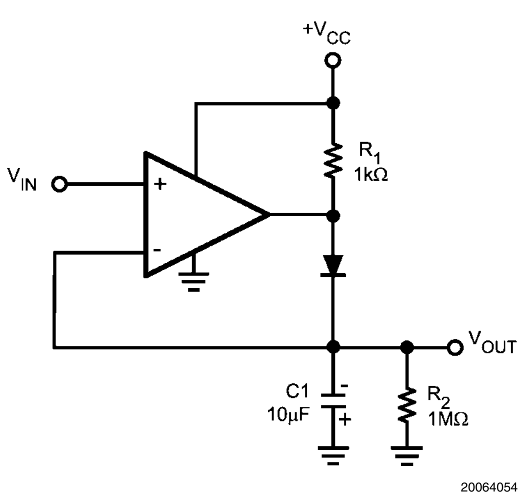


FIGURE 7. Positive Peak Detector

OR'ING THE OUTPUT

Since the output is an unconnected NMOS drain, many drains can be tied together, pulled up to V_{DD} by a single resistor to provide an output OR'ing function. If any of the comparator outputs is pulled low the output V_O goes down.

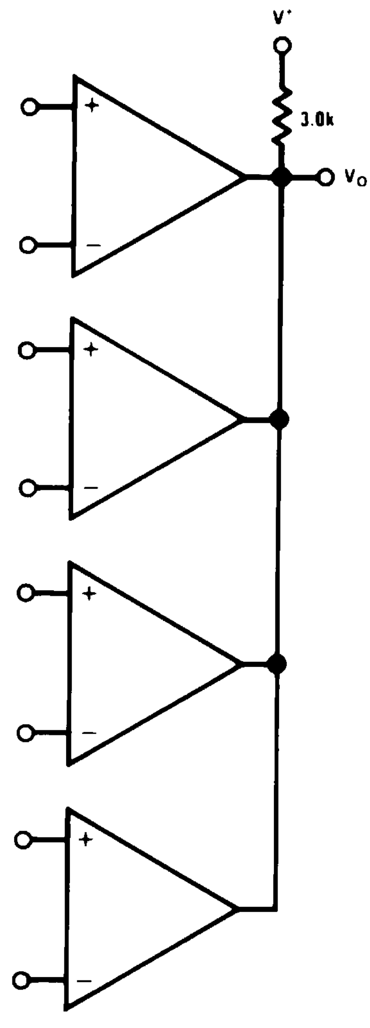


FIGURE 8. OR'ing the Outputs

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. Since there is no pull-up resistor, the only discharge path will be the 1MΩ resistor and any load impedance used. Decay time is changed by varying the 1MΩ resistor.

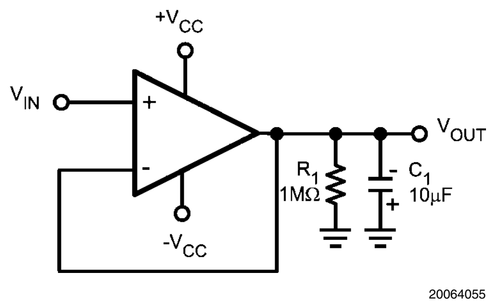


FIGURE 9. Negative Peak Detector

SQUARE WAVE GENERATOR

A typical application for a comparator is as a square wave oscillator. The circuit below generates a square wave whose period is set by the RC time constant of the capacitor $C_1$and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

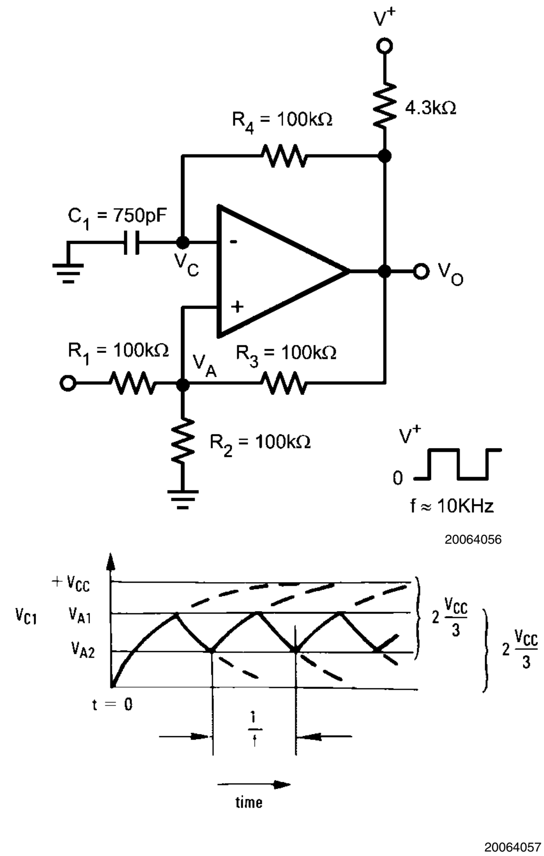


FIGURE 10. Squarewave Oscillator

To analyze the circuit, consider it when the output is high. That implies that the inverted input (V_C) is lower than the non-inverting input (V_A). This causes the C_1 to get charged through R_4, and the voltage V_C increases till it is equal to the non-inverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 || R_3}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

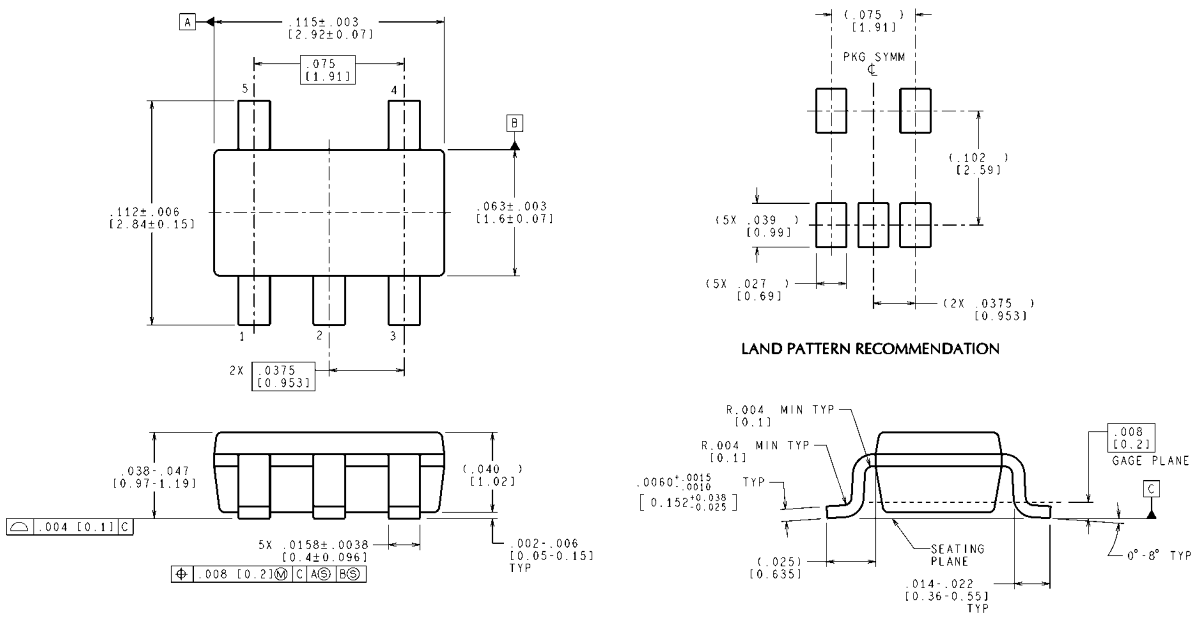
$$V_{A2} = \frac{V_{CC}\,(R_2 || R_3)}{R_1 + (R_2 || R_3)}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by R_4C_1.ln2. Hence the formula for the frequency is:

$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2)$

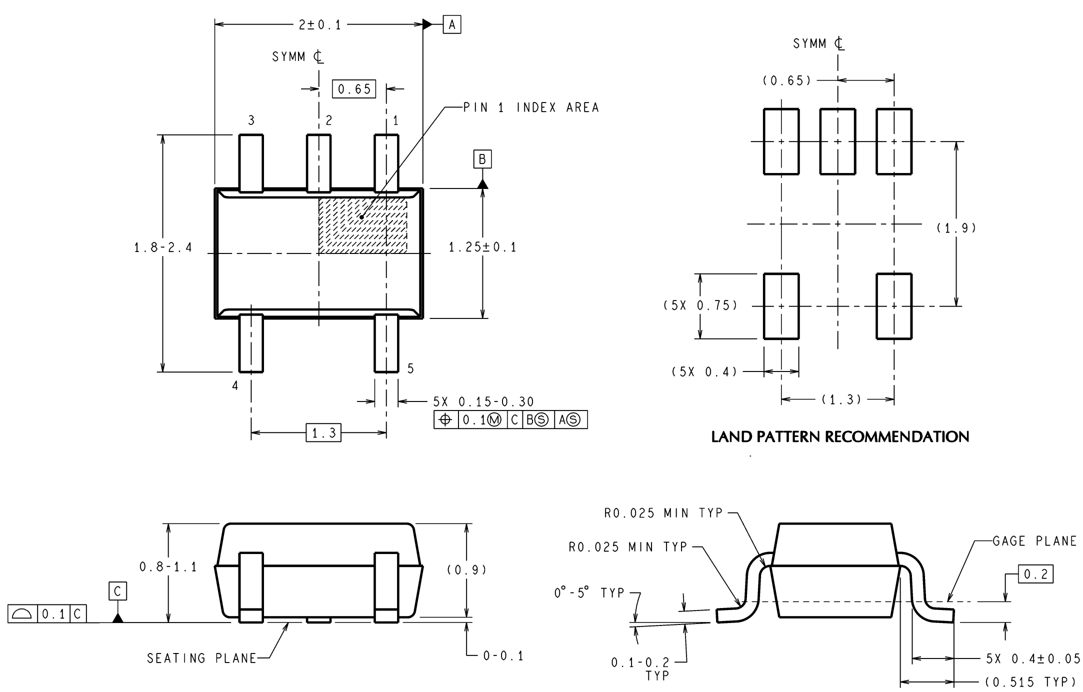
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MF05A (Rev D)

5-Pin SOT-23
NS Package Number MF05A



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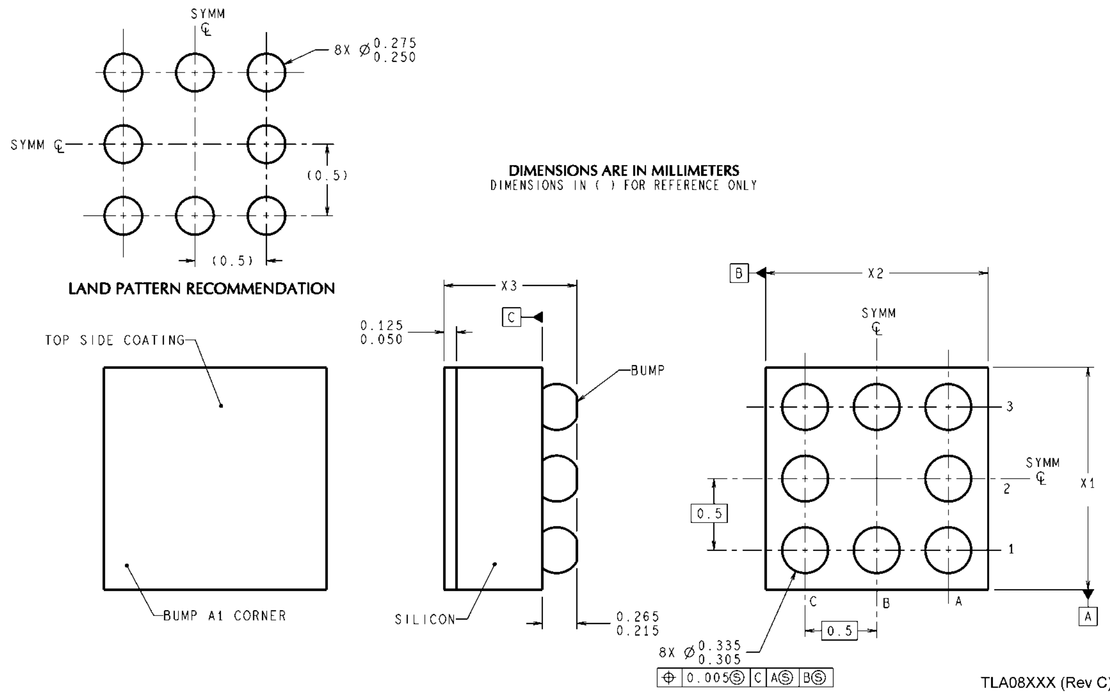
MAA05A (Rev D)

5-Pin SC-70
NS Package Number MAA05A



NOTE: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD
NS Package Number TLA08AAA
X1 = 1.514mm X2 = 1.514mm X3 = 0.600mm

Notes

Notes

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