AN966

Interfacing SPI™ Serial EEPROMs to Microchip PICmicro® Microcontrollers

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INTRODUCTION

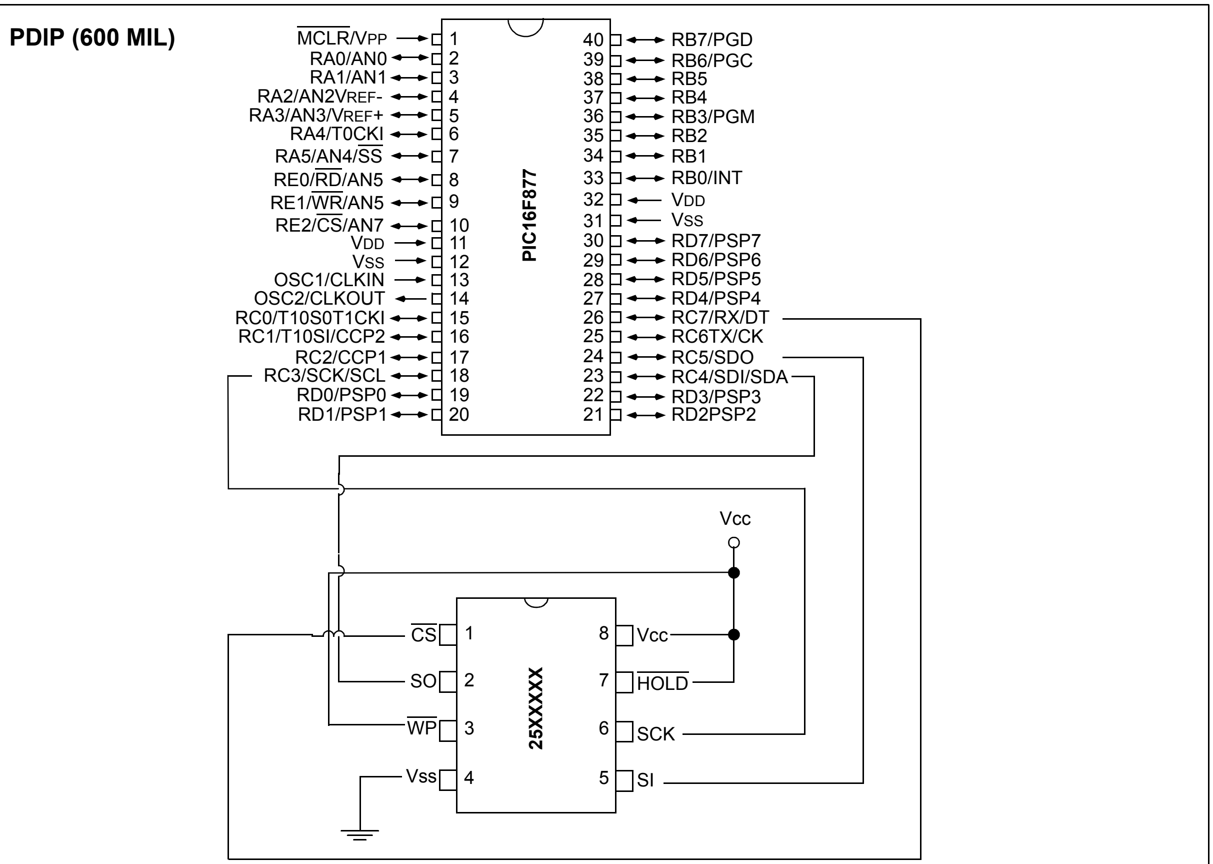
There are many different microcontrollers on the market today that are being used in embedded control applications. Many of these embedded control systems need nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low power consumption, and low cost, serial EEPROMs are a popular choice for nonvolatile storage.

Microchip Technology has addressed these needs by offering a full line of serial EEPROMs covering industry standard serial communication protocol for two-wire (I2C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges and packaging options.

This application note provides assistance and source code to ease the design process of interfacing a Microchip mid-range PIC16F877 microcontroller to a Microchip SPI serial EEPROM. The hardware SPI port on the microcontroller Master Syncronous Serial Port (MSSP) provides a simple three-wire connection to the EEPROM with no external "glue" logic.

Figure 1 describes the hardware schematic for interfacing between Microchip's SPI memories and the Microchip PIC16F877 microcontroller. The software was written assuming these connections.

FIGURE 1: CIRCUIT FOR PIC16F877 AND 25XXX SERIES DEVICES



Note: CS, WP and HOLD pins should all have pull-up resistors (~10k ohms).

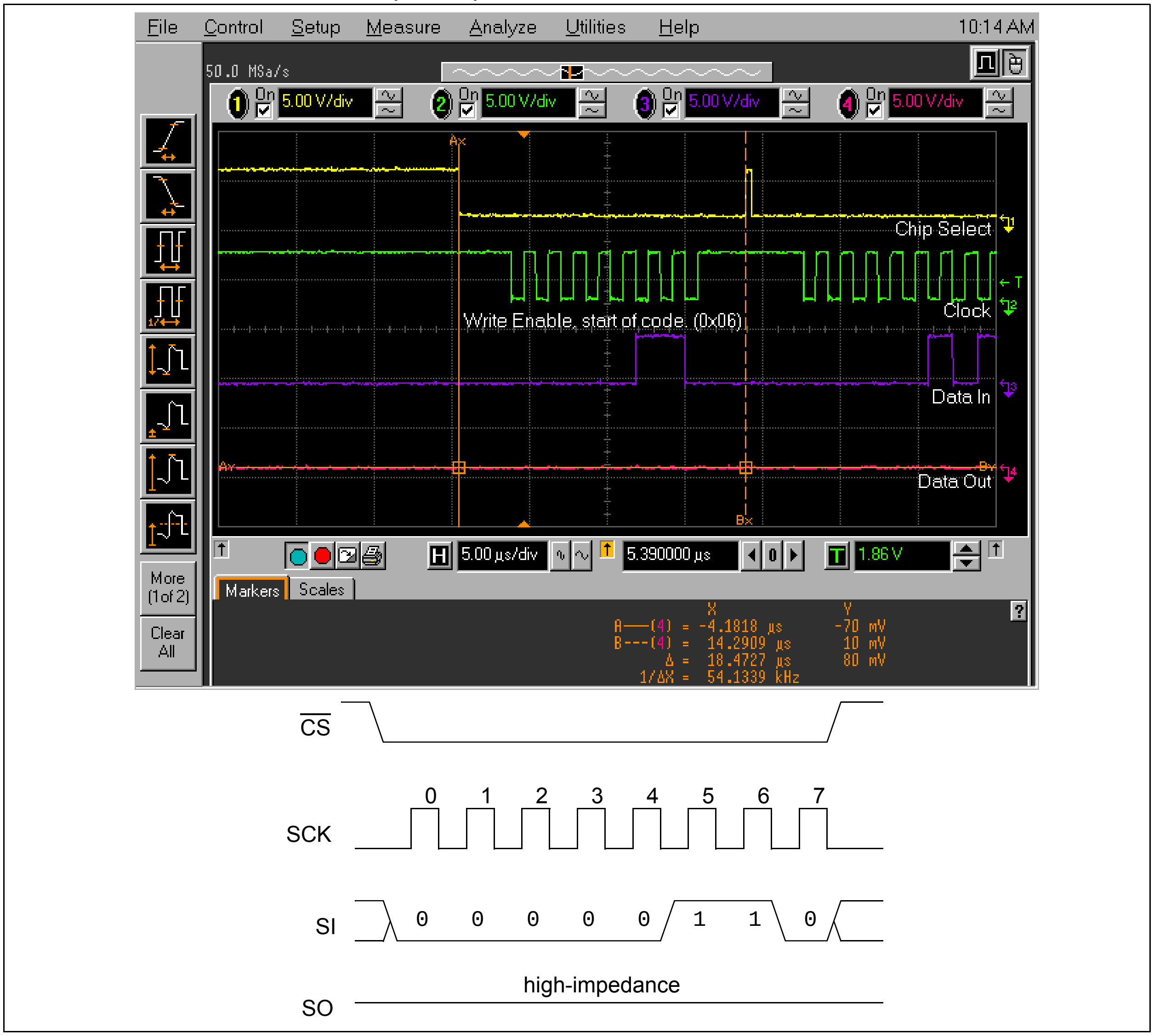
FIRMWARE DESCRIPTION

The program shows individual features of the SPI protocol and gives code samples of opcodes so that basic building blocks of a system can be put together for rapid deployment of electronics using SPI EEPROMs. The opcodes used in the program are Write Enable (WREN), Write, Read, Read Status Register (RDSR) (used in the program for WIP (Write-in-Process) polling), and Write Disable (WRDI). The oscilloscope pictures have markers that are shown from $\overline{CS}$ enable to $\overline{CS}$ disable for ease in reading. The data sheet version of the waveform is below the actual oscilloscope picture. The MSSP module is set up for Mode 1,1 operation at approximately 625 kHz. The code is written in modules and commented so changing modes, speeds, and modifying commands, such as sequential reads and page writes, are simple. The values represented in this application note are all hex values.

WRITE ENABLE

Figure 2 shows an example of the Write Enable command. Chip Select is brought low (active) and the opcode is sent out through the MSSP port. The Write Enable command must be given before a write is attempted to either the array or the Status Register. The WEL bit can be cleared by issuing a Write Disable command (WRDI), or it is automatically reset if the device is powered down or a write cycle is completed. Instances of this command can be found in the firmware by searching for “WREN”.

FIGURE 2: WRITE ENABLE (WREN)

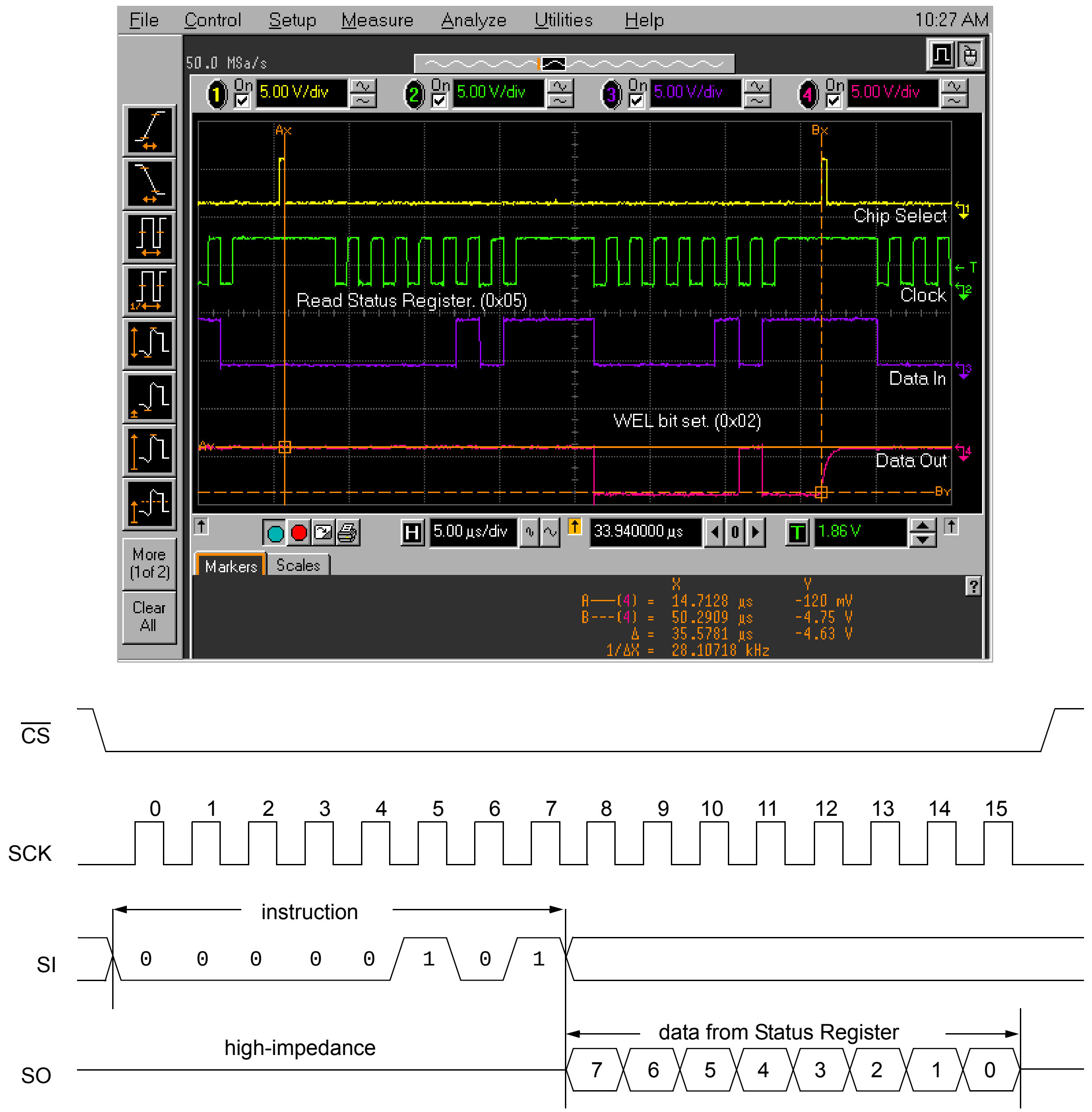


READ STATUS REGISTER TO CHECK FOR WEL BIT

Figure 3 shows an example of the Read Status Register command to check for the Write Enable Latch (WEL) bit. The WEL bit must be set before a write is attempted to either the Status Register or the array. It is good programming practice to check for the bit to be set before attempting the write.

Once again the device is selected using $\overline{\text{CS}}$ and the opcode 0x05 is received. Although it appears that the opcode is received twice, the second 8 bits are "don't cares" on the Data In pin and act as a "dummy byte" just to provide clock signals so that the Status Register can be shifted out on the Data Out pin. A value of 0x02 shows that the WEL bit in the Status Register has been set. The device is now ready to do a write on either the Status Register or the array.

FIGURE 3: READ STATUS REGISTER TO CHECK FOR WEL BIT (RDSR)

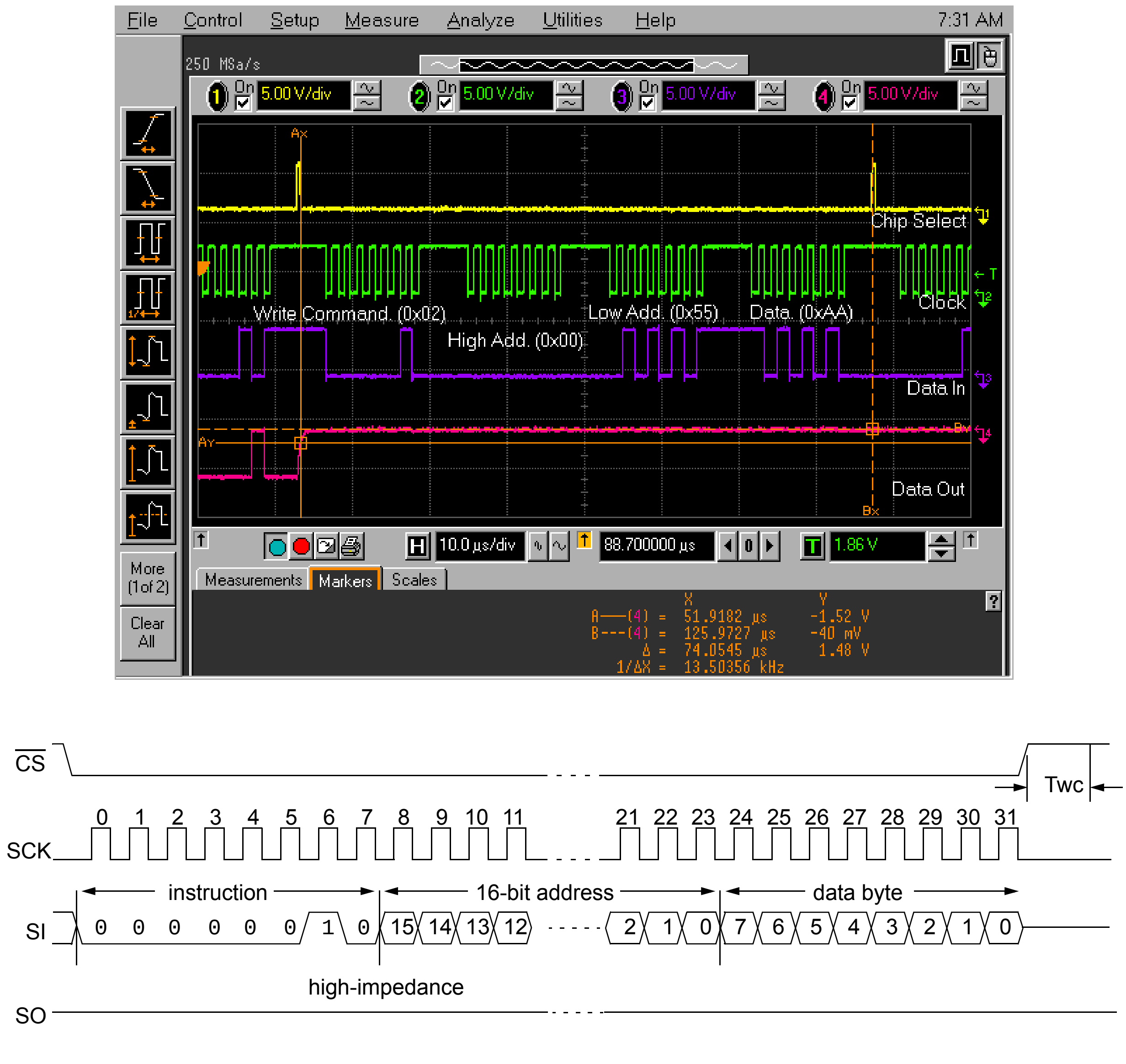


WRITE COMMAND (OPCODE, ADDRESS AND DATA)

Figure 4 shows an example of the Write command. For this waveform the device is selected and the opcode 0x02 is received. The High Address byte receives 0x00 followed by the Low Address byte 0x55. Finally, the data is clocked in which is 0xAA.

Once the Chip Select is toggled at the end of this command, the internal write cycle is initiated. After the internal write cycle has begun, the WIP bit in the Status Register can now be polled to check when the write finishes, or a delay needs to be added to the microcontroller firmware (~5ms) if the WIP bit is not being polled. This code uses WIP polling.

FIGURE 4: WRITE COMMAND, ADDRESS AND DATA

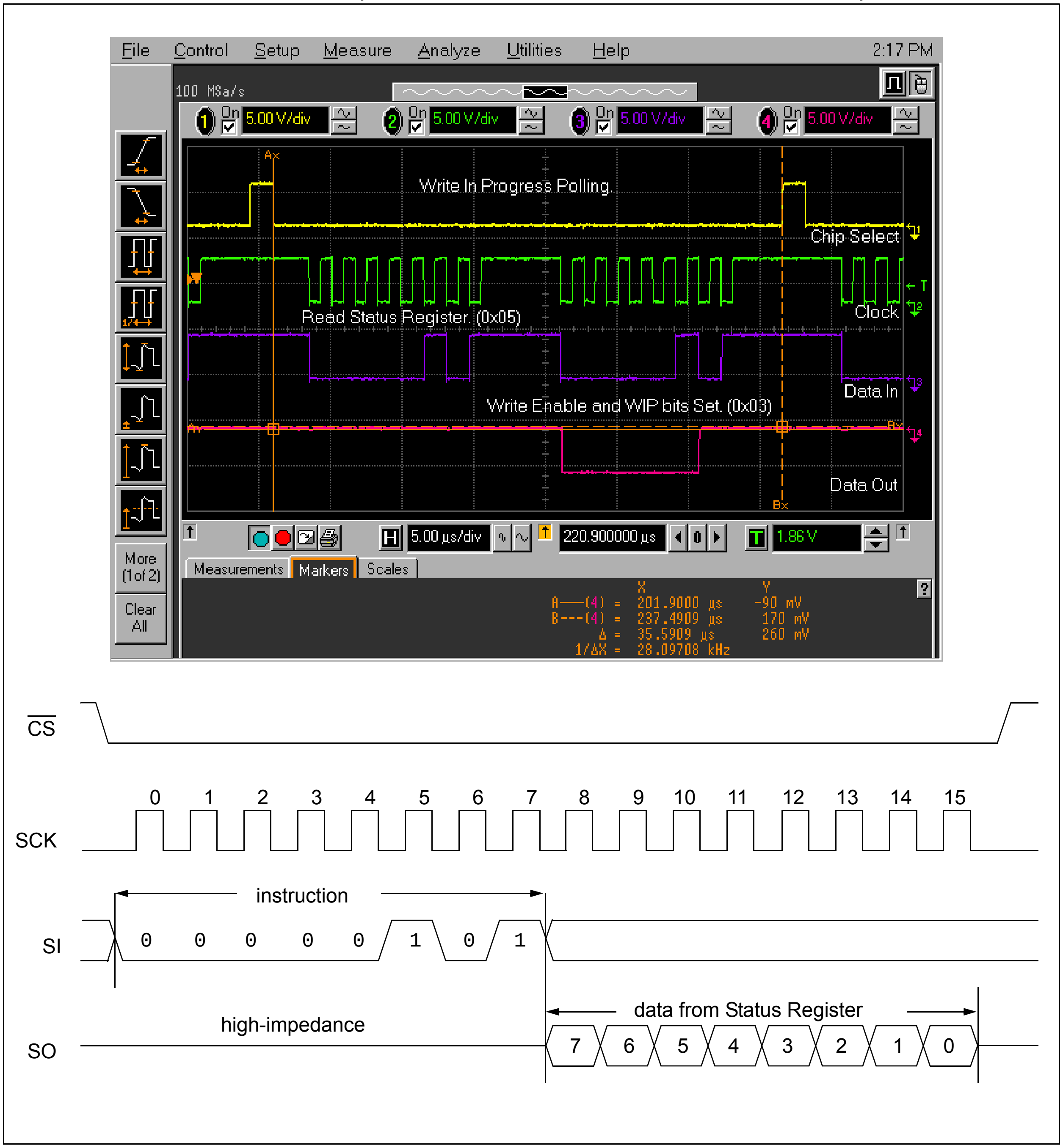


DATA POLLING (RDSR – CHECK FOR WIP SET)

After a valid Write command is given, the Status Register can be read to check if the internal write cycle has been initiated. It can also be monitored continuously to look for the end of the write cycle. In this case, the device is selected and the opcode 0x05 is received.

The Status Register contents are then shifted out on the Data Out pin, resulting in a value of 0x03. Figure 5 shows that both the WEL bit (bit 1) and the WIP bit (bit 0) are set (0x03), meaning the write cycle is in progress.

FIGURE 5: DATA POLLING (READ STATUS REGISTER TO CHECK WIP BIT)

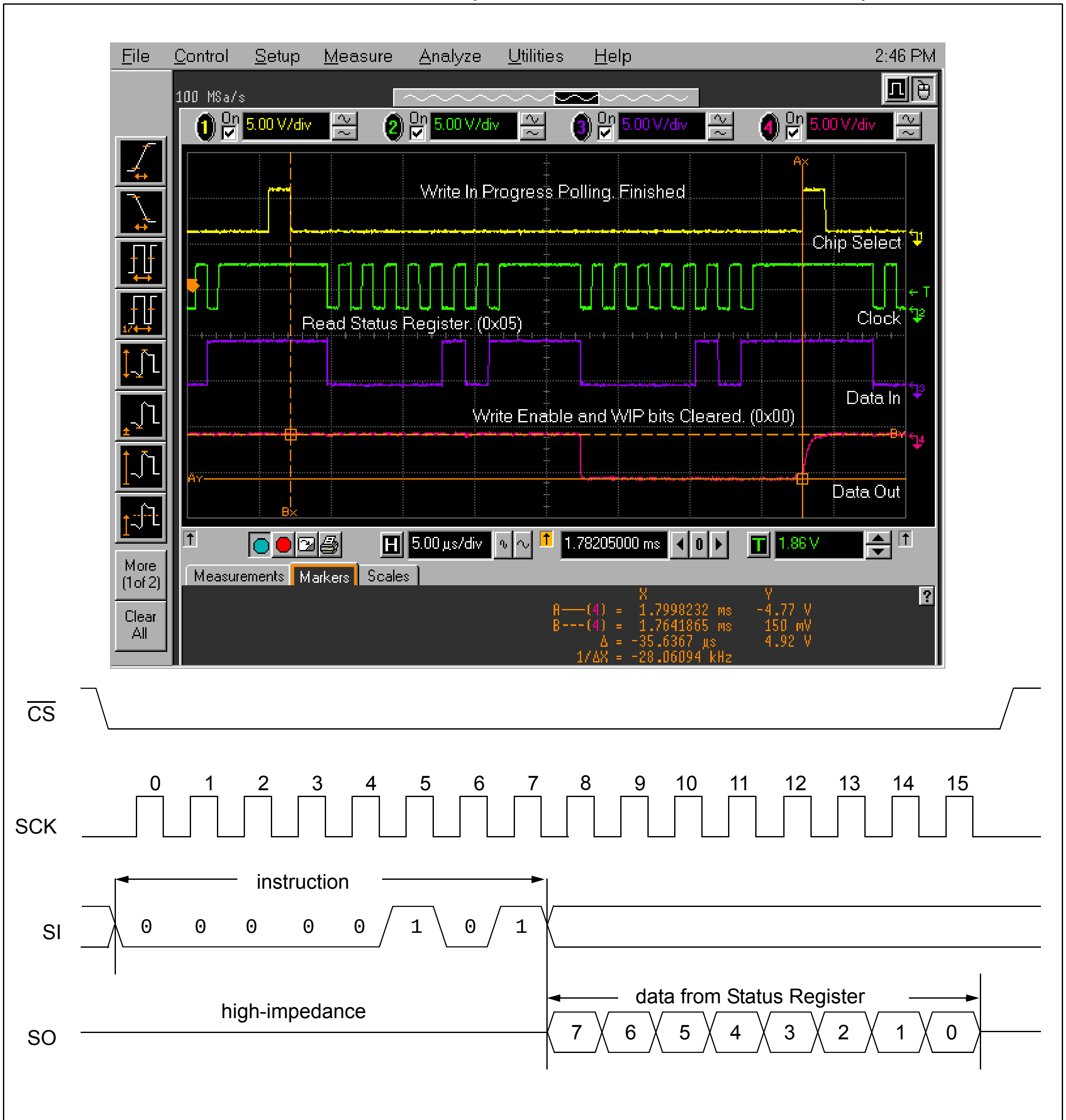


DATA POLLING FINISHED (RDSR – WIP BIT CLEARED)

The code was written to stay in a continuous loop and evaluate the status Register until the WIP bit is cleared. Figure 6 shows the Status Register Read command followed by a value of 0x00 being shifted out on the Data Out pin.

This indicates that the write cycle has finished and the EEPROM is now ready for additional commands. The WEL bit is also cleared at the end of a write cycle. This serves as additional protection against unwanted writes.

FIGURE 6: DATA POLLING FINISHED (RDSR – WIP & WEL BITS CLEARED)

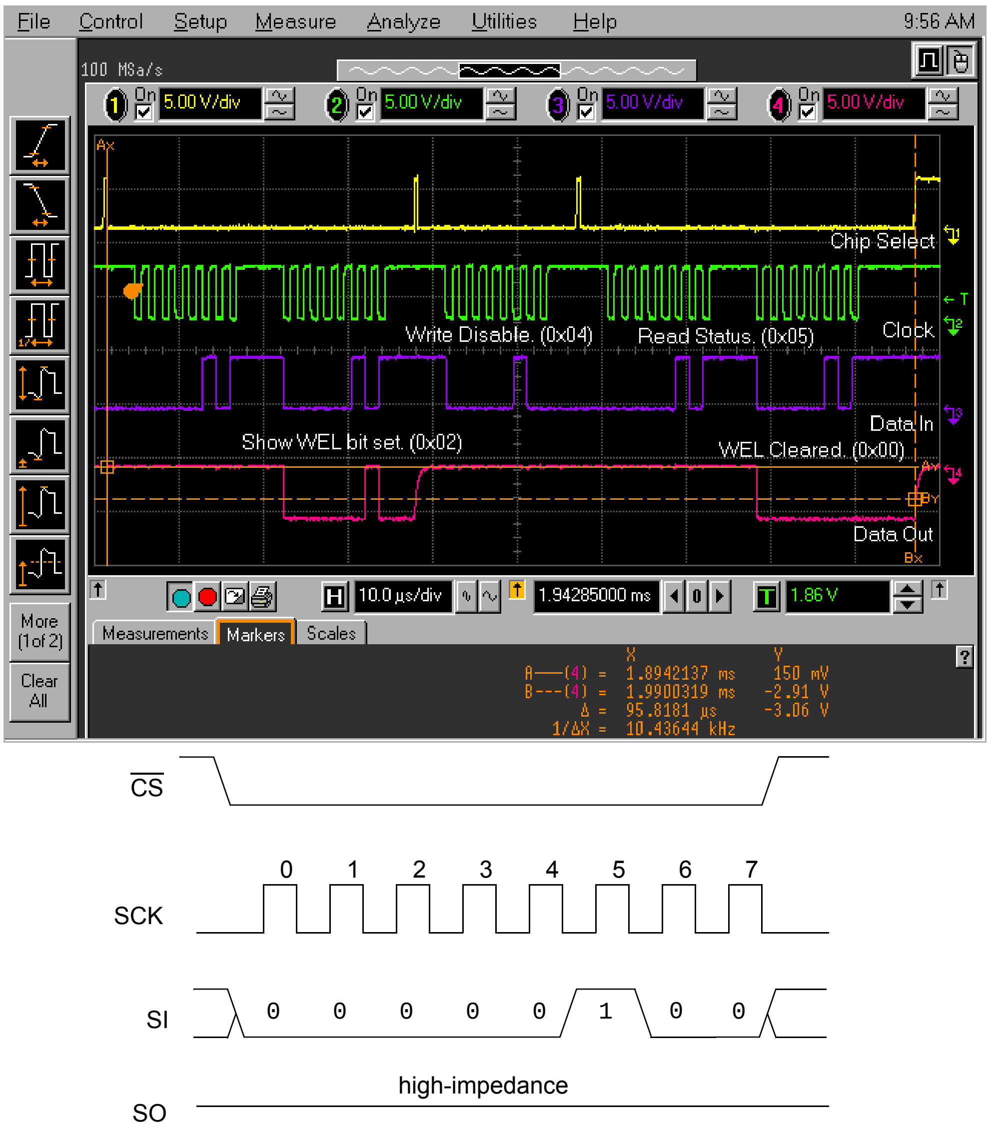


WRITE DISABLE COMMAND

Previously, we showed a Status Register Read to illustrate the WEL bit being set. Figure 7 shows the WEL being set followed by the WRDI command.

The Status Register is then read and indicates that the WEL bit has been cleared and the device will no longer accept Write commands to either the array or the Status Register.

FIGURE 7: RDSR FOR WEL SET AND THEN CLEARED AFTER WRDI COMMAND



CONCLUSION

This is an application note of the basic features of SPI communications using the MSSP module on one of Microchip's mid-range devices. The code is highly portable and can be used on many devices that have the MSSP module, possibly with very minor modifications. Using the code provided, designers can begin to build their own SPI libraries to be as simple or complex as needed. The code was tested on Microchip's PICDEM™ 2 Plus Demonstration Board with the connections shown in Figure 1.

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