SN74LVC2G157 SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCES207K-APRIL 1999-REVISED JANUARY 2007

FEATURES

- Available in the Texas Instruments
 NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{nd} of 6 ns at 3.3 V

GND [

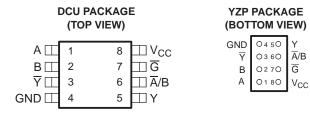
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C

5

 \neg Y

Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C

- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G157 features a common strobe (\overline{G}) input. When the strobe is high, Y is low and \overline{Y} is high. When the strobe is low, a single bit is selected from one of two sources and is routed to the outputs. The device provides true and complementary data.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC2G157YZPR	C3_
-40°C to 85°C	SSOP - DCT	Reel of 3000	SN74LVC2G157DCTR	C57
	VCCOR DCII	Reel of 3000	SN74LVC2G157DCUR	CE7
VSSOP – DCU	V330F - DC0	Reel of 250	SN74LVC2G157DCUT	C57_

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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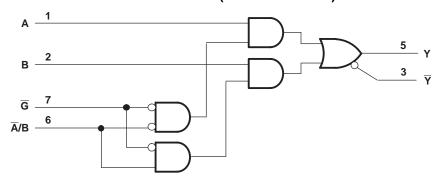
⁽²⁾ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



FUNCTION TABLE

	INP	JTS		OUTPUTS			
G	Ā/B	Α	В	Υ	Y		
Н	Χ	Χ	Χ	L	Η		
L	L	L	Χ	L	Н		
L	L	Н	Χ	Н	L		
L	Н	Χ	L	L	Н		
L	Н	Χ	Н	Н	L		

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the	ne high-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the	ne high or low state (2)(3)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND)		±100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (4)	DCU package		227	°C/W
		YZP package	-0.5 6.5 -0.5 V _{CC} + 0.5 -50 -50 ±50 ±100		
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 ⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.
 (4) The package thermal impedance is calculated in accordance with JESD 51-7.



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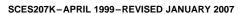
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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
.,	Complements	Operating	1.65	5.5	V
V_{CC}	Supply voltage	Data retention only	1.5		V
\/	High level input voltege	V_{CC} = 2.3 V to 2.7 V	1.7		V
V_{IH}	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		V
	upply voltage Data V_{CC} V_{CC}	V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
	Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
\/	Low level input valtage	V _{CC} = 2.3 V to 2.7 V		0.7	V
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	Output voltage	V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	High-level output current	V 2.V		-16	mA
		V _{CC} = 3 V		-24	
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
	Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 2.V		16	mA
		V _{CC} = 3 V		24	
	Low-level output current	V _{CC} = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1)	MAX	UNIT		
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V _{CC} - 0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
V _{OH}		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V		
		$I_{OH} = -16 \text{ mA}$	3 V	2.4		V		
		$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8				
		I _{OL} = 100 μA	1.65 V to 5.5 V		0.1			
		I _{OL} = 4 mA	1.65 V		0.45			
\/		I _{OL} = 8 mA	2.3 V		0.3	V		
V _{OL}		I _{OL} = 16 mA	3 V		0.4			
		I _{OL} = 24 mA	3 V					
	_	I _{OL} = 32 mA	4.5 V		0.55			
I ₁	A, B, or control inputs	V _I = 5.5 V or GND	0 to 5.5 V		±5	μΑ		
I _{off}		V_I or $V_O = 5.5 \text{ V}$	0		±10	μΑ		
I_{CC}		$V_1 = 5.5 \text{ V or GND}, \qquad I_0 = 0$	1.65 V to 5.5 V		10	μΑ		
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μΑ		
C _i	·	$V_I = V_{CC}$ or GND	3.3 V	5		pF		

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	A or B		4.4	14	2.1	8	2	6	1.4	4	
t _{pd}	Ā/B	Y or ₹	4.9	16	2.5	9	2.1	6	1.6	4	ns
	G		4.2	14	2	8	1.6	6	1.3	4	

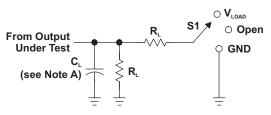
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V V _{CC} = 2.5		$V_{CC} = 3.3 \text{ V}$	V _{CC} = 5 V	UNIT
	PARAMETER	TYP TYP		TYP	TYP	UNIT	
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF

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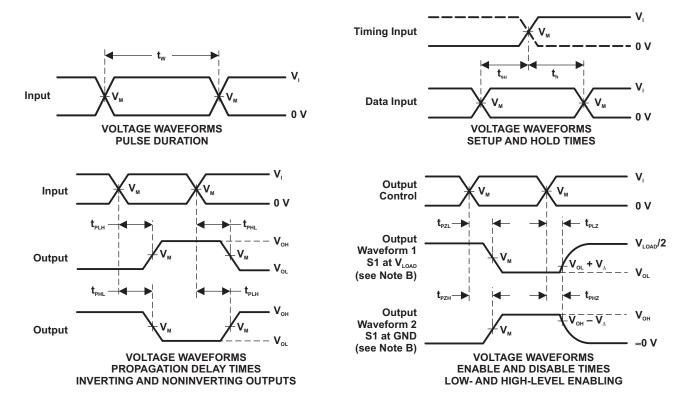
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INF	PUTS	V	V		D	
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _L	V _Δ
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
$2.5~V~\pm~0.2~V$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVC2G157DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC2G157DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC2G157DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC2G157DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC2G157DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G157DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G157DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G157DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G157DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G157YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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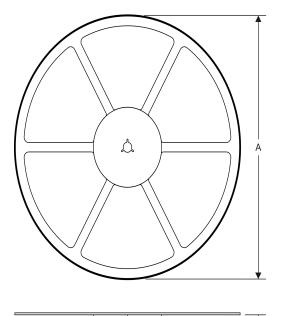
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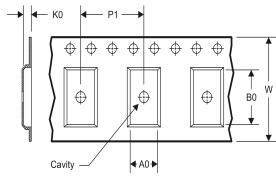
TAPE AND REEL INFORMATION

REEL DIMENSIONS





TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G157YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G157YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



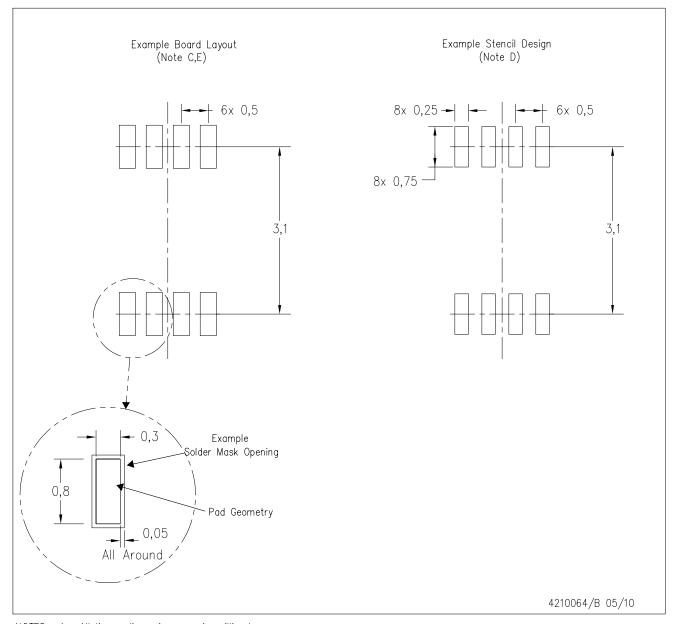
NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



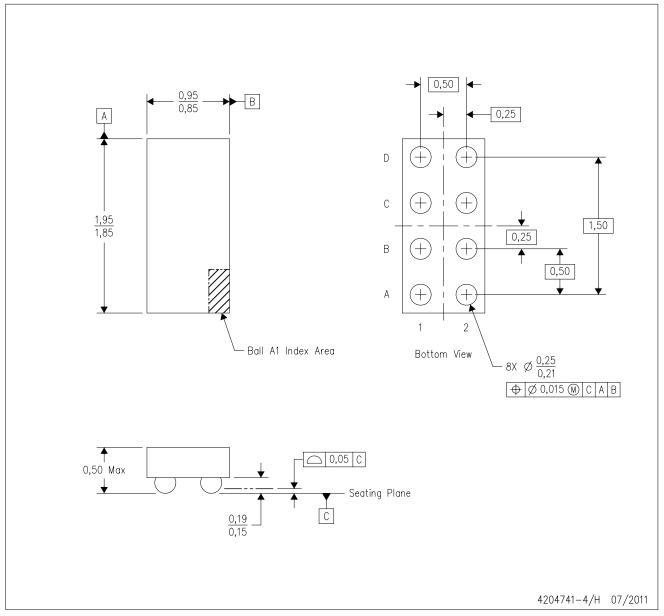
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree $^{\text{TM}}$ package configuration.
- D. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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