DESIGN AND ANALYSIS TECHNIQUES FOR DYNAMIC CURRENT MIRRORS

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To my son Lucien

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RESUME

De nos jours l'électronique fait de plus en plus appel à des circuits digitaux et de ce fait la technologie CMOS (Complementary Metal Oxide Semiconductor) devient dominante. Cette technologie CMOS, comparée à une technologie bipolaire, offre différents avantages, comme des dimensions geométriques réduites et une consommation faible.

Néanmoins le domaine analogique persiste car la nature des phénomènes physiques et leur perception est analogique. Des capteurs électroniques perçoivent ces événements analogiques et délivrent un signal de sortie en conséquence. Avant de pouvoir utiliser ce signal pour un traitement numérique il doit être mis en forme et traité de manière analogique.

Le miroir de courant est un élément fonctionnel de base dans la plupart des blocs analogiques. Il permet de multiplier et dupliquer un courant imposé, qui contient l'information (signal ou polarisation). Malheureusement, à cause des variations aléatoires au cours du processus de fabrication, les paramètres des transistors utilisés dans la réalisation des miroirs de courant sont affectés de différentes erreurs, telles que la variation de la tension de seuil et la variation du paramètre de transfer. Les courants de sortie de deux transistor dessinés identiques sont par conséquent différents.

Ce désappariement entre composants ainsi que le bruit en 1/f sont des limitations principales pour les circuits de haute précision. La technique standard consiste à réduire ces imperfections en augmentant simplement la taille des transistors et à noyer le désappariement des tensions de seuil dans une grande tension de grille.

Les techniques analogiques dynamiques exploitent l'absence de courant de grille d'un transistor MOS pour stocker temporairement une information analogique sur la capacité de grille. En utilisant séquentiellement le même transistor comme transistor d'entrée et de sortie d'un miroir de courant, la notion de désappariement disparaît. Cette technique d'échantillonnage permet d'augmenter la précision considérablement et de la pousser vers de nouvelles limites indépendantes de l'appariement entre transistors, donc des

variations du processus de fabrication. La précision des courants dépend alors de la capacité à mémoriser de manière exacte le signal.

L'idée de mémoriser des courants a été formulée il y a plus de dix ans déjà, mais il a fallu attendre l'avancement de la théorie sur les échantilloneurs-bloqueurs et le progrès de la technologie pour voir la première réalisation pratique performante d'un de ces circuit intégrés vers le début de 1988.

Cette thèse formule, étudie et analyse les différents aspects, possibilités, paramètres et limitations liés à ce nouveau type de miroirs de courant, appelés aussi copieurs de courants, qui repose sur un échantillonage de la tension de grille d'un transistor MOS. Des résultats expérimentaux permettent de mettre en évidence l'influence des améliorations proposées.

Le principe de mémorisation ainsi que les problèmes majeurs apparaissant lors de la commutation des transistors sont décrits. Des structures minimisant ces effets indésirables sont proposées, leurs avantages et désavantages comparés et des extensions possibles sont présentées. Les paramètres qui influencent la précision sont étudiés en détail, tel que les variations de la tension de drain, les courants de fuites, l'injection de charge, le bruit blanc et le bruit en 1/f. Les transitoires engendrés lors des commutations ainsi que le comportement dynamique d'une cellule de base sont analysés, et un compromis entre la précision et la vitesse en est déduit. Des considérations pratiques au sujet du "layout" sont énumérées et des résultats expérimentaux résument l'influence des différents paramètres. Le miroir de courant dynamique est implementé dans un filtre continu afin d'augmenter l'appariement des fréquences centrales. Finalement, des applications tels que filtre à courant commutés et convertisseur D/A & A/D sont mentionées.

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CHAPTER 1

INTRODUCTION

In this introductory chapter the principal motivations associated with this PhD thesis, the design and analysis techniques for dynamic current mirrors, are highlighted. The errors affecting a current mirror due to the imperfections of the MOS devices are shown and well known circuit techniques developed to overcome such limitations are presented. The published results of other research laboratories working on this subject are reviewed, and finally in the conclusion of this chapter the aim and structure of this thesis are outlined.

Today's world of electronics becomes more and more digital and therefore CMOS becomes the dominant technology. A CMOS process compared to a bipolar process offers several advantages, mainly a low power consumption which is important for portable systems powered by batteries or for large systems. Another point is the smaller device geometries, which increase the number of gates that can be packed on a single chip.

Parallel to the increasing digital domain the analog field persists, because the origin of physical phenomenons and their perception is analog. Electronic sensors perceive these analog events and deliver a corresponding output signal. If this analog signal is not suitable for digital processing some analog preconditioning must be done [YEN82]. Combining both types of signal processing on the same chip to obtain the best possible performances is therefore desirable [MID84].

CMOS technology has led to a wide use of voltages and charge transfers for signal processing. As the feature sizes shrink a lower supply voltage is imposed, which reduces the dynamic voltage range of the circuits. Because process parameters are chosen to optimize digital performances, the analog functional blocks have to adapt themselves to the restricted voltage range.

Current mode circuits offer a solution to these problems as they require only a baseline digital process and avoid many of the anticipated low voltage problems by operating in the current domain [HUG89]. Due to the non-linear current-voltage relationship the dynamic range of current-mode signals is larger than that of voltage-mode signals. Therefore the current mode approach can provide attractive and elegant solutions for many circuit and system problems [TOU90].

A ubiquitous elementary building block in most analog integrated circuits is the current mirror which is able to multiply and duplicate an imposed input current, that contains the information (bias or signal). The reproduced output current of is then available for any subsequent processing. Unfortunately, due to random process variations, transistor parameters are affected by a certain variation of the transconductance parameter and of the threshold voltage [SHY84], [LAK86]. Hence, the output currents of transistors which have been designed identically are different.

These random variations, the so-called devices mismatch, are a major limitation for most accurate and precise current mode circuit applications.

Another main limitation of CMOS circuits is the 1/f flicker noise of the MOS transistors. The standard technique to reduce this 1/f noise and the error due to mismatch is to increase the transistor area and to overwhelm the threshold mismatch with a high gate voltage overhead, which simultaneously increases the saturation voltage of the devices.

The performance of a mirror with low saturation voltage can be improved by using lateral bipolar transistors [VIT83]. The resulting current error can be lower than 1%, but the major handicap is that only one type of mirror can be built (source or sink depending on the technology used).

Special circuit techniques allow us to reduce the inherent noise and offset in MOS amplifiers, like the chopper technique [HSI81], [ENZ89], and the auto-zero technique [YEN82], [DEG85]. The auto-zero technique is also used to ensure adequate biasing of CMOS inverters or analog-to-digital converters [CAN82]. Dynamic element matching [VdP76] is based on the chopper technique and shifts the error components to higher frequencies. The drawback of this technique is the high residual output ripple, which for most applications must be filtered out by using external components. Furthermore multiple mirrors are difficult to implement.

Dynamic analog techniques [VIT85.1] exploit the absence of gate current to temporarily store some analog information on the gate capacitance of the MOS device. A reported application of this analog storage capability is the dynamic comparator [YEE78] which sequentially uses the same transistor as the two devices of a differential pair. With this auto-zero technique the very notion of mismatch disappears. The achievable precision is moved to new limits and depends on the capability of accurately storage the signal, mainly limited by charge injection from the MOS transistors used as switches.

Although the idea of current sampling was formulated over ten years ago [OGU78], the first accurate implementation dates from 1988, because the circuit theory and process technology did not allow researchers to obtain the expected results. In the "Electronics Letters" issue of December 1988 [DAU88] published the idea and some simulated results, which induced a series of publications during the year of 1989. Several research laboratories have focused on the subject during the last few years, with the reported results of [GRO89] concerning D/A converters, [NAI89.2] for A/D converters, [HUG89] for current mode circuits and filters, and ourselves [VIT88], [WEG89.1] for dynamic current mirrors.

The primary objective being pursued in this dissertation is to investigate the different possibilities, to design and to analyze the performances and limitations of a new type of current mirror, a so-called dynamic mirror or current copier. The goal is to build highly accurate current mirrors in the simplest and most compact way. The best strategy for a given problem can be chosen only if all parameters influencing the circuit performances are known.

The outline of this thesis is the following:

Chapter 2 presents the principle of memorization of a current copier. The main limitations which influence the achievable accuracy are deduced and cell structures which reduce these effects derived.

In **Chapter 3** the principle and the different configurations of dynamic current mirrors are extensively described, and their advantages and disadvantages discussed and compared. Possibilities of realizing multiple, multiplying and dividing current mirrors are highlighted.

Chapter 4 provides a deeper look at the different parameters, which limit the accuracy of a dynamic current mirror, namely drain voltage variations, leakage currents, noise and charge injection. The sampling of white noise and 1/f noise is analyzed and their contribution calculated. The influence of charge injection is evaluated and the interfering parameters shown.

The transient behavior is considered in **Chapter 5**, where the output spikes and the trade-off between speed and accuracy are highlighted.

Chapter 6 emphasizes layout considerations and the practical implementation of a dynamic current mirror.

Chapter 7 summarizes the experimental results obtained with such mirrors.

Chapter 8 deals with the different possible applications, focusing on a continuous time filter. The principle of D/A & A/D converters and switched current filters are outlined, and the extension to other functional blocs is suggested.

Finally **Chapter 9** provides summarizing remarks and conclusions.

A **Bibliography** where all the references mentioned in this thesis are listed in an alphabetical order is put at the end.

In **Appendix** A the MOS model, characteristics and definitions used in this thesis are listed, whereas **Appendix B** calculates the roots of the principal denominator of the transfer functions found in a dynamic current mirror. In **Appendix C the** mathematics used for noise calculations are considered. **Appendix D** describes the charge injection model used in this work. It is based on the analysis described in [WEG87].

These appendices are not absolutely necessary for the comprehension of the text, and are put in appendix to facilitate the reading.

CHAPTER 2

PRINCIPLE & STRUCTURES

of CURRENT COPIERS

The principle of memorizing and reproducing a current imposed by an external current source is introduced in this chapter. The notion of current copiers is defined and the parameters influencing the current accuracy are highlighted. Then the scheme of a dynamic current mirror is derived. The effect of drain voltage variations on the current precision are illustrated and structures which reduce these effects are deduced.

2.1 PRINCIPLE OF CURRENT COPIERS

The basic cell of a dynamic current mirror [VIT88], [WEG89], which is also reported as a current copier [DAU88] or sampled current circuit [VAL89], is represented in Fig. 2.1. This simple and elegant scheme, which slightly modified is also known as the current matching concept [NAI89] or as the self-calibration technique for D/A converters [GRO89], is built of an elementary sample-&-hold circuit connected to an MOS transistor, and of a toggle switch (S_y and S_z), which connects the device either to the input or the output.

The cycle of memorizing and reproducing a current is the following:

While the switches S_x and S_y are closed {Fig. 2.1(a)}, the current source feeds the input current to the diode-connected transistor T_m. During this phase switch S_z is open. After opening sampling switch S_x, capacitor C maintains ("memorizes") the gate voltage and thus the drain current of T_m remains equal to I_{in}. When S_y is open and S_z closed {Fig. 2.1(b)}, the memorized drain current is available at the output.
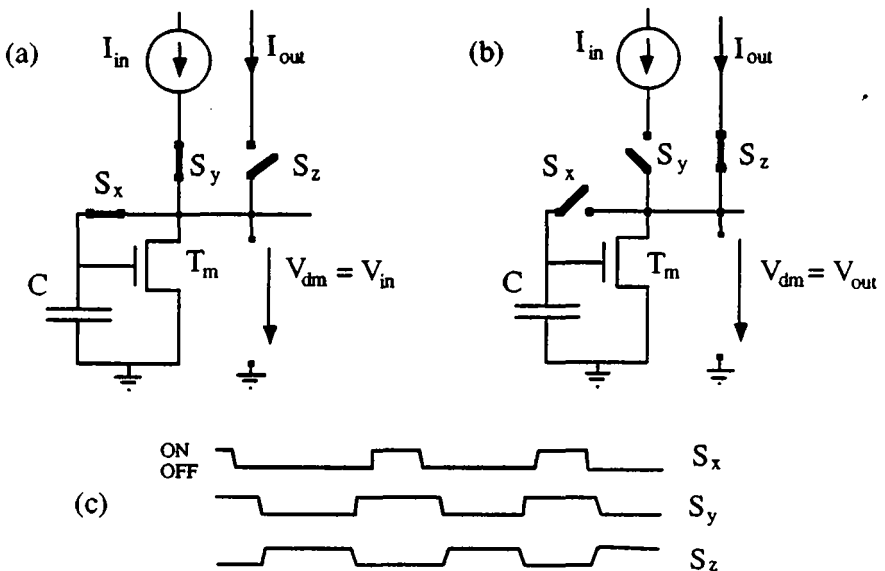
Figure 2.1:   Principle of a current copier or dynamic current mirror basic cell

Fig. 2.1(c) shows the corresponding clock phases. Transistor T_m works thus either as a drain-gate-connected transistor (switch S_x closed) or as an independent current source (switch S_x open).

Note that the value of the output current is independent of the parameters of transistor T_m and of linearity and hysteresis of the capacitor C. On the other hand the reproduced output current depends on the accuracy of gate voltage storage. Any error voltage ΔV on the storage capacitor C produces an output current error ΔI

$$\frac{\Delta I}{I_{in}} = \frac{I_{out} - I_{in}}{I_{in}} = \frac{g_{mm} \Delta V}{I_{in}} \tag{2.1}$$

where g_{mm} stands for the transconductance parameter of T_m.
(see Appendix A for more details on the MOS model, on the symbols and definitions used in this thesis).

2.2 PRINCIPAL ACCURACY LIMITATIONS

The performance of the basic cell of a dynamic current mirror is limited by the following major effects:

(a) charge injection of the MOS transistors used as switches :

When switching off an MOS transistor, the mobile charge in the inversion charge layer is shared between drain, source and substrate [SHI87], [WEG87], [EIC89]. A part of the charge released by sampling switch S_x is added to the charge already stored on the hold capacitor C and the resulting error voltage ΔV alters the value of the memorized drain current as shown by eq. (2.1).

(b) leakage currents of the reverse biased junctions:

The leakage currents at the gate node of T_m discharge the storage capacitor C. They determine the minimum switching frequency of the current copier for a given accuracy.
In the case of very low currents, the leakage currents to ground limit the absolute achievable accuracy.

(c) sampled noise :

White noise is undersampled and the power spectral density of the white noise component in the baseband is increased because of additional foldover terms. 1/f noise is cancelled at low frequencies due to the inherent auto-zero technique, which introduces a double zero at the origin. It will be shown that the undersampled 1/f noise produces an increase of the white noise in the baseband.

(d) drain voltage variations:

Usually V_{in} is different from V_{out}. When switching S_y and S_z, hence when switching from the input to the output, the voltage difference V_{in}-V_{out} is applied to the drain of T_m.

(d.1) transients or spikes:

When S_z is closed the output must produce some additional current to charge the parasitic capacitances at the drain of T_m to V_{out}. The resulting transients or "glitches" at the output have an amplitude which is proportional to the voltage step V_{in}-V_{out}.

(d.2) output conductance :

An important requirement is that the reproduced current should not depend on the output voltage. As in a classical static current mirror, the finite output conductance of T_m has to be minimized to obtain an accurate current mirror.

(d.3) capacitive divider between drain-to-gate capacitance C_{gd} and C:

Gate voltage variations are produced through the capacitive divider formed with the storage capacitance C and the parasitic drain-to-gate capacitance C_{gd} of T_m.

Chapter 4 deals extensively with these "Accuracy Limitations", calculates their influences and compares their contributions.

2.3 PRINCIPLE OF A DYNAMIC CURRENT MIRROR

The principle of a dynamic current mirror [WEG89.1], which is capable of memorizing and reproducing an imposed current I_{in}, is shown in Fig. 2.2(a). To ensure a continuous output current, two current copiers are needed, which function with complementary clocks {Fig. 2.2 (b)}.

The switching cycle remains identical to the one mentioned in § 2.1. Each time S_{xj} is closed (j=0 or 1), V_{in} adapts to the value of gate voltage corresponding to I_{in}. Therefore V_{in} varies stepwise as a function of time with an amplitude proportional to the mismatch of T_{m0} and T_{m1}.
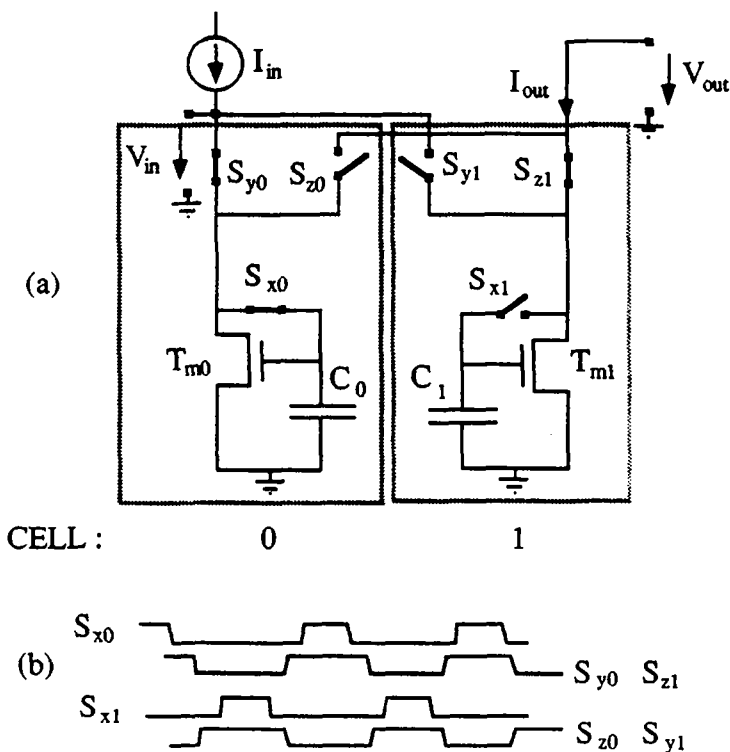
Figure 2.2:   Principle of a dynamic current mirror operating with two current copiers

It has to be pointed out that the value of the output current I_{out} is independent of transistor and capacitor matching, hence independent of process variations.

The drain voltage of T_{mj} must return to the value $V_{dmj} = V_{in}$ during the memorization phase {switches S_{xj} and S_{yj} closed, S_{zj} open}. When the current is restored {switches S_{xj} and S_{yj} open, S_{zj} closed}, it must jump to a value V_{out} imposed by the external load of the cell. The voltage step which occurs at the drain of T_m contributes to an important DC error through the output conductances and the parasitic drain capacitance C_{gd}.

2.4 CURRENT COPIER STRUCTURES

The objective being pursued in this section is to find a structure for a current copier, which reduces the voltage variations on the drain of T_m. According to the reflections made in the precedent paragraph and in section 2.2(d), V_{dm} should remain as constant as possible in spite of the imposed voltage difference $V_{in} - V_{out}$.

2.5.1 OP-AMP STRUCTURE

One possible solution, that performs current memorizing and restoring under constant drain voltage conditions, is based on active mirror considerations [NAI89.2], [VAL89].

During the memorization phase an operational amplifier forces the drain voltage V_{dm} to be equal to a bias voltage V_{bias}. Equilibrium is reached when the drain current of transistor T_m is equal to the input current. After copying, the cell is disconnected from the amplifier and $V_{out} = V_{bias}$ is imposed by the op-amp. The drawback of this approach is that the output potential is fixed and therefore the principle can only be applied successfully in applications where this condition can be satisfied.

2.5.2 CASCODED STRUCTURE

A much more elegant and simpler way of achieving a constant voltage V_{dm} is to implement a cascoded structure by means of a common-gate transistor [WEG89.1], [VIT90] in series with the main transistor T_m which leads to the solution represented in Fig. 2.3.
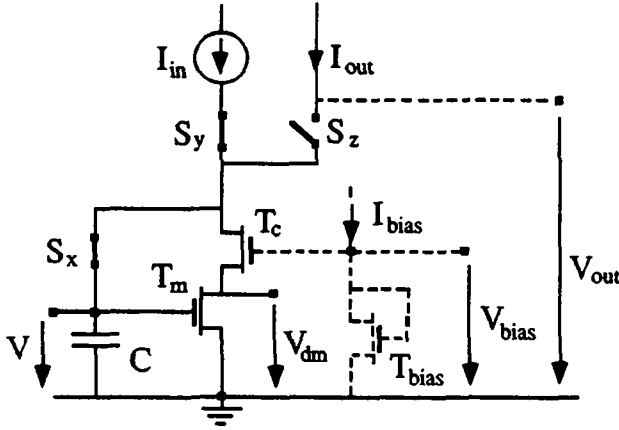
Figure 2.3: Cascoded current copier biased by an external current I_{bias}

The cascode combination of T_m and T_c is equivalent to a single transistor T_m with values of Early voltage V_E and of drain-to-gate capacitance C_{gd} increased and decreased, respectively, by a factor equal to the source to drain voltage gain of T_c. Because this gain can be as high as several hundred, the errors due to the output conductance g_{ds} and to the drain-gate capacitance C_{gd} are drastically reduced.

To increase the output dynamic range of this cell, the bias voltage V_{bias} should be as low as possible. The minimum value is given by the limit needed to keep T_m in saturation, which yields:

$$V_{bias} = V_{T0} + nV_{dm} + \sqrt{\frac{2nI_{in}}{\beta_c}} \geq V_{T0} + \sqrt{2nI_{in}} \left\{ \frac{1}{\sqrt{\beta_c}} + \frac{1}{\sqrt{\beta_m}} \right\} \qquad (2.2)$$

$$\text{with} \qquad V_{dm} \geq V_{dsat} = \sqrt{\frac{2I_{in}}{n\beta_m}} \qquad (2.3)$$

Eq. (2.2) can be expressed in function of the specific current I_{si} :

$$V_{bias} \geq V_{T0} + 2n\,U_T \left\{ \sqrt{\frac{I_{in}}{I_{sc}}} + \sqrt{\frac{I_{in}}{I_{sm}}} \right\} \qquad (2.4)$$

$$\text{with :} \qquad I_{si} = 2n\,\beta_i\,U_T^2 \tag{2.5}$$

The bias voltage V_{bias} can be produced by imposing an external current I_{bias} through a transistor T_{bias} as shown in dotted line in Fig. 2.3. The MOS voltage-current relationship in strong inversion leads to:

$$V_{bias} = V_{T0} + 2n\,U_T\sqrt{\frac{I_{bias}}{I_{sb}}} \tag{2.6}$$

Eqs. (2.4) and (2.6) yield

$$\frac{I_{bias}}{I_{sb}} \geq \left[\sqrt{\frac{I_{in}}{I_{sc}}} + \sqrt{\frac{I_{in}}{I_{sm}}}\right]^2 \tag{2.7}$$

The currents I_{si} are determined by the relative dimensions of the corresponding transistor T_i.

With the smallest possible value of V_{bias} given by eq. (2.4) the condition on V_{out} which keeps T_c in saturation is found to be:

$$V_{out} \geq 2\,U_T\left\{\sqrt{\frac{I_{in}}{I_{sm}}} + \sqrt{\frac{I_{in}}{I_{sc}}}\right\} \tag{2.8}$$

During the storage phase {Fig 2.1(a)} T_c and T_m must remain saturated which can be expressed by:

$$V_{T0} \geq 2\,U_T\left\{(1-n)\sqrt{\frac{I_{in}}{I_{sm}}} + \sqrt{\frac{I_{in}}{I_{sc}}}\right\} \tag{2.9}$$

The first term of the sum on the right is usually much larger than the second one, because T_c operates as close as possible to weak inversion and T_m to strong inversion. Furthermore the first term is negative, which means that inequality of eq. (2.9) is satisfied for any positive values of threshold voltage V_{T0}. In the case that inequality (2.9) cannot be satisfied, a source follower T_f introducing a voltage shift can be placed between the storage capacitor C and the gate of T_m [DAU88], [AEB90]. Because of

storage capacitor C and the gate of T_m [DAU88], [AEB90]. Because of stability considerations the large functional capacitor C and the switch S_x must be moved from the gate of T_m to the gate of T_f. In Fig. 2.4 the now stable structure is represented with the additional current source I_f which is needed to bias T_f.

Because the voltage steps V_{in}-V_{out} are still applied to S_y and S_z, the simple cascode cell configuration of figs. 2.3 & 2.4 is only applicable when the output current is used after the transients have faded out. The average current error due to the voltage step V_{in}-V_{out} still reduces the DC accuracy of such a cell.

Figure 2.4: Extended current copier with source follower
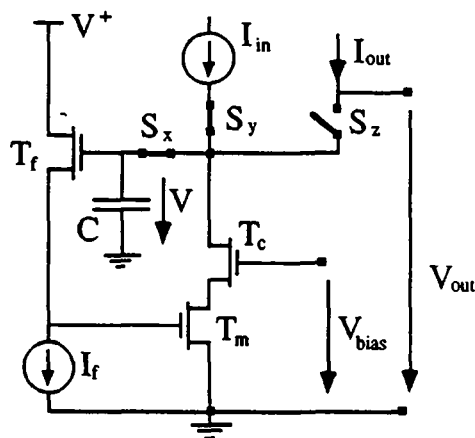
2.5.3 CURRENT COPIER WITH REDUCED TRANSCONDUCTANCE $g_{mm\Delta}$

According to eq. (2.1) the achievable current accuracy depends linearly on the error voltage ΔV and on the transconductance g_{mm}. To increase the current precision, the transconductance g_{mm} can be reduced by using a mirror structure with a modified basic cell, which memorizes only a current difference I_{in}-I_0. This principle, which was reported as the self-

The comparison of the transfer parameter β and β_Δ of two current copiers, which are built either with T_m or with $T_{m\Delta}$ and which operate with the same gate-to-source voltage V_{gs}, leads to

$$\beta_\Delta = \frac{I_{in}\text{-}I_0}{I_{in}} \beta \tag{2.10}$$

which is valid in strong inversion.

Introducing eq. (2.10) in the expression of transconductance $g_{mm\Delta}$ of $T_{m\Delta}$ yields:

$$g_{mm\Delta} = \sqrt{\frac{2\beta_\Delta (I_{in}\text{-}I_0)}{n}} = \frac{I_{in}\text{-}I_0}{I_{in}} g_{mm} \tag{2.11}$$

But to make this improved cell work correctly, the current difference I_{in}-I_0 must be positive to ensure that the diode-connected n-type transistor $T_{m\Delta}$ still is properly biased. Thus an additional current source I_0 of value close to, but always smaller than I_{in}, must be available. Furthermore V must be higher than the saturation voltage of I_0.
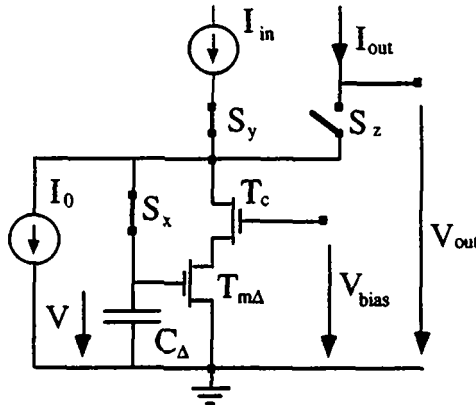
Figure 2.5:   Current copier memorizing the current difference I_{in}-I_0

Due to the lowered transconductance parameter $g_{mm\Delta}$, a larger voltage swing is needed to compensate for the current mismatch. Therefore, if a dynamic current mirror is built with two improved basic cells, the variations of V_{in} are increased in comparison with the variations of a normal basic cell.

2.5 SUMMARY

The current copier cell which successively memorizes and reproduces a given input current was illustrated and the principle of a dynamic current mirror introduced. The principal accuracy limitations were reviewed. Structures were proposed which reduce the influence of the voltage step at the drain of T_m, while switching from the input to the output or vice versa. A structure which reduces the transconductance parameter was presented. The relations between output voltage, input current, bias current and device geometries for different configurations were calculated.

CHAPTER 3

DYNAMIC CURRENT MIRROR

CONFIGURATIONS

In this chapter the focus is placed upon the practical implementation of dynamic current mirrors based on current copiers. Several possible structures of dynamic current mirrors performing the ratio 1:1 are presented, their advantages and disadvantages are discussed and the corresponding bias and output voltages calculated. The extension to a multiple and multiplying mirror is deduced and an algorithmic current divider is proposed.

3.1 BASIC MIRROR CONSIDERATIONS

In analog design a symmetrical structure is generally preferred to an asymmetrical one, because parasitic capacitances and leakage currents are balanced, mismatch components reduced, and the layout is facilitated. According to the considerations made in §§ 2.2 & 2.3 the practical implementation of a dynamic current mirror [WEG89.1] can be deduced. The toggle switches S_{yj} and S_{zj} are placed at the sources of the common-gate transistors T_{cj} to reduce the voltage difference which appears at their terminals.

3.1.1 EXTERNALLY BIASED DYNAMIC CURRENT MIRRORS

The structure of an externally biased dynamic current mirror is represented in Fig. 3.1. The condition on V_{bias} is:

$$V_{bias} = V_{T0} + nV_{dm} + \sqrt{\frac{2nI_{in}}{\beta_c}} \geq V_{T0} + 2nU_T \left\{ \sqrt{\frac{I_{in}}{I_{sc}}} + \sqrt{\frac{I_{in}}{I_{sm}}} \right\} \quad (3.1)$$
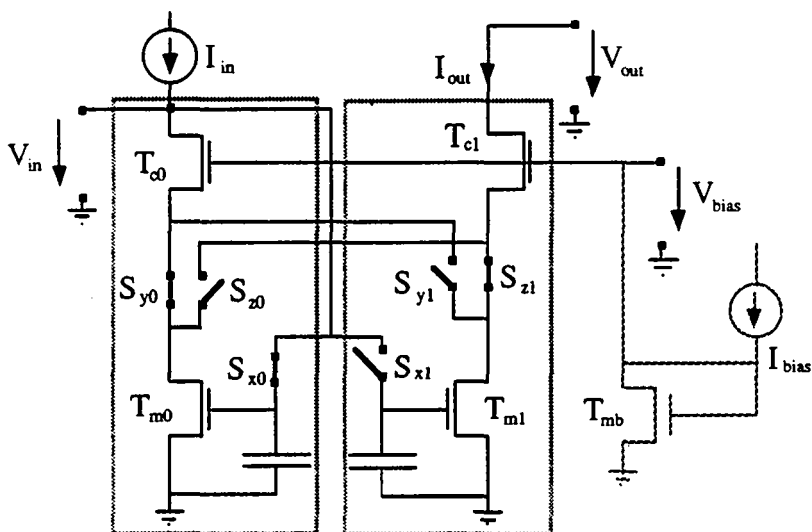
Figure 3.1:   Dynamic current mirror which is externally biased by I_{bias}

The bias circuit required for the dynamic current mirror is shown dotted.

3.1.2 SELF-BIASED DYNAMIC CURRENT MIRRORS

From the externally biased mirror of Fig. 3.1 a similar, self-biased current mirror can be deduced, which is much more compact. From Fig. 3.2 it can be seen that V_{in} is connected to V_{bias} and therefore biases the common gate transistors T_{cj} [WEG89.2].

The drawback of this structure is that the two transistors T_{c0} and T_{c1} *must* be located in separate wells, which are connected to their sources. Otherwise the condition, which expresses that V_{dmj} *(j=0,1)* must be larger than the saturation voltage V_{dsat} of T_{mj}, leads to relation (3.2) which is impossible to satisfy.

$$- 2U_T \sqrt{\frac{I_{in}}{I_{sc}}} > 0 \qquad\qquad (3.2)$$

Figure 3.2:   Self-biased dynamic current mirror with T_{cj} in separate wells

Therefore if an n-type current mirror is needed, a p-well technology must be available and vice versa for a p-type mirror.

For T_{c0} and T_{c1} located in separate wells, the following condition on the transconductance parameters β_i or on I_{si} must be fulfilled

$$\sqrt{\frac{\beta_m}{\beta_c}} = \sqrt{\frac{I_{sm}}{I_{sc}}} \leq \frac{n\text{-}1}{n} \tag{3.3}$$

For the limiting value of relation (3.3) the output voltage V_{out} is found to be:

$$V_{out} \geq 2U_T \{ n \sqrt{\frac{I_{in}}{I_{sm}}} + (1\text{-}n) \sqrt{\frac{I_{in}}{I_{sc}}} \} \tag{3.4}$$

Sometimes inequality (3.3) cannot be satisfied or, because of the technology, it is not possible to implement separate wells. In this case, the connection of S_{xj} of the self-biased dynamic current mirror of Fig. 3.2 must be modified to obtain the structure of a compact mirror represented in Fig. 3.3, a so-called "stacked" mirror structure [WEG89.1].

The drawback of this structure is its relatively high saturation voltage which increases $\dot{V}_{out}$ given by

$$V_{out} \geq V_{T0} + 2U_T \{ n \sqrt{\frac{I_{in}}{I_{sm}}} + \sqrt{\frac{I_{in}}{I_{sc}}} \} \tag{3.5}$$

which is more than a threshold voltage higher than V_{out} given by eq. (3.4). Note that eq. (3.5) remains valid whether T_{c0} and T_{c1} are in a separate well or not. Normally the first term of relation (3.5) is dominant because T_{mj} is biased in strong inversion, whereas T_{cj} operates as close as possible to weak inversion [VIT89].

Due to the two diode-connected transistors, which impose the voltages, the "stacked" mirror is uncritical even for a large current range. The devices of the input branch always remain in the saturated mode independently of the dimensions of the transistors.
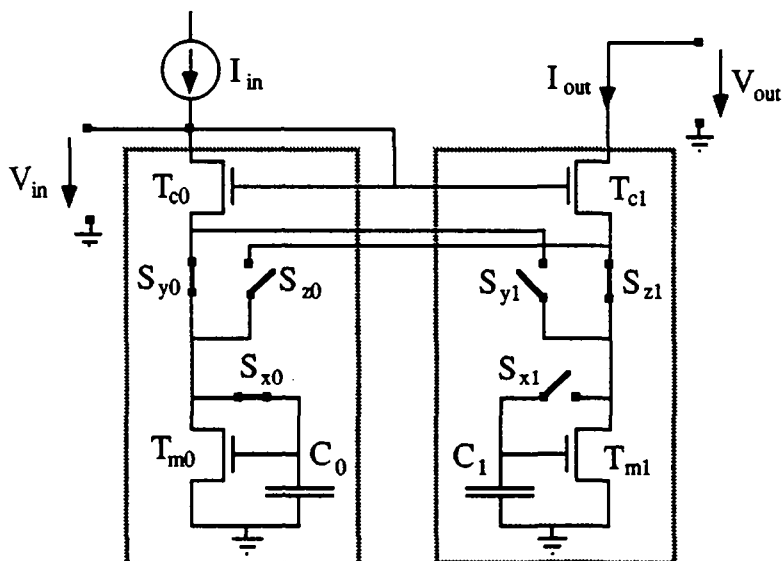
Figure 3.3: Self-biased, so-called "stacked" dynamic current mirror

Table 3.1 recapitulates the minimum output voltages V_{out} of the different structures mentioned in §§ 3.1.1 and 3.1.2.

Mirror of:	Minimal Output Voltages V_{out}	Particular Conditions
Fig. 3.1: ext. biased	$2U_T\left\{\sqrt{\dfrac{I_{in}}{I_{0m}}} + \sqrt{\dfrac{I_{in}}{I_{0c}}}\right\}$	$V_{bias} \geq V_{T0} + 2nU_T\left\{\sqrt{\dfrac{I_{in}}{I_{sc}}}+\sqrt{\dfrac{I_{in}}{I_{sm}}}\right\}$
Fig. 3.2: self-biased	$2U_T\left\{n\sqrt{\dfrac{I_{in}}{I_{0m}}} + (1-n)\sqrt{\dfrac{I_{in}}{I_{0c}}}\right\}$	$\sqrt{\dfrac{I_{sm}}{I_{sc}}} \leq \dfrac{n-1}{n}$
Fig.3.3: "stacked"	$V_{T0} + 2U_T\left\{n\sqrt{\dfrac{I_{in}}{I_{0m}}} + \sqrt{\dfrac{I_{in}}{I_{0c}}}\right\}$	None

Table 3.1: Comparison of the minimal output voltages V_{out} of the different structures

3.2 MULTIPLE AND MULTIPLYING MIRRORS

3.2.1 MULTIPLE CURRENT MIRRORS (1:1:...:1)

A multiple dynamic current mirror with n identical current outputs is obtained by simply repeating n-times the cascoded current copier, which involves a total of $(n+1)$ copiers.
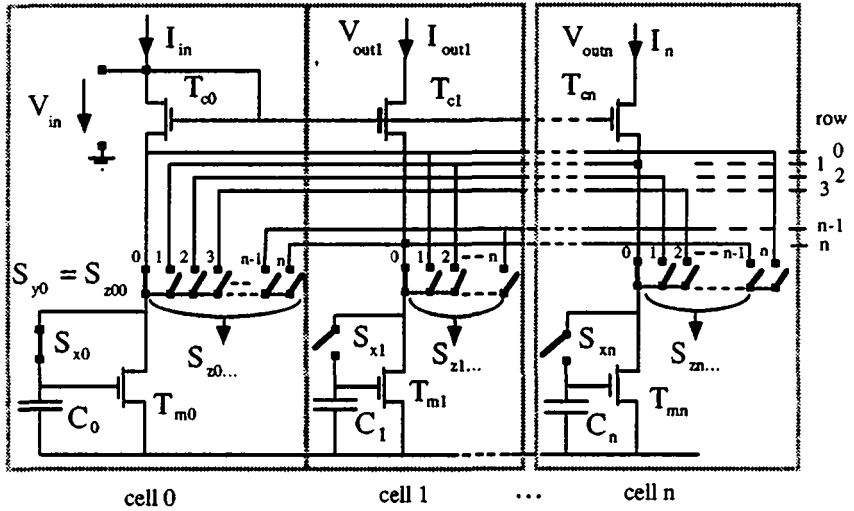
Figure 3.4:   Multiple "stacked" dynamic current mirror according to strategy (a)
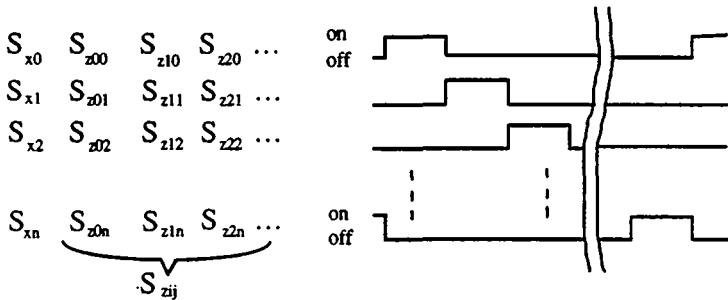
Figure 3.5:   Clock phases for the dynamic current mirror of Fig. 3.4

The two following switching strategies are possible, which lead to slightly different circuit schemes:

(a) all current copiers are identical and sweep sequentially each output while delivering the stored current, meaning that during a switching cycle *every cell is connected once to each of the outputs*.

(b) all current copiers, except copier 0, are identical and are connected to their corresponding output, or in other words copier 1 is always delivering the current to output 1, copier 2 to output 2, etc.. In opposition to strategy (a) *only copier 0 is sweeping all the outputs* and is delivering the output current in place of the cell that is being updated.

Let us first consider **strategy (a)**:

A corresponding self-biased and stacked circuit scheme, which is based on the dynamic current mirror of Fig. 3.3, is represented in Fig. 3.4 and the corresponding clock phases in Fig. 3.5.

Because the $(n+1)$ current copiers sweep each output an averaging effect occurs, which can increase the DC accuracy of the output currents. On the other hand, glitches are present $(n+1)$ times during a switching cycle, because $(n+1)$ current sources are connected to every output. The increase in DC accuracy obtained by the averaging effect is degraded due to these additional transients [WEG90.2].

The number of additional connections and the number of clock phases per cell increase linearly with the number of outputs (see table 3.2), which results in an important increase in size of each current copier.

From Fig. 3.5 it can be seen that each clock must drive n times the switches S_{zij} $(j{\neq}i)$, once S_{yj} (or S_{zii}) and once S_{xj}, which corresponds to a total of $(n+2)$ switches. This large capacitive load influences the slope of the clocks which degradation has to be counterbalanced by an adequate increase of size of the corresponding clock drivers.

The large number of connections and clock phases, hence the chip size, can be reduced with the help of **strategy (b)**. The corresponding self-biased "stacked" mirror and the switching sequence are shown in Fig. 3.6 and 3.7,

respectively. All the cells are identical, except cell 0, and each cell delivers the current to only one specific output, which reduces drastically the number of clock phases and connections.

Figure 3.6:   Multiple "stacked" dynamic current mirror according to strategy (b)

Figure 3.7:   Clock phases corresponding to the mirror of Fig. 3.6

The number of connections of an output cell is independent of n and remains equal to that of a current copier. The clock phases driving the switches S_{yj} and S_{zj} are complementary. The switches S_{zoj} are driven by the same clocks as S_{yj}, which simplifies the control logic of a mirror based on strategy (b).

Table 3.2 shows how an output cell of the multiple current mirror of Fig. 3.4 and Fig. 3.6 is modified as a function of the number of outputs n. An output cell of the multiple current mirror of Fig. 3.6 is independent of n and only the number of switches S_{zoj} varies as a function of the number of outputs. Approach (b) leads to a much simpler and more compact multiple current mirror than approach (a), with the only drawback being that cell 0 is slightly different from the other cells.

Note that it is also possible to build multiple dynamic mirrors with other mirror structures (Figs.3.1 & 3.2) or with variations of the current copier, as proposed in chapter 2.

	strategy (a): Circuit of Fig. 3.4	strategy (b): Circuit of Fig. 3.6
no. of clock phases per cell	$n+1+1$	3
no of additional connections per cell	$2\,(n-1)$	0
additional capacitance at drain	$(n-1)\,C_{Sz}$	0
transients per switching cycle	$(n+1)$	2
switches driven by each clock	$n+1+1$	3

Table 3.2: Comparison of the number of connections of strategy (a) & (b)

3.2.2 MULTIPLYING CURRENT MIRRORS (1:m:n)

Obviously the n continuous output currents of § 3.2.1 can be added to realize a *(1:m:n)* multiplying dynamic current mirror. Fig. 3.8 shows such a mirror with two outputs of value $2I_{in}$ and $(n-2)I_{in}$.

This mirror is based on strategy (b) or in other words, current copier 0 always takes the place of the cell which is updated. For the clock phase which is represented in Fig. 3.8, cell 0 is connected to the output labeled $2I_{in}$, while current copier 2 is being updated. It can be seen that the number of interconnections has been reduced by sharing the sources of the common-gate output transistors T_{cj} *(j=1, 2)* and T_{cj} *(j=3...n)*. Furthermore, this approach avoids the need to split S_{z0j} into several switches. Because the switches S_{z0j} *(j=1, 2)* and S_{z0j} *(j=3...n)* are replaced by S_{z02} and S_{z0n}, respectively, the control logic of these two switches is slightly modified.

The clock of S_{z02} is simply the "AND"-function of the clocks which activate cells 1 and 2, and, consequently, the clock controlling S_{z0n} is the "AND"-function of the clocks of the cells 3, 4,... and n.
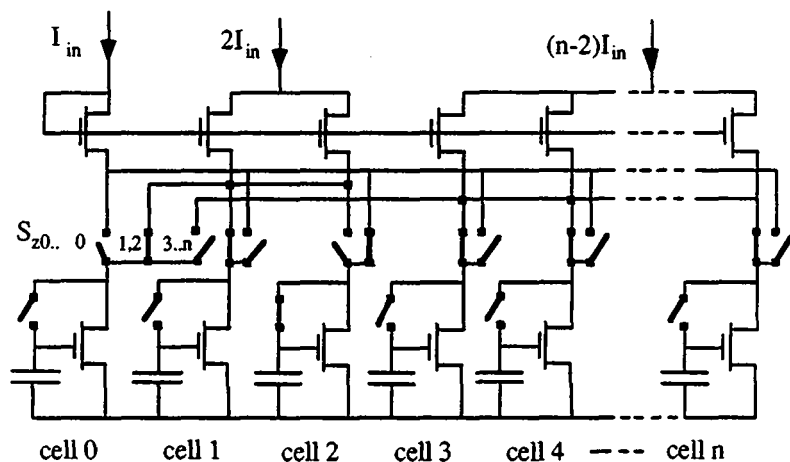
Figure 3.8:   Self-biased, stacked multiplying dynamic current mirror with two outputs; one of value $2I_{in}$ and one of value $(n-2)I_{in}$.

3.3 DIVIDING CURRENT MIRRORS

3.3.1 PRINCIPLE OF THE DIVISION BY 2 ($I_{out} = \frac{I_{in}}{2}$)

Due to the unavoidable transistor mismatch, it is not possible to divide a current I_{in} accurately by simply connecting n current copiers in parallel, since the input current would not be evenly shared among them.

With the help of the calibration scheme shown in Fig. 3.9 [ROB89.2], which performs a division by two, exactly half the input current can be forced to flow through the main transistor T_m, which delivers the output current. Transistor T_p and calibration transistor T_c form a so-called "locked pair" of transistors, since their output current sum equals the one of T_m.

$\widehat{x}$ = switch on in phase x (x=1, 2, 3)
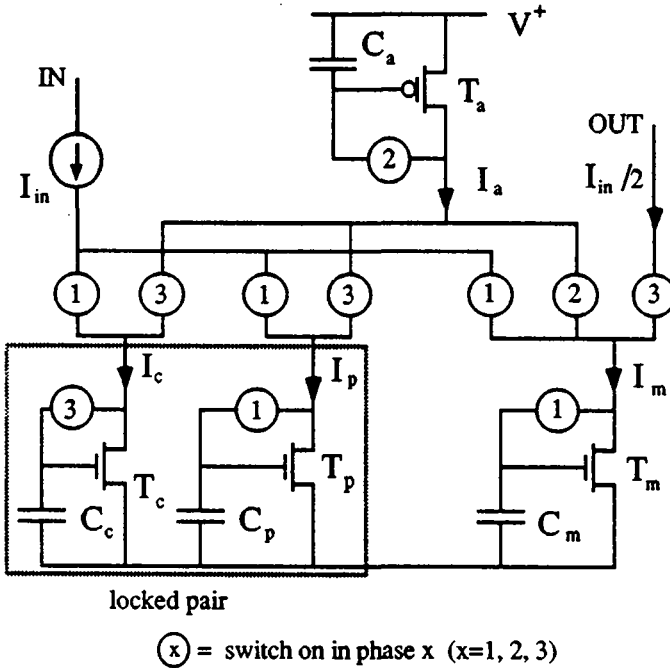
Figure 3.9:   Accurate divide-by-two dynamic current mirror: complete schematics

The circuit operates in three clock phases and the output current requires a few cycles to reach the correct current values. In Fig. 3.9 each switch is symbolized by a circled number, that indicates its phase of conduction. Each transistor can be connected either in a diode configuration (when a new current value is stored) or as an independent current source (when it reproduces the previously memorized current).

For the sake of clarity, the three different phases are represented explicitly in Fig. 3.10, where only the transistors which are active during the corresponding phase are represented.

The principle of accurate current division is the following:

During **phase 1**, transistors T_m and T_p share the input current I_{in} from which the previously established calibration current I_c is subtracted.
Thus, for cycle k:

$$I_{mk} = \frac{I_{ink} - I_{c(k-1)}}{2} (1+\varepsilon) \qquad (3.6)$$

$$I_{pk} = \frac{I_{ink} - I_{c(k-1)}}{2} (1-\varepsilon) \qquad (3.7)$$

where ε represents the mismatch between T_m and T_p. Note that for the first cycle (k=1), current I_{c1} of T_c is arbitrarily set to zero. Both currents, I_{mk} and I_{pk}, are memorized as voltages on the capacitors C_m and C_p, respectively.

During **phase 2**, the stored current I_{mk} is forced into the p-type transistor T_a, hence:

$$I_{mk} = I_{ak} \qquad (3.7)$$

During **phase 3**, the difference between current I_{ak} and I_{pk}, which is memorized by T_p, is stored in T_c as the new value of the calibration current I_{ck}:

$$I_{ck} = I_{mk} - I_{pk} = \varepsilon (I_{ink} - I_{c(k-1)}) \qquad (3.8)$$

Because in Fig. 3.9 T_c is a current sink, I_{ck} can only flow towards ground. This additional constraint on I_{ck} reduces the complexity of the circuit. It

avoids the use of T_c either as a current sink or a current source, and it also avoids the corresponding control-logic. Since I_{ck} is positive, T_m and T_p must be designed to ensure $\varepsilon > 0$.

The evolution of the calibration current I_{ck} can be obtained by introducing z-transforms into eq. (3.8), which yields:

$$I_c(z) = \frac{z\varepsilon}{z+\varepsilon} I_{in}(z) \tag{3.9}$$

Introducing $I_{in}(t) = I_{in}$ while $t \geq 0$ leads to:

$$I_c(z) = \frac{z\varepsilon}{z+\varepsilon} \frac{z}{z-1} I_{in} \tag{3.10}$$
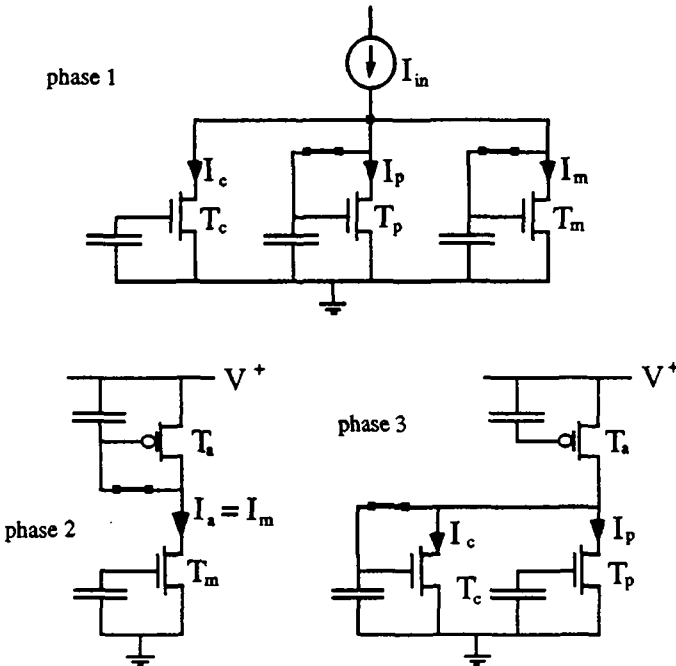
Figure 3.10: Accurate divide-by-two dynamic current mirror: scheme showing the different configurations for each phase

which yields the asymptotic or equilibrium value $I_{c\infty}$ of calibration current I_c:

$$I_{c\infty} = \lim_{z \to 1} (z\text{-}1)\,I_c(z) = \frac{\varepsilon}{1+\varepsilon}I_{in} \tag{3.11}$$

The equilibrium value of the output current $I_{m\infty}$ can be found either by introducing $I_{c\infty}$ in eq. (3.5) or by taking the z-transform of I_{mk} which leads to:

$$I_{m\infty} = \lim_{z \to 1} (z\text{-}1)\,I_m(z) = \lim_{z \to 1} (z\text{-}1)\frac{z(1+\varepsilon)}{2(z+\varepsilon)}\,I_{in}(z) = \frac{I_{in}}{2} \tag{3.12}$$

which is independent of the mismatch ε. This equilibrium is reached exponentially with a time constant τ [ROB89.2], [VIT90]

$$\tau = -\frac{1}{\ln(\varepsilon)} \; [cycles] \tag{3.13}$$

For example, τ is equal to 0.33 and 0.43 [cycles], while $\varepsilon = 5\%$ and $\varepsilon = 10\%$, respectively.

Therefore, after a few cycles the current I_{mk} settles to the desired value of $I_{in}/2$. Obviously the sum of the asymptotic values of the locked-pair corresponds also to half the input current. After the steady state is reached, the three-phase-cycle proceeds to update the stored voltages, which prevents the influence of leakage currents.

If the output current has to be available continuously, T_m and T_c must then be duplicated. It is also possible to duplicate only T_m. Then T_c must adapt its current to each T_m, which increases the time necessary for the updating of the current I_m.

Table 3.3 gives numerical values of I_m and I_c during phase 1 for two values of mismatch, $\varepsilon = 5\%$ and $\varepsilon = 10\%$.

	$\varepsilon = 0.05$		$\varepsilon = 0.10$	
$k =$	$I_{m(k)}$	$I_{c(k)}$	$I_{m(k)}$	$I_{c(k)}$
0	.525	0	.55	0
1	.49875	.05	.495	.1
2	.50006	.0475	.5005	.09
3	.49999	.04763	.49995	.091
4	.5	.04762	.50001	.0909
5	.5	.04762	.5	.09091
6	.5	.04762	.5	.09091

Table 3.3:   Evolution of I_{mk} and I_{ck} for two mismatch values ε between T_m and T_p

3.3.2 DIVISION BY ANY INTEGER NUMBER (1/n)

This principle can be extended to any integer value $n > 2$ by using $(n-1)$ "locked pairs" of transistors $T_{pi} - T_{ci}$. This involves the splitting of phase 3 into $(n-1)$ phases, which are necessary to update each calibration transistor T_{cj} of the locked pair. The total number of phases needed is then $(n+1)$, and the output current $\frac{I_{in}}{n}$ of T_m is available while all the locked-pairs are calibrated, thus during a fraction $\frac{n-1}{n+1}$ of the calibration cycle.

3.4 SUMMARY

The practical implementation of a dynamic current mirror of 1:1 ratio was investigated, which was built with two identical current copiers or basic cells. The gates of the input transistor T_{c0} and of the output transistor T_{c1} are connected together in a common-gate transistor configuration to reduce the drain voltage variations of the common-source transistors. The toggle switch is placed at the sources of the common-gate transistor, which reduces the amplitude of the transients and increases the DC current

accuracy. Externally biased dynamic current mirrors and two type of self-biased current mirrors were presented and their output voltage range were compared to each other. Two switching strategies which perform accurate multiple current outputs were studied, and the influence on the circuit complexity as a function of the number of current outputs was shown. The structure, which is more compact, was used to obtain a multiplying current mirror. Finally, the algorithm of an accurate divide-by-two current mirror was proposed and its asymptotic values were calculated. Its extension to any integer value was mentioned.

CHAPTER 4

ACCURACY LIMITATIONS

The accuracy limitations mentioned in chapter 2 are investigated and their influences on the circuit performance are studied. First the effect of drain voltage variations on the current accuracy are analyzed. Then the contribution of the different leakage currents to the gate voltage error is illustrated. A detailed analysis focusing attention upon both white and 1/f noise is presented. The noise spectral power density and the noise voltage at the gate node is calculated in the baseband, and the contributions of the different noise sources and their aliasing effects are highlighted. Finally the charge injection phenomenon is outlined and some strategies which reduce the influence of this effect are proposed.

4.1 INFLUENCE OF DRAIN VOLTAGE VARIATIONS

4.1.1 OUTPUT CONDUCTANCE g_{ds}

Channel length modulation contributes to an important current error, which can be represented by the drain-to-source conductance g_{ds}.
The cascoded structures presented in chapter 2 decrease the drain-to-source conductance g_{ds} of a current copier by the cascode gain. If the common-gate transistors T_{cj} and T_c are located in separate wells (Fig. 4.1), the total output conductance g_{ds} of a cell is found to be:

$$g_{ds} = g_{dsm} \frac{g_{dsc}}{g_{mc}} \qquad (4.1)$$

Figure 4.1:   Parasitic capacitances and conductances (dashed) of the current copier

If a common well is used, the transconductance g_{mc} is replaced by ng_{mc}, where n is typically between 1.5 and 2 and tends asymptotically to 1 with increasing gate voltage. Furthermore a supplementary term g_{dc} is added, which represents the conductance of the drain to the bulk of T_c [VIT89].

Thanks to the cascoded structure, the fraction of the output voltage ΔV_{out} which is transmitted to the drain of T_m and which produces drain variations ΔV_{dm}, is reduced to

$$\Delta V_{dm} = \Delta V_{out} \frac{g_{dsc}}{g_{mc}} \qquad (4.2)$$

Again if a common well is used, the transconductance g_{mc} is replaced by ng_{mc}. The resulting current error can be expressed as:

$$\frac{\Delta I}{I_D} = \frac{g_{dsm}}{I_D} \Delta V_{dm} = \frac{\Delta V_{dm}}{V_E} = \frac{g_{dsc} \Delta V_{out}}{g_{mc} V_E} \qquad (4.3)$$

with the Early voltage V_E given by

$$V_E = \lambda L_{ef} \qquad (4.4)$$

V_E is of the order of tens of volts and therefore steps of some hundred millivolts of V_{out} would produce an output current error of about 1% without a cascoded structure.

T_c lowers the effect of output voltage variations on the current accuracy, but there still remains a small voltage difference V_{sc}-V_{sco}, which is minimized if T_c and T_{c0} are matched. V_{bias} was calculated in § 3.1.

4.1.2 CAPACITIVE DIVIDER C_{gd} - C

When switching S_y and S_z a voltage step proportional to V_{sc}-V_{sco} is applied to the drain of T_m. A fraction ΔV is transferred to the capacitance C through the capacitive divider formed by the gate-to-drain capacitance C_{gd} and C. The resulting current error ΔI is:

$$\Delta I = g_{mm} \Delta V = \frac{g_{mm} C_{gd} (V_{sc}\text{-}V_{sco})}{(C + C_{gd})} \qquad (4.5)$$

4.1.3 OPTIMIZATION OF THE. RATIO C_G/C

The optimum is calculated for a given value of the storage capacitance C and for a given value of transconductance g_{mm}, hence of a fixed ratio $\frac{W_{ef}}{L_{ef}}$. An increase of the effective channel length L_{ef} reduces the current error ΔI due to g_{dsm} according to eq. (4.3), but increases ΔI due to C_{gd} {eq. (4.5)}, because the effective channel width W_{ef} must be modified to maintain the desired ratio. Both current errors can be written explicitly in function of the stored drain current I_D and of drain voltage variations ΔV_{dm}

$$\Delta I = g_{mm}\Delta V + g_{dsm}\Delta V_{dm} = \Delta V_{dm} I_D \left\{ \frac{2}{(V-V_{T0})} \frac{C_{gd}}{(C+C_{gd})} + \frac{1}{\lambda L_{ef}} \right\} \quad (4.6)$$

The total capacitance C at the gate node can be split into the gate capacitance C_G and into an additional capacitance C_{ad}.

$$C = C_G + C_{ad} = W_{ef} L_{ef} C'_{ox} (1 + \xi) \quad (4.7)$$

$$\text{with} \qquad \xi = \frac{C_{ad}}{C_G} = \frac{C_{ad}}{W_{ef} L_{ef} C'_{ox}} \quad (4.8)$$

If T_m works in strong inversion, W_{ef} can be extracted from the transfer parameter β_m. Then with the help of eq. (4.7) L_{ef} can be expressed as:

$$L_{ef} = (V-V_{T0}) \sqrt{\frac{\mu C}{2nI_D(1+\xi)}} \quad (4.9)$$

Replacing in eq. (4.6) and assuming $C \gg C_{gd}$ yields after differentiation to an optimum value ξ_{opt}:

$$\xi_{opt} = \frac{2\lambda L_{ov}}{V-V_{T0}} - 1 \quad (4.10)$$

which can also be expressed as:

$$\left\{\frac{C_G}{C}\right\}_{opt} = \frac{V\text{-}V_{T0}}{2\lambda L_{ov}} = \frac{I_{in}}{g_{mm}\,\lambda L_{ov}} \qquad (4.11)$$

Typical numerical values for the parameters above are (for a standard 3μ CMOS process) :

$$L_{ov} = 0.5\mu m \qquad \lambda = \frac{5V}{\mu m} \qquad V\text{-}V_{T0} = 0.5V$$

which leads to: $\qquad \xi_{opt} \approx 9$

In this case the auxiliary capacitor should be nine times larger than the gate capacitance, or in other words T_m must be sized to obtain C_G equal to 10% of C.

4.1.4 DIRECT CHARGE FLOW PATH

A third effect is due to the additional charge that is supplied from the output to charge the parasitic capacitances C_{gd} and C_d. When S_z has just been closed voltage V_{dm} changes from V_{sc0} to V_{sc}. Thus the current copier cell has just been switched from the input to the output. When switching back to the input (S_x and S_y closed, S_z open) the voltage V_{dm} is forced to V_{sc0} again and this additional charge is drained from the parasitic capacitances. This charge creates a current transient (current "glitch" or spike), which has no importance if the output current is only used after equilibrium is reached. However, if the current must be available continuously, these glitches are not acceptable. Furthermore they produce a DC error in the average output current given by:

$$\Delta I = f_{sw}\left(V_{sc}\text{-}V_{sc0}\right)\left(C_d + \frac{CC_{gd}}{C+C_{gd}}\right) \qquad (4.12)$$

where f_{sw} is the switching frequency [WEG89.2], [WEG90.2].

Chapter 5 "Dynamic Behavior & Transient Analysis" deals extensively with the origin of these glitches and shows their effects.

4.2 LEAKAGE CURRENTS

4.2.1 GENERAL CONSIDERATIONS

The input and the output currents are affected by the parasitic leakage currents of several reverse-biased pn-junctions flowing to ground. These leakage currents I_j are due to the generation of electron-hole pairs in the depletion region of the pn-junctions. They are proportional to the depletion-layer width and charge, and therefore depend on the applied reverse bias V_{rev}, as shown by eq. (4.13) [SZE81].

$$I_j \ \alpha \ \left(1 + \frac{V_{revj}}{V_{bi}}\right)^m \tag{4.13}$$

with built-in potential $\qquad V_{bi} = U_T \ ln \left(\frac{N_A N_D}{n_i^2}\right) \tag{4.14}$

where $m = 1/2$ for an abrupt junction and $1/3$ for a linearly graded junction. N_A and N_D are the acceptor and donor concentrations, respectively, and $n_i = 1.45 \cdot \frac{10^{10}}{cm^3}$ corresponds to the intrinsic carrier concentration of silicon at 300K.

These leakage currents can be represented by current sources connected between the corresponding node and ground according to Fig. 4.2, which represents the self-biased stacked dynamic current mirror of Fig. 3.2.

Note that the leakage currents of the capacitances are negligible in comparison to that of the pn-junctions.

4.2.2 LEAKAGE CURRENT SOURCES OF A DYNAMIC CURRENT MIRROR

Let us first assume that the on conductance g_{xj} of the sampling switch S_{xj} is negligible. During the storage phase the stored drain current I_{Dj} (j=0,1) is the difference between I_{in} and the leakage current sources, hence (according to Fig. 4.2)

$$I_{Dj} = I_{in} - I_{dc0} - I_{s0} - I_{dmj} - I_{xj} \tag{4.15}$$
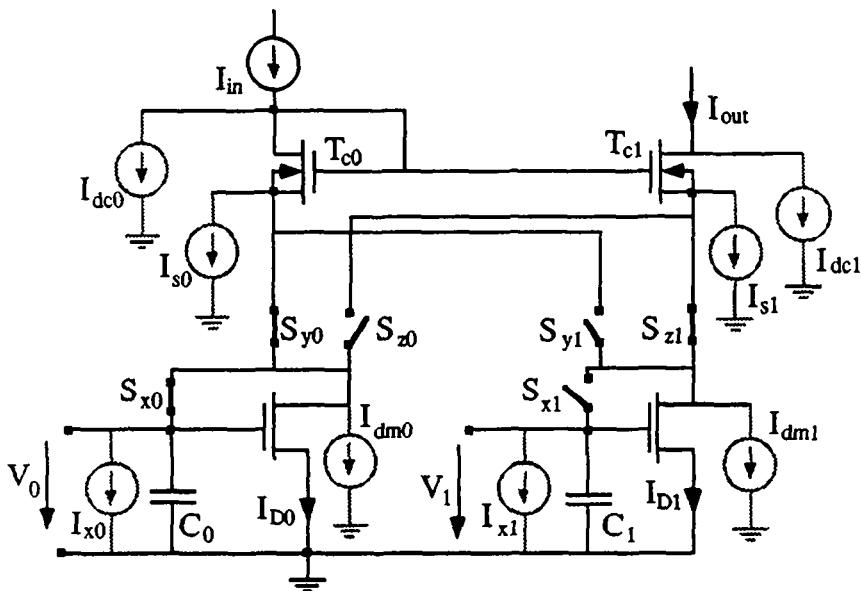
Figure 4.2: Different leakage current sources of a dynamic current mirror

where I_{xj} corresponds to the leakage currents at the gate node of T_{mj} I_{dmj} corresponds to the sum of the leakage currents at the drain node of T_{mj}, whereas I_{dc0} and I_{s0} stand for the leakage currents of T_{c0} at the source and the drain node, respectively.

During the restoring or copying phase t_{hj} the output current is

$$I_{outj}(t) = I_{Dj}(t) + I_{dmj} + I_{s1} + I_{dc1} \tag{4.16}$$

where the stored drain current $I_{Dj}(t)$ has become time dependent because of I_{xj} which discharges C_j. As a consequence, the gate voltage V_j varies linearly as a function of time t as shows Fig. 4.3. The gate voltage variations are supposed sufficiently small so that the small signal parameter g_{mmj} can be used. Introducing

$$I_{leak} = -I_{dc0} + I_{dc1} - I_{s0} + I_{s1} \tag{4.17}$$

the output current $I_{outj}(t)$ can be expressed as

$$I_{outj}(t) = I_{in} + I_{leak} - I_{xj} - g_{mmj}\frac{I_{xi}}{C_j}t \qquad (4.18)$$

Integrating eq. (4.18) over a time period $t_{h0}+t_{hl}$ leads to an average output current $\overline{\Delta I_{out}}$:

$$\overline{\Delta I_{out}} = I_{in} + I_{leak} - \frac{1}{t_{h0}+t_{hl}}\{t_{h0}I_{x0} + t_{hl}I_{xl} + \frac{g_{mm0}I_{x0}}{2\,C_0}t_{h0}^2 + \frac{g_{mml}I_{xl}}{2\,C_1}t_{hl}^2\} \quad (4.19)$$

If both current branches are matched term I_{leak} is cancelled out because $I_{dc0} \approx I_{dcl}$ and $I_{s0} \approx I_{sl}$. For $t_{h0} = t_{hl} = T_h$, $I_{x0} = I_{xl} \approx I_x$, $g_{mm0} \approx g_{mml} \approx g_{mm}$ and $C_0 \approx C_1 \approx C$ the current error ΔI due to leakage currents simplifies to

$$\Delta I = \overline{\Delta I_{out}} - I_{in} = -I_x\{1 + \frac{T_h g_{mm}}{2\,C}\} \qquad (4.20)$$

which shows clearly the limitation of the achievable accuracy due to the leakage current I_x of the sampling switch. The last term also sets a limit to the maximum duration T_h of the copying phase. A final limitation for very low currents still remains because of I_x.

Figure 4.3: Waveform of I_{out} for I_{in} = const. due to leakage currents while cell j is connected to the output

The voltage drop on the sampling switch conductance g_x due to the leakage current I_x may not be negligible during the storage phase. Assuming $g_x > g_0$, the drain voltage $V_{dm}(t)$ and the gate voltage $V(t)$ are affected as follows:

$$V(t) = V - \frac{T_h I_x}{C} e^{-t/\tau} + \frac{I_x}{g_{mm}} (e^{-t/\tau} - 1) \tag{4.21}$$

$$V_{dm}(t) = V + I_x \frac{g_{mm} - g_x}{g_x} \left\{ \frac{T_h}{C} e^{-t/\tau} - \frac{(e^{-t/\tau} - 1)}{g_{mm}} \right\} \tag{4.22}$$

with
$$\tau = \frac{C}{g_{mm}} \tag{4.23}$$

Note that voltage V corresponds to the gate voltage at equilibrium while $g_x > g_{mm}$ and that the drain capacitance C_d was neglected.

At time $t=0$ and $t\text{->}\infty$ eqs. (4.21) & (4.22) lead to

$$V(0) = V - \frac{T_h I_x}{C} \qquad\qquad V(t\text{->}\infty) = V - \frac{I_x}{g_{mm}} \tag{4.24}$$

$$V_{dm}(0) = V + I_x \frac{g_{mm} - g_x}{g_x} \frac{T_h}{C} \qquad V_{dm}(t\text{->}\infty) = V + I_x \frac{g_{mm} - g_x}{g_x g_{mm}} \tag{4.25}$$

Eq. (4.24) shows that the leakage currents I_x are a limit for the achievable accuracy while V is small, hence for low currents. If the voltage drop on g_x due to I_x is not negligible, the resulting increase of $V_{dm}(t)$ expressed by eq. (4.25) reduces the output dynamic range. In the case of a self-biased mirror, T_{c1} may exit saturation, whereas for an externally biased mirror T_{c0} may be cut-off. Furthermore, in the case of the bias circuit of Fig. 3.1, the additional voltage drop due to I_x must be taken into account when fixing V_{bias}, hence when designing T_{mb}.

4.3 NOISE ANALYSIS

4.3.1 GENERAL CONSIDERATIONS

The noise of an MOS transistor consists of [ALL87], [GRA84]:

(a) a low frequency noise component, which is reported as "1/f noise" or as flicker noise. Flicker noise has a spectral power density with a 1/f frequency dependence (hence its name), and is mainly due to carrier traps at the $Si-SiO_2$ interface.

(b) a white noise component the spectral power density of which is uniform. If the MOS transistor is biased in strong inversion, the main noise component is thermal noise, which is due to the random motion of electrons. On the other hand, shot noise, which is associated with the DC current flowing across the potential barrier, is the principal noise component, if the transistor is biased in weak inversion.

These noise sources are independent and can be represented in the small signal model of the MOS transistor either by a current generator from drain to source, or by a voltage source in series with the gate. An equivalent input noise resistance R_N can be defined for MOS transistors in saturation [VIT89],

$$R_N = \frac{\gamma}{g_m} + \frac{\rho}{fW_{ef}L_{ef}} \tag{4.26}$$

This noise resistance can be associated with the double sided voltage noise spectral power density $S_V(f)$ or with the double sided current noise spectral power density $S_I(f)$:

$$S_V(f) = 2kT R_N \qquad\qquad -\infty > f > +\infty \tag{4.27}$$

$$S_I(f) = g_m^2 S_V(f) = g_m^2 2kTR_N \qquad -\infty > f > +\infty \tag{4.28}$$

If the MOS transistors operate as switches, hence in the triode region, their equivalent noise resistance R_N is given by:

$$R_N = \frac{1}{\beta_{sw}(V_G - V_{T0} - nV_s)} = \frac{1}{g_{on}} \tag{4.29}$$

and $S_I(f)$ yields

$$S_I(f) = g_{on}{}^2 S_V(f) = 2kTg_{on} \qquad -\infty > f > +\infty \qquad (4.30)$$

Integrating S_V or S_I over the frequency domain leads to total voltage components V_N^2 or current noise components I_N^2, respectively.

According to eq. (4.26) & (4.28) $S_I(f)$ can be defined as:

$$S_I(f) = g_m^2 \; 2kT\{\frac{\gamma}{g_m} + \frac{\rho}{fW_{ef}L_{ef}}\} = 2kT\gamma \, g_m\{1 + \frac{f_k}{|f|}\} \qquad (4.31)$$

where $f_k = \dfrac{g_m \, \rho}{\gamma \, W_{ef} L_{ef}}$ is the so-called corner frequency, corresponding to the frequency where white and 1/f noise spectral densities are equal.

A dynamic current mirror is a sampled data circuit and therefore two kinds of noise sources are present:

(a) direct noise, which occurs when the output current is sinked

(b) sampled noise, which is due to the storage of the instantaneous value of a noise voltage on C, and which is superposed on the correct value of the gate voltage V.

The output current noise component I_N^2 is the superposition of these two noise currents.

4.3.2 IMPORTANCE OF DIRECT NOISE SOURCES

The different noise sources of a self-biased dynamic mirror are represented in Fig. 4.4. The following considerations remain valid for any kind of cascoded structure.

The total output current noise spectral power density $S_{Iout}(f)$ is the superposition of the noise sources represented in Fig. 4.4.

$$S_{Iout}(f) = S_{Ioc}(f) + S_{Iom}(f) + S_{Ioz}(f) \qquad (4.32)$$

where $S_{Iom}(f)$ and $S_{Ioz}(f)$ are the contributions to $S_{Iout}(f)$ of T_{mj} and g_{zl}, respectively.
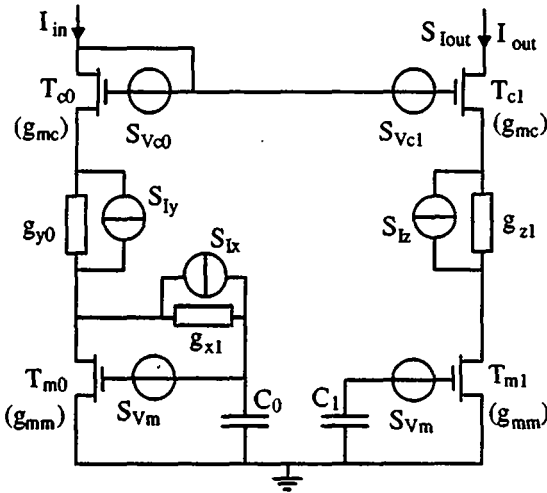
Figure 4.4: Noise sources of a cascoded dynamic current mirror (only the conducting switches are represented)

$S_{Ioc}(f)$ stands for the noise contribution of T_{c1} and for all the noise sources of the input branch of the circuit.

These contributions are:

(a)

$$S_{Ioz}(f) = \left[\frac{(n g_{mc} + g_{dsc}) g_{dsm}}{g_z (n g_{mc} + g_{dsm} + g_{dsc})}\right]^2 S_{Iz}(f) \approx g_{dsm}^2 \, S_{Vz}(f) \quad (4.33)$$

A high switch conductance g_z is desirable, hence $S_{Vz}(f)$ is very small.

(b) $S_{Ioc}(f)$, for a transistor T_{c1} located in a common well, is found to be :

$$S_{Ioc}(f) \approx \frac{g_{dsm}^2}{n^2} \left[S_{Vc1}(f) + \frac{S_{Iin}(f)}{g_{mc}^2}\right] \quad (4.34)$$

In this expression n is replaced by one if T_{c1} is in a separate well which is connected to the source.

(c) $S_{Iom}(f)$ can be expressed, regardless of whether T_{c1} is located in a common well or in a separate well, as:

$$S_{Iom}(f) \approx g_{mm}^2 S_{Vm}(f) \qquad (4.35)$$

From eq. (4.33) to eq. (4.35) it can be seen that the noise spectral power densities $S_{Ioz}(f)$ and $S_{Ioc}(f)$ are negligible compared to $S_{Iom}(f)$, hence only this noise spectral power density has to be taken into account.

4.3.3 INHERENT AUTOZEROING EFFECT IN THE CURRENT COPIER

The small signal representation of a basic cell and the waveforms of the different interfering currents are represented qualitatively in Fig. 4.5. The current variations are assumed to be small compared to the steady current, so that a small signal representation is acceptable.

The noisy current source $I_N(t)$ stands for all the noise sources of a current copier. The switch conductance g_x of S_x is assumed to be negligible to simplify the qualitative representation.

When switches S_x and S_y are closed, the instantaneous current error $\Delta I(t)$ is forced to be zero, because the drain node is connected to a high impedance, to the input current source I_{in}:

$$\Delta I(t) = I_N(t) + g_{mm} \Delta V_N(t) = 0 \qquad nT_s + T_h < t < (n+1)T_s \qquad (4.36)$$

Any kind of DC noise component or offset is cancelled, while the feedback loop is closed, because $\Delta V_N(t)$ is an image of $I_N(t)$.

At time $t = nT_s$ the sampling switch S_x is opened and the instantaneous value of $\Delta V_N(t) = \Delta V_N(nT_s)$ is frozen on C. $\Delta I(t)$ becomes:

$$\Delta I(t) = I_N(t) + g_{mm} \Delta V_N(nT_s) \qquad nT_s < t < nT_s + T_h \qquad (4.37)$$

where T_s is the sampling period, n an integer value and T_h the duration of the hold time.
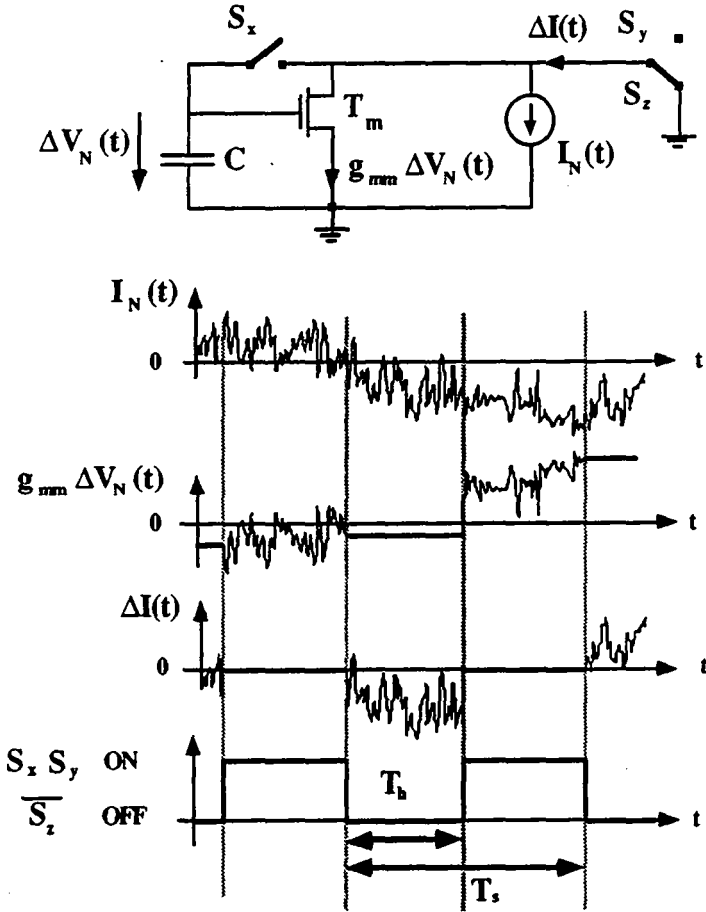
Figure 4.5:   Qualitative representation of the inherent autozeroing effect

Due to the periodical updating of the gate voltage $\Delta V_N(t)$ the current error $\Delta I(t)$ is forced to zero each time S_x and S_y are closed.

Because it is common practice to compare the noise performances of circuits with the noise expressed in volts, the following noise analysis refers to the gate voltage variations $\Delta V_N(t)$ on the storage capacitor C instead of $\Delta I_N(t)$, but both representations are equivalent. If $\Delta V_N(t)$ is known, the

corresponding current noise $\Delta I_N(t)$ is easily derived with the help of eq. (4.35).

Fig. 4.6 shows the functional block diagram where the noise source $I_N(t)$ has been split into $I_{NT}(t)$ and $I_{Ng}(t)$, which stand for the noisy transistor T_m and the noisy switch S_x, respectively. A priori it is not possible to neglect the noise of S_x during the storage phase, since a low sampling switch conductance g_x might be desired to reduce the charge injection in C.

During the storage phase the two noise sources $I_{NT}(t)$ and $I_{Ng}(t)$ produce variations of the gate voltage $\Delta V(t)$ through their transfer function $f(t)$ and $g(t)$, respectively. These gate voltage variations enter the sample-&-hold block, which in Fig. 4.6 is surrounded by a dotted line.

When T_m is switched back to the output to restore the current, the sampled noise component is added to the only direct noise component which is due to T_m. Because the direct noise component influences the output current during the restoring phase, its transfer function $k(t)$ is valid only in that configuration and during the hold time T_h.
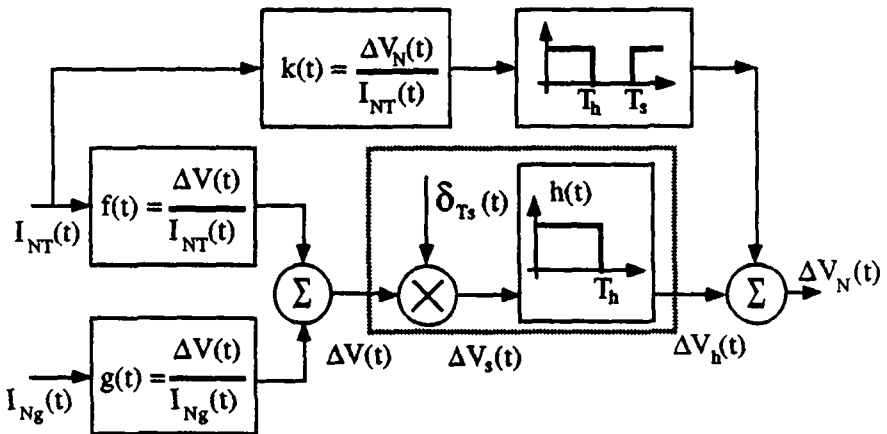

Figure 4.6:   Functional block diagram showing how the direct and sampled noise components on C are related to the noise sources $I_{NT}(t)$ and $I_{Ng}(t)$.

Finally the voltage noise component $\Delta V_N(t)$ on C can be expressed according to Fig. 4.6 as:

$$\Delta V_N(t) = \left[I_{NT}(t) * f(t) + I_{Ng}(t) * g(t) \right] * \left[\text{sample-\&-hold-block impulse response} \right]$$
$$+ I_{NT}(t) * k(t) * \text{[pulse-train-response]} \qquad (4.38)$$

where the "$*$" symbol stands for the convolution operator [COU84], and the pulse-train-response has been approximated in [FIS82] by $\sqrt{\frac{T_h}{T_s}}$. To evaluate eq. (4.38) the expressions of the sample-&-hold block impulse response and of the three transfer functions $f(t)$, $g(t)$ and $k(t)$ have to be found.

4.3.4 NOISE TRANSFER FUNCTIONS : $F(f)$, $G(f)$, $K(f)$

During the restoring phase only the direct noise component of source $I_{NT}(f)$ exists, according to Fig. 4.6 and to the considerations made in §4.3.2. The bilateral Fourier transform $K(f)$ of the direct transfer function $k(t)$ is given by the relation between the current noise spectral power density and the voltage noise spectral power density.

$$K(p) = \frac{\Delta V_N(p)}{I_{NT}(p)} = \frac{1}{g_{mm}} \qquad (4.39)$$
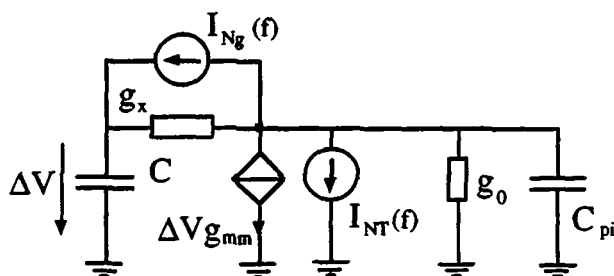
where $p = j2\pi f$.

Figure 4.7: Small signal scheme during the storage phase with noise sources $I_{NT}(f)$ and $I_{Ng}(f)$

In Fig. 4.7 C_{pi} stands for all the parasitic capacitances at the input node, at the drain of T_m, and includes the parasitic switch capacitances, whereas g_0 includes all the parasitic conductances at this node. Assuming that the conductance of the external current source I_{in} is much smaller than the parasitic conductance g_0 of the basic cell, the only remaining noise sources during current storage are $I_{NT}(f)$ and $I_{Ng}(f)$.

With the help of the small signal model of a basic cell during the storage phase (Fig. 4.7), the transfer function $F(p)$ and $G(p)$, corresponding to $f(t)$ and $g(t)$, respectively, can be found. During the storage phase the transfer functions $F(p)$ and $G(p)$ in the frequency domain are found to be:

$$F(p) = \frac{\Delta V(p)}{I_{NT}(p)}\bigg|_{I_{Ng}(p)=0} = -\frac{g_x}{D(p)} \tag{4.40}$$

and:

$$G(p) = \frac{\Delta V(p)}{I_{Ng}(p)}\bigg|_{I_{NT}(p)=0} = -\frac{g_0 + pC_{pi}}{D(p)} \tag{4.41}$$

where the denominator $D(p)$ is equal to:

$$D(p) = (g_{mm}+g_0)g_x + p[C(g_x+g_0)+C_{pi}g_x] + p^2CC_{pi} \tag{4.42}$$

Appendix B deals with the roots of denominator $D(p)$.

The Fourier transform $\Delta V(p)$ of the noise error $\Delta V(t)$ on C during storage is the sum of both noise contributions, hence:

$$\Delta V(p) = I_{NT}(p)\, F(p) + I_{Ng}(p)\, G(p) \tag{4.43}$$

Comparing the noise components induced on C due to $I_{NT}(p)$ or to $I_{Ng}(p)$ leads to:

$$\frac{\Delta V_{Ng}(p)}{\Delta V_{NT}(p)} = \frac{g_0(1+\frac{pC_{pi}}{g_0})\, I_{Ng}(p)}{g_x\, I_{NT}(p)} = \frac{g_0(1+\frac{pC_{pi}}{g_0})}{\sqrt{g_x\, g_{mm}}} \approx \frac{pC_{pi}}{\sqrt{g_x\, g_{mm}}} \tag{4.44}$$

where the approximation is valid while $\omega > \frac{g_0}{C_{pi}}$. In eq. (4.44) it is apparent that the contribution of the sampling switch noise is increasing with frequency. For frequencies lower than $\frac{\sqrt{g_x \, g_{mm}}}{2 \pi \, C_{pi}}$, the noise contribution of S_x is found to be negligible even if $g_x \approx g_0$.

4.3.5 SAMPLE-&-HOLD BLOCK

The sample-&-hold operation is based on two operators: namely an ideal sampler and a hold element. They are surrounded by dotted lines in Fig. 4.6. The first operator multiplies the input signal $\Delta V(t)$ with a sequence of Dirac distributions, which are modeled as follows:

$$\delta_{Ts} = \sum_{n=-\infty}^{+\infty} \delta(t-nT_s) \tag{4.45}$$

where δ_{Ts} represents the sampling operator [COU84]. Due to the multiplication of $\Delta V(t)$ with δ_{Ts} the continuous gate voltage is translated into a sampled one, hence

$$\Delta V_s(t) = \Delta V(t) \, \delta_{Ts} = \sum_{n=-\infty}^{+\infty} \Delta V(nT_s) \, \delta(t-nT_s) \tag{4.46}$$

The sequence of samples at time instants nT_s is retransformed by convolution with the second operator, the hold function $h(t)$, which is given by

$$h(t) = \begin{cases} 1 & for \, 0 \leq t \leq T_h \\ 0 & elsewhere \end{cases} \tag{4.47}$$

and yields

$$\Delta V_h(t) = \Delta V(t) \, \delta_{Ts} * h(t) = h(t) \cdot \sum_{n=-\infty}^{+\infty} \Delta V(nT_s) \, \delta(t-nT_s)) \tag{4.48}$$

The convolution in the time domain can be replaced by a multiplication in the frequency domain.

The bilateral Fourier transform δ_{fs} of sampling signal δ_{Ts} is found to be:

$$\delta_{fs} = \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \delta(f - \frac{n}{T_s}) = f_s \sum_{n=-\infty}^{+\infty} \delta(f - nf_s) \qquad (4.49)$$

where $f_s = \frac{1}{T_s}$, which leads to:

$$\Delta V_h(f) = \Delta V(f) \cdot \delta_{fs} \; H(f) = H(f) \; \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \Delta V(f - nf_s) \qquad (4.50)$$

where $H(f)$ is the Fourier transform of the hold function $h(t)$ defined by eq. (4.47) and represented in Fig. 4.6.

$$H(f) = \frac{sin(\pi f T_h)}{\pi f} \; e^{-j\pi f T_h} = T_h \; sinc(\pi f T_h) \; e^{-j\pi f T_h} \qquad (4.51)$$

The bilateral Fourier transform of the sampled-&-hold noise voltage $\Delta V_h(f)$ can be expressed as:

$$\Delta V_h(f) = \frac{T_h}{T_s} \; sinc(\pi f T_h) \; e^{-j\pi f T_h} \sum_{n=-\infty}^{+\infty} \Delta V(f - nf_s) \qquad (4.52)$$

where the last term corresponds to noise components which are shifted to the integer values of the sampling frequency f_s, and where the exponential function is due to the delay of $h(t)$.

Note that for a dynamic current mirror of ratio 1:1 the sampling frequency f_s is twice the switching frequency f_{sw}. Or in other words, the output sees only one transistor which is updated instantaneously with f_s and where $T_h = T_s$.

4.3.6 VOLTAGE NOISE $V_N(f)$ & VOLTAGE NOISE SPECTRAL POWER DENSITY $S_V(f)$ ON C

4.3.6.1 Expressions in the Time & Frequency Domain

The total voltage noise $\Delta V_N(t)$ on C, at the gate of T_m, can be written, according to Fig. 4.6 and to eq. (4.38), as:

$$\Delta V_N(t) = \{I_{NT}(t)*f(t) + I_{Ng}(t)*g(t)\}\, \delta_{T_s}*h(t) + I_{NT}(t)*k(t)*[p\text{-}t\text{-}r] \quad (4.53)$$

After replacing in eq. (4.53) the corresponding transfer functions by the expressions found in the precedent sections, the total voltage noise $\Delta V_N(f)$ on C in the frequency domain is found to be:

$$\Delta V_N(f) = \frac{T_h}{T_s}\, sinc(\pi f T_h)\, e^{-j\pi f T_h} \sum_{n=-\infty}^{+\infty} I_{NT}(f\text{-}nf_s)F(f\text{-}nf_s) + I_{NT}(f)\, K(f)\, \sqrt{\frac{T_h}{T_s}}$$

$$+ \frac{T_h}{T_s}\, sinc(\pi f T_h)\, e^{-j\pi f T_h} \sum_{n=-\infty}^{+\infty} I_{Ng}(f\text{-}nf_s)G(f\text{-}nf_s) \quad (4.54)$$

4.3.6.1 AUTOZERO TRANSFER FUNCTION OF T_m

The contribution of the noise current $I_{NT}(f)$ of the main transistor in eq. (4.49) can be rewritten as:

$$\Delta V_{NT}(f) = \frac{1}{g_{mm}} \sum_{n=-\infty}^{+\infty} X_n(f)\, I_{NT}(f\text{-}nf_s) \quad (4.55)$$

where $X_n(f)$ is defined as :

$$X_n(f) = \begin{cases} \sqrt{\dfrac{T_h}{T_s}} - \dfrac{g_{mm}\, g_x\, \dfrac{T_h}{T_s}\, sinc(\pi f T_h)\, e^{-j\pi f T_h}}{D(f)} & \text{for } n=0 \quad (4.56) \\[4mm] \dfrac{g_{mm}\, g_x\, \dfrac{T_h}{T_s}\, sinc(\pi f T_h)\, e^{-j\pi f T_h}}{D(f\text{-}nf_s)} & \text{for } n\neq 0 \quad (4.57) \end{cases}$$

with: $e^{-j\pi f T_h} = cos(\pi f T_h) + jsin(\pi f T_h)$ (4.58)

and $D(f)$ given by eq. (4.41).

The magnitude of $X_n(f)$ for low frequencies, hence in the baseband, is found to be:

for n=0

$$|X_0(f)| = \frac{T_h}{T_s} \sqrt{\left[\sqrt{\frac{T_s}{T_h}} \frac{g_{mm}}{g_{mm}+g_0} \frac{sin(2\pi f T_h)}{2\pi f T_h}\right]^2 + \left[\frac{g_{mm}}{g_{mm}+g_0} \frac{1-cos(2\pi f T_h)}{2\pi f T_h}\right]^2}$$

(4.59)

for n≠0

$$|X_n(f)| = \frac{T_h}{T_s} \frac{g_{mm}}{(g_{mm}+g_0)} \sqrt{sinc^2(\pi f T_h)}$$ (4.60)

The magnitudes $|X_0(f T_s)|$ and $|X_n(f T_s)|$ while $T_h = T_s$, are plotted in Fig. 4.8 for small values of $f T_s$. They are similar to the ideal transfer functions of an autozero amplifier [VIT85.2], [ENZ89].
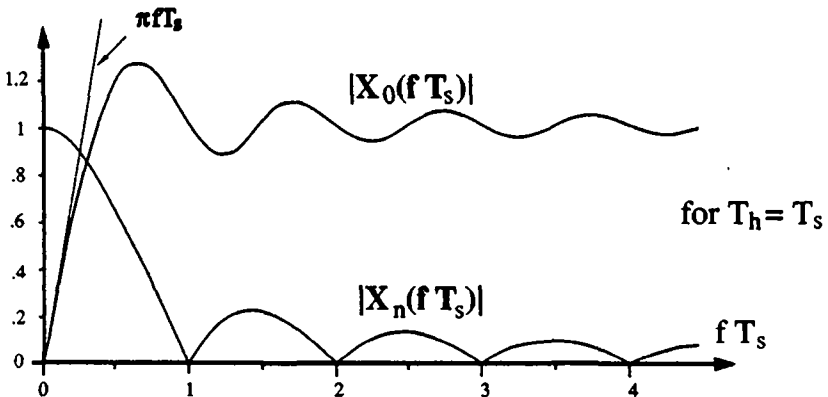

Figure 4.8:   Magnitude of the transfer functions $X_0(f T_s)$ and $X_n(f T_s)$ for $T_s = T_h$

It can easily be seen that the limit of $|X_0(f)|$ while $f \to 0$ and $g_{mm} \gg g_0$ is:

$$\lim_{f \to 0} |X_0(f)| \to \sqrt{\frac{T_h}{T_s}} \{ 1 - \sqrt{\frac{T_h}{T_s}} \} \qquad (4.61)$$

The first term of eq. (4.61) is due to the direct noise, whereas the second term stands for the sampled noise.

For $T_h = T_s$ the function $X_0(f)$ equals zero while $f \to 0$, according to the considerations made in §4.3.3 on the inherent autozeroing effect of a current copier. The offset of a transistor, which can be defined as the deviation of its threshold voltage compared to the ideal value, can be represented as a peak at $f = 0$. According to eq. (4.61) this peak is not completely cancelled at the origin for $T_h = T_s$, but rather attenuated by the ratio $\frac{g_0}{g_0 + g_{mm}}$.

4.3.6.3 Voltage Noise Spectral Power Density $S_V(f)$

From eq. (4.54) the noise voltage spectral power density $S_V(f)$ on C is deduced:

$$S_V(f) = \frac{S_{IT}(f)}{g_{mm}^2} |X_0(f)|^2 + \sum_{\substack{n = -\infty \\ n \neq 0}}^{+\infty} |X_n(f - nf_s)|^2 \frac{S_{IT}(f - nf_s)}{g_{mm}^2}$$

$$+ sinc^2(\pi f T_h) \sum_{n = -\infty}^{+\infty} |G(f - nf_s)|^2 S_{Ig}(f - nf_s) \qquad (4.62)$$

The last terms of eq. (4.62), which sum the low-pass filtered translated spectra $S_{IT}(f)$ and $S_{Ig}(f)$, are due to the undersampling of the spectral densities. These sums must be evaluated analytically and that is they are decomposed into their white noise foldover terms and into their $1/f$ foldover terms. These foldover terms are estimated with the help of the "equivalent noise bandwidth technique". Furthermore eq. (4.62) assumes that the shifted current spectral densities $S_{IT}(f - nf_s)$ and $S_{Ig}(f - nf_s)$ are uncorrelated [LIO79], [GOB83].

4.3.7 ALIASING EFFECTS

4.3.7.1 Equivalent Noise Bandwidth Technique

The "equivalent noise bandwidth technique" is extensively described in Appendix C for the white and the $1/f$ noise.

The open loop transfer function of the current mirror during the storage phase can be represented by

$$\frac{-1}{p\tau_d(1 + p\tau_p)} \tag{4.63}$$

with the time constants τ_d and τ_p (Appendix B).

The "equivalent white noise bandwidth" Δf_w is found to be

$$\Delta f_w = \frac{1}{4\tau_d} = \frac{\pi f_c}{2} \tag{4.64}$$

with the cut-off frequency

$$f_c = \frac{1}{2\pi\tau_d} = \frac{g_{mm}}{2\pi(C+C_{pi})} \tag{4.65}$$

Appendix C shows that relation (4.64) is always valid for a second order low-pass filter, independently of whether the poles are real or complex. Note that Δf_w only depends on τ_d and is independent of τ_p [VIT84]. If $\tau_d > 4\tau_p$ the poles of the closed loop function are real and hence can be split into two factors.

In the case of the $1/f$ noise, the "equivalent $1/f$ noise bandwidth" $\Delta f_{1/f}$ is given by

$$\Delta f_{1/f} = \frac{1}{2\pi\tau_d} \tag{4.66}$$

The result of eq. (4.66) is exact for a first order low-pass filter and a valid approximation for a second order low-pass filter, if τ_d is larger than τ_p. Appendix C shows this equivalence in the case of a first order, unity gain

low-pass filter, and the approximations made for a second order, unity gain low-pass filter.

Eq. (4.66) means that the 1/f noise power of an ideal low-pass filter with cut-off frequency $\Delta f_{1/f}$ is identical to the power of a real, first order low-pass with the same cut-off frequency f_c while the DC gain of the two filters is identical.

An undersampling factor N can be defined [ENZ89] as the closest integer number to:

$$N = \frac{2\Delta f}{f_s} = 2 \Delta f T_s \tag{4.67}$$

This undersampling factor corresponds to the maximum number of shifted spectra which still increase the noise density in the "equivalent bandwidth" and which have to be considered.

4.3.7.2 WHITE NOISE ALIASING

The foldover terms which are due to the white noise of the main transistor T_m, hence the infinite sum of the second term of eq. (4.62), can now be evaluated with the "equivalent noise bandwidth technique" and yields:

$$S_{VTwfold}(f) = \frac{g_x^2 g_{mm}^2 T_h^2 sinc^2(\pi f T_h)}{g_{mm}^2 T_s^2} \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{S_{ITw}(f-nf_s)}{|D(f-nf_s)|^2}$$

$$\approx \frac{T_h^2 sinc^2(\pi f T_h)}{T_s^2} \sum_{\substack{n=-\frac{N}{2} \\ n\neq 0}}^{+\frac{N}{2}} \frac{2kT\gamma g_{mm}}{(g_{mm}+g_0)^2}$$

$$= 2kT\gamma \frac{T_h^2 sinc^2(\pi f T_h)}{T_s^2 g_{mm}} \left\{ \frac{\pi f_c}{f_s} -1 \right\} \tag{4.68}$$

where $S_{ITw}(f) = 2kT\gamma g_{mm}$ is the white noise current spectral density of T_m.

The total double sided white noise voltage spectral power density $S_{VTw}(f)$ on C due to T_m can be expressed as:

$$S_{VTw}(f) = \frac{2kT\gamma}{g_{mm}} |X_0(f)|^2 + S_{VTwfold}(f) \qquad (4.69)$$

If the aliasing effect dominates, $\frac{\pi f_c}{f_s} \gg 1$, $S_{VTw}(f)$ can be approximated by

$$S_{VTw}(f) = \frac{2kT\gamma}{g_{mm}} \left\{ |X_0(f)|^2 + \frac{T_h^2 sinc^2(\pi f T_h)}{2 T_s \tau_d} \right\} \qquad (4.70)$$

For $T_h = T_s$ and $f > f_s$, $|X_0(f)|$ can be approximated by one, which yields

$$S_{VTw}(f) = kT\gamma \left\{ \frac{2}{g_{mm}} + \frac{T_s sinc^2(\pi f T_s)}{(C+C_{pi})} \right\} \qquad (4.71)$$

where τ_d is given in Appendix B and the first term corresponds to the direct noise of T_m. The result, which was obtained by [DAU90] using a switched capacitance approach [GOB83] and neglecting any autozero considerations, consisted in the foldover term of eq. (4.71). Furthermore, the white noise of the sampling switch S_x was neglected in [DAU90] and also the aliasing effect of 1/f noise.

The contribution of the white noise of S_x, hence the infinite sum of the third term of eq. (4.62), is found to be:

$$S_{Vgw}(f) = \frac{g_0^2}{g_x^2} \frac{T_h^2 sinc^2(\pi f T_h)}{T_s^2 g_{mm}^2} \frac{T_s}{2\tau_d} \left\{ 1 + \frac{\tau_0^2}{\tau_d \tau_p} \right\} S_{Igw}(f)$$

$$\approx kT \frac{C_{pi}^2 T_h^2 sinc^2(\pi f T_h)}{g_x T_s g_{mm}^2 \tau_d^2 \tau_p} \overset{T_h = T_s}{\approx} kTT_s \frac{C_{pi}}{C (C+C_{pi})} sinc^2(\pi f T_s)$$

$$(4.72)$$

with $S_{Igw}(f) = 2kTg_x$ and $\tau_0 = \frac{C_{pi}}{g_0}$ (Appendix C).

If $\dfrac{\pi f_c}{f_s} \gg 1$, the aliasing effects of T_m and S_x can be compared to each other which yields

$$\frac{S_{VTwfold}(f)}{S_{Vgwfold}(f)} = \gamma \frac{C}{C_{pi}} \tag{4.73}$$

4.3.7.3 1/F NOISE ALIASING

The second term of eq. (4.62) can be written as:

$$S_{VI/f\text{-}fold} = \frac{T_h^2 g_x^2 g_{mm}^2 sinc^2(\pi f T_h)}{T_s^2} \frac{2kT\rho}{W_{ef}L_{ef}} \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \{ \frac{1}{f\text{-}nf_s} \frac{1}{|D(f\text{-}nf_s)|^2} \} \tag{4.74}$$

The discontinuities for $f = nf_s$ are cancelled out by the double-zero of the $sinc^2(f \pi T_h)$-function when $T_h = T_s$ [ENZ89].

The foldover term $S_{II/f\text{-}fold}(f)$, which is represented by the infinite sum of eq. (4.74), is evaluated by using the "equivalent noise bandwidth technique" as described in Appendix C. Therefore the infinite sum is approximated by only a limited number $N = \dfrac{2f_c}{f_s}$ of terms.

$$S_{VI/f\text{-}fold} \approx \frac{T_h^2 sinc^2(\pi f T_h)}{T_s^2} \frac{2kT\rho}{W_{ef}L_{ef}} \sum_{\substack{n=-\frac{N}{2} \\ n\neq 0}}^{+\frac{N}{2}} \frac{1}{f\text{-}nf_s} \tag{4.75}$$

with $g_0 \ll g_{mm}$. For $f < f_s$ this sum can be evaluated and yields:

$$S_{VI/f\text{-}fold} \approx \frac{T_h^2 sinc^2(\pi f T_h)}{T_s} \frac{2kT\rho}{W_{ef}L_{ef}} \{ 2K_{Eul} + ln\frac{f_c^2 - f^2}{f_s^2 - f^2} \} \tag{4.76}$$

where $K_{Eul} = 0.57721566...$ the so-called *"Euler's constant"*, which is found in finite integrals or summations.

For $f \ll f_s$ the aliasing effect of $1/f$ noise in the baseband can be considered as an increase of the white noise.

$$S_{V1/f\text{-}fold} \approx \frac{T_h^2 \, sinc^2(\pi f T_h)}{T_s} \frac{4kT\rho}{W_{ef}L_{ef}} \left\{ K_{Eul} + ln\frac{f_c}{f_s} \right\} \qquad (4.77)$$

The formula given by [ENZ89], which evaluates the foldover terms due to $1/f$ noise for a first order circuit in the baseband in a double sided spectral representation,

$$S_{V1/f\text{-}fold} \approx \left(\frac{T_h}{T_s}\right)^2 \, sinc^2(\pi f T_h) \, \frac{4kTT_s\rho}{W_{ef}L_{ef}} \left\{ 1 + ln\frac{2f_c}{3f_s} \right\} \qquad (4.78)$$

differs from eq. (4.77) only by a constant term in the expression of the parenthesis. Appendix C shows that the term which is independent of f_s or f_c in the parenthesis of eq. (4.78) tends to K_{Eul}, while the precision of the approximation used is increased. Note that eq. (4.77) is exact for a first order low-pass filter and a valid approximation for a second order low-pass filter with real poles. While the poles are identical, $\Delta f_{1/f}$ is reduced by a factor two and so is the constant term in the parenthesis, hence eq. (4.77) can be considered to be an upper limit on $S_{V1/f\text{-}fold}$.

The contribution of $1/f$ noise of the sampling switch S_x is negligible, because it corresponds to a modulation of the switch conductance g_x.

4.3.8 NOISE SPECTRAL POWER DENSITY $S_V(f)$ IN THE BASEBAND

In the baseband, hence for $f < f_s$, the voltage noise spectral power density $S_{VT}(f)$ on C due to T_m can be summed according to (4.70) & (4.76). In the case of $T_h = T_s$ $S_{VT}(f)$ reduces to:

$$S_{VT}(f) = \frac{2kT}{g_{mm}} \left\{ \gamma + \frac{g_{mm}\,\rho}{|f|W_{ef}L_{ef}} \right\} |X_0(f)|^2 + 2kT\gamma \, \frac{sinc^2(\pi f T_s)}{g_{mm}} \left(\frac{\pi f_c}{f_s} - 1 \right)$$

$$+ 2kT \, sinc^2(\pi f T_s) \, \frac{T_s\,\rho}{W_{ef}L_{ef}} \left\{ 2K_{Eul} + ln\frac{f_c^2 - f^2}{f_s^2 - f^2} \right\}$$

$$\qquad (4.79)$$

In the baseband $|X_0(f)|$ can be approximated by $\pi f T_s$ which yields

$$S_{VT}(f) \approx \frac{2kT\gamma}{g_{mm}f_s} \left\{ \frac{\pi^2}{f_s}f^2 + [\pi f_c - f_s] \ sinc^2(\pi f T_s) \right\}$$

$$+ \frac{2kT\rho}{f_s W_{ef}L_{ef}} \left\{ \frac{\pi^2}{f_s}f + [2K_{Eul} + ln\frac{f_c^2 - f^2}{f_s^2 - f^2}] \ sinc^2(\pi f T_s) \right\} \quad (4.80)$$

For $f \ll f_s$ and $\frac{\pi f_c}{f_s} \gg 1$ eq. (4.80) can be expressed as:

$$S_{VT}(f) \approx \frac{2kT\gamma\pi}{g_{mm}} \frac{f_c}{f_s} \ sinc^2(\pi f T_s)$$

$$+ \frac{4kT\rho}{f_s W_{ef}L_{ef}} \left\{ \frac{\pi^2}{2f_s}f + [K_{Eul} + ln\frac{f_c}{f_s}] \ sinc^2(\pi f T_s) \right\}$$

$$= kTT_s \ sinc^2(\pi f T_s) \left\{ \frac{\gamma}{C+C_{pi}} + \frac{4\rho}{W_{ef}L_{ef}}[K_{Eul}+ln\frac{f_c}{f_s}] \right\} + \frac{2kT\rho}{W_{ef}L_{ef}} \frac{\pi^2}{f_s^2}f$$

$$(4.81)$$

where f_c is given by eq.(4.65). From eq. (4.81) it can be seen, that the foldover terms of the white noise depend linearly on the ratio $\frac{f_c}{f_s}$, whereas the foldover terms of the 1/f noise only increase logarithmically with the ratio $\frac{f_c}{f_s}$. In the baseband the effect of 1/f foldover noise can be considered as an increase of the white noise. Note that usually the first term is dominant.

The voltage noise spectral power density of S_x on C due to white noise, is given by eq. (4.71). In the case of $T_h = T_s$, $S_{Vgw}(f)$ reduces to:

$$S_{Vgw}(f) = kT \frac{g_0^2}{g_x} \frac{sinc^2(\pi f T_s)}{g_{mm}^2} \frac{T_s}{\tau_d} \left\{ 1 + \frac{\tau_0^2}{\tau_d\tau_p} \right\}$$

$$\approx kTT_s \frac{C_{pi}}{C(C+C_{pi})} \ sinc^2(\pi f T_s) \quad (4.82)$$

Because $S_{Vg}(f)$ and $S_{VT}(f)$ are uncorrelated, the total double sided voltage noise spectral power density $S_V(f)$ is simply the sum of eq. (4.79) & (4.82).

4.4 CHARGE INJECTION BY ANALOG SWITCHES

4.4.1 GENERAL CONSIDERATIONS

The scheme of a dynamic current mirror uses several switches, which are all realized with MOS transistors. To close these switches, minority carriers have to be attracted into the channel by the gate voltage.

When the switching transistor is turned off, these channel charges are released and alter the voltages on the capacitances at both ends of the transistor [VIT85.2], [WEG87]. The disturbance of the sampled voltage due to such carriers is a major limitation to the accuracy of sampled circuits.

A dynamic current mirror is based on a sample-&-hold circuit, and hence its performance depends on the accurate storage capability of the gate voltage. For this reason the charge injection or clock feedthrough phenomenon is analyzed in detail in Appendix D.

4.4.2 INTERFERING PARAMETERS

The amount of charge injected into the hold capacitor C depends on the following parameters (according to Appendix D):

- on the normalized switching parameter B, which is given by

$$B = (V_{GON} - V_{TE}) \sqrt{\frac{\beta}{a \, C}} \qquad (4.83)$$

(where a is the slope of the gate voltage, which controls the switch)

- on the ratio of the hold to source capacitors $\dfrac{C}{C_s}$

Fig. 4.9 regroups these parameters and shows the variation of the normalized injected charge $\dfrac{\Delta Q}{Q_{tot}}$ into C as a function of B and $\dfrac{C}{C_s}$.

Note that the overlap capacitances C_{gh} and C_{gs} of the switch, which couple the gate to the hold and to the source capacitance, respectively, shift the corresponding $\dfrac{C}{C_s}$ curve either up or down depending on the sign of the difference $C_{gh} - C_{gs}$.
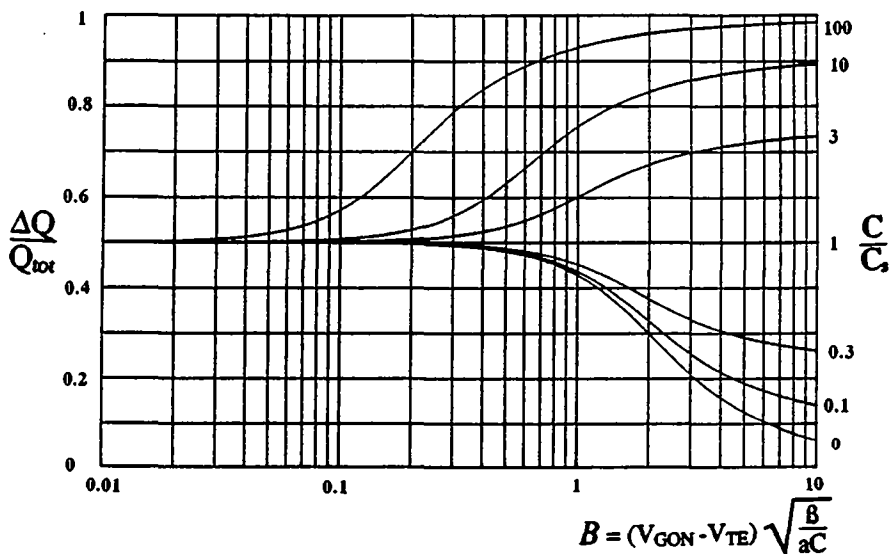
$$B = (V_{GON} - V_{TE}) \sqrt{\frac{\beta}{aC}}$$

Figure 4.9:   Normalized diagram showing the amount of normalized charge $\frac{\Delta Q}{Q_{tot}}$
injected in C as a function of the switching parameter B and the
capacitance ratio $\frac{C}{C_s}$ [VIT85.2].

4.4.3 STRATEGIES

Several strategies are possible which either reduce the amount of charge
injected into C or which balance the charges injected into both end
capacitors.

If the channel charge is equitably shared between drain and source, it is
possible to compensate the excessive charge ΔQ on the holding capacitor C
with "symmetrical dummy switches". This requires an adequate design of
the switching parameters and a carefully optimized layout (see Chapter 6).
The residual charge Δq is ultimately limited by the degree of matching
between the main switch and the "symmetrical dummy switches".

If B is chosen much larger than 1 and $C_s \gg C$ all charges released flow back
into the source capacitor C_s during the decay of V_G and the amount of

injected carriers into C is reduced. But a high value of B means a small gate slope a, hence a long switch-off time, which is often not acceptable, because it limits the operating speed of the circuit.

If $C_s = C$ it is obvious that the channel charges are evenly shared between source and drain, and only a mismatch of the overlap capacitances contributes to a charge difference. It is often not possible to exactly balance the value of a functional capacitor C with that of an estimated, parasitic capacitance C_s.

Another possibility is to choose small values for B, which ensure the equipartition of the total channel charge. An advantage of this strategy arises from the fact that the slope of the graph shown in Fig. 4.9 is small, hence a dispersion of certain parameters does not influence significantly the charge distribution.

The switching parameter B can be reduced with the help of the effective gate voltage, the slope a, and the capacitor C.

If "dummy switches" are used, the minimal switch is given by twice the minimal transistor size, which determines the transfer parameter β of the sampling switch. The chosen process determines the minimal possible transistor size, and therefore the minimal β.

The slope a depends on the driving capability of the inverters used and on the parasitic capacitances which have to be charged and discharged. The estimation of slope a is therefore very inaccurate, but the larger slope a, the better the charge equipartition.

The error voltage ΔV depends on the value of C, because

$$\Delta V = \frac{\Delta Q}{C} \qquad (4.84)$$

The corresponding current error of a dynamic current mirror is given by eq. (2.1). The maximal value of C is limited by the occupied area on the chip and by the operating speed (see Chapter 5).

The last parameter which can be modified is the effective gate voltage $(V_{GON} - V_{TE})$. Furthermore, reducing $(V_{GON} - V_{TE})$ reduces also the channel conductance g_x, hence the total channel charge Q_{tot}.

4.4.4 REDUCTION OF THE TURN-ON VOLTAGE V_{GON} OF THE SAMPLING SWITCH S_X

The total channel charge Q_{tot} of sampling switch S_x is related to its g_x by:

$$Q_{tot} = \frac{g_x L_{ef}^2}{\mu} \tag{4.85}$$

where the conductance is found to be in:

weak inversion $\qquad\qquad g_x = \frac{I_{Dsat}}{U_T} \tag{4.86}$

strong inversion $\qquad g_x = \sqrt{2n\beta I_{Dsat}} = \beta(V_{GON} - V_{TE}) \tag{4.87}$

Note that while $g_x \to 0$ the drain voltage V_{dm} of $T_m \to \infty$, and therefore it is not possible to cancel out Q_{tot} by reducing g_x to zero (see also § 4.2.2).

One possible scheme which adjusts the gate turn-on voltage of sampling switch S_x to the input voltage V_{in} and therefore reduces g_x is shown in Fig. 4.10.

Figure 4.10:   Circuit which adjusts the gate turn-on voltage V_{GON} of sampling switch S_x to the input voltage V_{in}

The purpose of this circuit is to reproduce the source potential of S_x at the source of T_x', hence to reproduce the potential of node A at node A'. This is implemented with the aid of the two matched transistors T_a and T_b.

Now, sampling switch S_x is turned on by driving its gate by the gate voltage of T_x', with the aid of voltage follower T_f and through the inverter *Inv*. The inverter is built either with p-channel and n-channel devices or only with n-channel transistors depending on the value of potential A.

It has to be pointed out that the tuning circuit of Fig. 4.10 contains two loops which can introduce instabilities. After calculating the open loop transfer function the phase margin Φ can be approximated as:

$$\Phi = \frac{\pi}{2} - arctg \frac{g_{mx} \cdot C_2}{g_{mf} C_1} \tag{4.88}$$

where the capacitances C_1 and C_2 are represented in Fig. 4.10, and the transconductances are those of T_x' and T_f, respectively. Eq. (4.88) is obtained by cancelling approximately a pole with a zero which reduces the 3rd order equation. As the zero is smaller than the pole, eq. (4.88) is too pessimistic.
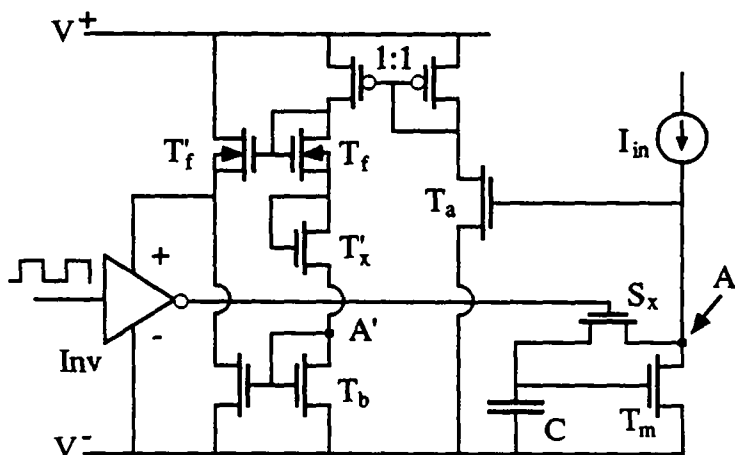

Figure 4.11: Circuit adjusting the gate voltage V_{GON} of sampling switch S_x to the input voltage V_{in}

If Φ approaches zero, hence $\dfrac{g_{mx} \cdot C_2}{g_{mf} C_1}$ is large, eq. (4.88) shows that instability may occur.

Another scheme, which is based on a similar idea is proposed in Fig. 4.11 [WEG89.2]. It has no stability problems but the gate voltage of S_x depends not only on the parameters of T'_x, but also on the matching of T_f and T'_f, or in other words, on the similarity of their corresponding gate-to-source voltages.

The relation between the source and the gate voltages of S_x and T'_x in Fig. 4.10 & 4.11 can be calculated with the help of Fig. 4.12, where it is assumed that the potential at node A is identical to the potential at node A'.

The conductance g_x which is now adapted depends on the operating mode of transistor T'_x and can be expressed, according to Fig. 4.12, as:

T_x' in weak inversion $\qquad g_x = \dfrac{\beta_x}{\beta'_x}\, g'_x = \dfrac{\beta_x}{\beta'_x}\dfrac{I_{in}}{U_T}$ \hfill (4.89)

T_x' in strong inversion $\qquad g_x = \sqrt{\dfrac{\beta_x}{\beta'_x}}\, g'_x = \dfrac{\beta_x}{\sqrt{\beta'_x}}\,\sqrt{2nI_{in}}$ \hfill (4.90)

Figure 4.12:   Relation between gate and source voltages of T_x' and S_x
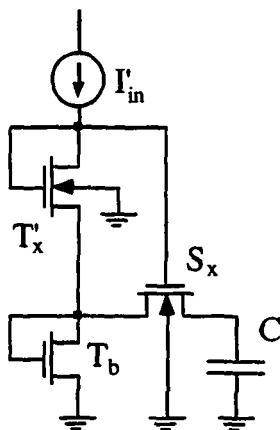
From eq. (4.89)&(4.90) it can be seen that the adapted conductance g_x is affected by the circuit which adjusts the turn-on voltage of the sampling switch.

If the turn-off voltage is chosen to fall only little beyond V_{TE}, the gate voltage swing of S_x is reduced and optimized around V_{in}, hence the amount of charge injected through the coupling of the overlap capacitances is minimized.

Another possibility to reduce the effect of charge injection is based on feedback rather than matching [DAU88], [VIT90]. The scheme is equivalent to that of offset compensation by a low sensitivity auxiliary input used in the design of operational amplifiers [VIT85.2]. It needs two steps to store the gate voltage. A capacitive attenuator reduces the influence of charge injection of the second sample-&-hold into the critical gate node. After optimizing the capacitive attenuator the residual gate voltage error ΔV can be reduced.

4.5 Summary

The principal accuracy limitations of current copiers were investigated and their influences were calculated. The effects due to the drain voltage variations of the basic cell were analyzed in detail. The influence of the leakage currents on the DC accuracy and on the absolute achievable precision were illustrated. A new complete noise analysis of the current copier was presented for the white and the 1/f noise, which took into account the inherent autozeroing effect of a dynamic current mirror. The aliasing effects of white and 1/f noise were considered for the second order low-pass filter of the current copier. The noise contributions of the main transistor and of the sampling switch were calculated and led to the estimation of the voltage noise spectral power density on hold capacitor C. The parameters influencing the distribution of the sampling switch channel charge were discussed and new strategies which reduce the effect of charge injection on the memorized gate voltage were proposed.

CHAPTER 5

DYNAMIC BEHAVIOR

&

TRANSIENT ANALYSIS

The transient behavior of a dynamic current mirror is investigated in this chapter. The two critical switching configurations and the influence of clock delays on the accuracy are presented. A simplified transient analysis is shown, the resulting glitches are illustrated and their origin explained. Finally the trade-off between the speed and the accuracy due to the conductance of the sampling switch g_x and its associated charge is highlighted.

Dynamic current mirrors are time varying circuits. This means that a different circuit configuration is present at each switching event. The analysis of the dynamic behavior of dynamic current mirrors providing non-unity ratios can be reduced to one with a 1:1 ratio, because only two basic cells are interfering while switching. To reduce the complexity of the notation the two interfering cells are named 0 and 1, like for a mirror of ratio 1:1.

For continuous time applications the amplitude and the main time constant of the transients (glitches) are very important. Their importance is limited when the currents must only be available in a specific time window and it is possible to wait until the transients have faded.

5.1 CRITICAL SWITCHING CONFIGURATIONS

5.1.1 INFLUENCE OF CLOCK DELAY

It seems obvious that the sampling switch S_{xj} must only be closed when S_{yj} is closed, according to the representation in Fig. 2.1c. Otherwise the gate voltage memorized on C_j is not representative of the input current I_{in} and an output ripple is generated.

Until now we have assumed that S_{yj} and S_{zk} ($j=0,1$ and $k=1,0$) can be switched simultaneously, which corresponds to an ideal case impossible to perform in practice. The influence of overlapping or non-overlapping clocks on the circuit configuration in the case of a "stacked" current mirror is shown in Fig. 5.1 and Fig. 5.2 [WEG90.1]. The configurations corresponding to an externally biased mirror can easily be deduced.

If the clocks overlap, S_{yj} and S_{zk} ($j=0,1$ and $k=1,0$) are all closed at the same time (all four switches) and the internal nodes are connected together as represented in Fig. 5.1. A new current mirror is formed with T_{c0} and with T_{c1}. The internal parasitic capacitances C_{pxx} represented dashed are charged by currents provided by this new current mirror and are discharged by the currents memorized in the basic cells. Hence the internal node voltage varies proportionally to the mismatch of T_{c0} and T_{c1}.

In the case of non-overlapping clocks, S_{yj} and S_{zk} are all open at the same time and the different parts of the mirror are disconnected from each other

as shown in Fig. 5.2. As a consequence parasitic capacitances C_{pis}, C_{pos} are charged by the input currents, whereas C_{pid}, C_{pod} are discharged by the currents memorized in the basic cells.
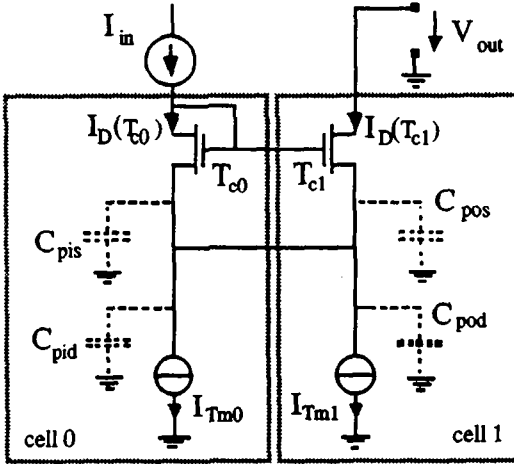

Figure 5.1:   Circuit configuration with overlapping clocks for S_{yj} and S_{zk}
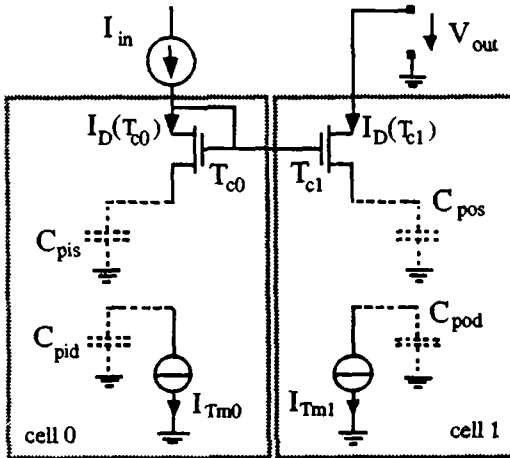

Figure 5.2:   Configuration with non-overlapping clocks for S_{yj} and S_{zk}

It will be shown that even if the time spent in such a configuration is small, large transients and non-linear effects occur and important AC components are produced; the transistors may temporarily come out of saturation, and the DC accuracy of the mirror is completely spoiled. Hence it corresponds to the worst case situation and must absolutely be avoided.

These two critical circuit configurations have been simulated with the circuit simulator program ESACAP [STA88] and the results are plotted in Figs. 5.3 & 5.4. Fig. 5.3 shows the simulated drain current variations of transistors T_{c0} and T_{cj} for the "stacked" dynamic current mirror of Fig. 3.3, whereas Fig. 5.4 shows them for the externally biased circuit shown in Fig. 3.1. The clocks where excessively delayed to better show the drain current variations.

The parameters of the simulations are: the input current I_{in} is equal to 1μA; the storage capacitor C_j is 5pF; the mismatch between the transistors T_{c0} and T_{c1} biased in weak inversion is 5mV, whereas the mismatch between T_{m0} and T_{m1} which operate in strong inversion is equal to 7.5mV. The parasitic capacitances at the internal nodes C_{p0} and C_{pi} are both 0.5pF.

5.1.2 QUALITATIVE EXPLANATION OF THE EFFECT

The two critical switching situations are:

(1) During the time period t_{1a} (Fig. 5.3) and t_{3a} (Fig. 5.4) both switches S_{yj} and S_{zj} are closed, which corresponds to the situation represented in Fig. 5.1. At time t_{1b} and t_{3b} switches S_{yj} or S_{zj} are opened and only at time t_{1c} and t_{3c} is the sampling switch S_{xj} closed, thus T_{mj} is diode connected.

(2) During the *time period* t_{2a} (Fig. 5.3) and t_{4a} (Fig. 5.4) both switches S_{yj} and S_{zj} are open, which corresponds to the situation represented in Fig. 5.2. At time t_{2b} and t_{4b} the corresponding switches S_{yj} or S_{zj} are closed and only at time t_{2c} and t_{4c} is the sampling switch S_{xj} closed again.

The current variations observed at the beginning of time t_{1a} are due to the balancing of the two voltages of the source capacitances of T_{cj} through the switch resistances of S_{yj} and S_{zj}. During the time period t_{1a} and in the case of a self-biased current mirror (Fig. 5.3), a new mirror is formed with transistors T_{cj}, while the two internal nodes are shorted. The drain currents of these transistors are modified as a function of their mismatch.
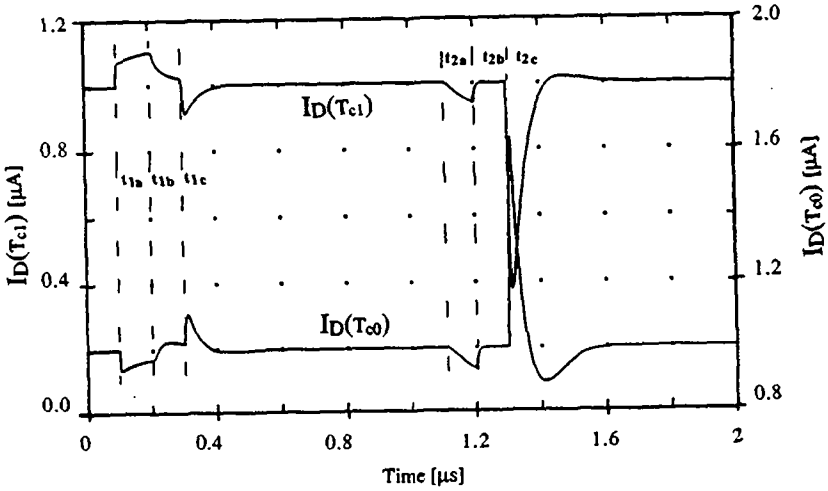
TRANSIENT ANALYSIS

Figure 5.3:   Simulated drain currents of T_{cj} of the current mirror of Fig. 3.3 for excessive overlapping and non-overlapping clocks
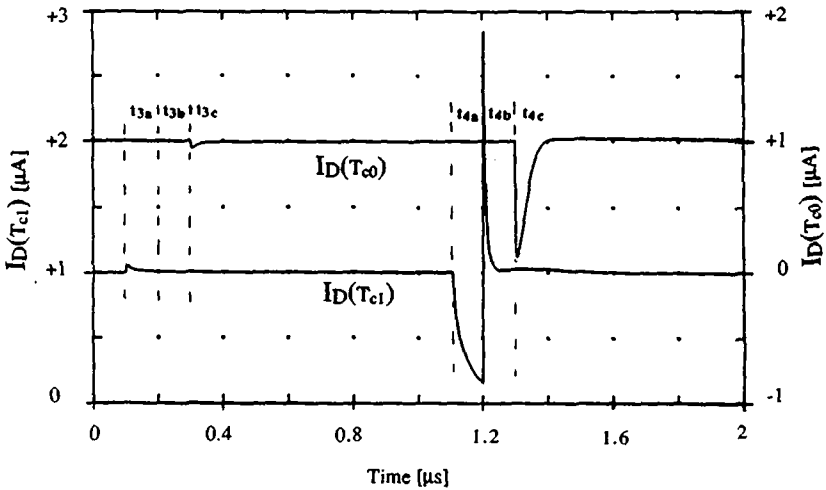
TRANSIENT ANALYSIS

Figure 5.4:   Simulated drain currents of T_{cj} of the current mirror of Fig. 3.1 for excessive overlapping and non-overlapping clocks

Thus the sum of the incoming currents, at the source node, is different from the sum of the outgoing ones, which are equal and fixed to approximately $2I_{in}$.This current difference loads the parasitic capacitances C_{pxx} connected to this internal node, and decreases or increases the node voltage depending on the sign of this difference.

During t_{1b} these internal nodes converge to an equilibrium voltage that satisfies the current balance. As soon as S_{xj} is closed (at the beginning of t_{1c}) the internal node voltages are forced back to the DC values imposed by the external current source I_{in} and therefore parasitic capacitances have to be discharged or charged from their excessive or missing charge, respectively, which was accumulated during t_{1a}. The importance of the glitches at t_{1b} or t_{1c} depend on the quantity of charge accumulated during t_{1a}. The current variations observed are proportional to the time period t_{1a} and to the mismatch of transistors T_{cj}, hence to the initial voltage difference V_{dm1}-V_{dm0} at the drains of T_{mj}.

During time period t_{2a} the source nodes of T_{c0} and T_{c1} are disconnected from the drain nodes of transistors T_{m0} and T_{m1}. The voltage at the source nodes of T_{c0} and T_{c1} increases rapidly as they are charged by a current of about I_{in}, whereas the drain voltages of T_{m0} and T_{m1} decrease, because they are discharged by the memorized drain current of value I_{in}. During t_{2b} these internal nodes are connected together again, converge to an equilibrium voltage to satisfy the current balance and, as the incoming currents are equal to the outgoing ones, the voltages remain constant. As soon as S_{xj} is closed (at the beginning of t_{2c}) the internal node voltages are forced back to the DC values and therefore parasitic capacitances have to be discharged from the excessive charge accumulated during t_{2a}. The current variations observed are proportional to time period t_{2a}, to the initial voltage difference V_{dm1} - V_{dm0} and to the input current I_{in}, thus much larger then in the case mentioned before.

Similar considerations allow us to explain the current variations shown in Fig. 5.4 for an externally biased mirror. Due to the external, fixed bias voltage V_{bias} the difference between the two critical configurations mentioned above is increased as shows Fig. 5.4, and for the worst case configuration variations of magnitude even larger than the input current can occur. For these variations the small signal analysis is not valid.

Due to such important glitches the transistors building up the dynamic current mirror may temporarily exit saturation and non-linear effects may be generated. Furthermore important AC components are added to the DC current and the DC accuracy of the mirror can be completely lost.

For well designed clocks, where the time spent in the "all-switches-closed" configuration (t_1, t_3) is minimized, the glitches can be reduced to a small percentage of the input current and depend on: (a) the mismatch between the transistors T_{m0}, T_{m1} and T_{c0}, T_{c1}; (b) the output voltage through the output conductance of T_{c1}; (c) the parasitic capacitances C_{pxx}; (d) the switch resistances and (e) the clock overlapping of the switches.

It has to be pointed out that during a cycle the glitches may all be of the same polarity, thus they do not cancel each other out. Therefore the DC accuracy of a dynamic current mirror depends on its switching frequency and on the above mentioned parameters [WEG89.2]. Special attention has to be paid to the design of the clock phases, as the amplitude of the transients is increased by non-synchronous switching of S_{yj} and S_{zk}.

5.2 SIMPLIFIED TRANSIENT ANALYSIS

5.2.1 ASSUMPTIONS

To analyze the dynamic current mirror, several assumptions have to be made, otherwise the order of the circuit is too high and no significant results can be obtained in a straightforward manner. The following assumptions are usually accepted:

(a) the functional capacitances C_j are much larger than the parasitic capacitances C_{pxx}

$$C_j \gg C_{pxx} \tag{5.1}$$

(b) the switch resistances R_y and R_z of S_{yj} and S_{zk}, respectively, are much smaller than the transconductances g_{mi}

$$R_z \approx R_y \approx R \qquad R\, g_{mi} \ll 1 \tag{5.2}$$

The switch resistances R_y and R_z have to be small in order to avoid an excessive voltage drop on the switches and to minimize the effect of switch resistance mismatch.

The time constants associated with C_{pxx} and with R are small compared to the other ones in the circuit. Therefore the ratio between the time constants is large enough, so that their influence on the circuit can be treated separately. This means that for $t \gg RC_{pxx}$ the following relation between the voltages at the switch terminals is valid

$$V_{sj}(t) = V_{dj}(t) + I_{mj}R \qquad (5.3)$$

where V_{sj} and V_{dj} $(j=0 \text{ or } 1)$ are defined according to Fig.5.5.

To reduce the number of nodes, the input node is considered to be once at high impedance $\{ \Delta V_{in}(t) = \Delta V_{s0}(t) \}$ and once at low impedance $\{ \Delta V_{in}(t) = 0 \}$. The equations obtained are now much simpler to handle, the analysis is considerably facilitated and the results obtained are the limiting cases of the real results. If the input node is considered to be at low impedance, the parasitic capacitances C_{pxs} include the gate-to-source capacitance C_{gs} of T_{cj}.

The offset of the transistors are assumed to be sufficiently small. So a small signal analysis is possible. The effect of charge injection due to S_{yj} and S_{zj} can be taken into account by modifying the initial conditions on C_{pxx}.

5.2.2 SWITCHING CONFIGURATIONS

The switching configurations which will be considered correspond to the configurations simulated in Fig. 5.3 and 5.4 during time t_1 and t_3, respectively (overlapping clock configurations).

(a) S_{xj} is opened $(j=0 \text{ or } 1)$
(b) S_{yj} and S_{zk} are closed (overlapping configuration) $(j=0,1, k=1,0)$
(c) S_{yk} and S_{zj} are opened (cells have been interchanged) $(j=0,1, k=1, 0)$
(d) S_{xj} is closed $(j=1, 0)$

(a) After opening S_{xj} the stored current I_{mj} is slightly different from I_{in} due to charge injection and noise, and therefore V_{s0} changes. The circuit drifts from its equilibrium value.
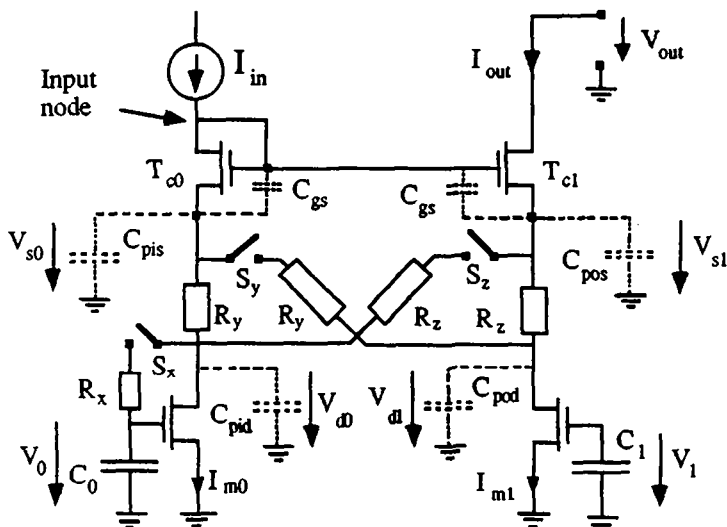
Figure 5.5:   Notation used for the simplified analysis of the transients

*(b)*When closing the switches S_{yj} and S_{zk}, the voltages on both sides of these switches are rapidly balanced with time constant

$$\tau_b = \frac{R\, C_{po} C_{pi}}{2\,(C_{po} + C_{pi})} \qquad (5.4)$$

where $C_{px} = C_{pxd} + C_{pxs}$. The resulting node voltages V_{sx} and V_{dx} depend on the parasitic capacitance ratio, hence

$$V_{slb} = V_{s0b} = \frac{C_{po}}{C_{po} + C_{pi}}\, V_{sla} + \frac{C_{pi}}{C_{po} + C_{pi}}\, V_{s0a} \qquad (5.5)$$

where the index *a* and *b* refer to the voltages during phase *(a)* and *(b)*, respectively. If the circuit remains in this situation, it drifts from its initial equilibrium values, because the internal nodes are charged by current sources which depend on the voltage mismatch ΔV_T of T_{c0} and T_{c1}, and are discharged by the stored currents I_{m0} and I_{m1}.

(c) After interchanging cell *0* and cell *1*, the voltages in each branch are balanced with a time constant

$$\tau_c = R \frac{C_{pod} C_{pos}}{C_{pod} + C_{pos}} \tag{5.6}$$

for the output branch. The resulting node voltages depend on the parasitic capacitance ratio

$$V_{s1c} = \frac{C_{pos}}{C_{po}} V_{s1b} + \frac{C_{pod}}{C_{po}} V_{s0b} \tag{5.7}$$

$$V_{s0c} = \frac{C_{pis}}{C_{pi}} V_{s0b} + \frac{C_{pid}}{C_{pi}} V_{s1b} \tag{5.8}$$

with $V_{d1b} \approx V_{s0b} - I_{in} R \approx V_{s0b}$ and $V_{d0b} \approx V_{s1b} - I_{in} R \approx V_{s1b}$.

(d) When S_{xj} is closed V_{djd} is forced to be equal to V_j and all the excessive charge accumulated during the phases *(a)* to *(c)* form a spike with an area equal to this charge.

5.2.3 INFLUENCE ON THE OUTPUT CURRENT: AC & DC

Assuming that transistor T_{c1} is externally biased (or that the impedance of the input node is low), the variations of the output current $\Delta I_{out}(t)$ are given by:

$$\Delta I_{out}(t) = g_{mc} \{ V_{s1a} - V_{s1d}(t) \} \tag{5.9}$$

Assuming that both branches are matched, hence $C_{pox} = C_{pix}$, the current transients $\Delta I_{out}(t)$ occurring at the output can be approximated by [WEG90.2]:

$$\Delta I_{out}(t) \approx g_{mc} \frac{C_{pod}}{C_{po}} (V_{s1} - V_{s0}) e^{(-t/\tau_{mo})} \tag{5.10}$$

where the main time constant τ_{mo} of the output cell is

$$\tau_{mo} = \frac{C_{po}}{g_{mc}} \tag{5.11}$$

The output time constant due to external loads is not included in τ_{mo}.

The average DC current error due to glitches can be found after integrating eq. (5.10), which leads to:

$$\overline{\Delta I_{out}} = \frac{1}{T_{sw}} \int_0^{T_{sw}} \Delta I_{out}(t) \, dt = (V_{s1} - V_{s0}) \, f_{sw} \, C_{pod} \qquad (5.12)$$

where $f_{sw} = \frac{1}{T_{sw}}$ is the switching frequency.

The average output current error $\overline{\Delta I_{out}}$ depends linearly on the switching frequency f_{sw} and is independent of I_{in}, because the current-dependent term g_{mc} of eq. (5.10) is cancelled out by τ_{mo} after integration. If $V_{out} \approx V_{in}$, the voltage difference $V_{s1} - V_{s0}$ may be approximated by the threshold mismatch ΔV_T between T_{c1} and T_{c0}.

It has to be pointed out that $V_{s1} - V_{s0}$ may remain of the same sign during the whole switching cycle. All the transients then have the same polarity and do not cancel each other out. The observed DC output error is the sum of all these errors due to the glitches.

While the input node is assumed to be at high impedance a modulation of the gate of T_{c1} occurs. The input node follows the variations of the source voltage V_{s0}:

$$\Delta I_{out}(t) = g_{mc} \{ V_{s0d}(t) - V_{s1d}(t) - (V_{s0a} - V_{s1a}) \} =$$

$$= g_{mc} \frac{C_{pod}}{C_{po}} (V_{s1} - V_{s0}) \{ e^{(-t/\tau_{mo})} + (1 + \partial) \, e^{(-t/\tau_s)} \} \quad (5.13)$$

where τ_{mo} is given by eq. (5.11) and τ_s is the settling time constant of the input cell during the storage phase (see Appendix B and § 5.3.1). ∂ stands for the relative variations of the input voltage V_{in} due to the mismatch of T_{mj}, which are transmitted to the output through the common-gate transistor T_{cj}. This additional term ∂ increases the amplitude of the glitches, but does not affect the DC accuracy, as it changes sign during a cycle, hence:

$$\overline{\Delta I_{out}} = f_{sw} \, C_{pod} \, (V_{s1} - V_{s0}) \, (1 + \frac{g_{mc}}{C_{po} \tau_s} + \partial - \partial) \approx f_{sw} \, C_{pod} \, \Delta V_T \qquad (5.14)$$

The comments made above for an externally biased current mirror remain valid.

5.3 SPEED VERSUS ACCURACY

If the current to be mirrored is variable, the role of the storage phase is not only to compensate for the effect of leakage currents, but also to update the value of the stored gate voltage V, in order to allow the variations to be followed by the output current. Correct updating is only possible if the storage time duration t_0 is longer than the settling time τ_s of the sample-&-hold formed by T_m, S_x and C. Assuming small perturbations, the settling behavior of this circuit can be examined by means of the small signal model of Fig. 4.7, where the gate-to- drain capacitance C_{gd} is neglected.

5.3.1 SETTLING TIME CONSTANT τ_s

The denominator of the transfer function of the sample-&-hold circuit is found to be according to eq. (4.42) and Appendix B:

$$D(p) = (g_{mm} + g_0) g_x \left\{ 1 + p\tau_d (1 + p\tau_p) \right\} \tag{5.15}$$

with:

$$\tau_d = \frac{C(g_x + g_0) + C_{pi} g_x}{g_x g_{mm}} \tag{5.16}$$

$$\tau_p = \frac{C\, C_{pi}}{C(g_x + g_0) + C_{pi} g_x} \tag{5.17}$$

The two poles are

$$p_{1,2} = -\frac{1}{2\tau_p} \pm \sqrt{\frac{1}{4\tau_p^2} - \frac{1}{\tau_d \tau_p}} \tag{5.18}$$

For $\tau_d \gg 4\tau_p$, it settles exponentially with time constant τ_d. While $4\tau_p > \tau_d$, the response is a damped oscillation with an envelope time constant $2\tau_p$. A global settling time constant τ_s may be approximated as

$$\tau_s = \tau_d + 2\tau_p = \frac{C^2(1 + \frac{g_0}{g_x})^2 + C_{pi}^2 + 2CC_{pi}(1 + \frac{g_0}{g_x} + \frac{g_{mm}}{g_x})}{g_{mm}\left(C(1 + \frac{g_0}{g_x}) + C_{pi}\right)} < t_0 \tag{5.19}$$

which must be 7 times smaller than the duration of the storage phase t_0 to ensure that equilibrium is reached with an accuracy of better than 1000ppm, and 10 times smaller for an accuracy better than 50ppm.

If g_x is high, τ_d is larger than $4\tau_p$ and τ_s is given by

$$\tau_d \approx \frac{C+C_{pi}}{g_{mm}} \tag{5.20}$$

If g_x is small, an overshoot of the gate voltage appears and τ_s can be approximated by

$$2\tau_p = \frac{C\,C_{pi}}{g_x[C(1+\frac{g_0}{g_x})+C_{pi}]} \tag{5.21}$$

Since the sampling frequency $f_s < \frac{1}{t_0}$ eqs. (5.20) & (5.21) put an upper limit on f_s and C, and a lower limit on g_x and g_{mm}.

5.3.2 SPEED-ACCURACY TRADE-OFF

The sampling switch conductance g_x can be expressed as (eq. 4.79):

$$g_x = \frac{\mu Q_{tot}}{L_{ef}^2} \tag{5.22}$$

The residual charge injection after compensation is $\Delta Q_{inj} = \alpha Q_{tot}$ and induces an error voltage ΔV on the *storage capacitor* C, hence an output current error ΔI_{error}, which can be written as:

$$\frac{\Delta I_{error}}{I_{in}} = \frac{g_{mm}\Delta V}{I_{in}} = \frac{\alpha L_{ef}^2}{I_{in}\,\mu}\frac{g_{mm}g_x}{C} \tag{5.23}$$

The first term depends on the technology of the device, whereas the second term can be expressed as a function of the storage time constants τ_d and τ_p. For the realistic situation where $g_x \gg g_0$ and $C \gg C_{pi}$, eq. (5.23) simplifies to:

$$\frac{\Delta I_{error}}{I_{in}} = \frac{\alpha L_{ef}^2 C_{pi}}{I_{in}\,\mu}\frac{1}{\tau_d\tau_p} \tag{5.24}$$

which shows that neither τ_d nor τ_p should be too small.

After introducing the settling time τ_s, the optimum value of τ_d and τ_p which minimizes eq. (5.24) is found to be

$$\tau_d = 2\tau_p = \frac{\tau_s}{2} \tag{5.25}$$

which yields [VIT90]

$$\frac{\Delta I_{error}}{I_{in}} = \frac{8 \; \alpha L_{ef}^2 C_{pi}}{I_{in} \; \mu} \; \frac{1}{\tau_s^2} \tag{5.26}$$

Introducing the numerical values of a standard process shows the significance of eq. (5.26).

$L = 2\mu m$ $C_{pi} = 0.2pF$ $I_{in} = 4\mu A$

$\alpha = 0.5$ (no compensation of charge injection)

$\mu = 700 \; cm^2/Vs$ (n-channel)

$\tau_s = 0.1 \; \mu s$ (compatible with $f_s = 1MHz$)

which results in $\dfrac{\Delta I_{error}}{I_{in}} = 1000$ppm.

Furthermore eq. (5.26) shows the direct dependence of the charge injection compensation α on the accuracy.

5.4 SUMMARY

The dynamic behavior of a dynamic current mirror was analyzed, the different switching configurations were shown and their influence on the output current was highlighted. It was pointed out that the different current sources of a dynamic current mirror should not be disconnected from the circuit even for a short time. Otherwise the circuit could enter the worst case configuration. A simplified analysis illustrated the influence of the switching configurations upon the transients. The current error as a function of different parameters for a self-biased and an externally biased mirror was calculated. A high sampling switch conductance reduces the acquisition time, but on the other hand, increases the amount of injected charge on the hold capacitance. This led to a speed versus accuracy trade-off as a function of the operating mode and value of the sampling switch conductance.

CHAPTER 6

LAYOUT

&

DESIGN

CONSIDERATIONS

Some layout and design considerations at the cell and circuit levels are taken into account and some principles presented, which should be considered while designing a dynamic current mirror.

6.1 GENERAL CONSIDERATIONS

The accuracy of a dynamic current mirror is to a first order approximation insensitive to the mismatch of the devices or to the parameters of the technology which are used. It has been shown in the preceding chapter that the mismatch between the components increases the amplitude of the glitches and also degrades the DC accuracy, because a certain amount of charge is lost at every switching. Furthermore eq. (4.55) shows that the offset between the main transistors is reduced by the ratio $\frac{g_{mm}}{g_0}$, which means that a small device mismatch increases the possible achievable accuracy. In [VIT89] the basic layout techniques for analog design and principal layout rules are listed.

Dynamic analog techniques combine digital circuits with fast clocks and analog circuits with sensitive inputs. It is important to physically separate these two types of circuits as much as possible and to isolate the sensitive analog nodes. For example the gate of T_m is a sensitive node, which can be isolated by putting S_x into a separate well. Furthermore a guard ring which is connected to the analog ground reduces the parasitic coupling through the substrate.

6.2 CELL LEVEL

Clock jitter can modify the optimum, ideal switching sequence of a cell. A longer clock overlap or, even worse, lack of overlap of the clock phases of S_y and S_z may be the consequence. The optimum switching moment of sampling switch S_x depends on the actual state of S_y and S_z. If S_x is not switched at the right moment, a large current ripple may occur [WEG90.1]. The clock delays between these three switches determine the switching configuration of the cell. Driving one cell by only one external clock reduces the influence of clock jitter and increases the control over the switching instants. An elementary cell becomes larger, because several inverters have to be added. But the number of connection lines at the circuit level is drastically reduced and additional clock delays due to different connecting paths are avoided.

Summarizing the important or sensitive points:

- S_y and S_z must be overlapping for the shortest possible period;
- if a "dummy switch compensation" is used, the complementary phase clock $\overline{S_x}$ must be activated only after that the sampling switch S_x has released all its charges in order not to influence charge sharing;
- furthermore the falling time of S_x must be very short in order to favor the equipartition of the channel charge of the sampling switch;
- only one external clock must drive each cell to reduce the influence of clock jitter.

It is therefore desirable to produce the different clocks for S_x, S_y and S_z locally, at the cell level.

6.2.1 CLOCK PHASE GENERATION WITH SIMPLE INVERTERS

Figure 6.1 shows the circuit which produces the four needed clock phases of an elementary cell and which fulfills the above mentioned conditions. The pulse-shaping stage is only used while the rise and fall times of the cell clock are too slow.

In Fig. 6.2 the waveforms of the clock phases of the circuit in Fig. 6.1 are represented, which are obtained by modulating parameter β of the corresponding inverters. τ stands for the delay of one inverter stage.
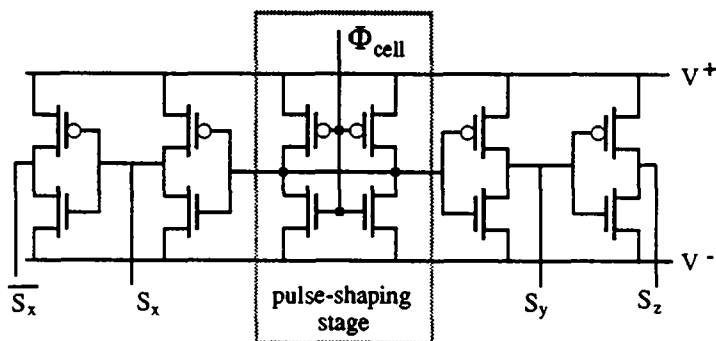

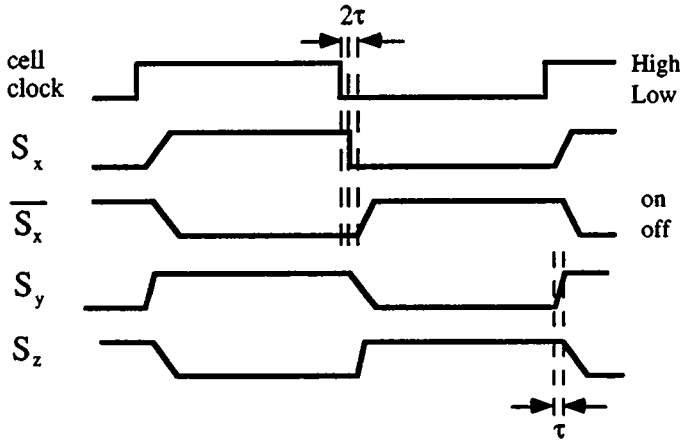**Figure 6.1:**   Inverter stage producing the four clock phases of an basic cell

Figure 6.2: Clock phases produced by the inverter stage of Fig. 6.1, which is driven
by only one external clock

Note that the fall time of the trailing-edge of S_x is short in order to favor
the equipartition of the channel charges. Furthermore the rise time of the
leading-edges of S_y and S_z are smaller than the fall time of the
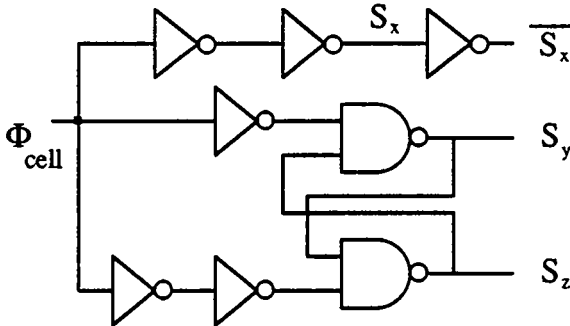corresponding trailing-edges in order to avoid a worst case situation.

Figure 6.3: Circuit generating overlapping clocks for S_y and S_z which is based on
NAND gates

6.2.2 *CLOCK PHASE GENERATION WITH NAND/NOR GATES*

Fig. 6.3 represents another possibility for the clock phase generation for a basic cell based on NAND-gates. This circuit needs no modulation of the transfer parameter β, but it is larger than the one represented in Fig. 6.1. The two NAND gates make sure that the transition from 1 to 0 can only occur after the other output has been set to 1. Again $\overline{S_x}$ is activated after S_x.

6.2.3 *LAYOUT OF THE SWITCHES*

It has been been shown in Appendix D that one possible strategy to control charge injection of S_x is to achieve equipartition of its channel charge. With the help of "dummy switches", the charge released by S_x can then be compensated, hence the term α is reduced. For minimal length MOS switches the overlap capacitances are of the same importance as the gate capacitance. "Symmetrical dummy switches" as represented in Fig. 6.4 lower the effect of asymmetrical overlap capacitances. The charge of the parasitic capacitances labeled by the same capital letter cancel each other out, because they are driven by the complementary clocks ϕ and $\overline{\phi}$. Compensation accuracy is then limited to the mismatch of β and V_T between S_x and its "symmetrical dummy switches" $\overline{S_x}$.
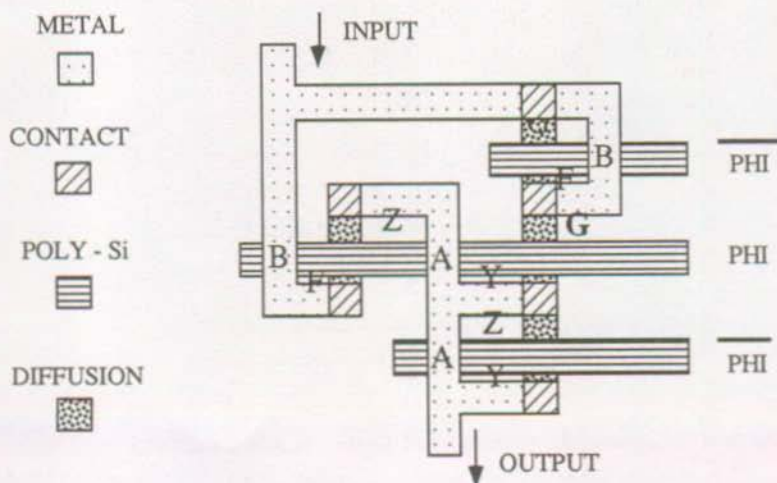

Figure 6.4: Layout of the sampling switch S_x with its symmetrical dummy switches

Note that the layout proposed in Fig. 6.4 compensates the overlap capacitances C_{gd} and C_{gs} but also the important parasitic metal-poly capacitances. For example capacitance "G" consists of the gate-to-diffusion overlap capacitance but also of the parasitic capacitance metal-poly.

Charge injection of the switches S_y and S_z increases the amplitude of the transients. A first order compensation can be obtained by using a switch configuration like the one shown in Fig. 6.5. Again the capacitances labeled with the same capital letters have the same value and are driven by complementary clocks. Furthermore the poly-line has the same length for both switches. If it is not possible to match the poly-lines of S_y and S_z, the shorter poly-line is used for S_y to avoid an additional delay τ with respect to S_z in order to favor simultaneous switching (see Fig. 6.2).

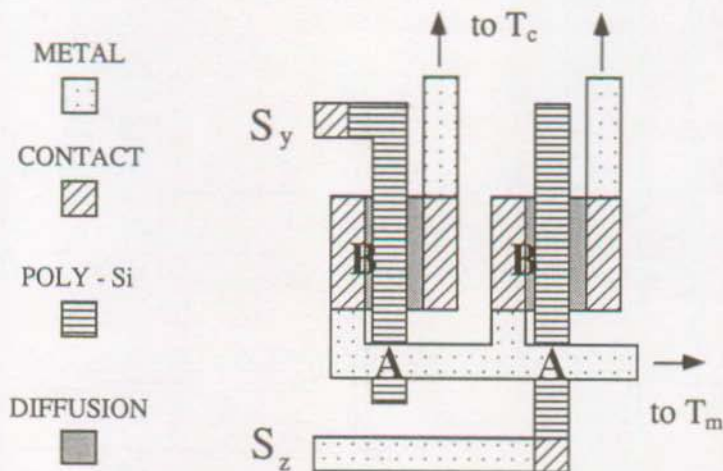For multiple current mirrors the structure proposed in Fig. 6.5 can be extended.

Figure 6.5:   Layout of the switches S_y and S_z which reduces the variations at the drain node of the current copier while switching

6.3 CIRCUIT LEVEL

For multiple current mirrors with several cells, it is important that all cells switch at the same time. The phase clock diagram of Fig. 3.10 shows that one cell after another must be activated, or in other words, each hold capacitor C_j is sequentially updated during a switching cycle.

The easiest way to fulfill this is to drive the cell clocks with the help of a clocked shift register based on dynamic logic considerations as shown in Fig. 6.6.

There are different ways to initialize the looped shift register. One possibility which is easy to implement and which does not add a supplementary delay in the clock path is represented in Fig. 6.6. As long as the reset is active the state of the different outputs is fixed and only one cell is activated. In order to avoid an incorrect initialization of the shift register, the reset command is latched and disabled synchronously with Φ_1.
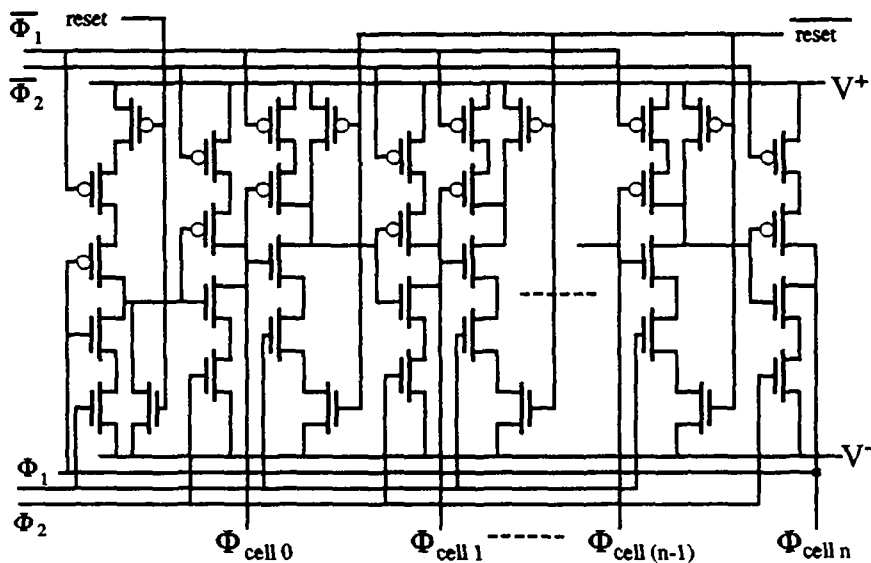

Figure 6.6:   Dynamic, clocked shift register generating the cell clocks

It is important to keep a good matching between the clock paths in order not to introduce delays between the cell clocks. Otherwise two cells may be activated at the same time with the consequences mentioned in the previous chapter.

6.3 SUMMARY

Some design and layout tricks were illustrated which reduce to a first order approximation the amplitude of glitches or transients which occur when switching. A "symmetrical dummy switch" was proposed which reduces the amount of charge injected into the hold capacitor C by the parasitic capacitances, hence reduces the value of the parameter α. The sensitivity to clock jitter is reduced when the different clock phases are generated locally at cell level.

CHAPTER 7

EXPERIMENTAL RESULTS

&

MEASUREMENTS

Experimental and measured results are presented which were obtained with different dynamic current mirror structures and for different current ratios. AC and DC measurements are shown, which illustrate the influence of the previously mentioned parameters or circuit configurations on the current accuracy.

7.1 GENERAL CONSIDERATIONS

The following results were obtained with a measuring system made up of the following elements:

(a) highly accurate, calibrated voltmeters, which offered the possibility of integrating their input to reduce the influence of noise;

(b) calibrated resistances (to several ppms), which were connected in the input and the output current path;

(c) the supply voltage was taken from batteries to reduce the influence of power supply variations;

(d) a PC, which incremented the input current, controled the output voltages, processed the output data of the voltmeters and displayed the results;

(e) an oscilloscope with the possibility of averaging its input, which reduced the magnitude of the observed noise variations. Otherwise the variations of the output current were overwhelmed by the noise variations and the AC photographies did not represent the desired signals.

The measuring system used calibrated resistances to convert accurately the different currents into voltages, which then could be tested by the voltmeters and by the oscilloscope. The accuracy of the measuring system is about 50 ppm at $1\mu A$, decreasing to 200 ppm for 50nA.

Dynamic n-type and p-type, self-biased and externally-biased cascoded current mirrors of different structures and different current ratios were integrated in a 3μ p-well CMOS technology with self-aligned contacts (SACMOS) [LUS85].

The first dynamic current mirror was integrated with all the clock phases externally controllable. The influences of the different clock configurations on the current accuracy and the sensitivity of the circuit on clock delays was verified. Furthermore it was possible to have access to the internal nodes of this circuit, but the price to pay was an important increase of the parasitic capacitances C_{px}. To increase the accuracy, the next circuits had no access to the internal nodes and operated either with one external phase per basic cell or even with only one external phase per mirror.

The influence of the different parameters on the DC accuracy were measured on an n-type mirror of ratio 1:1. These results are expected to remain qualitatively valid also for a p-type mirror or for mirrors of different current ratios.

Because of the limited power supply, the type of current-voltage conversion and because of the desired accuracy of the measuring system, the input current can only vary linearly. Several hundred chips of dynamic current mirrors coming from different wafers were measured and only little spread was observed. With the help of auxiliary switches, the different dynamic current mirror configurations are obtained on the same chip and are built with the same transistors. So the comparison of the different kinds of mirrors is valid.

7.2 AC MEASUREMENTS

7.2.1 *VARIATIONS OF INPUT VOLTAGE $V_{in}(t)$ AND OUTPUT CURRENT $I_{out}(t)$*

7.2.1.1 All Clock Phases Work Correctly

time-axis:
$\Delta t = 200\,\mu s$ / div;

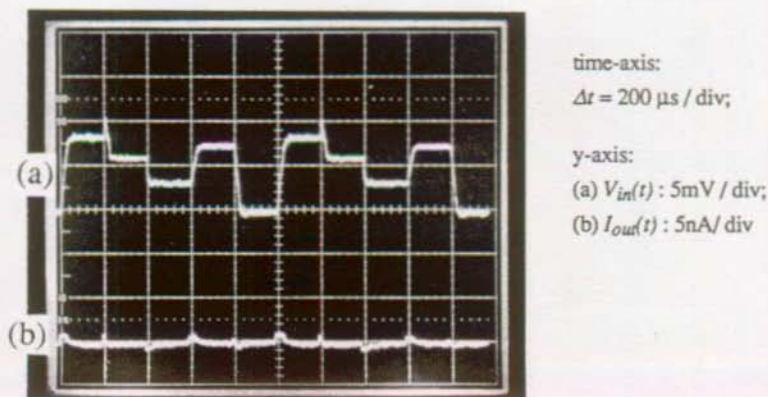y-axis:
(a) $V_{in}(t)$: 5mV / div;
(b) $I_{out}(t)$: 5nA/ div

Figure 7.1:   Photograph of waveforms of $V_{in}(t)$ and $I_{out}(t)$ for an n-type mirror of ratio 1:4 while I_{in}=1μA. All clocks work correctly.

In Figure 7.1 the measured variations of the input voltage $V_{in}(t)$ and of the output current $I_{out}(t)$ of a self-biased n-type current mirror of ratio 1:4, while all clock phases work correctly, are shown.

Due to the mismatch of the five mirror transistors T_{mj}, the input voltage $V_{in}(t)$ (Fig. 7.1a) varies stepwise. In Fig. 7.1b the variations of the output current $I_{out}(t)$ are much smaller than 1250 ppm, corresponding to one division.

7.2.1.2 One Phase is Artificially Delayed

In Figures 7.2 & 7.3 the clock of one basic cell is artificially delayed to show the influence of the different switching configurations. In Fig. 7.2 the same mirror of ratio 1:4 is represented as in Fig. 7.1. The photograph of Fig. 7.3 shows the waveform of a mirror of ratio 1:1, where a phase was delayed and the control voltage V_{gx} of the sampling switch was reduced.

A large glitch can be observed in Figs. 7.2 b & 7.3b, which is due to the all-switches-open configuration (worst case). Even more in Fig. 7.2b the value of the memorized current is altered, because the sampling instant is not synchronized with switching instant of the toggle switch.
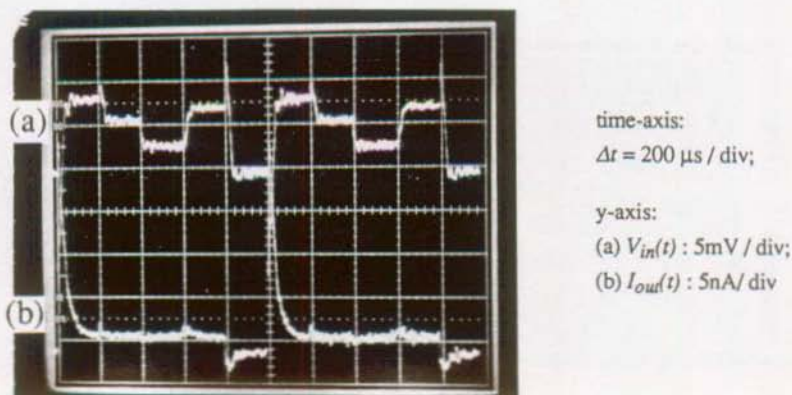

time-axis:
$\Delta t = 200\ \mu s$ / div;

y-axis:
(a) $V_{in}(t)$: 5mV / div;
(b) $I_{out}(t)$: 5nA/ div

Figure 7.2:   Photograph of $V_{in}(t)$ (a) and of $I_{out}(t)$ (b) for a self-biased n-type mirror of ratio 1:4 while I_{in} =1μA. One phase is delayed.

time-axis:
$\Delta t = 200\ \mu s$ / div;

y-axis:
(a) $V_{in}(t)$: 10mV / div;
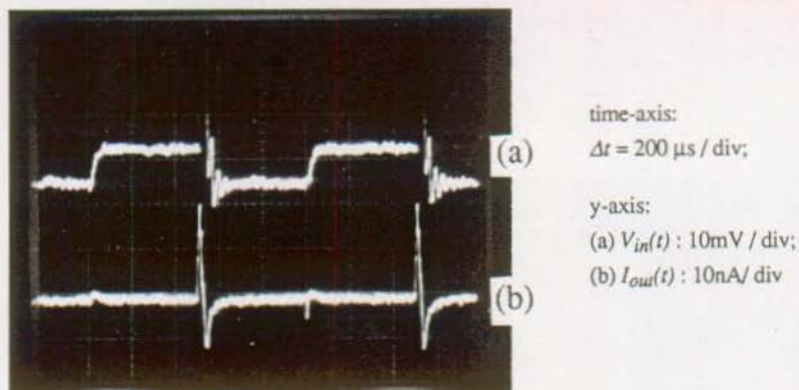(b) $I_{out}(t)$: 10nA/ div

Figure 7.3: Photograph of $V_{in}(t)$ (a) and $I_{out}(t)$ (b) for an externally-biased, n-type current mirror of ratio 1:1. **One phase is delayed.**

A low sampling switch conductance g_x reduces the sensitivity to the sampling instant as shown in Fig. 7.3b, because the stored voltage V on C_j can only change slowly.

On the other hand, due to the small value of g_x an overshoot or oscillation of $V_{in}(t)$ and a large glitch occur (Fig. 7.3a). When all phases work correctly, $V_{in}(t)$ varies stepwise, $I_{out}(t)$ is constant flat and no important glitches occur.

The time constant observed in Fig. 7.2b is due to the high value of the resistive load, which is needed to accurately convert $I_{out}(t)$ into a measurable voltage and does not correspond to the main output time constant τ_{mo}, mentioned in § 5.2.3. This can be verified by estimating the value of the parasitic capacitances of the probe, and by observing the current independence of the time constant of Fig. 7.2b.

7.2.1.3 Basic Cell with a Reduced Transconductance $g_{mm\Delta}$

Figs. 7.4 shows $V_{in}(t)$ and $I_{out}(t)$ for a self-biased n-type current mirror of ratio 1:1, which has a modified basic cell with a reduced transconductance $g_{mm\Delta}$.

All the clock phases work correctly, and the ratio of the bypassing current I_0 towards the input current I_{in} is equal to 0.85. According to the reflections

of §2.3.5 the voltage variations $V_{in}(t)$ are increased due to the reduced transconductance parameter. Nevertheless the current variations $I_{out}(t)$ are much smaller then one division, which corresponds to 1250 ppm.

time-axis:
$\Delta t = 100 \ \mu s$ / div;

y-axis:
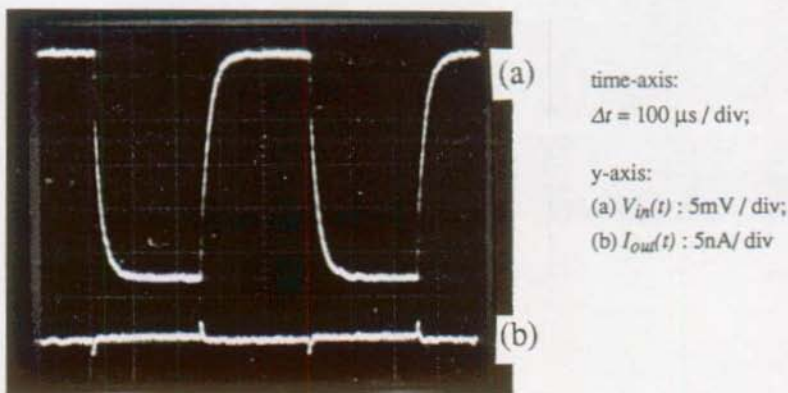(a) $V_{in}(t)$: 5mV / div;
(b) $I_{out}(t)$: 5nA/ div

Figure 7.4:   Photograph of the waveforms of $V_{in}(t)$ (a) and of $I_{out}(t)$ (b) for a "stacked" n-type mirror of ratio 1:1 and for $I_{in} = 1\mu A$. The basic cell of the mirror operates with a reduced transconductance $g_{mm\Delta}$ and $\frac{I_Q}{I_{in}} = 0.85$

time-axis:
$\Delta t = 100 \ \mu s$ / div;

y-axis:
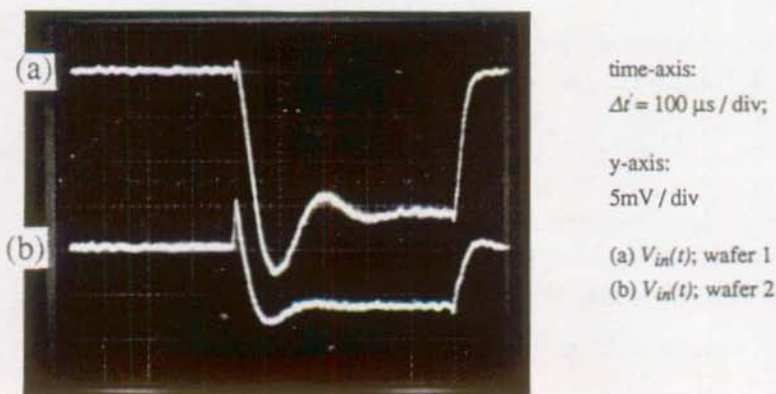5mV / div

(a) $V_{in}(t)$; wafer 1
(b) $V_{in}(t)$; wafer 2

Figure 7.5:   Photograph of the waveforms of $V_{in}(t)$ of two n-type mirrors of ratio 1:1 from different wafers, for $I_{in} = 1\mu A$. The overshoot is due to the low conductance g_x of the sampling switch S_x

7.2.1.4 Mismatch between Two Mirrors

Figure 7.5 represents $V_{in}(t)$ of two mirrors of ratio 1:1, which were taken from different wafers. An overshoot of the input voltage occurs which is due to the control circuit which reduces the sampling switch conductance g_x.

7.2.2 MAIN TIME CONSTANT τ_{m0} OF THE OUTPUT CELL

The photograph of Fig. 7.6 explicitly shows $\tau_{mo} = \frac{C_{po}}{g_{mc}}$ by representing the waveform of the internal output node V_{dm1} for two different current values. The internal node capacitance C_{po} is artificially increased by that of the probe and the clocks are delayed to provide a better representation. The currents are $I_{in} = 0.2$ μA (Fig. 7.6a) and $I_{in} = 0.8$ μA (Fig. 7.6b). As the common-gate transistor T_{cj} works in weak inversion, g_{mc} is proportional to I_{in}, thus to $\frac{1}{\tau_{mo}}$. It has to be pointed out that the glitches in Fig. 7.6 are of the same polarity, hence they do not cancel each other out and the DC current error depends on the switching frequency as will be seen in the next section.
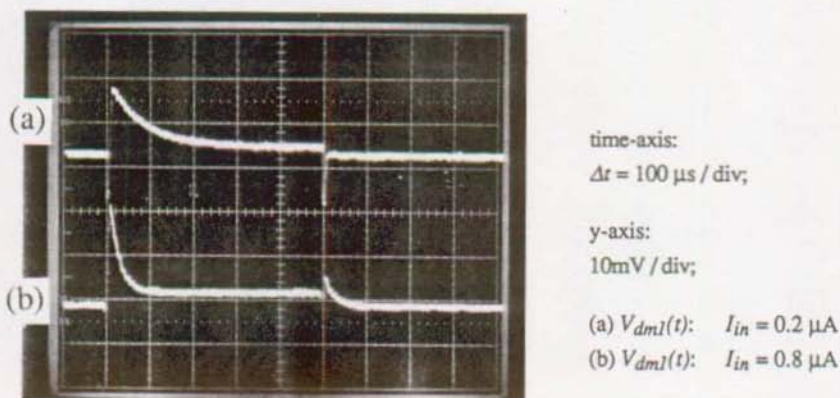

time-axis:
$\Delta t = 100$ μs / div;

y-axis:
10mV / div;

(a) $V_{dm1}(t)$: $I_{in} = 0.2$ μA
(b) $V_{dm1}(t)$: $I_{in} = 0.8$ μA

Figure 7.6:   Waveform at node V_{dm1} which shows the main time constant $\tau_{mo} = \frac{C_{po}}{g_{mc}}$ of the output cell for two different current values:

(a) $I_{in} = 0.2$ μA,   (b) $I_{in} = 0.8$ μA

7.3 DC MEASUREMENTS

The following measurements were obtained by making an average on four
measurements, which reduces the influence of the noise.

7.3.1 MULTIPLYING MIRROR OF RATIO 1:1, 1:2 AND 1:4

Figure 7.7 represents the measured accuracy of a dynamic current mirror
of ratio $I_{in} : I_{out1} : I_{out2} : I_{out4} = 1{:}1{:}2{:}4$ as a function of the input current I_{in}.
The switching frequency f_{sw} is kept to 1kHz for the three different current
ratios and the output is connected to an output voltage $V_{out} = 3V$. The output
currents are normalized to x times the input current I_{in}, where x
corresponds to the specific current ratio. The clock phases are produced
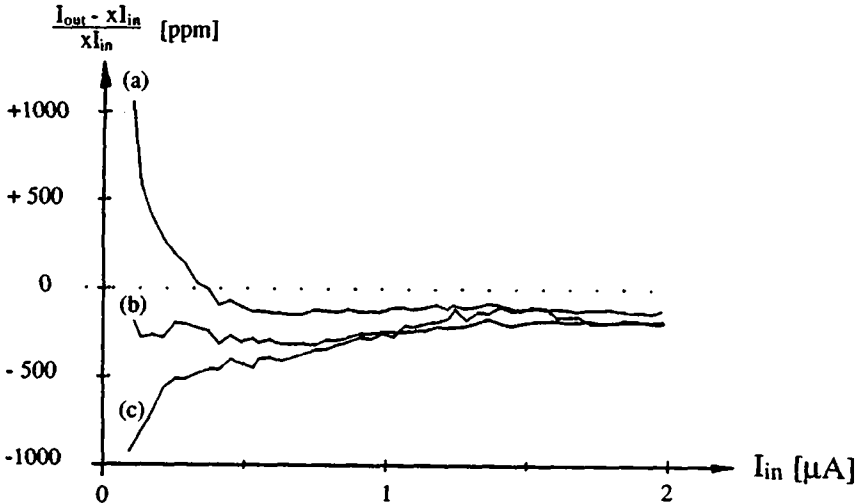locally.

Figure 7.7:   Measured error $\varepsilon = \dfrac{I_{out} - xI_{in}}{xI_{in}}$ [ppm] for a self-biased n-type mirror

switching at frequency $f_{sw} = 1\text{kHz}$ as a function of I_{in}.

(a) $\dfrac{I_{out}}{I_{in}} = 1{:}1$, x=1   (b) $\dfrac{I_{out}}{I_{in}} = 1{:}2$, x=2   (c) $\dfrac{I_{out}}{I_{in}} = 1{:}4$, x=4
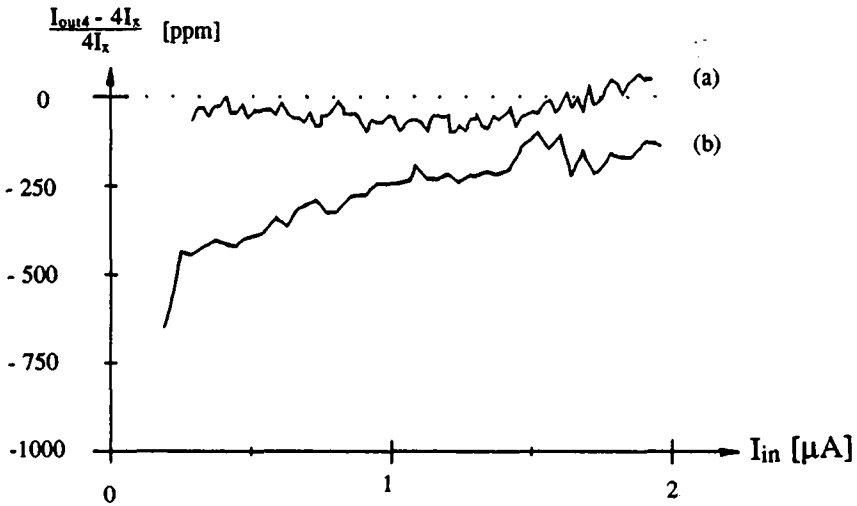
Figure 7.8:   Measured error $\varepsilon = \frac{I_{out4}-4I_x}{4I_x}$ [ppm] for a "stacked" n-type mirror of ratio

$I_{in}:I_{out1}:I_{out4}$ = 1:1:4 as a function of I_{in} for V_{out} = 3V and f_{sw} = 1kHz.

Curve (a) $I_x=I_{out1}$;   Curve (b) $I_x=I_{in}$

The circuit operates with only one external phase per cell and is designed for a nominal input current I_{in} of 0.75 μA.

At low currents the accuracy is limited by the mismatch of the leakage currents of the reverse biased junctions (see §4.2), whereas at higher currents this effect becomes negligible. Therefore the measured results show a large spread at low currents. Furthermore the accuracy increases as the V_T mismatch and the charge injection is drowned in the higher gate voltage overhead.

Figure 7.8 represents the measured error of a "stacked" n-type current mirror with two outputs of ratio $I_{in} : I_{out1} : I_{out4}$ = 1:1:4, which is obtained by repeating six elementary cells. During the measurement, V_{out} is equal to 3V and f_{sw} to 1kHz. Curve (a) compares the two output currents I_{out1} and I_{out4} to each other, hence $I_x = I_{out1}$, whereas curve (b) shows the current

error while $I_x = I_{in}$. The accuracy is better when two output currents are compared to each other (curve a) than if an output current is compared to an input current, because first-order errors cancel each other out.

Figure 7.9 represents the measured error of an n-type current mirror of ratio $I_{in}:I_{out2}:I_{out4}$=1:2:4 with two outputs. Curves (a,b) stand for wafer 1 and curves (c,d) for wafer 2. I_{out} is equal to $2I_{in}$ for the curves (a,c) and to $4I_{in}$ for the curves (b,d), while V_{out} is equal to 3V and f_{sw} is 1kHz. For low currents the accuracy depends on the uncontrollable mismatch of the leakage currents, whereas for large currents the accuracy is better than 500ppm.
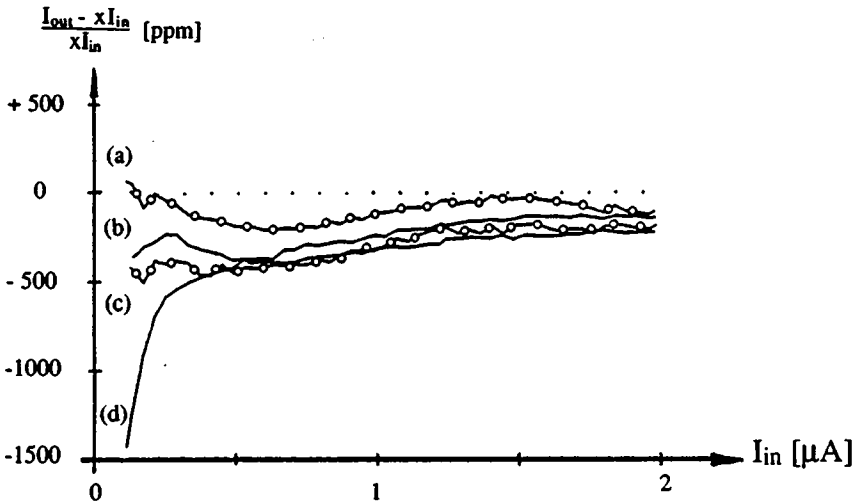

Figure 7.9:   Measured error $\varepsilon = \frac{I_{out}\text{-}xI_{in}}{xI_{in}}$ [ppm] for "stacked" n-type mirrors of ratio

$I_{in}:I_{out2}:I_{out4}$ = 1:2:4 as a function of I_{in} (V_{out} = 3V, f_{sw} = 1kHz)

(a,b) wafer 1;   (c,d) wafer 2;   (a,c) ratio 1:2;   (b,d) ratio 1:4

7.3.2 BASIC CELL WITH A REDUCED TRANSCONDUCTANCE $g_{mm\Delta}$

In Figure 7.10 the error $\varepsilon = \frac{I_{out}\text{-}I_{in}}{I_{in}}$ of a mirror operating with a normal basic cell (Figs. 7.10c,d) is compared to that of a mirror operating with an improved basic cell with a reduced transconductance $g_{mm\Delta}$ (Fig. 7.10a,b) as has been shown in § 2.5.3.

The ratio of the input current to the output current $\frac{I_{out}}{I_{in}} = 1$ and the ratio of the bypassing current versus the input current $\frac{I_0}{I_{in}}$ is equal to 0.85. The output voltage is constant during the measurement: $V_{out} = 3V$ for the curves of Figs. 7.10a,c and $V_{out} = 2V$ for Figs. 7.10b,d. It is visible that the output conductance is not affected by using either the normal basic cell or the improved one. The improvement in accuracy is about a factor of six, corresponding to the ratio of the stored current in the improved structure and the normal configuration, respectively, in accordance with the theory.
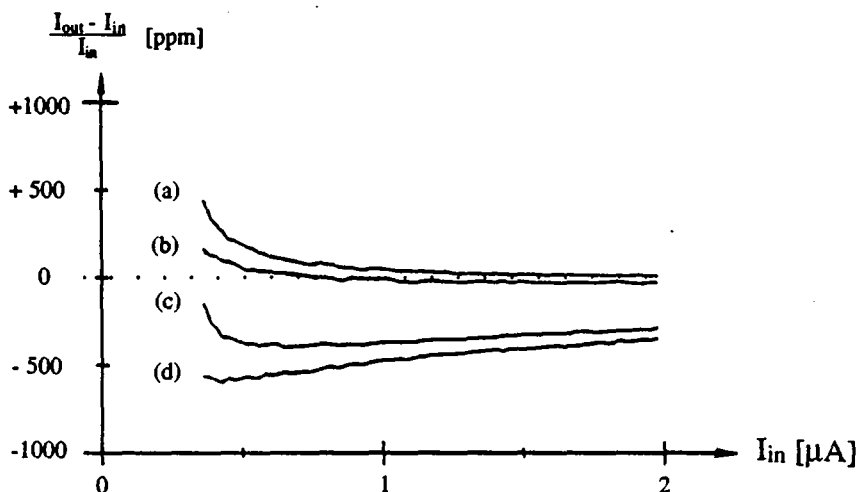

Figure 7.10:   Measured error $\varepsilon = \frac{I_{out}\text{-}I_{in}}{I_{in}}$ [ppm] for n-type mirror of ratio 1:1 as a function of I_{in} for $V_{out} = 3V$ (a,c) and $V_{out} = 2V$ (b,d).

(a,b) basic cell operating with a reduced transconductance $g_{mm\Delta}$ ($\frac{I_0}{I_{in}} = 0.85$); (c,d) normal basic cell

7.3.3 MULTIPLE CURRENT MIRROR WITH EIGHT OUTPUTS

The measured output currents of a multiple current mirror with eight outputs which are all in a unity ratio, hence $I_{in} : I_{out1} : ... : I_{out8} = 1: 1:...:1$, is shown in Fig. 7.11.

This particular mirror was designed to achieve an accuracy better than 500ppm at 1μA, while the outputs are compared to each other. With the help of auxiliary switches this current mirror can also operate like a static current mirror. The observed dispersion of the output currents is of $\sigma \approx$ 7000ppm for a static mirror, whereas for the dynamic current mirror σ is equal to 250ppm. This multiple dynamic current mirror is used for the continuous time filter application proposed in § 8.1.
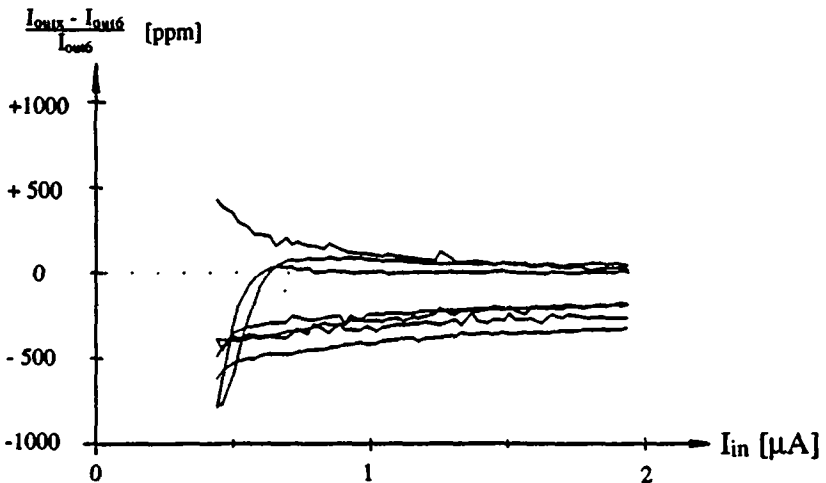

Figure 7.11:   Measured error $\varepsilon = \frac{I_{out6} - I_{outx}}{I_{out6}}$ [ppm] for an externally biased n-type

mirror of ratio $I_{in}:I_{out1}:I_{out2}:..I_{out7}:I_{out8} = 1:1:1...:1:1$ as a function of I_{in}

with $V_{out} = 2V$ and $f_{sw} = 1kHz$

7.3.4 P-TYPE MIRROR WITH ONE EXTERNAL CLOCK

Figure 7.12 represents the measured accuracy of a self-biased p-type current mirror which works with only one external clock and which is designed for a nominal current I_{in} of 1μA.

Due to layout problems the phase delay is not optimized, thus a small variation of the DC accuracy, which is reproducible with all these circuits, can be seen.

During the measurements V_{out} (referred to a supply of 0V and +5V) is once equal to 3V(curves a,b) and once to 2V(curve c). The switching frequency f_{sw} is 600Hz to reduce the DC effect of the glitches. Graph (b,c) show the accuracy for the same p-type mirror, whereas graph (a) shows it for a p-type mirror from another wafer. Again for larger currents the accuracy is increased.
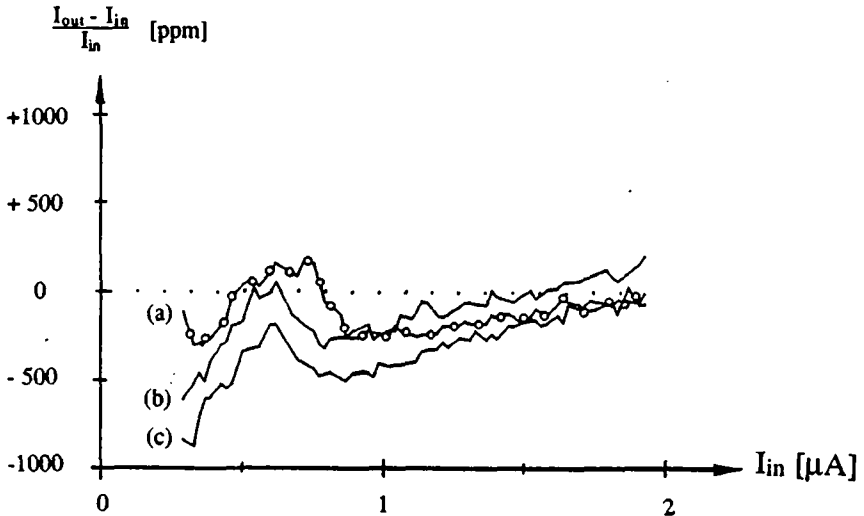

Figure 7.12: Measured error $\varepsilon = \frac{I_{out} - I_{in}}{I_{in}}$ [ppm] for a self-biased p-type mirror of ratio 1:1 as a function of I_{in} and $f_{sw} = 600$Hz.

   (a) $V_{out} = 2$V, wafer 1   (b) $V_{out} = 2$V, wafer 2
   (c) $V_{out} = 3$V, wafer 2

7.3.5 INFLUENCE OF THE CLOCK FREQUENCY

Figure 7.13 shows the increase of the current error ε for higher frequencies, whereas Fig. 7.14 zooms in around the origin.

In Figure 7.13 the linear decrease of the accuracy as a function of the switching frequency f_{sw} is shown. The measured DC current is the average current over a fixed time period of all the DC and AC components. When f_{sw} is increased the number of glitches which occur during this period are also increased. If the common-gate transistor T_{c1} and the diode-connected transistor T_{c0} operate in weak inversion, the absolute current error due to transients is constant for a given clock configuration as shows eq. (5.12). Therefore the relative error varies proportionally to the current value as is shown in Fig. 7.13 for three different current values. The slope of these curves and even their sign depend on the clock configurations and on the mismatch between the diode-connected transistor T_{c0} and the common-gate transistor T_{c1} as was presented in §5.2.3. As long as T_{c0} and T_{c1} operate in weak inversion, $V_{dm1} - V_{dm0}$ remains constant and the current error $\Delta I(t)$ is independent of I_{in}.
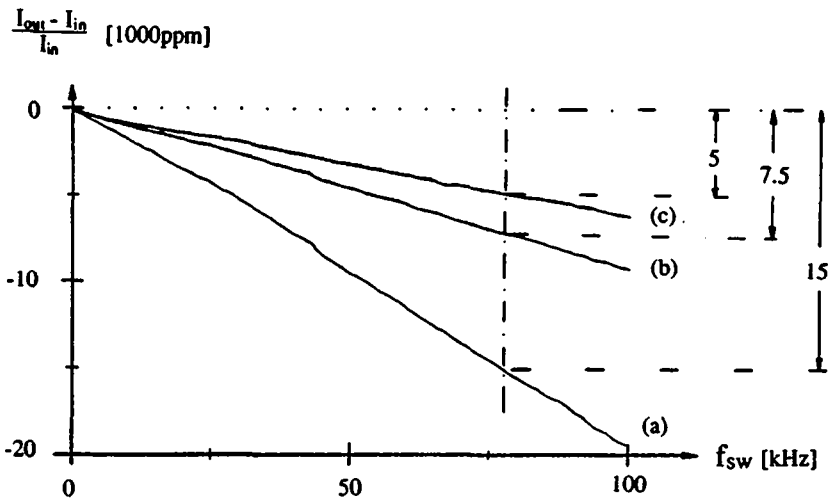

Figure 7.13:   Measured error $\varepsilon = \dfrac{I_{out}-I_{in}}{I_{in}}$ [1000ppm] for a self-biased n-type mirror of a

ratio 1:1 as a function of f_{sw} for three different input currents I_{in}

(a) $I_{in} = .25\mu A$ (b) $I_{in} = .5\mu A$ (c) $I_{in} = .75\mu A$.

In Figure 7.13 it is not visible that for low values of f_{sw} the performances of the mirror decrease.

Figure 7.14 shows the increase of the current error for very low switching frequencies for two chips taken from wafer 1 (curves a,b) and wafer 2 (curves c,d). The error increase at low frequencies is due to the discharge of the storage capacitor C_j by the leakage currents of the sampling switch junctions a shows eq. (4.20). Note that the current error due to the leakage currents superposes to the current error due to the glitches.

If typical numerical values for the example shown in Fig. 7.14' are introduced, the switching frequency f_{sw} needed to obtain an accuracy of 50ppm is found to be about 600Hz.

Furthermore Fig. 7.14 shows that the output current can increase or decrease as a function of f_{sw}, that the slope may be larger or smaller than zero, depending on the sign of the voltage difference $V_{dm1}-V_{dm0}$.
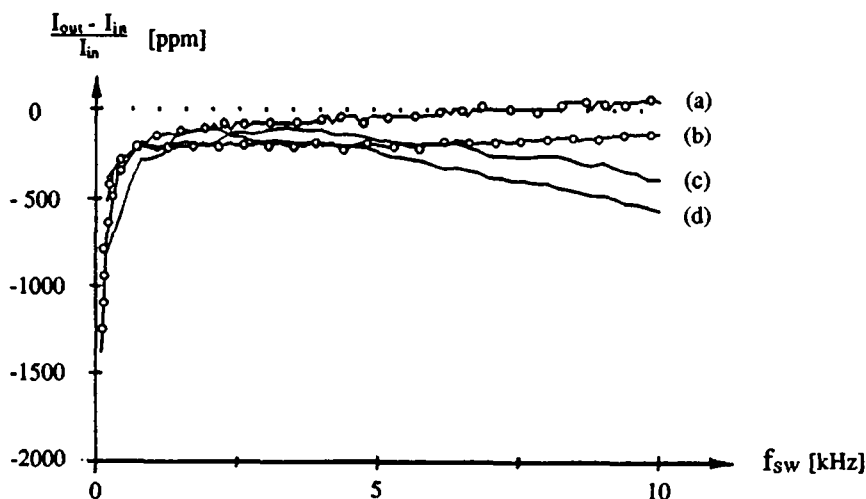

Figure 7.14: Measured error $\varepsilon = \dfrac{I_{out}-I_{in}}{I_{in}}$ [ppm] due to leakage currents and glitches for two self-biased n-type mirrors of ratio 1:1 as a function of f_{sw}.

wafer 1:	(a) $I_{in} = .25\mu A$	(b) $I_{in} = .5\mu A$
wafer 2	(c) $I_{in} = .25\mu A$	(d) $I_{in} = .5\mu A$

7.3.6 INFLUENCE OF THE SAMPLING SWITCH GATE-ON VOLTAGE V_{gx}

In Figs. 7.15&7.16 the influence of the sampling switch turn-on voltage V_{gx} on the accuracy for three different input currents is shown. In Figure 7.15 all cell clocks work correctly whereas in Fig. 7.16 the clock of one cell is delayed. Curves (b)&(c) of Fig. 7.15 show that the cancellation of charge injection by symmetrical dummy switches is quite accurate. For a given turn-on voltage the larger the currents are, the lower the channel charge of S_x is. Furthermore, the relative importance of a gate voltage error is smaller. For small currents (curve a) the assumption that the channel charge of S_x is evenly shared among source and drain is not valid.

Another consequence of the sampling switch gate control circuit is the reduced sensitivity to clock delays as shows Fig. 7.16. While g_x is small the stored voltage V_j on C_j can not change instantaneously with the drain voltage V_{dmj} and the current variations through T_{mj} remain small.
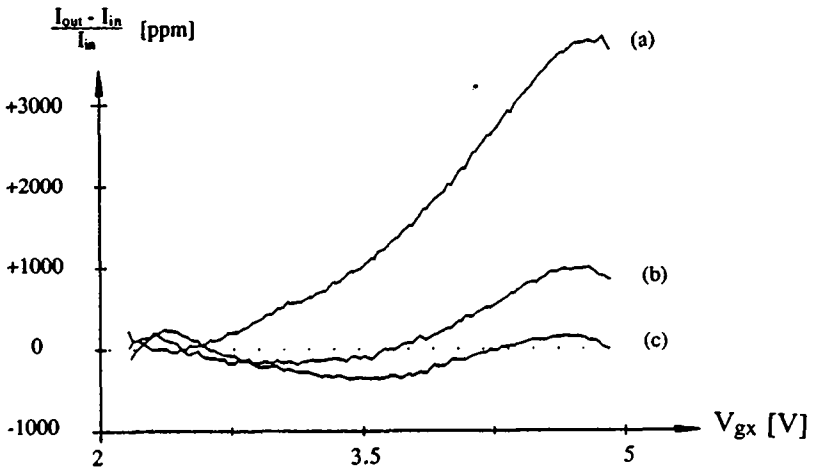

Figure 7.15: Measured error $\varepsilon = \frac{I_{out} - I_{in}}{I_{in}}$ [ppm] as a function of sampling switch turn-on voltage V_{gx} for a self-biased n-type mirror of ratio 1:1.

(a) $I_{in} = .25\mu A$ (b) $I_{in} = .5\mu A$ (c) $I_{in} = .75\mu A$

If the circuit is in "clock overlapping" configuration (§5.1) and the sampling switch S_x is closed too fast (before S_z is open), a current directly flows from the output through the diode-connected mirror transistor T_{mj}. As a consequence a large current glitch occurs at the output and the DC accuracy is spoilt. If V_{gx} is increased even more, the charge error on C_j due to the incorrect sampling may become even larger than the total channel charge of S_x. The additional charge is provided by the output during the "clock overlapping" configuration, and cannot simply be an overcompensation of the charge injection. Finally the accuracy of the mirror may decrease to that of a static one.

The reduction of the turn-on voltage V_{gx} favors the equipartition of the channel charge (§ 4.4), because the switching parameter B decreases.
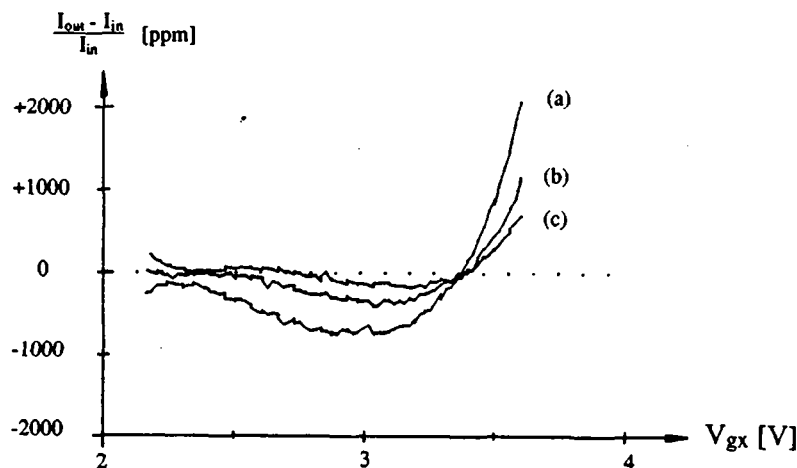

Figure 7.16: Measured error $\varepsilon = \dfrac{I_{out} \cdot I_{in}}{I_{in}}$ [ppm] as a function of V_{gx} for an n-type

mirror of ratio 1:1, while one cell clock is delayed.

(a) $I_{in} = .25\mu A$ (b) $I_{in} = .5\mu A$ (c) $I_{in} = .75\mu A$

7.4 NOISE MEASUREMENTS

The noise of a dynamic current mirror was measured with the help of a
FFT spectrum analyzer. The output current noise was first converted into a
voltage using a load resistance R_{load} of 3.3MΩ. This voltage noise was then
amplified by 40dB with a low noise bandpass amplifier which had an input
resistance of 100MΩ. The transconductance g_{mm} for a quiescent current I_{in}
equal to 1 μA was 3.2 $\frac{\mu A}{V}$. The total gain introduced in the noise path was of

60dB, where 20dB were due to the product of transconductance and load,
hence $g_{mm}R_{load}$. The value of the storing capacitor C was about 5.5pF and
the parasitic capacitance C_{pi} was estimated to be about 0.3pF.

The double sided voltage white noise spectral power density $S_{VTw}(f)$ at the
gate node of T_m before sampling was equal to (theoretically) 55 $\frac{nV}{\sqrt{Hz}}$, which

corresponds to -145 $\frac{dBV}{\sqrt{Hz}}$. The double sided voltage noise spectral power

density $S_{VTw}(f)$ in the baseband after sampling and bandpass amplification
was found to be (theoretically) - 63 $\frac{dBV}{\sqrt{Hz}}$ and - 69 $\frac{dBV}{\sqrt{Hz}}$ for f_s equal to 2kHz

and 8kHz, respectively. On the other hand, the white noise voltage density
of R_{load} is about 33dB smaller than $S_{VTw}(f)$ at f_s = 2kHz, hence it was
negligible.

If the aliasing effect of the white noise dominates, an increase of the
sampling frequency f_s by four reduces the voltage noise spectral power
density in the baseband by 6dB.

In Figure 7.17 the measured voltage noise spectral power density in the
frequency band 0-50Hz (baseband) is represented in $\frac{dBV}{\sqrt{Hz}}$, while f_s is equal to

2kHz (7.17a) and 8kHz (7.17b). Note that the photograph represents the
single sided voltage noise spectral power density, which must be reduced by
3dB if it is compared to the double sided spectral power density $S_{VT}(f)$.

The measured decrease of the baseband noise is of about 6dB while the
sampling frequency is increased by a factor of four in accordance with the
theory. The value of the measured noise at the marker is about - 66 $\frac{dBV}{\sqrt{Hz}}$ for

f_s = 8kHz, hence it accords with the above predicted values. At f_s = 2kHz
the foldover terms of the white noise spectral power density $S_{VTwfold}(f)$
made out the 94% of $S_V(f)$. The spike visible was due to the 50Hz of the

supply network and even with the help of a grounded box it was not possible to cancel it out completely.

frequency
x-axis: 5 Hz / div

y-axis: 2dB / div

(a) $f_s = 2kHz$
(b) $f_s = 8kHz$

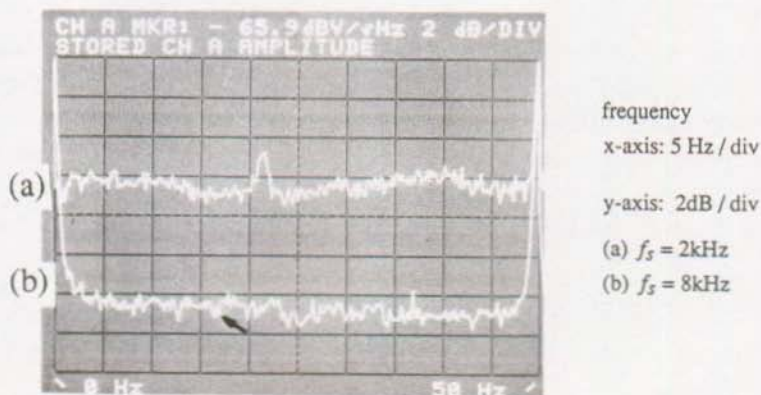**Figure 7.17:** Photograph of the measured noise spectral density in the baseband (0 -50 Hz) in $\frac{dBV}{\sqrt{Hz}}$ for two sampling frequencies f_s in 1:4 ratio
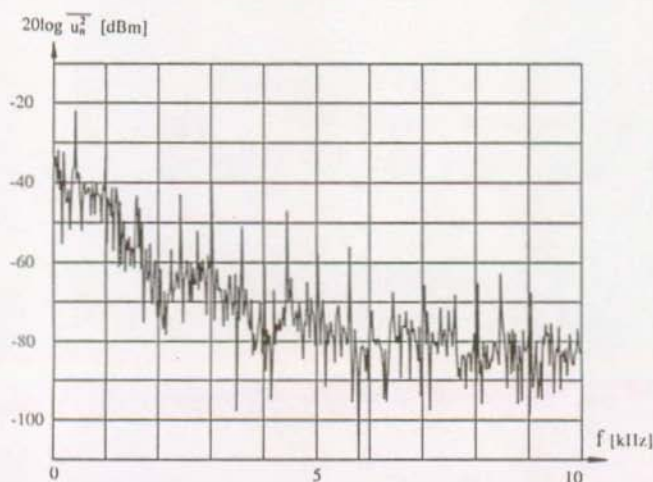

Figure 7.18: Measured noise spectral power density in [dBm] while $f_s = 2kHz$

Figure 7.18 shows the spectral noise density up to 10kHz for $f_{sw} = 1$kHz and measured in [dBm]. Note that the bandwidth used for the measurements represented in Fig. 7.18 is 10Hz and therefore to obtain the $\frac{dBV}{\sqrt{Hz}}$ characteristic 7.8 dB must be subtracted from to the measurements (10 dB for the bandwidth and -2.2 dB for the conversion [dBm] to [dBV]).

The large spikes are due to the glitches which occur at any switching, whereas the 50 Hz component already mentioned introduces the other smaller spikes. The zeros of the sinc-function at the sampling frequency f_s are not visible because of the spikes occurring at the switching frequency f_{sw}. Nevertheless a sinc-shape can be guessed from Fig. 7.18. The thermal noise spectral power density $S_{VT}(f)$ at the output of the bandpass filter for $f > f_s$ is found to be about -85 $\frac{dBV}{\sqrt{Hz}}$, whereas the noise spectral power density of R_{load} is -93 $\frac{dBV}{\sqrt{Hz}}$.

7.5 DIE PHOTOGRAPH

Figure 7.19 shows a die photograph of a dynamic current mirror with two outputs, which is built with three basic cells, hence a mirror with a ratio 1:1:1. Because of additional switches this dynamic current mirror can operate either with a normal basic cell or with an improved basic cell.
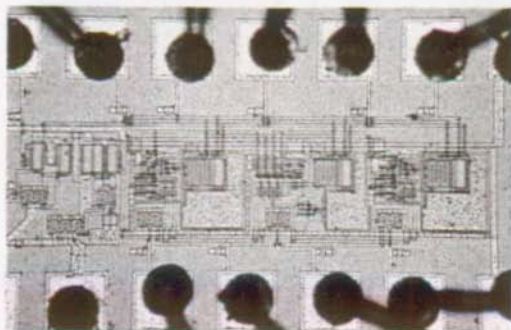
Figure 7.19:   Die photograph of a dynamic current mirror of ratio 1:1:1

The storage capacitors C_j are equal to 3pF and, since the mirror DC accuracy is not depended on mismatch, they can have different shapes.

7.6 SUMMARY

Several kind of dynamic current mirrors were integrated in a 3μ CMOS technology. The DC and AC performances of multiple and multiplying, self-biased and externally-biased dynamic current mirrors were presented. The obtained results were discussed and related to the theory from the preceding chapters. The influences of clock delays, leakage currents and of the sampling switch turn-on voltage on the accuracy were extensively illustrated and the limitations shown. Finally some noise measurements were shown. The predicted theoretical values of the undersampled noise in the baseband were close to the measured ones.

CHAPTER 8

APPLICATIONS

From the analysis provided in the previous chapters it is possible to realize a highly accurate building block, a dynamic current mirror. However, two problems that still remain and which must be addressed, are:

(i) for continuous-time applications the spikes may introduce a harmonic distortion which can result in the modulation of the signal;

(ii) for time variable applications the main time constant is a function of the magnitude of the stored current.

The prime application being investigated in this chapter is a continuous-time filter. It requires accurate current sources, which must be available continuously, to match the center frequencies of each filter cell. Other application are also referenced within the framework like A/D & D/A converters and switched current filters.

8.1 CONTINUOUS TIME FILTERS

8.1.1 GENERAL CONSIDERATIONS

Fully-integrated, monolithic continuous-time filters perform a variety of signal processing tasks in both the audio and video domain. A possible approach is to implement these filters while making use of capacitors and MOS transconductance elements only [KHO84], [NED86], [KRU88]. These elements are subsequently which are realized with the help of operational transconductance amplifiers *(OTAs)*.

The center frequency of a bandpass filter cell is determined with the ratio of a transconductance g_m towards a capacitor C. If, in a high order filter, a center frequency mismatch between the individual filter cells exists, the passband response (gain, passband width and passband ripple) is degraded, as will be shown in this section. This degradation can be avoided if the matching between the center frequencies of the individual cells is increased, hence the matching between C and g_m. If the corresponding MOS transconductances operate in weak inversion, an increase in current matching corresponds to an increase in transconductance matching. The spread of the center frequencies is then limited to the spread of the capacitors.

For these reasons a 4th order bandpass filter is realized which uses dynamic current mirrors to match the transconductances of each cell. To verify the influence of the transconductance matching on the center frequencies the bias currents of the *OTAs* which operate in weak inversion are delivered by either a static current mirror or a dynamic current mirror.

8.1.2 A 4TH ORDER LC COUPLED BANDPASS FILTER WITH CENTER FREQUENCY MISMATCH

At least two resonant LC cells must be involved, if the associated center frequencies are to be compared and therefore the minimum filter order becomes four. The influence of the mismatch between the two individual resonant cells on the passband response of the whole filter is analyzed using a coupled network method. In the case where the center frequency mismatch is zero the analysis of the two individual resonant cells is already presented in [DES82].
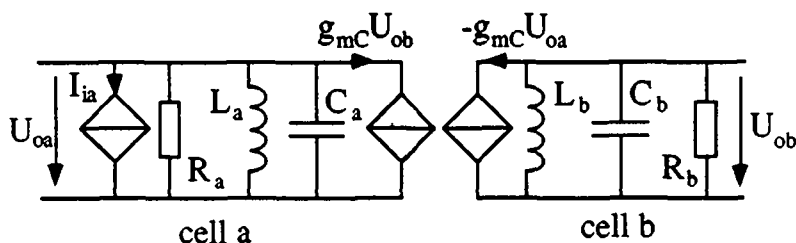
Figure 8.1:   Small signal representation of the 4th order coupled LC bandpass filter

In Fig. 8.1 a coupled 4th order LC bandpass filter is represented which is based on two coupled LC cells. Note that the input is the current source I_{ia} and that U_{oa} is the output voltage of cell a.

The notation used for the analysis is the following (with $k = a, b$):

input current:
$$I_{ia} = g_{mia}U_{ia} \tag{8.1}$$

center frequency
$$f_k = \frac{\omega_k}{2\pi} = \frac{1}{2\pi\sqrt{L_k C_k}} \tag{8.2}$$

quality factor:
$$Q_k = \frac{R_k}{L_k\,\omega_k} = R_k C_k\,\omega_k \tag{8.3}$$

detuning factor:
$$x_k = \frac{\omega}{\omega_k} - \frac{\omega_k}{\omega} \tag{8.4}$$

admittance:
$$Y_k = j\omega C_k + \frac{1}{R_k} + \frac{1}{j\omega L_k} = \frac{1}{R_k}\left\{1 + jQ_k x_k\right\} \tag{8.5}$$

center frequency difference:

$$\Delta f = f_a - f_b \tag{8.6}$$

The filter transfer function is found to be:

$$\frac{U_{ob}}{U_{ia}} = \frac{g_{mC}\, g_{mia}\, R_a R_b}{1 + g_{mC}^2 R_a R_b + j\{Q_a x_a + Q_b x_b\} - Q_a Q_b x_a x_b} \tag{8.7}$$

While the following approximation is valid

$$Q = \sqrt{R_a \omega_a C_a\, R_b \omega_b C_b} \approx Q_a \approx Q_b \tag{8.8}$$

the amplitude at the resonance ($x_a \approx x_b \approx 0$) can be expressed as

$$\frac{U_{ob}}{U_{ia}} \approx \frac{g_{mC}\, g_{mia}\, R_a R_b}{1 + g_{mC}^2\, R_a R_b} \tag{8.9}$$

The goal is to find the analytical expressions for the extremes of the transfer function given by eq. (8.7), hence for the passband response, as a function of x_a and x_b The differentiation of eq. (8.7) leads to a 3rd order equation where the solutions for $Q > \frac{1}{2}$ are found to be:

$$\omega_0 = \frac{\omega_a + \omega_b}{2} \tag{8.10}$$

$$\omega_{1,2} = \omega_0 \pm \frac{1}{2}\sqrt{\Delta\omega^2 + \frac{g_{mC}^2}{C_a C_b}} \tag{8.11}$$

If $\Delta\omega \gg \dfrac{g_{mC}}{\sqrt{C_a C_b}}$ then

$$\omega_1 = \omega_a \qquad \omega_2 = \omega_b \tag{8.12}$$

If $\Delta\omega \ll \dfrac{g_{mC}}{\sqrt{C_a C_b}}$ then

$$\omega_{1,2} = \omega_0 \pm \frac{g_{mC}}{2\sqrt{C_a C_b}} \tag{8.13}$$

For $Q < \frac{1}{2}$ only the solution ω_0 exists [DES82]. Note that $g_{mC} = \omega_0 \sqrt{C_a C_b}$ is called the critical coupling and corresponds to the value of g_{mC}, where the power transfer between cell a and b is maximum.

The qualitative interpretation of eqs. (8.12)&(8.13) is the following:

The first solution ω_0 is independent of any coupling coefficient g_{mc} or quality factor Q. Frequency f_0 is the arithmetic average of both center frequencies f_a and f_b. While $Q > \frac{1}{2}$, it corresponds to a minima of the passband transfer function, whereas for $Q < \frac{1}{2}$ it is a maxima .

If $\Delta\omega$ is large compared to $\frac{g_{mC}}{\sqrt{C_a C_b}}$ {eq. (8.12)}, the resonance peak of one cell is placed outside the passband of the other cell, and therefore at the resonance frequency of one cell the signal is attenuated by the other. Therefore the gain in the passband is drastically reduced and the extremes correspond to the individual center frequencies. The coupling factor between these cells does not interfere and the filter response is simply the superposition of the both filter responses. On the other hand, if $\Delta\omega$ is small compared to $\frac{g_{mC}}{\sqrt{C_a C_b}}$ {eq. (8.13)}, the extremes vary proportionally to g_{mC}.

To illustrate eq. (8.13) a bandpass filter corresponding to the one represented in Fig. 8.1 is simulated with a circuit simulator program [JOE89] for a center frequency mismatch $\Delta\omega = 0$ and $\Delta\omega = 0.008\ \omega_0$. The numerical values used for the simulations are reported in Table 8.1.

	g_{mc} curve (a)	g_{mc} curve (b)	g_{mia}	$C_a = C_b$	$R_a = R_b$	L_a	L_b
Fig. 8.2: $\Delta\omega = 0$	0.135 $\frac{\mu A}{V}$	0.27 $\frac{\mu A}{V}$	0.65 $\frac{\mu A}{V}$	72.6 pF	10 MΩ	2.23 H	2.23 H
Fig. 8.3: $\frac{\Delta\omega}{\omega_0} = 0.8\%$	0.135 $\frac{\mu A}{V}$	0.27 $\frac{\mu A}{V}$	0.65 $\frac{\mu A}{V}$	72.6 pF	10 MΩ	2.23 H	2.16 H

Table 8.1:   Numerical values used for the simulations shown in Figs. (8.2) & (8.3)
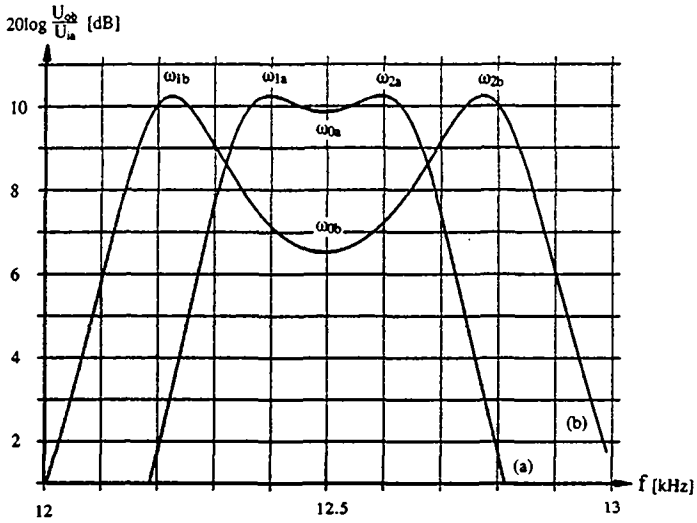
Figure 8.2:   Simulation of the passband response $20log \frac{U_{\rho b}}{U_{ia}}$ for $\Delta\omega = 0$ for two g_{mC} in a

1:2 ratio.   (a) $g_{mC1} = .135 \frac{\mu A}{V}$ (b) $g_{mC2} = .27 \frac{\mu A}{V}$
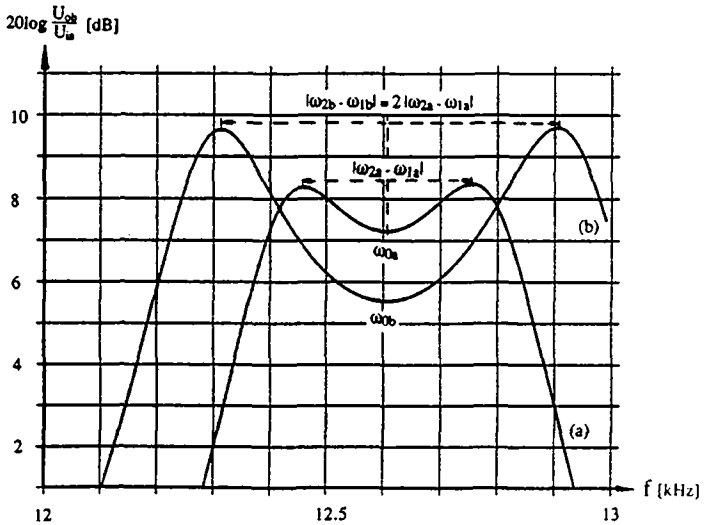

Figure 8.3:   Simulation of the passband response $20 log \frac{U_{\rho b}}{U_{ia}}$ for $\frac{\Delta\omega}{\omega_0} = 0.8\%$ for two

g_{mC} in a 1:2 ratio. (a) $g_{mC1} = .135 \frac{\mu A}{V}$ (b) $g_{mC2} = .27 \frac{\mu A}{V}$

According to eq. (8.13) ω_1 and ω_2 depend linearly on g_{mC}. Figures. 8.2 & 8.3 show the simulated results of the passband response while g_{mC} varies by a factor of two. While no frequency mismatch exists, hence $\Delta\omega$ is equal to zero, the gain of the passband as a function of g_{mc} remains unchanged, and g_{mC} only affects ω_1 and ω_2 (Fig. 8.2). While a small center frequency mismatch exists ($\frac{\Delta\omega}{\omega_0} = 0.8\% < \frac{g_{mC}}{\sqrt{C_a C_b}}$), ω_1 and ω_2 increase linearly with g_{mC} (Fig. 8.3). Note that the gain in the passband increases with g_{mC}.

8.1.3 SYNTHESIS OF THE FOURTH ORDER LC FILTER

The objective of this section is to determine the equivalent continuous-time filter which can be associated to the coupled *LC* filter of Fig. 8.1.

This *LC* filter is transformed into the g_mC filter of Fig. 8.4 after:

- replacing the two dependent current sources by gyrator g_{mc}

- and implementing the inductances by using a gyrator, where one side is connected to a capacitor C_k'. The inductance value L_k is determined by C_k' and by the transconductances of the gyrator g_{mLk} and $g_{mL'k}$ (*k=a,b*)

$$L_k = \frac{C_k'}{g_{mLk}\, g_{mL'k}} \tag{8.14}$$

The center frequency of the circuit of Fig. 8.4 is given by:

$$f_{ok} = \frac{\omega_{0k}}{2\pi} = \frac{1}{2\pi\sqrt{L_k C_k}} = \sqrt{\frac{g_{mLk}\, g_{mL'k}}{C_k C_k'}} \tag{8.15}$$
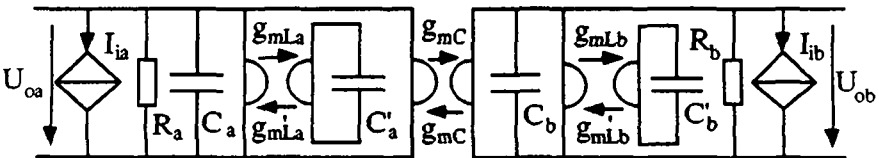

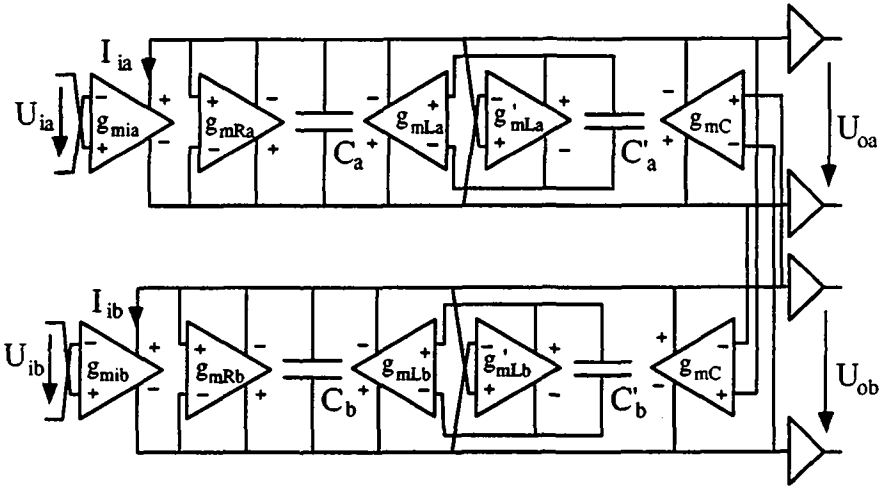**Figure 8.4:**   Equivalent 4th order coupled *LC* bandpass filter

Figure 8.5: 4th order g_mC bandpass filter built with two identical 2nd order cells

As a good matching between the center frequencies of the two cells is required, the goal is to built a filter with two identical 2nd order cells. Therefore elements are added in order to match the parasitic capacitances of both cells a and b. For example, a dependent current source I_{ib} of value zero is added to cell b.

From Fig. 8.4 the equivalent 4th order g_mC bandpass filter of Fig. 8.5 can be deduced. The gyrators are realized using two cross-coupled $OTAs$ [JOE86]. If the input of an OTA is connected to its corresponding output, the OTA operates like a resistance of value

$$R_k = \frac{1}{g_{mRk}}   \tag{8.16}$$

If g_{mc} is zero, the center frequencies of each 2nd order filter cell of Fig. 8.5 can be measured individually with the help of four output buffers.

In the differential structure of Fig. 8.5 the parasitic output capacitances are in parallel with the functional capacitors C_i. The $OTAs$ of Fig. 8.5 are realized with fully differential, linearized transconductance amplifiers, the common-mode of which is stabilized with transistors biased in the triode region [KRU88]. Note that the transconductances of linearized $OTAs$ are

smaller (about 3-6 times) than the one's of non-linearized *OTAs* [JOE86]. The layout is simplified by choosing

$$g_{mRa} = g_{mRb} = g_{mC} = \frac{g_{mia}}{2} = \frac{g_{mib}}{2} \qquad (8.17)$$

Transconductance g_{mik} of the input *OTA* is chosen to be twice as large as the others to compensate the 6dB loss at the resonance while the bias currents are identical, according to eq. (8.9).

8.1.4 *SIMULATIONS AND EXPERIMENTAL RESULTS*

An experimental g_mC bandpass filter based on Fig. 8.5 has been integrated. The influence of the different interfering parameters can be verified, because the transconductances of the *OTAs* can be controlled individually.

The layout structure of the filter is similar to the one used for large continuous-time filters [KRU88], [KRU90], that is an array of *OTAs* and capacitors C. To reduce the capacitance mismatch large capacitor values are chosen, which implies a passband response in the audio range. With the aid of auxiliary switches, the filter can operate either with a static current mirror or with a dynamic current mirror. The bias currents of the *OTAs* are delivered by these current mirrors, and therefore the matching of the four transconductances g_{mLk} and g_{mLk}' is a function of the current accuracy.

The measured passband responses for cells a and b of the g_mC bandpass filter of Fig. 8.5 are represented in Figs 8.6 & 8.7. In this particular example the mismatch between the capacitances is negligible. Therefore the matching of the center frequencies shows the accuracy of the corresponding current mirrors. In Fig. 8.6 a static current mirror delivers the bias currents, whereas in Fig. 8.7 a dynamic current mirror is used. Curve a represents the transfer function of cell a and curve b shows the transfer function which corresponds to cell b.

It is possible to disconnect the current mirrors from the rest of the circuit and to measure individually the output currents. At $I_{in} = 1\mu A$ the measured spread of static current mirrors is found to be $\sigma_I \approx 7200ppm$, whereas for dynamic current mirrors $\sigma_I \approx 240ppm$.

Figure 8.6:   Measurement of the individual passband responses $20log\frac{U_{ok}}{U_{ik}}$ of cell a ($k=a$, curve a) and b ($k=b$, curve b). The filter operates with a static current mirror.
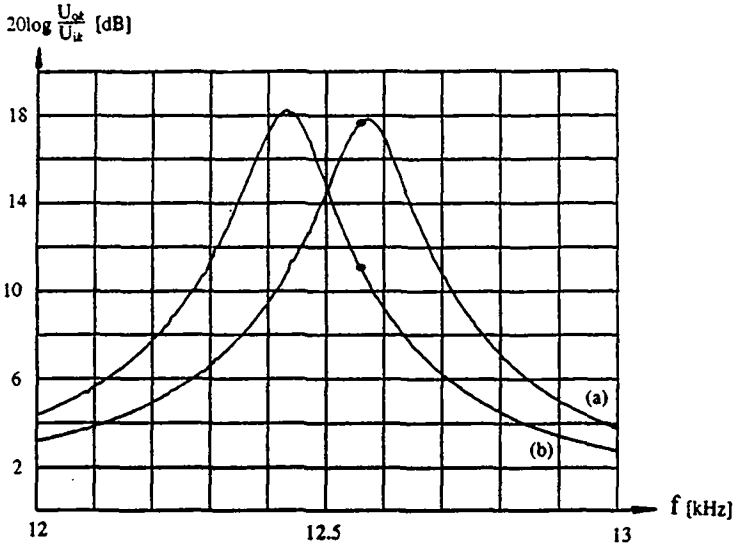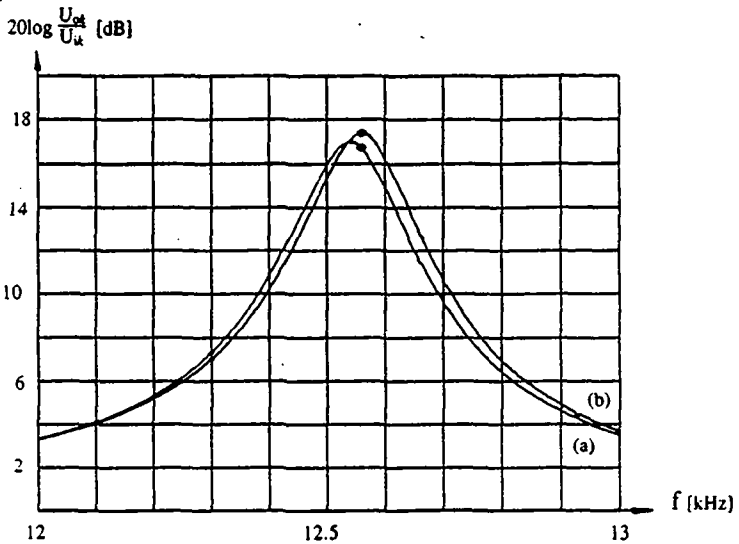

Figure 8.7:   Measurement of the individual passband responses $20log\frac{U_{ok}}{U_{ik}}$ of cell a ($k=a$, curve a) and b ($k=b$, curve b). The filter operates with a dynamic current mirror.

If a multiple of the sampling frequency falls inside the passband, the spikes of the output current may produce a small ripple on the passband response.

The transconductances are built with linearized *OTAs*, each of them needing two current sources for the bias. According to Fig. 8.5 two capacitors and two *OTAs* are necessary to fix one center frequency, which implies four current sources. To match the parasitic capacitances to ground, each capacitor is split into two equal parts. Then the ends of both capacitors are cross-coupled, so that they are connected to the metal and to the poly.

Because the capacitor oxide is processed during a different fabrication step than the gate oxide of the transistors, the spread of the current sources σ_I and of the capacitances σ_C can be assumed to be statistically independent. The current sources are distributed all over the chip area, that's why they are also assumed to be uncorrelated. The spread of the center frequencies $\sigma_{\omega o}$ can then be expressed as [PAP65]

$$\sigma_{\omega o} = \sqrt{\frac{\sigma_I^2}{4} + \frac{\sigma_C^2}{2}} \qquad (8.18)$$

In Table 8.2 the measured spread $\sigma_{\omega o}$ and σ_I are reported for $I_{in} \approx 1\mu A$ and σ_C is then calculated using eq. (8.18).

The spread $\sigma_{\omega o}$ and σ_I were obtained by measuring 40 chips out of three different wafers for a center frequency of 10kHz. The chips with more than 1.5% spread of the center frequency (4 chips) were excluded.

| | measured [1000ppm] | | calculated [1000ppm] |
	$\sigma_{\omega o}$	σ_I	Σ_C
static current mirror	6.8	7.2	8.1
dynamic current mirror	4.7	0.24	6.6

Table 8.2:   Calculation of σ_C from the measured values of $\sigma_{\omega o}$ and σ_I

σ_C remains constant and can be estimated when σ_I approaches zero, hence in the dynamic current mirror configuration. From Table 8.2 it is also visible, that the spread of the current sources is not independent from the spread of the capacitances σ_C, hence a certain correlation exists.

The capacitances do not have a common center of geometry, because the filter is built as an array of cells like in other continuous-time filters [KRU90]. A possible gradient (oxide thickness) may be at the origin of the large value σ_C which is observed.

Finally the $g_m C$ bandpass filter of Fig. 8.5 is simulated with a CMOS continuous-time filter program [JOE89]. The numerical values used during the simulations are given in Table 8.3. The center frequency mismatch is introduced by increasing g_{mLb} from 5.7 $\frac{\mu A}{V}$ (curve a) to 5.8 $\frac{\mu A}{V}$ (curve b).

Figure 8.8 shows the simulated passband responses while eq. (8.13) is valid, hence $\Delta\omega \propto \frac{g_m C}{\sqrt{C_a C_b}}$ for two values of center frequency mismatch, $\Delta\omega = 0$ (a) and $\frac{\Delta\omega}{\omega_0} \approx 0.8\%$ (b). In Table 8.3 the numerical values are listed. The measured passband response is shown in Fig. 8.9, which can compared to the simulation of Fig. 8.8, because the same parameters are chosen. As it is expected, the passband response is improving (gain, ripple, bandwidth) while the mismatch of the center frequencies is reduced.

	g_{mc}	g_{mia}	g_{mib}	$C_a = C_b$	$R_a = R_b$	g_{mLa}	g_{mLb}
Fig. 8.8: $\Delta\omega = 0$	0.135 $\frac{\mu A}{V}$	0.65 $\frac{\mu A}{V}$	0 $\frac{\mu A}{V}$	72.6 pF	10 MΩ	5.7 $\frac{\mu A}{V}$	5.7 $\frac{\mu A}{V}$
Fig. 8.9: $\frac{\Delta\omega}{\omega_0} = 0.8\%$	0.135 $\frac{\mu A}{V}$	0.65 $\frac{\mu A}{V}$	0 $\frac{\mu A}{V}$	72.6 pF	10 MΩ	5.7 $\frac{\mu A}{V}$	5.8 $\frac{\mu A}{V}$

Table 8.3:   Numerical values used for the simulations shown in Figs. (8.8) & (8.9)
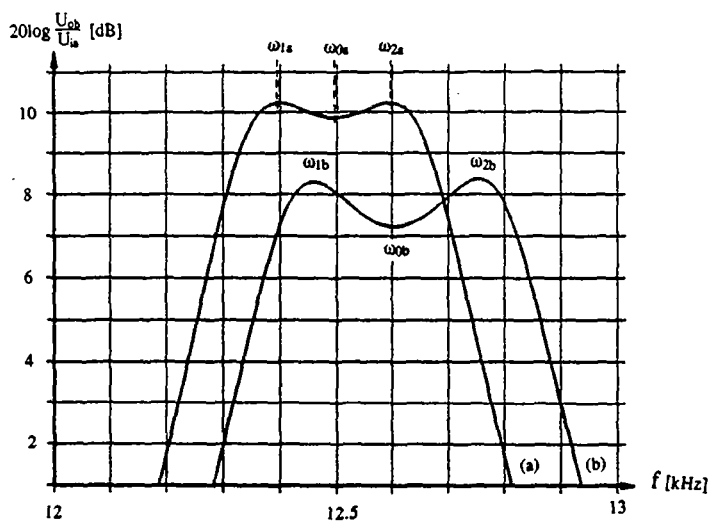
Figure 8.8:   Simulation of the passband response $20log \frac{U_{ob}}{U_{ia}}$ (filter of Fig. 8.5)

(a) $\Delta\omega = 0$;   (b) $\frac{\Delta\omega}{\omega_0} = 0.8\%$
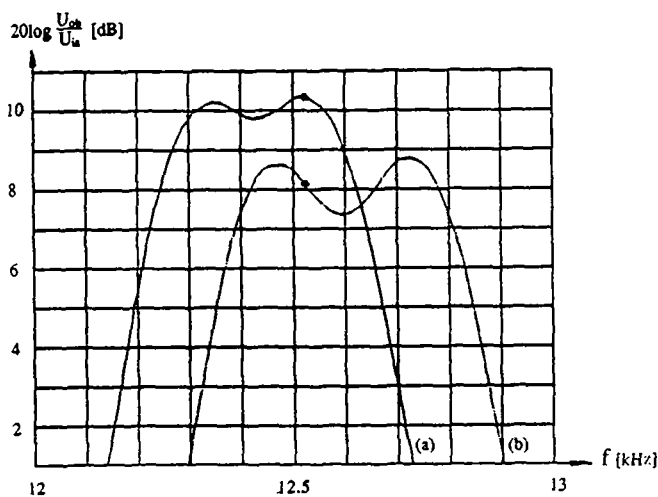

Figure 8.9:   Measurement of the passband response $20 \, log \, \frac{U_{ob}}{U_{ia}}$
(curve a) dynamic mirror;   (curve b) static mirror;

8.2 D/A & A/D CONVERTERS

Several groups have reported on A/D and D/A converters based on the idea of current copiers [GRO89], [NAI89.2], [ROB89.1], [VAL90], [DEV89].

One such D/A converter that has been published is a 16bit self-calibration D/A for audio applications [GRO89]. A multiple dynamic current mirror with 64 outputs uses improved basic cells to produce accurately the 6 MSB's. The LSB's are provided by dividing one of these outputs by a 10-bit resolution network.

A/D converters based on current mode circuits are expected to operate at faster speed, lower consumption and reduced die size for a given resolution than switched capacitor circuits [NAI89.2], [ROB89.1], [VAL90]. A ratio independent algorithmic A/D converter based on switched capacitor implementation [LIE84] is proposed by [NAI89.2] where the performances are 10 bit ($\pm 0,9$bit) with a conversion time of 40µs. A cyclic A/D converter, which uses some of the improvements mentioned in the previous chapter, achieves 14bit (± 0.7) with a reference current of 40µA. The power consumption is of 2.5mW and the conversion time is 175µs [DEV91].

A pipelined A/D converter structure, which is based on [TEM85], was presented in [ROB89.1], where the fundamental limitations like noise and charge injection are related to the achievable resolution. The theoretical analysis predicts a throughput rate of 6µs for a 12bit converter (± 0.5LSB) with a 3µm technology. But no experimental results are available.

The drawback of these structures is the multiplication of the input signal, which increases noise and limits the achievable accuracy. Furthermore a speed-accuracy trade-off is involved due to the cycle-to-cycle varying signals. The conversion time depends on the input signal because of the transconductance involved in the main time constant.

A pipelined architecture which has not the above mentioned drawbacks is proposed by [DEV89] and is based on current dividers. The input signal is not processed, but compared to a reference current which is divided by two through the stages. Since only static currents are processed it is inherently faster than the previously described converters. Once all the divider

currents have settled, the converter is ready to operate. The theoretical analysis predicts a 2µs per cycle for a 12bit converter (±0.5LSB) with a reference current of 100µA, and a 3µm technology. The operating speed is mainly limited by the parasitic capacitances of the current comparator.

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8.3 OTHER APPLICATIONS

Other reported applications are switched current filters [HUG89], where the signal is represented by current samples in contrast to switched-capacitor circuits which use charge samples. The main advantages of this technique compared to switched capacitor filters is the low power voltage requirement and the use of a standard digital CMOS process, which requires no floating capacitors. The current storage is achieved with a derivation of the current copier [HUG90], [ALL90]. Due to the delay introduced by the current storage some fundamental filter functions like integration and differentiation can be performed. The filter design is deduced from the transfer functions given in the z-domain similar to the signal flow graph synthesis used for switched capacitor circuits.

Other possible applications are suggested in [VIT90], where some more complicated functions based on translinear circuits are proposed, namely an adjustable current mirror, a normalization circuit, a current conveyor and a PTAT voltage circuit.

The idea of the normalization circuit is exploited by [AEB90] in the case of an array with eight channels. Simulations show that the circuit operates correctly. The chip area needed for the circuit to achieve accuracy, hence the dimensions of the layout, is quite large compared to the area obtained by simply increasing the surface of the corresponding transistors.

8.4 SUMMARY

Dynamic current mirrors were implemented in a continuous-time filter. The passband responses change as a function of the increase of matching of the transconductances according to the theoretical previsions and to

simulations. The matching of the center frequencies while using a static current mirror is about 0.7%, hence comparable to the accuracy of the current mirror itself. The matching of the center frequencies is increased because four current sources fix the value of the transconductances and therefore an average effect occurs. With the aid of dynamic current mirrors the accuracy of the bias currents is increased ($\sigma_I \approx 240$ppm) and the matching of the center frequencies is then limited by the matching of the capacitors. Because the capacitors do not have the same center of geometry, their matching is reduced by the existing gradient (oxide thickness and doping). A possible improvement would consist in developing and implementing a structure with a common center of geometry for the capacitors (layout) as used in switched capacitor techniques. So it would be possible to profit entirely from the increase of matching provided by a dynamic current mirror.

Other applications based on the current copier principle such as D/A & A/D converters and switched current filters are outlined.

CHAPTER 9

CONCLUSIONS

A new type of a highly accurate MOS current mirror was investigated which eliminates the main limitations of standard mirrors such as mismatch and 1/f noise. This mirror requires no trimming and is insensitive to the matching of the transistors and to the non-linearities of the capacitances, thus to process variations. The dynamic current mirror, whose basic cell is also called a current copier, only needs a baseline digital CMOS process without any floating capacitances. Its accuracy is independent of the external conditions like temperature variations, because the gate voltage, hence the stored drain current, is always updated.

The performances of current copiers depend on parameters like charge injection, clock jitter, drain voltage variations, sampled noise and leakage currents. In order to overcome these limitations or to reduce the sensitivity to the above mentioned parameters, different circuit techniques and adequate design tricks were proposed and their advantages and disadvantages discussed. These issues should be taken into account while designing current copiers.

Design formulas were given for the specific circuits and particular operating conditions so that the resulting current error was kept small. Experimental results of different types of dynamic current mirrors, which operated under different conditions, confirmed the theoretical influence of the different parameters on the accuracy. The improvement in accuracy of dynamic current mirrors was about 200 compared to static CMOS mirrors.

The current copier which provides a discontinuous copy of the input current was extended to obtain continuous multiple copies as well as current multiplication or division by integer numbers.

The undersampled white noise of the main transistor and of the sampling switch was calculated using the notion of equivalent noise bandwidth, which was also extended to the 1/f noise. The obtained approximation of the undersampled 1/f noise was more accurate than the one which was obtained with an alternative approach. It was shown that the 1/f noise in the baseband is cancelled out and that it can be considered as an increase of the white noise.

Dynamic current mirrors and current copiers may become an ubiquitous building block in most accurate current mode applications. Different

current mode circuits already use them, like D/A and A/D converters, neural networks and switched current (SI) filters. Perhaps the principle can be extended to other circuits in order to create very precise analog CMOS building blocks. As shows the amount of recent publications, the interest in the current mode approach is increasing.

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APPENDICES

MOS MODEL, DEFINITIONS,

SYMBOLS & CHARACTERISTICS

The symbols and definitions that are used for n- and p-channel transistors are shown in Fig. A.1. The analysis assumes a symmetrical device, hence source V_S and drain V_D voltages can be interchanged.
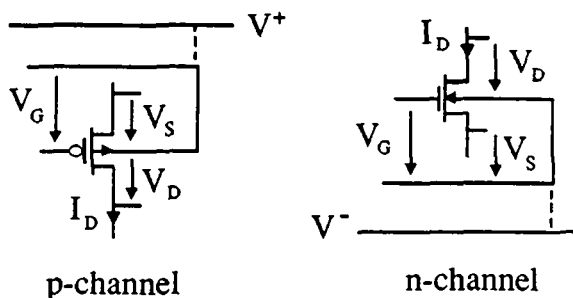

p-channel   n-channel

Figure A.1: Symbols and definitions for an n- and a p-channel MOS transistor

V_S, V_D and gate voltage V_G are referred to the local substrate which is either the general substrate of the circuit or a separate well. The substrate will be omitted when it is connected to one rail of the power supply (V^+ for p-channel, V^- for n-channel).

The MOS transistor can be characterized by the following parameters [VIT85.1], [VIT89], [TSI87]:
- the gate threshold voltage V_{T0} for $V_S=0$
- the factor n which represents the reduction of the gate voltage effect due to fixed charges in the channel
- the specific current I_s
- the saturation current I_{Dsat}
- the transfer parameter β

β is defined as:

$$\beta = \mu C'_{ox} \frac{W_{ef}}{L_{ef}} \tag{A.1}$$

where μ is the mobility of charge carriers and C'_{ox} the gate oxide capacitance per unit area. The effective channel length L_{ef} and channel width W_{ef} of the transistor are defined by the layout, the tolerances and the overlap given by process parameters.

The effective gate threshold voltage V_{TE} will be assumed to depend linearly on the source voltage V_S:

$$V_{TE} = V_{T0} + nV_S \tag{A.2}$$

The factor n stands for the effect of substrate modulation. It is usually between 1.5 and 2 for small gate voltage values and tends to 1 with increasing V_G [VIT89].

The specific current I_s [ENZ89] determines whether the device operates in weak inversion ($I_{Dsat} < I_s$) or in strong inversion ($I_{Dsat} > I_s$):

$$I_s = 2n\beta U_T^2 = 2n\mu C'_{ox} U_T^2 \frac{W_{ef}}{L_{ef}} \tag{A.3}$$

with $\qquad\qquad U_T = \frac{kT}{q} \tag{A.4}$

The saturation voltage V_{Dsat} is defined as:

$$V_{Dsat} = \frac{V_G - V_{T0}}{n} = V_s + 2U_T \sqrt{\frac{I_{Dsat}}{I_s}} \qquad (A.5)$$

If the transistor operates in **strong inversion** it is modeled by the following relations:

triode or linear $I_D = \beta \ (V_D - V_S) \ \{V_G - V_{T0} - \frac{n}{2} (V_S + V_D)\}$
(conduction)

$$= \beta \ (V_D - V_S) \ \{V_G - V_{TE} - \frac{n}{2} (V_D - V_S)\} \qquad (A.6)$$

saturation $I_D = I_{Dsat} = \frac{\beta}{2n} \ \{V_G - V_{T0} - nV_S\}^2$

$$= \frac{\beta}{2n} \ \{V_G - V_{TE}\}^2 \qquad (A.7)$$

where eq. (A.6) is valid while $V_D < V_{Dsat}$ and eq. (A.7) for $V_D > V_{Dsat}$.

The drain current in **weak inversion** is given by:

$$I_{Dsat} = I_s \ e^{\frac{V_G - V_{T0}}{nU_T}} \ \{e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}}\}^2 \qquad (A.8)$$

which reaches its saturation value when the term in V_D becomes negligible, thus for the minimum possible value of the saturation voltage

$$V_{Dsat} = V_s + (2 \ to \ 6)U_T \qquad (A.9)$$

The small signal transconductance in saturation $g_m = \frac{dI_{Dsat}}{dV_G}$ is given by:

weak inversion $g_m = \frac{I_{Dsat}}{nU_T} \qquad (A.10)$

strong·inversion $g_m = \sqrt{\dfrac{2\beta I_{Dsat}}{n}} = \dfrac{\beta}{n}(V_G - V_{TE})$ (A.11)

Furthermore, the residual drain to source conductance g_{ds} in saturation due to the channel shortening effect can be approximated by:

$$g_{ds} = \frac{I_{Dsat}}{V_E} = \frac{I_{Dsat}}{\lambda L_{ef}}$$ (A.12)

where the Early voltage V_E is of the order of tens of volts, λ is a process parameter and its unit is $\dfrac{V}{\mu m}$. The Early voltage also increases slowly with the gate voltage and thus is minimum in weak inversion.

This leads to the small signal model in saturation represented in Fig. A.2 for $V_d > V_s$. Note that C_{gd} or C_{gs} is the sum of the overlap capacitance and of the functional capacitance and that C_{gb} is zero in strong inversion [VIT89]. If the source potential is connected to the bulk the sum of the drain conductions is labeled g_0.
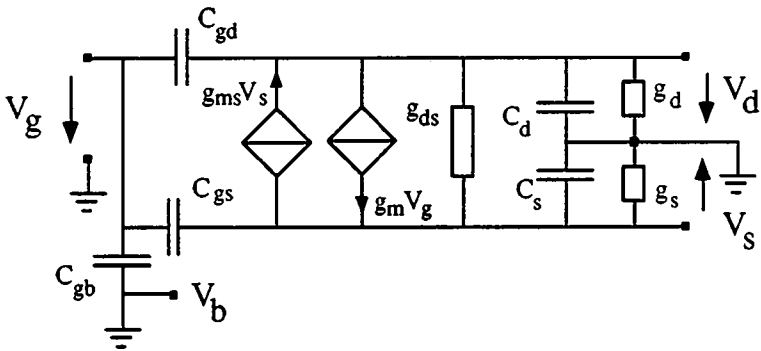

Figure A.2:   Small signal model in saturation for $V_d > V_s$

APPENDIX B

OPEN LOOP TRANSFER FUNCTION

OF THE STORAGE PHASE

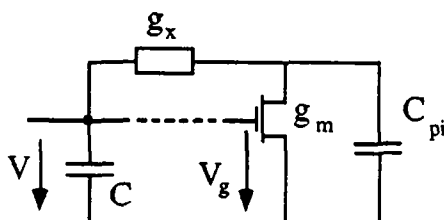The small signal model during the storage phase is given in Fig. (B.1).

Figure B.1: Small signal representation of the current copier during the storage phase
which is used for the open loop transfer function

If the loop is opened at the dotted line {Fig. (B.1)} the open loop transfer function can be expressed as

$$Z(p) = \frac{V(p)}{V_g(p)} = \frac{-1}{p\tau_d(1 + p\tau_p)} \tag{B.1}$$

with:

$$\tau_d = \frac{C(g_x+g_0)+C_{pi}g_x}{g_x\,g_{mm}} = \frac{1}{2\pi f_c} \tag{B.2}$$

$$\tau_p = \frac{C\,C_{pi}}{C(g_x+g_0)+C_{pi}g_x} = \frac{1}{2\pi f_{c2}} \tag{B.3}$$

where τ_d and τ_p are the time constants of the circuit. Mostly τ_d and τ_p can be approximated by:

$$\tau_d \overset{\substack{g_x \gg g_0 \\ C \gg C_{pi}}}{\approx} \frac{C}{g_{mm}} \qquad \tau_p \overset{\substack{g_x \gg g_0 \\ C \gg C_{pi}}}{\approx} \frac{C_{pi}}{g_x} \tag{B.4}$$

The two poles of the closed loop circuit are (roots of $1-Z(p) = 0$)

$$p_{1,2} = -\frac{1}{2\tau_p} \pm \sqrt{\frac{1}{4\tau_p^2} - \frac{1}{\tau_d\tau_p}} \tag{B.5}$$

While the approximations expressed in eq. (B.4) are valid the real solutions of eq. (B.5) are found to be:

$$p_1 = -\frac{1}{\tau_d} \overset{g_x \gg g_0}{\approx} \frac{g_{mm}}{C+C_{pi}} \overset{C \gg C_{pi}}{\approx} \frac{g_{mm}}{C} \tag{B.6}$$

$$p_2 = -\frac{1}{\tau_p} \overset{g_x \gg g_0}{\approx} \frac{(C+C_{pi})g_x}{C\,C_{pi}} \overset{C \gg C_{pi}}{\approx} \frac{g_x}{C_{dpi}} \tag{B.7}$$

If the approximations expressed in eq. (B.4) are not valid, the response is a damped oscillation with an envelope of $2\tau_p$ according to eq. (B.5).

Therefore a global settling time constant τ_s may be reasonably approximated by:

$$\tau_s < \tau_d + 2\tau_p = \frac{C(g_x + g_0) + C_{pi}g_x}{g_x\ g_{mm}} + \frac{2\ C\ C_{pi}}{C(g_x + g_0) + C_{pi}g_x}$$

$$\approx \frac{g_x(C + C_{pi})^2 + 2\ g_{mm}CC_{pi}}{g_xg_{mm}(C + C_{pi})} \tag{B.8}$$

The denominator $D(p)$ of the transfer functions can be expressed as, according to eq. (4.42) and to the small signal scheme of Figs. 4.7 & B.1:

$$D(p) = (g_{mm} + g_0)g_x\{1 + p\tau_d(1 + p\tau_p)\} \tag{B.9}$$

While the poles are given by eqs. (B.6) & (B.7), the transients of the transfer functions with denominator $D(p)$ decrease exponentially with time and no overshoot occurs.

APPENDIX C

EQUIVALENT NOISE

BANDWIDTH

C.1 DEFINITION

The "equivalent noise bandwidth" Δf is defined as the bandwidth, which is needed to obtain the same noise power at the output of an ideal low-pass filter than at the output of a low-pass filter, while both DC gains are identical. It is hence defined as:

$$V_{Nw}^2 = \int_{-\infty}^{+\infty} S_N(f)/A(f)/^2 \, df = \int_{-\Delta f}^{+\Delta f} S_N(f) \, df \qquad (C.1)$$

Note that the "equivalent noise bandwidth" Δf depends on the noise spectral power density $S_N(f)$.

C.2 EQUIVALENT WHITE NOISE BANDWIDTH

C.2.1 FIRST ORDER LOW-PASS FILTER

For a first order, unity-gain low-pass filter given by

$$A(f) = \frac{1}{1 + 2\pi j \frac{f}{f_c}} \tag{C.2}$$

the white noise voltage component V_{Nw}^2 is found to be:

$$V_{Nw}^2 = \int_{-\infty}^{+\infty} \frac{S_{Nw} \, df}{(1 + |\frac{f}{f_c}|^2)} = S_{Nw} \pi f_c = \int_{-\Delta f_w}^{+\Delta f_w} S_w df = 2\Delta f_w \, S_{Nw} \tag{C.3}$$

where S_{Nw} is the "white noise spectral power density", which is frequency independent, Δf_w is the "equivalent white noise bandwidth" f_c is the cut frequency of the first order low-pass filter. From eq. (C.3) Δf_w can be expressed as:

$$\Delta f_w = \frac{\pi f_c}{2} \tag{C.4}$$

C.2.2 SECOND ORDER LOW-PASS FILTER

In the case of a second order unity gain low-pass filter, the second order low-pass transfer function $A(p)$ can be written as:

$$A(p) = \frac{1}{1 + p\alpha(1 + p\beta)} \tag{C.5}$$

with $p = j\omega = j2\pi f$.

C.2.3 REAL POLES:

If $\alpha > 4\beta$ the poles of eq. (C.5) are real, eq. (C.5) can be written as:

$$A(p) = \frac{1}{(1 + p\gamma_1)(1 + p\gamma_2)} \tag{C.6}$$

where $\alpha = \gamma_1 + \gamma_2$. Note that $\beta = \dfrac{\gamma_1\gamma_2}{\gamma_1+\gamma_2}$ always smaller than α.

Eq. (C.1) becomes:

$$V_{Nw}^2 = \int_{-\infty}^{+\infty} \frac{S_{Nw}(f)\,df}{(1+|f\gamma_1|^2)(1+|f\gamma_2|^2)} = \frac{S_{Nw}}{2\pi} \frac{1}{\gamma_1-\gamma_2^2} \left[\int_{-\infty}^{+\infty} \frac{\gamma_1\,dx}{1+|x|^2} - \int_{-\infty}^{+\infty} \frac{\gamma_2\,dx}{1+|x|^2} \right]$$

$$= \frac{S_{Nw}}{2(\gamma_1+\gamma_2)} = \frac{S_{Nw}}{2\alpha} = \int_{-\Delta f_w}^{+\Delta f_w} S_{Nw}\,df = 2\Delta f_w\, S_{Nw} \tag{C.7}$$

with $x = 2\pi f \gamma_1$ and

$$\Delta f_w = \frac{1}{4\alpha} \tag{C.8}$$

C.2.4 IMAGINARY POLES: GENERAL CASE

If the poles of $A(p)$ are imaginary, eq. (C.5) can be written as:

$$A(j\omega) = \frac{1}{(1-\omega^2\alpha\beta) + j\omega\alpha} \tag{C.9}$$

hence

$$|A(\omega)|^2 = \frac{1}{|1-\omega^2\alpha\beta|^2 + |\omega\alpha|^2} = \frac{1}{1+\omega^2\alpha(\alpha-2\beta)+\omega^4\alpha^2\beta^2} \tag{C.10}$$

Eq. (C.10) yields:

$$\Delta f_w = \frac{1}{4\pi} \int_{-\infty}^{+\infty} \frac{d\omega}{1+b\omega^2+c^2\omega^4} = \frac{1}{8\pi\sqrt{c}} \int_{-\infty}^{+\infty} \frac{dx}{\sqrt{x}\,(1+\frac{b}{c}x+x^2)} \tag{C.11}$$

with:
$$b = \alpha(\alpha\text{-}2\beta) \qquad c = \alpha\beta \quad x = c\omega^2 \qquad (C.12)$$

which according to [GRA65] p. 297 can be solved after replacing with $cos(t) = \dfrac{b}{2c}$, hence $1 + cos(t) = \dfrac{\alpha}{2\beta}$, leads to:

$$\Delta f_w = \frac{1}{4\pi\sqrt{c}} \; (\text{-}\pi)\frac{sin(\text{-}\frac{t}{2})}{sin(t) \; sin(\frac{\pi}{2})} = \frac{1}{4\sqrt{2c}}\frac{1}{\sqrt{1+cos(t)}} = \frac{1}{4\alpha} \qquad (C.13)$$

which surprisingly depends only on the linear term α [VIT84].

Example: Transfer Function F(p)

According to eq. (4.40)&(4.42) $F(p)$ is given by:

$$F(p) = A_{DC} \; \frac{1}{1+p\alpha\{1+p\beta\}} \qquad (C.14)$$

with the DC value:
$$A_{DC} = \frac{1}{(g_{mm}+g_0)} \qquad (C.15)$$

from Appendix B:
$$\alpha = \tau_d = \frac{C(g_x+g_0)+C_{pi}g_x}{g_x \, g_{mm}} \qquad (C.16)$$

$$\beta = \tau_p = \frac{C \, C_{pi}}{C(g_x+g_0)+C_{pi}g_x} \qquad (C.17)$$

The "equivalent white noise bandwidth" Δf is found to be:

$$\Delta f_w = \frac{1}{4\alpha} = \frac{1}{4\tau_d} \; \approx \; \frac{g_{mm}g_x}{C(g_x+g_0)+C_{pi}g_x} \qquad (C.18)$$

C.2.5 SECOND ORDER LOW-PASS WITH A SINGLE ZERO

The transfer function $B(p)$ of a second order low-pass with a single zero is given by:

$$B(p) = \frac{1+p\delta}{1+p\alpha\{1+p\beta\}} \qquad (C.19)$$

and
$$|B(\omega)|^2 = \frac{1 + |\omega\delta|^2}{1+\omega^2\alpha(\alpha-2\beta)+\omega^4\alpha^2\beta^2} \qquad (C.20)$$

which can be decomposed into a first term identical to eq. (C.9) and a second term depending on $|\omega\delta|^2$. The "equivalent white noise bandwidth" Δf_w is the sum of both contribution, hence:

$$\Delta f_w = \Delta f_{w1} + \Delta f_{w2} \qquad (C.21)$$

where $\Delta f_{w1} = \dfrac{1}{4\alpha}$. The second term Δf_{w2} is calculated after substitution with the parameters given in eq. (C.12)

$$\Delta f_{w2} = \frac{\delta^2}{2\pi\sqrt{c^3}} \int_{-\infty}^{+\infty} \frac{\sqrt{x}\ dx}{(1 + \frac{b}{c}x + x^2)} = \frac{\delta^2}{4\sqrt{c^3}} \frac{sin(\frac{t}{2})}{sin(t)} \qquad (C.22)$$

Introducing the results of eq. (C.13)&(C.22) in eq.(C.21) Δf_w is found to be:

$$\Delta f_w = \frac{1}{4\alpha}\{1 + \frac{\delta^2}{\alpha\beta}\} \qquad (C.23)$$

Example: Transfer Function $G(p)$

According to eq. (4.41)&(4.42) $G(p)$ is given by:

$$G(p) = A_{DC} \frac{1+p\delta}{1+p\alpha\{1+p\beta\}} \qquad (C.24)$$

where:

$$A_{DC} = \frac{g_0}{(g_{mm}+g_0)g_x} \qquad (C.25)$$

$$\delta = \tau_0 = \frac{C_{pi}}{g_0} \qquad (C.26)$$

and α and β given by eq. (C.16)&(C.17).

Finally the "equivalent white noise bandwidth" Δf_w is:

$$\Delta f_w = \frac{1}{4\tau_d}\{1 + \frac{\tau_0^2}{\tau_d\tau_p}\} = \frac{g_x g_{mm}}{4[C(g_x+g_0)+C_{pi}g_x]} \{1+\frac{(g_{mm}+g_0)g_x}{g_0^2} \frac{C_{pi}}{C}\} \qquad (C.27)$$

C.3 EQUIVALENT 1/F NOISE BANDWIDTH

C.3.1 FIRST ORDER LOW-PASS FILTER

The 1/f noise voltage component $V_{N1/f}^2$ is given by the integral over the frequency domain of the 1/f noise density. But $V_{N1/f}^2$ is divergent because of the pole at the origin. Nevertheless the 1/f noise power of a low-pass filter can be compared to the one of a ideal low-pass filter using the definition given in eq. (C.1), which leads to the "equivalent 1/f noise bandwidth" $\Delta f_{1/f}$.

The first order low-pass filtered 1/f noise voltage component $V_{N1/f}^2$ is:

$$V_{N1/f}^2 = K \int_{-\infty}^{+\infty} \frac{df}{(1+|\frac{f}{f_c}|^2)f} \qquad (C.28)$$

which must be compared to the first order ideal low-pass filtered 1/f noise voltage component.

$$V_{N1/f}^2 = K \int_{-\Delta f_{1/fc}}^{+\Delta f_{1/fc}} \frac{df}{f} \qquad (C.29)$$

where $\pm\Delta f_{1/fc}$ correspond to the upper and lower limits of integration, respectively, which are normalized to f_c.

Because eq. (C.28) is not defined at the limits and a discontinuity exists for $f \to 0$, it is rewritten as

$$V_{N1/f}^2 = 2K \lim_{\substack{a \to 0 \\ b \to \infty}} \int_a^b \frac{df}{(1+|\frac{f}{f_c}|^2) f} = 2K \lim_{\substack{a \to 0 \\ b \to \infty}} \left[ln\frac{b}{a} + \frac{1}{2} ln\frac{1+a^2}{1+b^2} \right] \quad \text{(C.30)}$$

where a and b correspond to the upper and lower limits of integration normalized to f_c, respectively. Rewriting eq. (C.29) as

$$V_{N1/f}^2 = 2K \lim_{c \to 0} \int_c^{\Delta f_{1/fc}} \frac{df}{f} = 2K \lim_{c \to 0} \left[ln\frac{\Delta f_{1/fc}}{c} \right] \quad \text{(C.31)}$$

where c is the normalized lower limit of integration for the ideal low-pass filter normalized to f_c. Identifying eq. (C.30) & (C.31) leads to:

$$\lim_{\substack{a \to 0 \\ b \to \infty}} \left[ln\frac{b}{a} + \frac{1}{2} ln\frac{1+a^2}{1+b^2} \right] = \lim_{c \to 0} \left[ln\frac{\Delta f_{1/fc}}{c} \right] \quad \text{(C.32)}$$

The lower limit is the same for both integrals, hence $a = c$, which yields:

$$\lim_{b \to +\infty} ln \frac{b}{\sqrt{1+b^2}} = ln \Delta f_{1/fc} = ln \frac{\Delta f_{1/f}}{f_c} \quad \text{(C.33)}$$

and finally:

$$\Delta f_{1/f} = f_c \lim_{b \to +\infty} \frac{b}{\sqrt{1+b^2}} = f_c \quad \text{(C.34)}$$

which means that $\Delta f_{1/f}$ is equal to the cut frequency f_c of the low-pass filter. Therefore

$$\Delta f_{1/f} = f_c \quad \text{(C.35)}$$

Note that if another normalization frequency than f_c is chosen, it is cancelled out in eq.(C.33). This means that the $1/f$ noise power of an ideal first order low-pass with cut frequency f_c is identical to the power of a low-pass with the same cut frequency f_c.

C.3.2 SECOND ORDER LOW-PASS WITH REAL POLES

The voltage noise component function V_{NIlf}^2 can be written as:

$$V_{NIlf}^2 = 2K \int_a^b \frac{df}{f(1+|2\pi f\gamma_1|^2)(1+|2\pi f\gamma_2|^2)} = 2K \int_a^b \frac{dx}{x(1+|x|^2)(1+|\rho x|^2)} \quad (C.36)$$

with $\rho = \dfrac{\gamma_2}{\gamma} = \dfrac{f_c}{f_{c2}}$, $\rho < 1$ and $x = 2\pi f\gamma$. The limits a and b are normalized to

γ. Substituting in eq. (C.36) y for ρx leads to:

$$2K \frac{1}{1-\rho^2} \left[\int_a^b \frac{dx}{x\,(1+|x|^2)} - \rho^2 \int_{\rho a}^{\rho b} \frac{dy}{y\,(1+|y|^2)} \right]$$

$$= 2K \frac{1}{1-\rho^2} \left\{ \lim_{\substack{a\to 0 \\ b\to +\infty}} \left[\ln\frac{b}{a} + \frac{1}{2}\ln\frac{1+a^2}{1+b^2} \right] - \rho^2 \lim_{\substack{a\to 0 \\ b\to +\infty}} \left[\ln\frac{b}{a} + \frac{1}{2}\ln\frac{1+\rho^2 a^2}{1+\rho^2 b^2} \right] \right\}$$

$$= 2K \left\{ \lim_{\substack{a\to 0 \\ b\to +\infty}} \left[\ln\frac{b}{a} \right] + \lim_{\substack{a\to 0 \\ b\to +\infty}} \frac{1}{2(1-\rho^2)} \left[\ln\frac{1+a^2}{1+b^2} - a^2 \ln\frac{1+\rho^2 a^2}{1+\rho^2 b^2} \right] \right\}$$

$$= 2K \left\{ \lim_{\substack{a\to 0 \\ b\to +\infty}} \left[\ln\frac{b}{a} \right] + \lim_{b\to +\infty} \frac{1}{2(1-\rho^2)} \left[\ln\frac{1}{1+b^2} \frac{(1+\rho^2 b^2)\rho^2}{1^{\rho^2}} \right] \right\}$$

$$\approx 2K \left\{ \lim_{\substack{a\to 0 \\ b\to +\infty}} \left[\ln\frac{b}{a} \right] + \lim_{b\to +\infty} \frac{1}{2(1-\rho^2)} \ln\left[\rho^{2\rho^2} (b^2)^{\rho^2-1} \right] \right\}$$

$$= 2K \left\{ \lim_{\substack{a\to 0 \\ b\to +\infty}} \frac{1}{(1-\rho^2)} \ln\left[\frac{\rho^{\rho^2}\, b^{\rho^2-1}\, b^{1-\rho^2}}{a^{1-\rho^2}} \right] \right\}$$

$$\approx 2K \left\{ \lim_{a\to 0} \ln\frac{b^0}{a} + \frac{\rho^2}{1-\rho^2} \ln(\rho) \right\} \quad (C.37)$$

Equation (C.37) is identified with the ideal low-pass filtered voltage noise, hence eq. (C.31), and yields

$$\lim_{a\to 0} \ln\frac{b^0}{a} + \frac{\rho^2}{(1-\rho^2)} \ln(\rho) = \lim_{c\to 0} \ln\frac{\Delta f_{1lf_c}}{c}$$

$$\Delta f_{1lf} \overset{\rho=\frac{f_c}{f_{c2}}}{=} f_c \left\{ \frac{f_c}{f_{c2}} \right\}^{\frac{\rho^2}{1-\rho^2}} \overset{\rho < 1}{\approx} f_c \quad (C.38)$$

which means that the "equivalent $1/f$ noise bandwidth" $\Delta f_{1/f}$ can be approximated by the cut frequency f_c while the poles are real under the condition that:

$$\frac{\rho^2}{1-\rho^2} = \frac{f_c^2}{f_{c2}^2 \cdot f_c^2} \quad \overset{f_c^2 < f_{c2}^2}{\Rightarrow} \quad 0 \qquad (C.39)$$

C.3.3 SECOND ORDER LOW-PASS WITH IDENTICAL POLES

While the poles are identical, hence $\rho=1$, the "equivalent $1/f$ noise bandwidth" is found to be:

$$\Delta f_{1/f} = f_c \frac{1}{\sqrt{e}} \qquad (C.40)$$

with : $ln \sqrt{e} = 0.5$

C.4 APPROXIMATION OF THE SUM $\displaystyle\sum_{\substack{n=-N \\ n\neq 0}}^{+N} \frac{1}{f-nf_s}$

The following sum must be evaluated for $f < f_s$.:

$$\sum_{\substack{n=-N \\ n\neq 0}}^{+N} \frac{1}{f-nf_s} = \frac{1}{f_s} \sum_{\substack{n=-N \\ n\neq 0}}^{+N} \frac{1}{x-n} = T_s \left\{ \sum_{n=1}^{+N} \frac{1}{x+n} + \sum_{n=1}^{+N} \frac{1}{x-n} \right\} \qquad (C.41)$$

where $x = \dfrac{f}{f_s}$.

According to [GRA65] p.2 equ.(0.131) the following approximation is valid while $N \to \infty$

$$\sum_{m=1}^{+N} \frac{1}{m} \overset{N \to +\infty}{\approx} K_{Eul} + ln N \qquad (C.42)$$

with K_{Eul} being the Euler's constant and equal to $0.57721566...$
Eq. (C.43) can be written as

$$T_s \sum_{m=1+x}^{N+x} \frac{1}{m} + T_s \sum_{m=x-1}^{x-N} \frac{1}{m} \approx T_s \left\{ 2K_{Eul} + ln \left(\frac{N-x}{1-x} \frac{N+x}{1+x} \right) \right\} \quad \text{(C.43)}$$

Eq. (C.45) can be approximated in the baseband, hence for $x \ll 1$, by:

$$T_s \left\{ 2K_{Eul} + ln \left(\frac{N^2-x^2}{1-x^2} \right) \right\} \approx 2T_s \left\{ K_{Eul} + ln \, N \right\} \quad \text{(C.44)}$$

This result can also be illustrated by the approach proposed by [ENZ89] in appendix 2. The discrete serie is approched by a continuous function and the summation replaced by an integration. This conversion introduces an error, which is partially compensated by shifting the function by one half to the right. A more accurate way is to introduce K_{Eul} instead (see also the next paragraph).

$$\sum_{m=1}^{N} \frac{1}{m} \overset{N->+\infty}{\approx} K_{Eul} + \int_{x=1}^{+N} \frac{dx}{x} \approx K_{Eul} + ln \, N \quad \text{(C.45)}$$

where $x = m - \frac{1}{2}$.

C.5 1/F FOLDOVER NOISE IN THE BASEBAND FOR A FIRST ORDER LOW-PASS FILTER

Equation (4.78) given by [ENZ89] is an approximation of the infinite sum $\sum_{m=1}^{+\infty} \frac{1}{m}$. The approximation becomes more precise, the more terms are added separately, because of the high value of the slope for the first terms. The higher the lower limit is chosen the more the approximated value

. approaches K_{Eul} as is shown in this paragraph. The expression in eq. (4.78) is found by approximating the discrete function by a continuous function, which is shifted by one half to the right, and by replacing the summation by an integration.

The parenthesis of eq. (4.78) can be written as follows:

$$\left\{ 1 + ln\frac{2f_c}{3f_s} \right\} = \left\{ 1 + ln\frac{2}{3} + ln\frac{f_c}{f_s} \right\} = \left\{ K_m + ln\frac{f_c}{f_s} \right\} \tag{C.46}$$

where K_m is the constant term which depends on the lower limit m. Comparing both approaches reduces now to a comparison of K_{Eul} to K_m.

The higher the lower limit m is chosen, the more K_m tends towards K_{Eul}. Therefore the approximation of eq. (4.77) is a better approximation for the foldover terms of the 1/f noise. Note that eq. (4.77) remains valid for a second order low-pass filter with real poles as is shown in §C.3. For a second order low-pass filter with identical poles the constant term in the parenthesis is reduced by $ln\{\sqrt{e}\} = 0.5$.

In Table C.1 the values of K_m are compared to K_{Eul} as a function of the lower limit m.

Lower limit m	1	2	3	4
$K_m =$	$1 + ln\frac{2}{3}$ $= 0.5945$	$1 + \frac{1}{2} + ln\frac{2}{5}$ $= 0.5837$	$1 + \frac{1}{2} + \frac{1}{3} + ln\frac{2}{7}$ $= 0.5806$	$1 + \frac{1}{2} + \frac{1}{3} + \frac{1}{4} + ln\frac{2}{9}$ $= 0.5793$
$(K_m - K_{Eul}) \ 10^{-3}$	17.319	6.494	3.355	2.04

Table C1:   Comparison of K_m and $K_{Eul} = 0.5772166...$

APPENDIX D

CHARGE INJECTION ANALYSIS

D.1 GENERAL CONSIDERATIONS

Most modern analog MOS circuits include an elementary sample-and-hold circuit that combines a sampling switch, implemented by at least one transistor, with a holding capacitor. The major limitation to the accuracy of this circuit is the disturbance of the sampled voltage when the transistor is turned off. One cause is noise, which results in random sequences of small perturbations and which has been analyzed §§ 4.3. The other is charge injection due to carriers released from the channel and to coupling through gate-to-diffusion overlap capacitances.
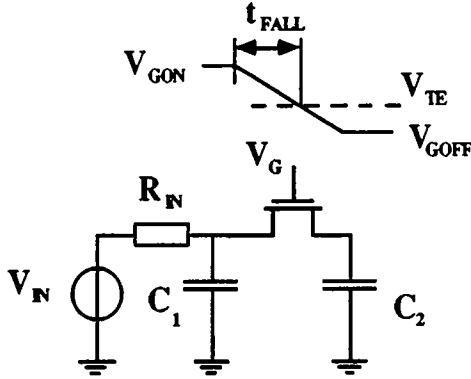
Figure C.1:   Circuit used for charge injection analysis

The analysis assumes a symmetrical transistor and a linear variation of the gate voltage V_G (with respect to the bulk) between *ON* and *OFF* values V_{GON} and V_{GOFF} as shows Fig. D.1 for a n-channel transistor..

The effective gate threshold voltage V_{TE} will be assumed to depend linearly on the input voltage V_{IN}, according to:

$$V_{TE} = V_{T0} + n_0 V_{IN} \tag{D.1}$$

The constant slope is assumed during switching off:

$$a = \frac{V_{GON} - V_{TE}}{t_{FALL}} \tag{D.2}$$

where t_{FALL} is the time needed for the gate voltage to reach the effective threshold voltage V_{TE}. Further assumptions are equilibrium of the terminal voltages before switching off and

$$t_{FALL} \ll R_{IN} C_1 \tag{D.3}$$

which allows one to neglect the effect of the signal source during switching off, or in other words, all the channel charge is distributed among both terminal capacitors and no charge is lost to the source.

Other important values are the total gate capacitance C_G, which includes both overlap capacitances C_{ov}, and the total charge Q_{tot} released at switching off

$$Q_{tot} = C_G \, (V_{GON} - V_{TE}) \tag{D.4}$$

This charge increases if the transistor is widened to reduce the transfer time constant. It can be pointed out that this charge is a linear function of V_{TE}, thus a linear function of V_{IN}, as far as eq. (D.1) is valid. It results in a linear dependence of charge injection with V_{IN}, which has been confirmed experimentally [WIL85].

The longest time needed by mobile charges to reach one end of the channel is proportional to [TUR86], [KUO86].

$$T_0 = \frac{n L^2}{\mu(V_{GON} - V_{TE})} \tag{D.5}$$

By switching off the transistor the mobile charges of the inversion charge layer are shared between drain, source and substrate and change the value of the voltage across the capacitors. The fraction of charge ΔQ_2 of the total channel charge released onto the holding capacitor C_2 causes an error voltage of:

$$\Delta V_2 = \frac{\Delta Q_2}{C_2} \tag{D.6}$$

This error voltage limits the accuracy of high performance analog CMOS circuits as they need large transistors (which entails a high channel charge) and small capacitors to reduce the transfer time constant.

The prediction of the error voltage ΔV_2 in the general case of Fig. D.1 is based on the following qualitative physical description of the charge injection phenomenon in the MOS transistor.

A rapid variation of the gate voltage causes a variation of the surface potential as the amount of mobile charges cannot change instantaneously. The surface potential induces an immediate variation of the depletion width, which compensates the excessive charge. Equilibrium corresponding to the new gate voltage is reached by the subsequent charge flow to drain and source. A fraction of the charge in the channel escapes to

the substrate leading to charge pumping [BRU69], [DEC74], [HEI65] which is due to trapping at the interface and to recombination in the channel and into the substrate.

The part of the channel charge which flows to the substrate reduces the total charge on the terminal capacitors, and therefore its proportion has to be evaluated.

D.2 CHARGES LEAKING TO THE SUBSTRATE

Measurements of the collected charge at drain and source as a function of the gate off voltage V_{GOFF} and the fall time t_{FALL} (Fig. D.2) have been realized.
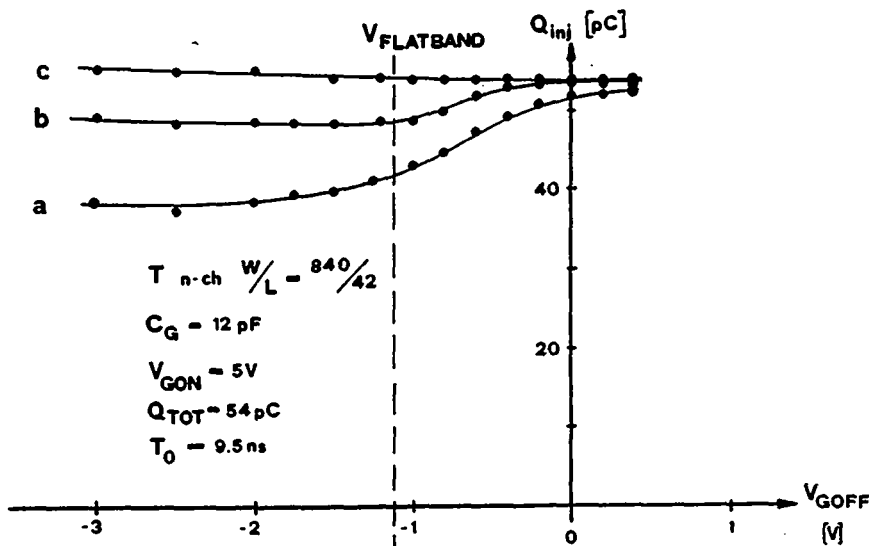

Figure D.2:   Measured total charge injected at drain and source as a function of gate off voltage V_{GOFF} (n-channel device, $\frac{W}{L} = \frac{840}{42}$, C_G = 12pF, V_{GON} = 5V, V_{TE} = 0.5V, Q_{tot} = 54pC, T_0 = 9.5ns).

Different fall times t_{FALL} are considered:

(a) $\frac{t_{FALL}}{T_0} = 0.63$,   (b) $\frac{t_{FALL}}{T_0} = 2.4$ (c) $\frac{t_{FALL}}{T_0} = 42$

Measurements for $\dfrac{T_0}{t_{FALL}}$ larger than 1 were obtained with the help of long transistors, which corresponds to situation of a short fall time. At long fall times (the switch-off time is longer than the channel transit time) nearly all the channel charge of the transistor is collected by drain or source and even a low voltage V_{GOFF} does not change the amount of injected charge. The inversion charge layer can follow the gate voltage variation. When the gate voltage V_G reaches V_{TE} most of the channel charge has already been injected and the total injected charge Q_{inj} at drain and source does not vary with V_{GOFF}.

At short fall times an increase of the charges flowing into the substrate is observed while V_{GOFF} decreases until the flatband voltage V_{FB} is reached. These charges going to the substrate reduce the total amount of injected charge at drain and source.
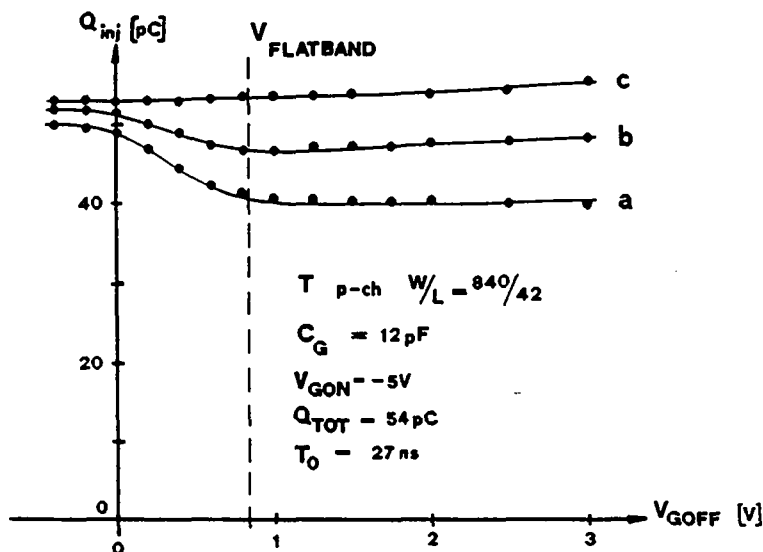

Figure D.3: Measured total charge injected at drain and source as a function of gate off voltage V_{GOFF} (p-channel device, $\dfrac{W}{L} = \dfrac{840}{42}$, $C_G = 12\text{pF}$, $V_{GON} = 5\text{V}$, $V_{TE} = -0.45\text{V}$, $Q_{tot} = 54\text{pC}$, $T_0 = 27\text{ns}$).

Different fall times t_{FALL} are considered:

(a) $\dfrac{t_{FALL}}{T_0} = 0.22$ (b) $\dfrac{t_{FALL}}{T_0} = 0.85$ (c) $\dfrac{t_{FALL}}{T_0} = 15$

Beyond V_{FB}, charge injection remains constant. The physical explanation is that most of the channel charge has not yet flown back to drain and source when the gate voltage V_G reaches V_{TE}. If V_G is reduced further, most of the mobile charges will be prevented from escaping to the substrate by the surface potential barrier. This barrier is progressively lowered when V_{GOFF} is reduced, which explains why an increasing proportion of the channel charge escapes to the substrate. Therefore Q_{inj} is progressively reduced and saturation is reached when V_{GOFF} is approximately equal to the flatband voltage V_{FB}, which eliminates the barrier.

Figure D.3 shows an equivalent situation for a p-channel transistor.

Summarizing, if the fall time is longer than the channel transit time and the gate off voltage V_{GOFF} just slightly smaller then the threshold voltage V_{TE}, than the substrate current is negligible. In the practical case of short transistors, as used for pass-transistors, which have a very short channel transit time T_0, one can assume that the charges lost through the substrate can be neglected.

D.3 MODELS

D.3.1 GENERAL MODEL

The flow of mobile charges in the channel can be expressed using the continuity equation [SZE81]:

$$\frac{\partial n(x,y,t)}{\partial t} = \frac{1}{q} div \, J(x,y)) + G - U \tag{D.7}$$

where $J(x,y)$ stands for the current density, q for the elementary charge, $n(x,y,t)$ for the carrier density and y refers to the axis along the channel and x to the one perpendicular to it, into the substrate. G and U stand for the generation and recombination rate respectively.

Because the charge leaking to the substrate due to mobile carriers can be neglected, it can be assumed that the current density $J(x,y)$ depends only on y and that $(U-G) = 0$. Using the simple linear expression between the induced channel charge density Q_{si} and the quasi Fermi level Φ_n of the mobile charges

$$Q_{si} = C'_{ox} \, (V_G - V_{T0} - n_0 \Phi_n) \qquad (D.8)$$

where C'_{ox} is the gate oxide capacitance per unit area. Introducing the relation between the quasi Fermi level and the current density $J(y,t)$ one can transform the continuity equation (D.7) into (D.9)

$$\frac{\partial}{\partial t} Q_{si}(y,t) = \frac{\mu}{n_0 C_{ox}} \frac{\partial}{\partial y} \left[Q_{si}(y,t) \frac{\partial}{\partial y} Q_{si}(y,t) \right] \qquad (D.9)$$

where : $\qquad Q_{si}(y,t) = - \int q n(x,y,t) dx$

$Q_{si}(y,t)$ is a unknown function of t and y only which we have to calculate. The boundary conditions may be expressed if the terminating impedances on the drain and source side are specified. Using the sample-and-hold circuit of Fig. D.1 they can be expressed as follows (assuming that C_{ov} is equal to zero):
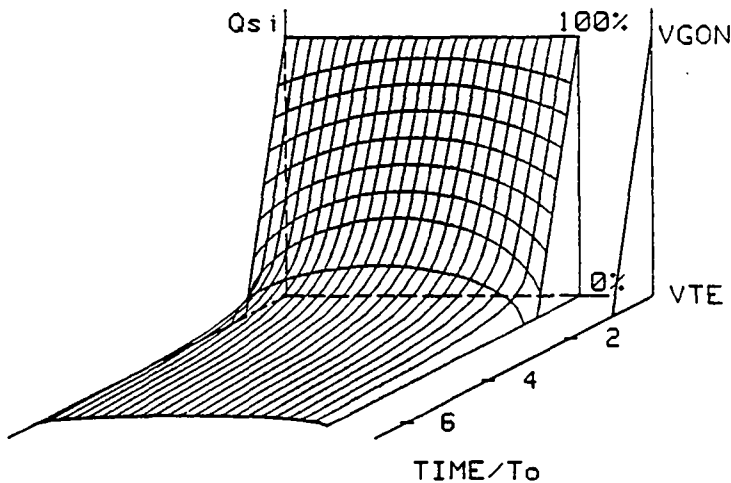

Figure D.4:   Evolution of minority carrier density along the channel as a function of time and position. $\frac{t_{FALL}}{T_0} = 1$, $C_2 = 10 \, C_1 = 100 \, C_G$
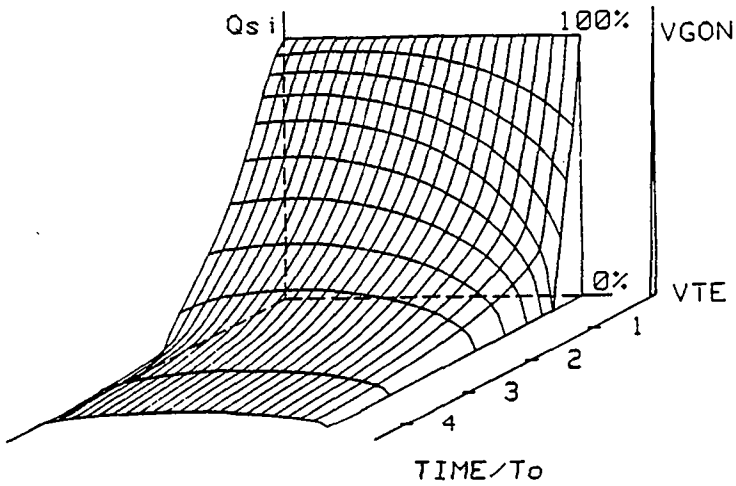
Figure D.5: Evolution of minority carrier density $Q_{si}(y,t)$ along the channel as function of time t and position y. $\frac{t_{FALL}}{T_0} = 0.1$, $C_G = 10\,C_2 = 100\,C_1$

$$-\frac{\mu W_{ef}}{n_0 C_G} Q_{si}\,(y,t)\,\frac{\partial}{\partial y}\,Q_{si}\,(y,t)\bigg/_{source} = C_1\frac{dV_1}{dt} \qquad (D.10)$$

$$+\frac{\mu W_{ef}}{n_0 C_G} Q_{si}\,(y,t)\,\frac{\partial}{\partial y}\,Q_{si}\,(y,t)\bigg/_{drain} = C_2\frac{dV_2}{dt} \qquad (D.11)$$

The nonlinear and non-stationary differential eq. (D.9) may be solved numerically using the finite element method coupled with a simple Runge-Kutta method [RAH84].

From the numerical solution $Q_{si}(y,t)$ one can find the variation of the quasi Fermi level along the channel using eq. (D.8) and derive the charge injection values at drain and source by integrating (D.10)&(D.11).
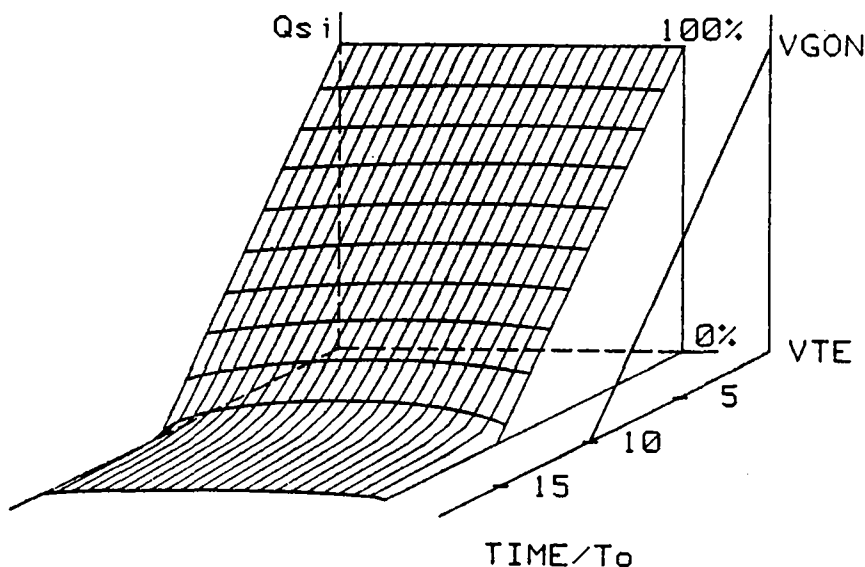
Fig. D.6:   Evolution of minority carrier density $Q_{si}(y,t)$ along the channel as function

of time t and position y. $\frac{t_{FALL}}{T_0} = 10$, $C_2 = 10\,C_1 = 100\,C_G$.

The evolution of the mobile charge density $Q_{si}(y,t)$ along the channel (y-axis) as a function of time and position is shown in the Figs. D.4, D.5 & D.6. At short fall times (Fig. D.4) the mobile charges follow a curved profile with a higher conductance in the center of the channel than at both extremities, because those in the center do not have enough time to flow to drain or source. The resulting electric field in the channel pushes the carriers to each side. As soon as pinch-off is reached at both ends the terminal impedances have no influence anymore. If this occurs early enough half the total channel charge is collected by source and by drain.

A non-symmetrical electric field along the channel (Fig. D.5) may only be obtained with a very short fall time and with a value of C_1 or C_2 much smaller than the gate capacitance C_G. However, it does not correspond to any practical case. Long fall times will be considered in the following section.

D.3.2 SIMPLIFIED MODEL (ELECTRICAL MODEL)

Figure D.6 shows that for long fall times with

$$T_{FALL} \gg T_0 \tag{D.12}$$

and large enough capacitor values

$$C_1 \text{ and } C_2 \gg C_G \tag{D.13}$$

the profile is homogeneous all along the channel. The channel on-conductance can therefore be represented, while V_G is higher than V_{TE}, as a time variable conductance $g[V_G(t)]$

$$g[V_G(t)] = \beta \left\{ V_G(t) - V_{TE} \right\} = \beta \left\{ V_{GON} - at - V_{TE} \right\} \tag{D.14}$$

For a gate voltage lower than V_{TE} the channel conductance is assumed to be equal to zero, which means that weak inversion effects are neglected.

Thus, the transistor can be represented as a time variable conductance $g[V_G(t)]$ associated with the distributed gate oxide capacitance and the two overlap capacitances C_{ov}, as shown in Fig. D.6 [VIT82], [VIT85]. Drain and diffusion capacitances are included in C_1 and C_2.
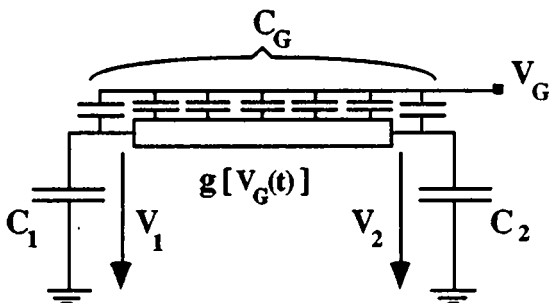

Figure D.7:   Model of the charge injection analysis where substrate currents are assumed to be negligible
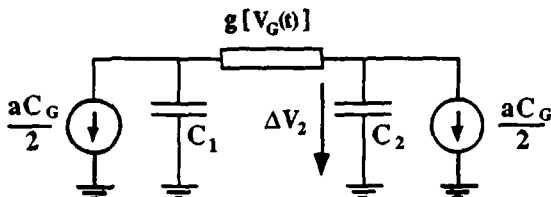
$$g\,[\,V_G(t)\,]$$

Figure D.8:   Final simplified model for charge injection analysis

If conditions (D.12)&(D.13) are satisfied the variation with time of the surface potential at any point of the channel is negligible with respect to that of the gate. Thus the linear decrease of V_G with a slope a across the distributed gate capacitance C_G is equivalent to a constant current source of total value aC_G flowing symmetrically to both ends. This leads to the final model of Fig. D.8.

Resolving this circuit yields the following normalized differential equation:

$$\frac{dV}{dT} = (T - B)\left[\left(1 + \frac{C_2}{C_1}V + 2\,T\frac{C_2}{C_1}\right] - 1\right.$$ (D.15)

where the normalized factors are [VIT85]:

$$V = \frac{\Delta V_2}{\frac{C_G}{2}\sqrt{\frac{a}{\beta C_2}}}$$ (D.16)

$$T = \frac{t}{\sqrt{\frac{C_2}{a\beta}}}$$ (D.17)

$$B = (V_{GON} - V_{TE})\sqrt{\frac{\beta}{aC_2}}$$ (D.18)

The numerical solution for different values of the capacitor ratio $\frac{C_2}{C_1}$ by integrating eq. (D.15) during the switch-off time $(0<T<B)$ leads to the diagram of Fig. D.10 representing the charge injection ratio $\frac{\Delta Q_2}{Q_{tot}}$ as a

function of the characteristic switching parameter B [VIT85]. This diagram shows that for small values of B, equipartition of charge is obtained independently of capacitance ratio $\frac{C_2}{C_1}$. For large values of B, which are reached if the fall time is very long, voltage equilibrium is approached asymptotically, which yields to a charge distribution proportional to $\frac{C_2}{C_1}$. For intermediate cases, corresponding to most realistic situations, the charge distribution strongly depends on the switching parameter B.

$$B = (V_{GON} - V_{TE}) \sqrt{\frac{\beta}{aC_2}}$$
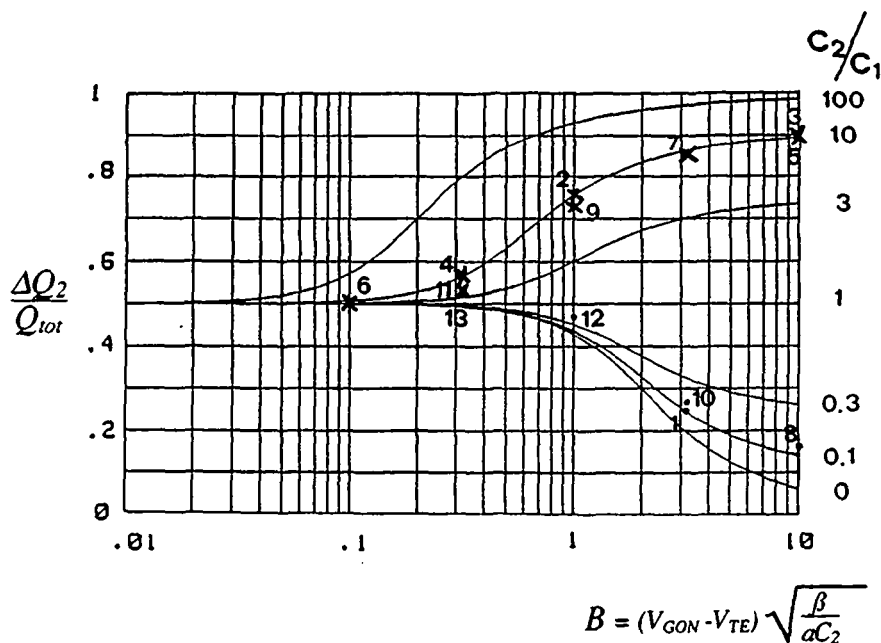
Figure D.9: Normalized diagram showing the amount of charge ΔQ_2 injected in C_2 as a function of switching parameter B and capacitance ratio $\frac{C_2}{C_1}$ [VIT85].

Various points calculated from the numerical model for marginal situations (see Table D.1) are reported for $\frac{C_2}{C_1} = 10$ (X) and $\frac{C_2}{C_1} = 0.1$ (O). None of the points showing visible discrepancy (7-13) corresponds to a realistic case.

The effect of non-symmetrical overlap capacitances has to be taken into account as for short transistors (as used for pass-transistors) their difference ΔC_{ov} can be an important fraction of the total gate capacitance.

Therefore the two symmetrical current sources of a value of $\frac{aC_G}{2}$ on each side (Fig. D.7) have to be replaced by one of a value of $\frac{a(C_G+C_{ov})}{2}$ and by one of $\frac{a(C_G-C_{ov})}{2}$.

Assuming that the charge redistribution is not affected by a small variation of B, a first order correction can be obtained by adding the charge difference due to the asymmetrical overlap capacitances leading to eq. (D.19).

$$\Delta V_{2asym} = \Delta V_2 (1 \pm \frac{\Delta C_{ov}}{C_G}) \qquad (D.19)$$

where the positive sign corresponds to the case of larger overlap capacitance on side of capacitor C_2.

No.	$\frac{t_{FALL}}{T_0}$	$\frac{C_2}{C_G}$	$\frac{C_2}{C_1}$	Comments
1	100	10	0.1	
2	100	100	10	
3	100	1	10	
4	10	100	10	Fig. D.6
5	10	0.1	10	
6	1	100	10	Fig. D.4
7	1	0.1	10	
8	1	0.01	0.1	
9	0.1	0.1	10	Fig. D.5
10	0.1	0.01	0.1	
11	0.01	0.1	10	
12	0.01	0.01	0.1	
13	0.001	0.1	0.1	

Table D.1:   Various points calculated for different values of $\frac{C_2}{C_G}$ and $\frac{t_{FALL}}{T_0}$ in the case of $\frac{C_2}{C_1} = 10$ and $\frac{C_2}{C_1} = 0.1$

In summary, the parameters of this simplified model are the gate voltage V_{GON}, the effective threshold voltage V_{TE} (which includes the effect of the substrate modulation according to eq. (D.1), the slope a of the gate voltage, the value of the capacitor C_2, the ratio $\frac{C_2}{C_1}$, the transfer parameter β of the transistor and the difference of the overlap capacitances ΔC_{ov}.

To check the importance of conditions (D.12)&(D.13) for the validity of this simplified model, various points corresponding to various values of $\frac{T_{FALL}}{T_0}$ and $\frac{C_2}{C_G}$ were calculated numerically with eq. (D.9),(D.10)&(D.11).
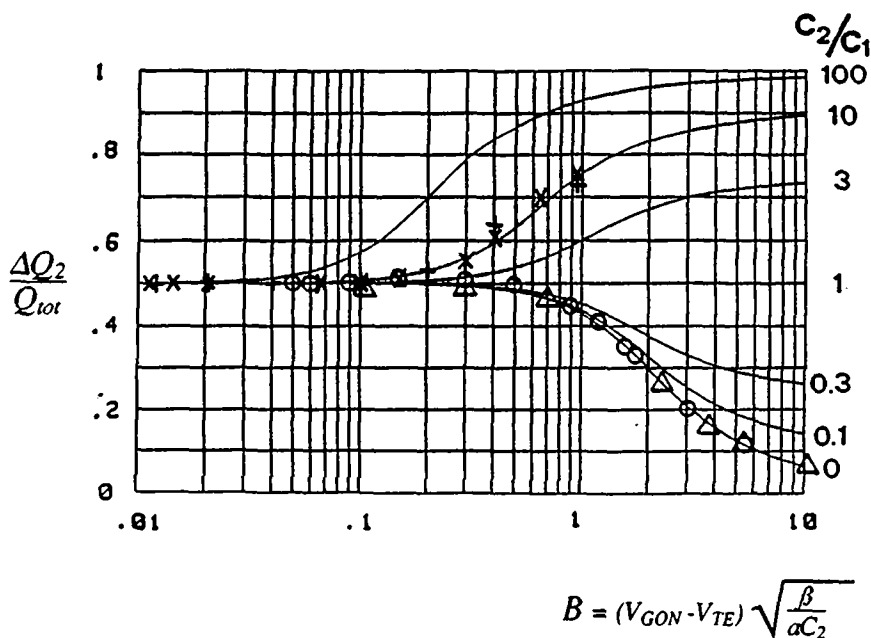

$$ B = (V_{GON} - V_{TE}) \sqrt{\frac{\beta}{aC_2}} $$

Figure D.10:   Measured injections ΔQ_2 in C_2 for symmetrical transistors.

(1) n-channel $\frac{W}{L}$ =10000/22 , C_G = 79pF, V_{TE} = 0.5V, $\frac{C_2}{C_1}$ = 0, C_2 = 39.3nF. V_{GON} = 2V (O); V_{GON} = 3.5V (Δ).

(2) p-channel $\frac{W}{L}$ = 840/42 , C_G = 12pF, V_{TE} = -0.45V, $\frac{C_2}{C_1}$ = 10, C_2 = 27.3nF and C_1 = 2.9nF, V_{GON} = -5V (X,+)

The slope a is the independent variable

Some of these points are given in table D1 and reported in the diagram of figure D.9. It can be seen that the correspondence is perfect for all points satisfying eq. (D.12)&(D.13) (only points 1, 2, 4 of this category have been reported for the sake of clarity). Even when the conditions are only marginally fulfilled (points 3,5,6,7), results still agree within a few percent. All the points for which a large discrepancy is observed correspond to non-realistic situations.

At short fall times the channel is quickly pinched off and is no longer homogeneous as assumed in the simplified model. However, the fact that the channel conductance is not uniform does not influence the equal sharing of the channel charge to drain and source predicted by the model for small values of B, but only the time needed to evacuate all the mobile charges from the device.

D.4 EXPERIMENTAL RESULTS

The experimental verification was carried out by measuring the circuit of Fig. D.1. To increase the accuracy of the measurements and to reduce noise, a guard box, large transistors and load capacitors were used. Each measurement point is the mean value of over 200 samples which reduces the effect of added noise, specially for low injections.

All device parameters were individually measured. Care was taken to respect the conditions discussed § D.2 for negligible charge flow to the substrate. Calibration of the total channel charge was obtained for each measurement by connecting the drain to the source. The precision of the measurements is estimated to be within a few percent in the worst cases.

The influence of all the parameters mentioned before has been separately tested. In Fig. D.10 the experimental results for a n-channel ($\frac{W}{L}$ =10000/22 and a ratio $\frac{C_2}{C_1}$ = 0) and for a p-channel ($\frac{W}{L}$ = 840/42 and $\frac{C_2}{C_1}$ =10) are reported.

Fig. D.11 shows the experimental results for a ratio $\frac{C_2}{C_1}$ =0 and a p-channel transistor $\frac{W}{L}$ = 1000/10 having a large asymmetry of overlap capacitances ($\frac{\Delta C_{ov}}{C_G}$ = ± 0.17). After correcting by eq. (D.19) a good

agreement is obtained with the theoretical curve, which demonstrates the
validity of this equation.

Several other measurements have been carried out by using other
transistors and other capacitances. Where it was possible the experiments
were made with p- and n-channel transistors of the same dimensions.
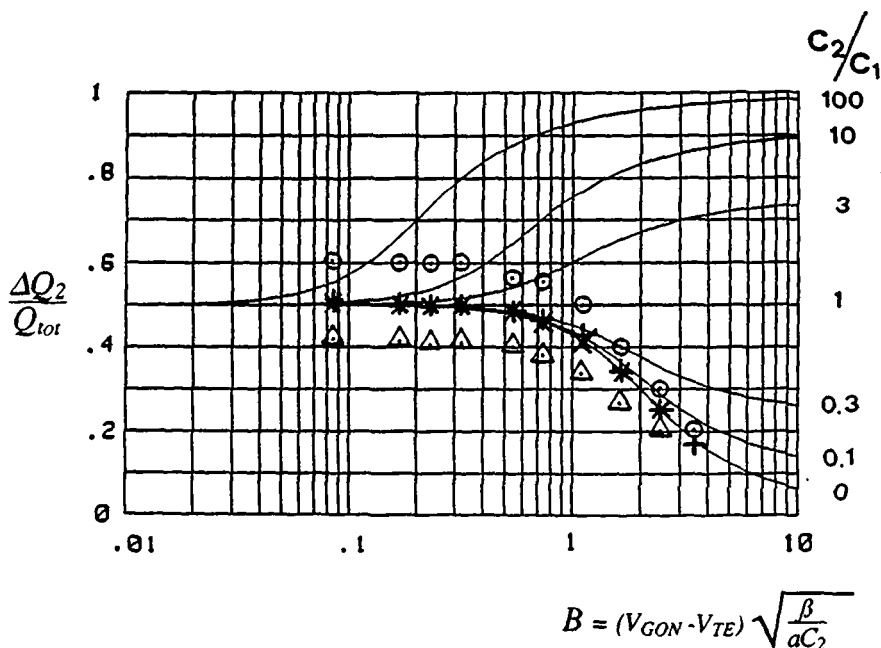All results show a good correlation with the theoretical curves.

$$B = (V_{GON} - V_{TE}) \sqrt{\frac{\beta}{aC_2}}$$

Figure D.11:   Measured injections ΔQ_2 in C_2 for asymmetrical overlap capacitances

$\frac{\Delta C_{ov}}{C_G} = \pm\, 0.17$ for a p-channel device: $\frac{W}{L} = 1000/10$, $V_{GON} = -5V$, $V_{TE} = -0.45V$, $\frac{C_2}{C_1} = 0$, $C_G = 6pF$, $C_2 = 2.9nF$.

C_{ov} larger on C_2 side: measured (O); after correction with eq. (D.19) (+);
C_{ov} smaller on C_2 side: measured (Δ); after correction with eq. (D.19) (X);
The slope a is the independent variable

D.5 CONCLUSIONS

Charge injection has been approached using numerical modeling to support a simplified model, which allows designers to predict the amount of charge injection as a function of different parameters. It has been shown theoretically and experimentally that this model remains valid in any practical situation, as long as the amount of charge leaking to the substrate is negligible. For short fall times ($T_{FALL} \ll T_0$) this must be ensured by avoiding gate off voltage values that are much lower than threshold V_{TE}. Experimental results obtained by varying the different parameters agreed with the injections obtained by the models. The simplified model, concentrates all the relevant parameters in an injection diagram (Fig. D.9) and allows one to predict quickly the amount of charge injection in order to decide on a possible strategy.

A first strategy is to choose C_1 much larger than C_2 (very low impedance of the signal source) and the switching parameter B much larger than 1, so that all the charges released into C_2 flow back into C_1 during the decay of the gate voltage and ΔQ_2 tends to zero (some easily calculable additional charge is due to the coupling through overlap capacitances after switching off). The drawback is the long time needed for switching off.

A second possibility is to balance the values of both capacitors [BIE80]. By symmetry, half the channel charge flows in each capacitor and can be compensated by half-sized dummy switches that are switched on when the main switch is blocked [SUA75].

A third solution eliminates the need for equal capacitor values by choosing a value of B much smaller than 1, which also ensures equipartition of the total charge. Charge compensation can be achieved using a single half-sized dummy switch.

If the switch is implemented with a pair of complementary transistors controlled by complementary clock signals, the two types of charge released may partially compensate each other. This kind of compensation is not very efficient since it depends on the input voltage V_{IN} and since no real matching exists between p and n channel transistors. In addition, the residual charge injection can be shown to depend on the timing and skew of the two complementary clocks, which may translate jitter into amplitude

noise [VAN86]. A good procedure is therefore to turn off completely the first transistor before switching off the second. The problem can then easily be reduced to that of a single switch.

In any case the unavoidable mismatch and the uncertainty of the parameters limits the achievable compensation of charge injection. To ensure the best possible compensation, the dummy switches must have the same configuration and be as close as possible to the main switch.

Such carefully implemented compensation can reduce charge injection by one, maybe two orders of magnitude. Further improvements require special circuit techniques, such as full differential implementation and active compensation by low sensitivity auxiliary input [ALL82], [VIT85], [DEG85].

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