Section 19. Voltage Reference

HIGHLIGHTS

This section of the manual contains the following major topics:

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Voltage Reference

PICmicro MID-RANGE MCU FAMILY

19.1 Introduction

The Voltage Reference module is typically used in conjunction with the Comparator module. The comparator module's inputs do not require very large drive, and therefore the drive capability of the Voltage Reference is limited.

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of V_{REF} values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Figure 19-1. The block diagram is given in Figure 19-1. Within each range, the 16 steps are monotonic (i.e. each increasing code will result in an increasing output).

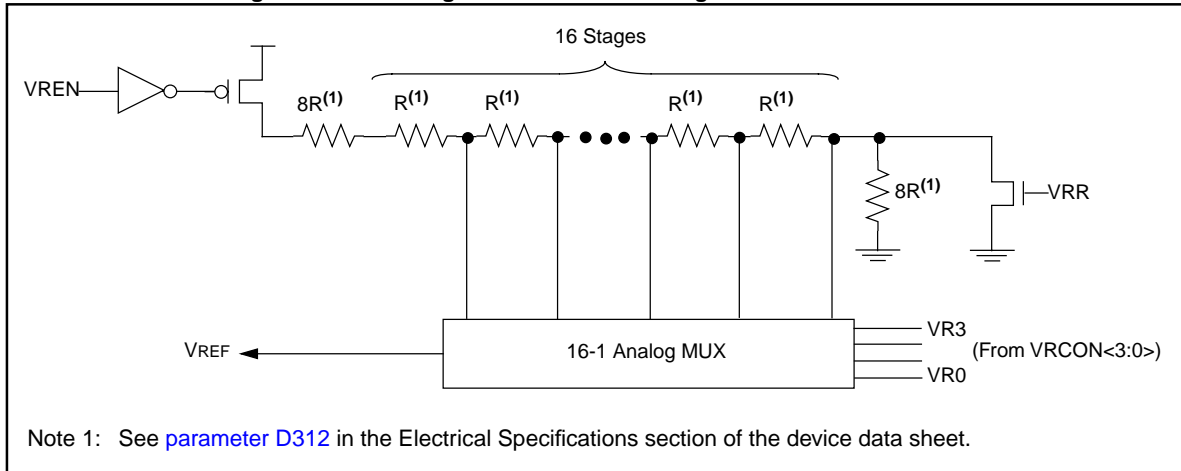**Figure 19-1: Voltage Reference Block Diagram**

Note 1: See parameter D312 in the Electrical Specifications section of the device data sheet.

Table 19-1: Typical Voltage Reference with V_{DD} = 5.0V

VR3:VR0	V_{REF}	
	VRR = 1	VRR = 0
0000	0.00 V	1.25 V
0001	0.21 V	1.41 V
0010	0.42 V	1.56 V
0011	0.63 V	1.72 V
0100	0.83 V	1.88 V
0101	1.04 V	2.03 V
0110	1.25 V	2.19 V
0111	1.46 V	2.34 V
1000	1.67 V	2.50 V
1001	1.88 V	2.66 V
1010	2.08 V	2.81 V
1011	2.29 V	2.97 V
1100	2.50 V	3.13 V
1101	2.71 V	3.28 V
1110	2.92 V	3.44 V
1111	3.13 V	3.59 V

19.2 Control Register

Register 19-1: VRCON Register

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0

bit 7   bit 0

bit 7   **VREN:** V_{REF} Enable

**VREN:** V_{REF} Enable
1 = V_{REF} circuit powered on
0 = V_{REF} circuit powered down

bit 6   **VROE:** V_{REF} Output Enable
1 = V_{REF} is internally connected to Comparator module's V_{REF}. This voltage level is also output on the V_{REF} pin
0 = V_{REF} is not connected to the comparator module. This voltage is disconnected from the V_{REF} pin

bit 5   **VRR:** V_{REF} Range selection
1 = 0V to 0.75 V_{DD}, with $V_{DD}/24$ step size
0 = 0.25 V_{DD} to 0.75 V_{DD}, with $V_{DD}/32$ step size

bit 4   **Unimplemented:** Read as '0'

bit 3:0   **VR3:VR0:** V_{REF} value selection $0 \leq VR3{:}VR0 \leq 15$

When VRR = 1:

$V_{REF} = (VR{<}3{:}0{>}/\ 24) \bullet V_{DD}$

When VRR = 0:

$V_{REF} = 1/4 * V_{DD} + (VR3{:}VR0/\ 32) \bullet V_{DD}$

Legend	
R = Readable bit	W = Writable bit
U = Unimplemented bit, read as '0'	- n = Value at POR reset

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19.3 Configuring the Voltage Reference

The Voltage Reference can output 16 distinct voltage levels for each range.

The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 1: V_{REF} = (VR3:VR0/24) x V_{DD}

if VRR = 0: V_{REF} = (V_{DD} x 1/4) + (VR3:VR0/32) x V_{DD}

The settling time of the Voltage Reference must be considered when changing the V_{REF} output. Example 19-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with V_{DD} = 5.0V.

Generally the V_{REF} and V_{DD} of the system will be known and you need to determine the value to load into VR3:VR0. Equation 19-1 shows how to calculate the VR3:VR0 value. There will be some error since VR3:VR0 can only be an integer, and the V_{REF} and V_{DD} levels must be chosen so that the result is not greater then 15.

Equation 19-1: Calculating VR3:VR0

When VRR = 1

$$VR3:VR0 = \frac{V_{REF}}{V_{DD}} \; X \; 24$$

When VRR = 0

$$VR3:VR0 = \frac{V_{REF} - V_{DD}/4}{V_{DD}} \; X \; 32$$

19.4   Voltage Reference Accuracy/Error

The full range of V_{SS} to V_{DD} cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 19-1) keep V_{REF} from approaching V_{SS} or V_{DD}. The Voltage Reference is V_{DD} derived and therefore, the V_{REF} output changes with fluctuations in V_{DD}. The absolute accuracy of the Voltage Reference can be found in the Device Data Sheets electrical specification parameter D311.

19.5   Operation During Sleep

When the device wakes up from sleep through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the Voltage Reference should be disabled.

19.6   Effects of a Reset

A device reset disables the Voltage Reference by clearing the VREN bit (VRCON<7>). This reset also disconnects the reference from the V_{REF} pin by clearing the VROE bit (VRCON<6>) and selects the high voltage range by clearing the VRR bit (VRCON<5>). The V_{REF} value select bits, VRCON<3:0>, are also cleared.
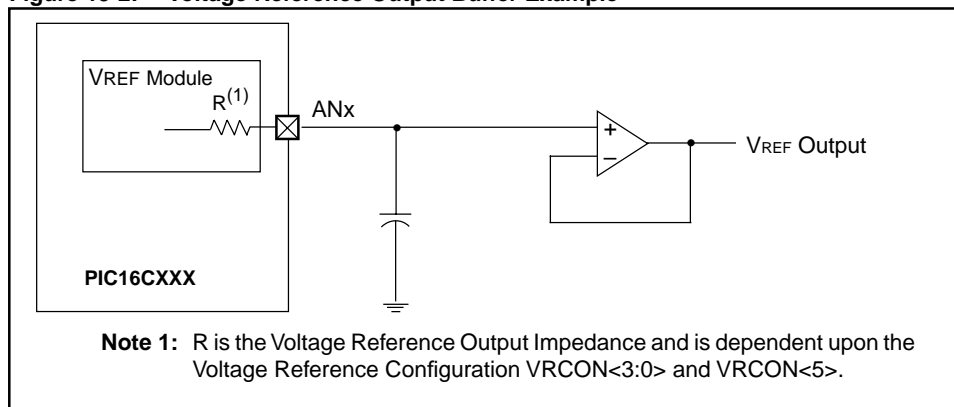
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19.7 Connection Considerations

The Voltage Reference Module operates independently of the comparator module. The output of the reference generator may be connected to the VREF pin if the corresponding TRIS bit is set and the VROE bit (VRCON<6>) is set. Enabling the Voltage Reference output onto the VREF pin with an input signal present will increase current consumption. Configuring the VREF as a digital output with VREF enabled will also increase current consumption.

The VREF pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the Voltage Reference output for external connections to VREF. Figure 19-2 shows an example buffering technique.

Figure 19-2: Voltage Reference Output Buffer Example

Note 1: R is the Voltage Reference Output Impedance and is dependent upon the Voltage Reference Configuration VRCON<3:0> and VRCON<5>.

19.8   Initialization

Example 19-1 shows the steps to configure the voltage reference module.

Example 19-1:   Voltage Reference Configuration

```
    MOVLW    0x02        ; 4 Inputs Muxed to 2 comparators
    MOVWF    CMCON       ;
    BSF      STATUS,RP0  ; go to Bank1
    MOVLW    0x07        ; RA3:RA0 are outputs
    MOVWF    TRISA       ; outputs
    MOVLW    0xA6        ; enable VREF
    MOVWF    VRCON       ; low range set VR3:VR0 = 6
    BCF      STATUS,RP0  ; go to Bank0
    CALL     DELAY10     ; 10 µs delay
```

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19.9   Design Tips

Question 1:   *My VREF is not what I expect.*

Answer 1:

Any variation of the device VDD will translate directly onto the VREF pin. Also ensure that you have correctly calculated (specified) the VDD divider which generates the VREF.

Question 2:   *I am connecting VREF into a low impedance circuit, and the VREF is not at the expected level.*

Answer 2:

The Voltage Reference module is not intended to drive large loads. A buffer must be used between the PICmicro's VREF pin and the load.

19.10   Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to Voltage Reference are:

Title   **Application Note #**

Resistance and Capacitance Meter using a PIC16C622   AN611

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19.11   Revision History

Revision A

This is the initial released revision of the Voltage Reference description.