Overview

Decoupling is a means to overcome physical and time constraints typically found in a Power Distribution System (PDS) of digital circuits. Decoupling reduces switching noise in a PDS. When transistors switch within the IC, current is drawn and a voltage drop across the PDS results in ripple noise. Decoupling capacitors act as a reservoir of energy located near the point of requirement. They deliver energy during switching periods with enough reserves to maintain required voltage levels.

Decoupling Design

As the decoupling capacitor takes the role as a power supply during spikes in device consumption, a voltage drop occurs across the cap's internal impedance. The voltage and current requirements of the IC dictates the maximum impedance of the decoupling capacitor in order to maintain power during the spikes. The target impedance (Ztarget) for the LOGIC Devices Video Memories is calculated as follows.

Ztarget = Allowed Ripple / Current
= (+/- % VCC max allowance) x (VCC nominal) / Ipeak

Approximate 3.3V power rail requirements:
Ipeak = 50mA/pad x 12pads = 600mA
Ztarget = (10%)(3.3) / 600mA = 0.55 ohm

Approximate 1.8V power rail requirements:
Ipeak = 1.25A
Ztarget = (10%)(1.8) / 1.25A = 0.14 ohm

Frequency Considerations

High frequency decoupling requires the capacitor model to include its Equivalent Series Model, which is a capacitor, inductor, and resistor in series. This is essentially a tuned band-stop passive filter with a frequency response. The circuit has a resonance frequency:

Fresonance = 1 / (2*pi*sqrt(L*C))

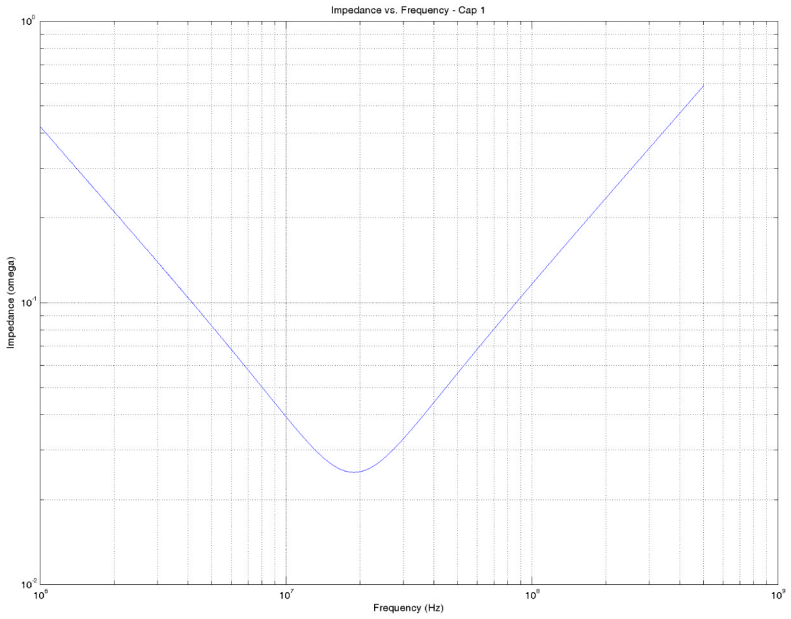
Real Non-Ideal Capacitors

Below are example impedance values for a "real" 1nF capacitor on a PCB:

```
C=47e-9;        % parasitic cap of cap
R=20e-3;        % equivalent series resistance of cap
Lself=2e-9;     %parasitic inductance of cap
Lmount=0.8e-9;  % parasitic inductance of PCB lands, traces, and VIAs
L = Lself + Lmount;
```

Resonant frequency for this example is roughly 14MHz as seen in the impedance profile below. Multiple caps in parallel are required to reduce the impedance to a desired target impedance (Ztarget) level. Adding capacitors in parallel simply lowers the impedance without shifting the impedance profile in terms of frequency response.

0.047nF Real Capacitor Impedance Profile



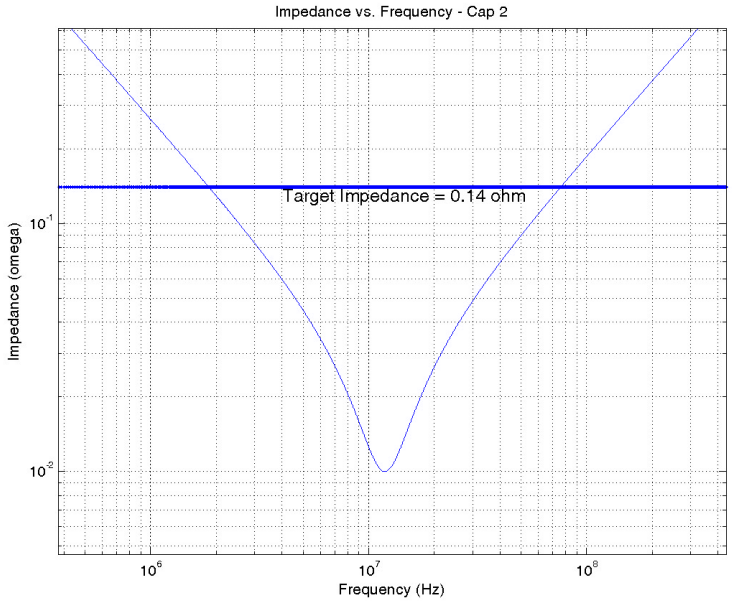
Decoupling Circuit Design

Each power plane's decoupling circuit should be tuned to attain less than target impedance over the frequency of the current spikes. Decoupling of narrow band of current spike frequencies can be handled by selecting a single decoupling capacitor value that provides target impedance over the narrow range of frequencies. Building decoupling that provides low impedance over a wide range of frequencies requires parallel combination of multiple capacitor values. Small values tend to have less of an impact on the impedance profile, so a greater number of smaller capacitors are needed to yield the same impact as a smaller number of larger capacitors. In order to keep the impedance profile smooth and free of anti-resonance spikes, a capacitor is generally needed at least in every decade of the capacitor value range. A good rule of thumb is to double the quantity of capacitors for every decade of decrease in value. For example: 7 x 2.2uF / 13 x 0.22uF / 26 x 0.022uF.

1.8V Core Power Plane

The peak current for the core 1.8V plane is driven primarily by memory accesses which occur between roughly 1/10th and 1/5th of the clock frequency. Most HD video applications run at a clock rate of 74.25MHz. The resonant frequency of the decoupling circuit could be placed at say 10MHz. The relatively narrow band impedance profile should remain below target impedance up to 74MHz. Parallel capacitors of a single value can be used for lowering the impedance to fit the target profile.

1.8V PDS Impedance Profile: 6 x 0.1uF

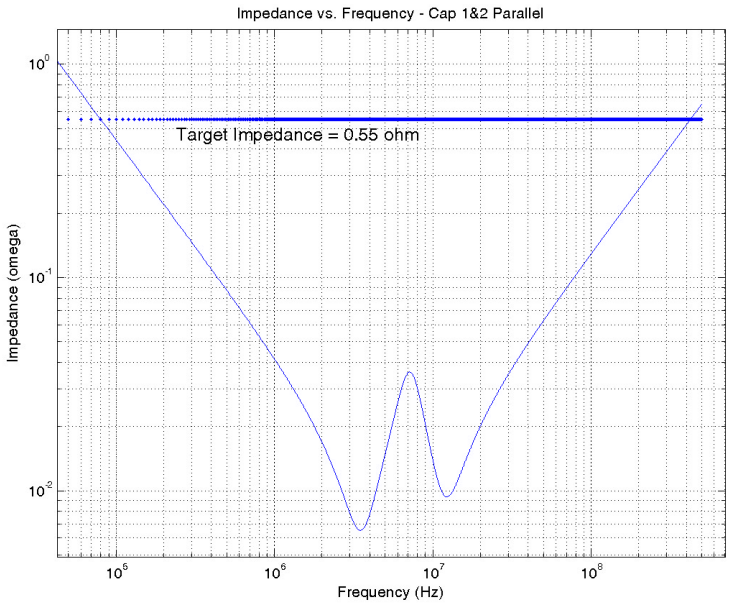


Quantity	Capacitive Values (uF)	Parasitic Inductance (nH)	Parasitic Resistance (ohm)
8	0.1	1.8	0.06

3.3V I/O Power Plane

Peak current for the I/O VCC is jointly dependent on clock frequency and data patterns. Decoupling for the I/O plane must span a broad range of frequencies. The I/O current peaks occur when the output data changes, which would be a maximum of ½ the clock frequency (37MHz). Taking the third harmonic into consideration, would need to attain the target impedance up to 111MHz.

1.8V PDS Impedance Profile: 3 x 1uF || 6 x 0.1uF



Quantity	Capacitive Values (uF)	Parasitic Inductance (nH)	Parasitic Resistance (ohm)
3	1	2.0	0.02
6	0.1	1.8	0.06

Recommendations

Minimum Number of Parallel Caps to Attain Target Impedance Levels:

3.3V I/O Power Rail (VCCI,VCCO):
3 x 1uF
6 x 0.1uF

1.8V Core Power Rail (VCCINT):
6 x 0.1uF

The following diagram is the reverse side view of a possible PCB layout. With 5 caps per side, we can accommodate up to 20 capacitors (10 x 0.1uF for the 1.8V rail -- 3 x 1uF || 7 x 0.1uF for the 3.3V rail). The closer the VCC cap connection is to the physical VCC pin, the better. Minimizing current loop is crucial for high frequency decoupling. Bringing vias closer together and reducing the height of the vias and capacitor are helpful. A rule of thumb for trace inductance is 10nH/in.

Suggested Arrangement of Capacitors on PCB (under side view)