Designing An Ultrasound Pulser with MD1812/MD1813 Composite Drivers

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Introduction

The MD1812 and the MD1813 are two unique composite return-to-zero (RTZ) pulser drivers for ultrasound applications. The ICs have built-in level shifters that provide negative P-MOS gate DC bias and fast AC coupled gate drive signals. They enable the fast damping functions necessary to generate return-to-zero bipolar pulses, and are also able to keep the zero-state to as long as needed, even to infinity. These kinds of fast return-to zero and DC coupled features are very useful for medical ultrasound imaging equipment, piezoelectric transducer drivers, material flaw detection, ultrasonic NDT detection, and sonar ranger applications, especially for those that need to launch ultrasound in pseudo-random codes.

Designing a Pulser with the MD1812/13

This application note describes how to use MD1812 or MD1813 to design the basic channel of an ultrasound transmitter with the RTZ feature. The circuit is a single channel ultrasound transmitter using the MD1812 or MD1813 to drive TC6320 & TC2320 MOSFETs. It can generate fast return to zero waveforms. The output of high voltage to transducer has ±2A source and sink current capability. A CPLD programmable logic circuit and on-board 40MHz crystal oscillator generate a fast logic signal to control the pulse circuit. The CPLD has a six-pin JTAG connection for Xilinx's USB or a convenient parallel-port programming link cable.

The circuit consists of one MD1812K6 or MD1813K6 in a 16-lead 4x4x0.9mm QFN package, driving TC6320FGs and TC2320FGs, two complementary high-voltage P and N-channel MOSFETs in one single SO-8 package. The input stage of the MD1812/13 is a high-speed level translator that is able to operate with logic input signals of 1.2V to 5.0V amplitude. In this circuit, the CPLD output logic is typically 3.3V. An adaptive threshold circuit is used with the OE pin inside of the MD1812 to set the level translator threshold to the middle of the input logic 0 and logic 1 levels. The OE pin serves a dual purpose. First, its logic 1 level is used to compute the threshold voltage level for the channel input level translators. Second, when OE is low, the outputs are disabled, with the A and C outputs high and the B and D outputs low (for MD1812 only). This assists in properly pre-charging the coupling capacitors that may be used in series in the gate drive circuit of external PMOS and NMOS FETs.

The MD1812/13 level translator uses a proprietary composite drive circuit, which provides DC coupling, together with high-speed operation. The output pin, OUT_C, is designed to drive the return-to-zero PMOS FET through a capacitor as fast as an AC coupling gate driver, and OUT_G provides delayed DC coupling negative biased gate control to the same PMOS FET. The OUT_C swings between V_H and V_L voltages, while OUT_G is within V_{SS} or V_{NEG} levels. Note that the OUT_C and OUT_G pins of one chip are designed to drive together for one PMOS FET, and that the PMOS FET source is typically connected to the same potential of the MD1812/13 V_{SS} voltage. Each of the output stages of OUT_A, OUT_B, OUT_C & OUT_D of MD1812/13 are capable of peak currents of up to ±2.0A, depending on the supply voltages used and load capacitance. But a 2kΩ resistor, R36, must be between OUT_G and the gate of the PMOS FET, which is driven by the OUT_C through a capacitor. This configuration provides the optimal series resistance value of the gate DC bias driver circuit.

The output stage of the MD1812/13 has separate power connections enabling the output signal high and low levels to be chosen independently from the driver supply voltages. As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V and –5V, and the output high and low levels may be varied anywhere over the range of +5V to -5V. In this design example, MD1812/13's V_{DD} and V_H are both powered by +10V, V_{SS} and V_L are grounded, and V_{NEG} is –10V. The source pin of the RTZ PMOS FET driven by the OUT_C and OUT_G pins is connected to ground.

PCB Layout Techniques

It is very important that the slab at the bottom of the IC package, which is the IC substrate "pin", be externally connected to the V_{NEG} pin to make sure it always has the lowest potential in any condition.

Use high-speed PCB trace design practices that are compatible with the circuit's operating speed. The internal circuitry of the MD1812/13 can operate at up to 100MHz, with the primary speed limitation being due to load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors should be as close to the supply pins as possible. The V_{SS} and V_L pins should have low inductance feed-through connections that are connected directly to a solid ground plane. If these voltages are not zero, they will require bypass capacitors similar to the positive power supplies. The V_{DD} and V_H supplies determine the output logic levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with a low-impedance bypass capacitor at the chip's pins. A ceramic capacitor of up to 1.0µF may be appropriate. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. A common voltage source and local decoupling capacitor may be used for the V_{DD} and V_H pins, which should always have the same DC level applied to them. For applications that are sensitive to jitter and noise, insert another ferrite bead between V_{DD} and V_H and decouple each pin separately.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small value resistor in series with the output to obtain better waveform integrity at the load terminals. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. Pay particular attention to the parasitic coupling from the driver's output to the input signal terminals. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V, even small coupling voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

Testing the Ultrasound Pulser

The MD1812 RTZ pulser design example is tested with the following power supply voltage and current limiting: V_{PP} 0 to +100V 5mA, V_{NN} 0 to -100V 5mA, V_{DD} = +10V 50mA, V_{NEG} -10V 5mA, V_{CC} +3.3V, 90mA.

The HV_{OUT} signal appears at the SMA connector J6. There is a 5:1 attenuation of the signal, due to the value of resistor R11. When driving a real transducer load, the value of this resistor should be reduced in value to match the load impedance.

The HV_{OUT} signal passes through jumper J5, which can be used to terminate the HV_{OUT} signal in a dummy load, comprising a 220pF capacitor in parallel with a 1kΩ resistor. When an external load is connected, the dummy load is not required, and J5 can be configured to pass the signals straight through to the output connector J6.

All the on-board test points are designed to work with an active oscilloscope probe, such as the Tektronix P6243 1MΩ active probe. Because TP7 is connected to the HV_{OUT}, where potentially damaging voltages could be present, make sure that V_{PP}/V_{NN} does not exceed the probe limit. If using another type of high impedance oscilloscope probe for the test points, ensure that the ground lead connections to the circuit board ground plane are as short as possible.

There are multiple frequency and waveform combinations that can be selected as bipolar pulses, PW or CW waveforms. An external clock input can be used if the on-board 40MHz-oscillator is disabled.

The external trigger input can be used to synchronize the output waveforms. There are five push buttons for selecting demo waveform, frequency, phase, and MD1812 chip enable functions. Color LEDs indicate the demo selection states. The CH1 output allows the monitoring of one of the 5 inputs (IN_A, IN_B, IN_C, IN_D or O_E) of the MD1812/13 via the select button.

The MD1812 and the MD1813 are very similar in function. The only differences between them are the control of the OE (MD1812) vs VLL (MD1813) pin and their logic functions. Please read their data sheets for the details. In this design example, the CPLD program is using an on-board solder jumper, R34, to sense the difference and works accordingly.

The example MD1812/13 pulser circuit schematic, detail signals definitions, and some measured waveforms are shown below.

Operating Supply Voltages

Sym	Parameter	Min	Typ	Max	Units
V_{NEG}	Negative Drive Supply	-12	-10	-4.5	V
V_{DD}	Positive Drive Supply	4.5	10	12	V
V_{CC}	Logic Supply	1.8	3.3	4.0	V
V_{PP}	TC6320 HV Positive Supply	0	-	100	V
V_{NN}	TC6320 HV Negative Supply	-100	-	0	V

Current Consumption

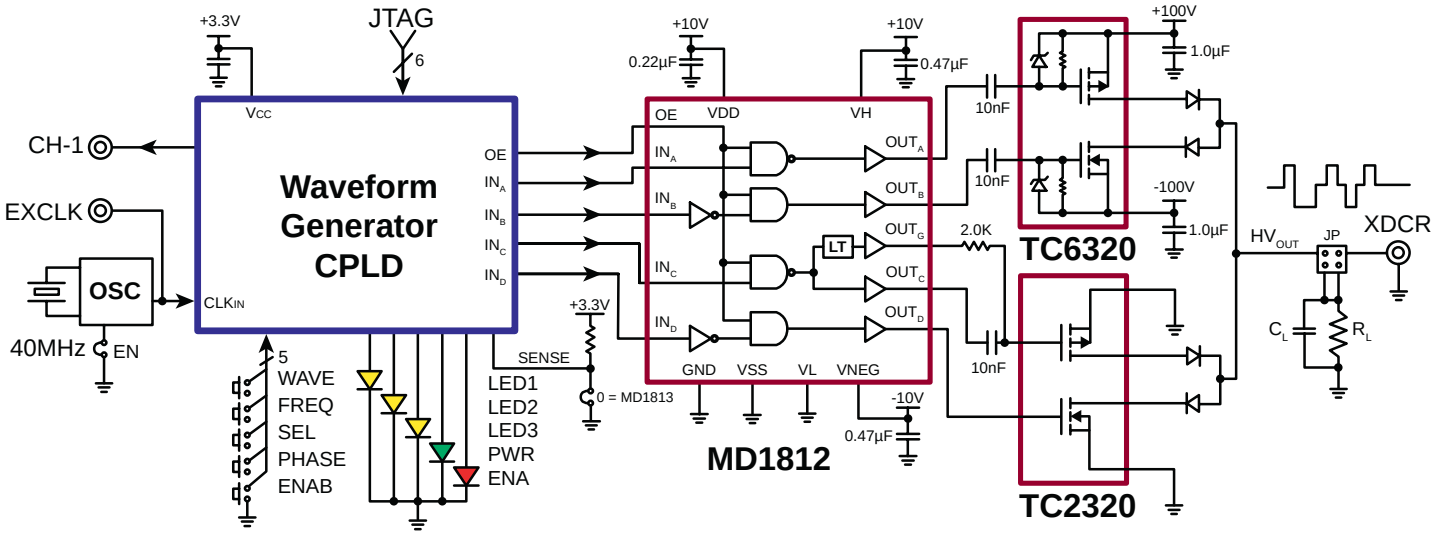
Sym	Typ	Units	Condition
I_{DD}	2.5	mA	V_{DD} = 12V
I_{H}	1.0	mA	V_{H} = 12V
I_{NEG}	2.0	mA	V_{NEG} = -12V
I_{CC}	70	mA	V_{CC} = 3.3V
I_{PP}	3.0	mA	V_{PP} = 100V
I_{NN}	3.0	mA	V_{NN} = -100V

Waveform C, 20MHz, 8 cycles
Load: 220pF//1k

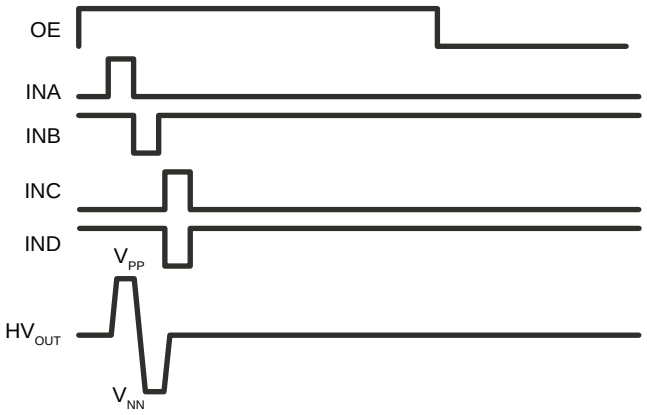
Clock, Signal, and Trigger Frequency

Internal Clock (MHz)	A_{OUT}/B_{OUT} Signal (MHz)	Internal Trigger (Hz)	External Trigger (Hz)
40	20	5000	9750> f_{ET} >5000
20	10	2500	4880> f_{ET} > 2500
10	5.0	1250	2440> f_{ET} > 1250
5.0	2.5	625	1220> f_{ET} >625
2.5	1.25	312.5	610> f_{ET} >312.5
1.25	0.625	156.25	305> f_{ET} >156.25
0.625	0.3125	78.125	152.5> f_{ET} >78.125

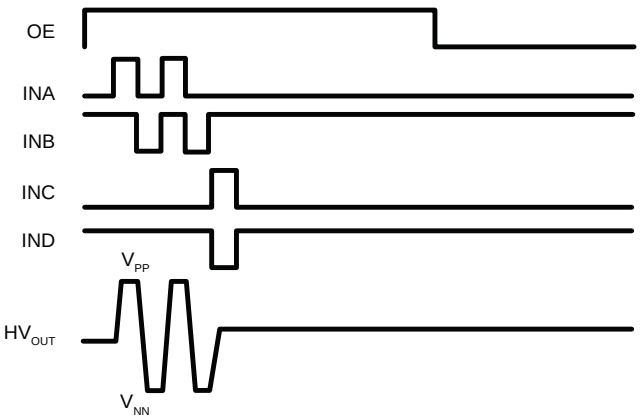
Pulser Circuit Schematic



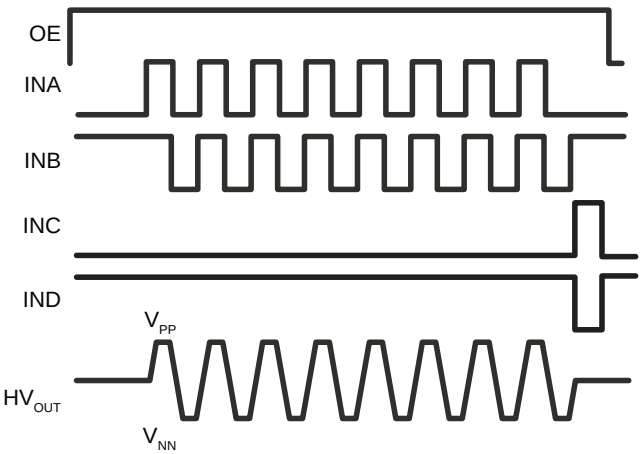
Waveform A



Waveform B

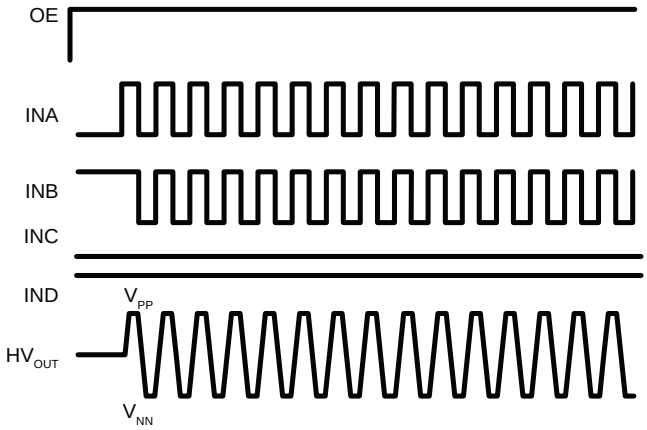


Waveform C



Note: The duty cycle of the PW burst is set about 0.2% for limited power dissipation

Waveform D



Note: The duty cycle of the PW burst is set about 25% at ≤5.0MHz for limited power dissipation.

MD1812/13 Reference Design

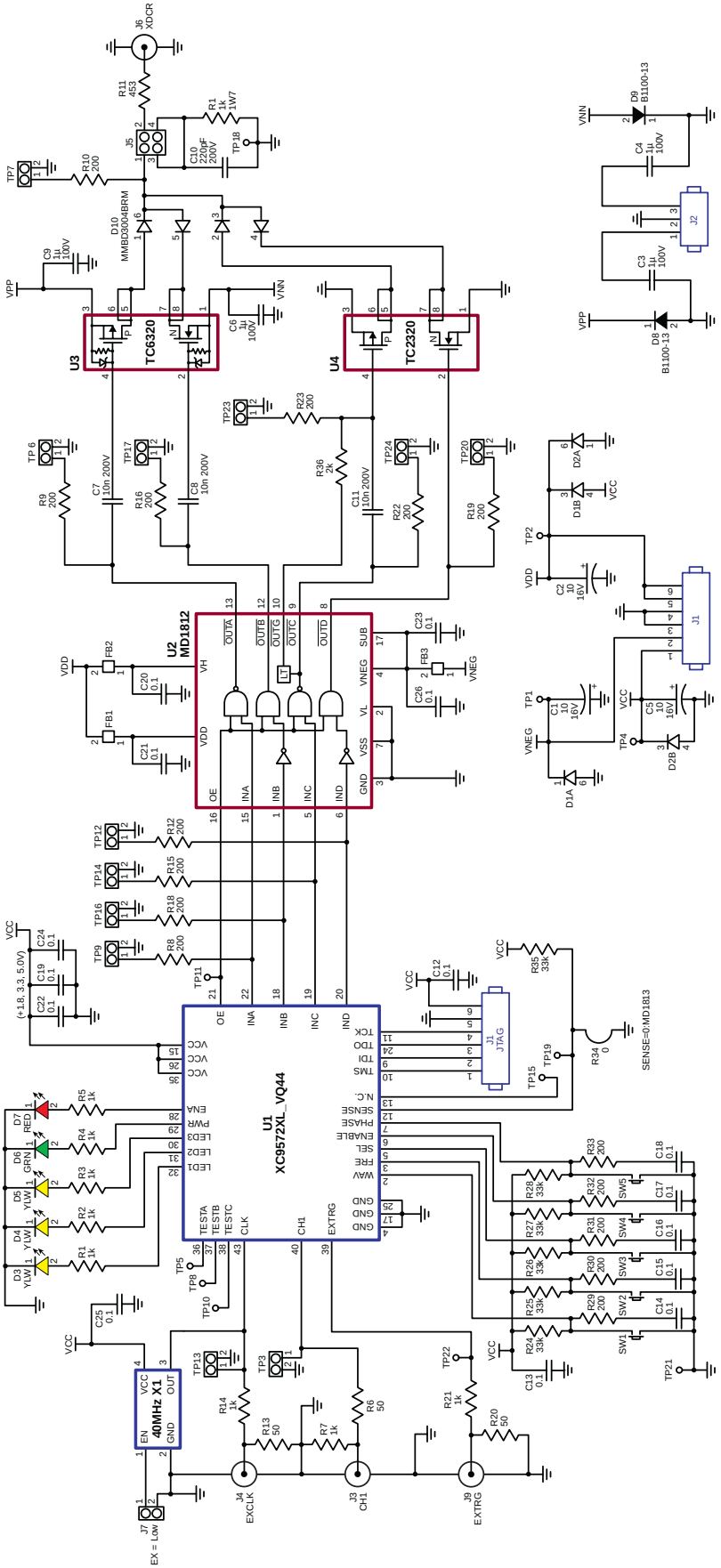


Fig. 1 Waveform of 2.5MHz

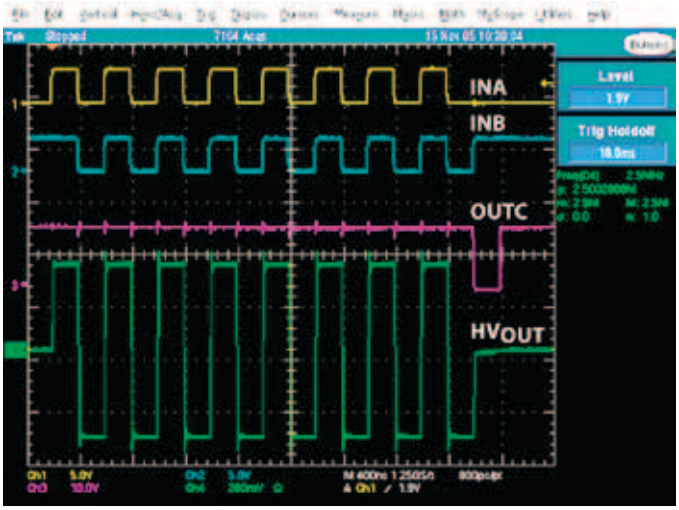


Fig. 2 Waveform of 5MHz

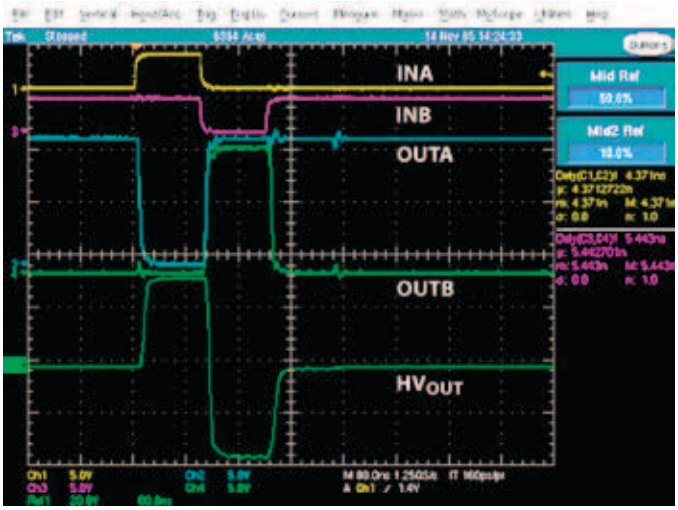


Fig. 3 Waveform of 10MHz

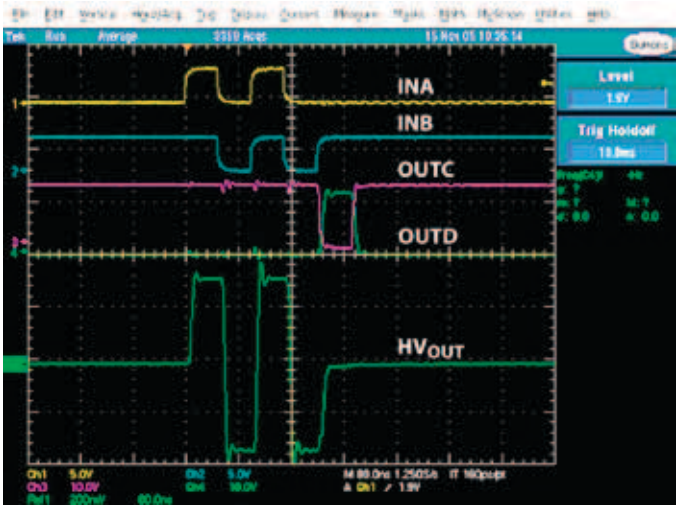


Fig. 4 Waveform of 10MHz Inverting

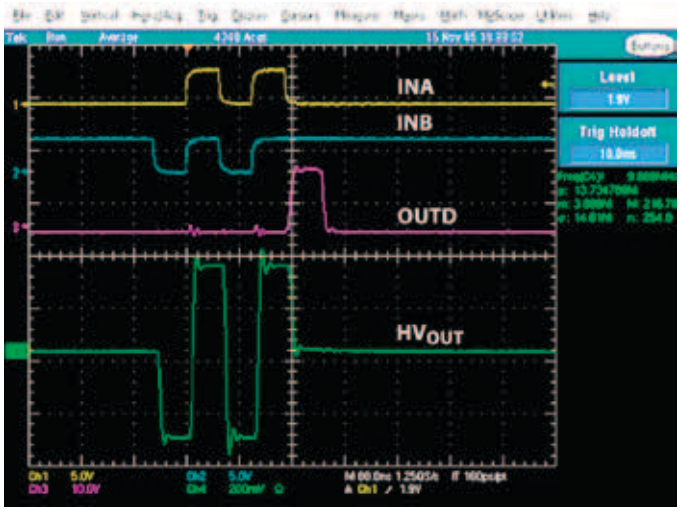


Fig. 5 Waveform of 20MHz 8 Cycles

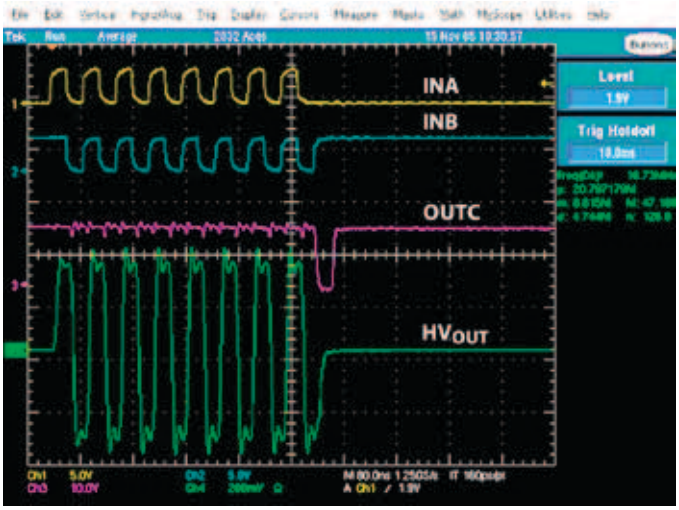


Fig. 6 Waveform of 5mHz & Delay Readings

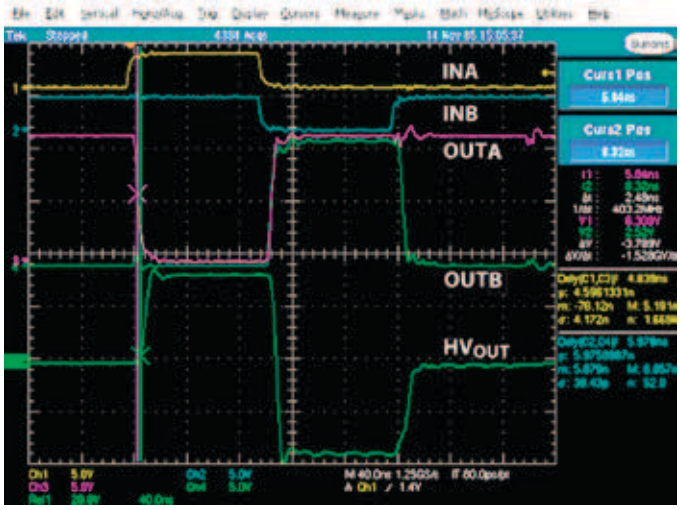


Fig. 7 Waveform of 10MHz

(at IN_C, OUT_C, OUT_G, and P- Gate, V_{DD} = 12V, V_{NEG} = -10V)

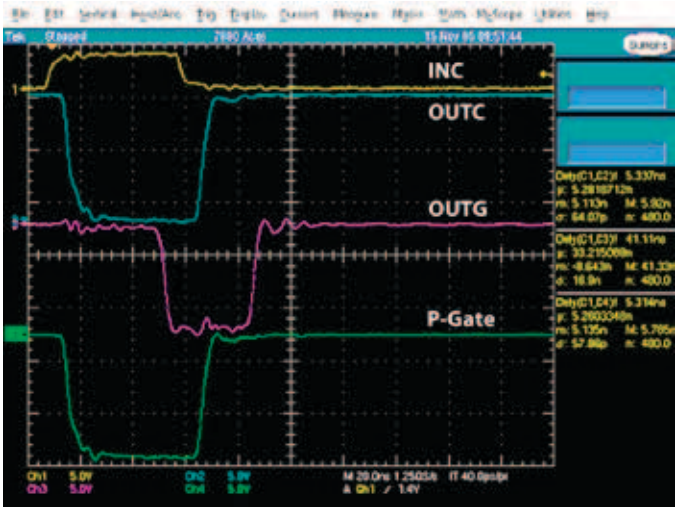
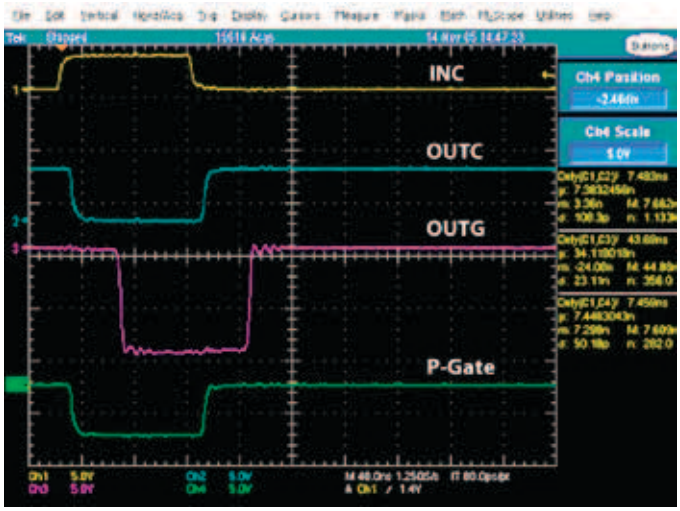


Fig. 8 Waveform of 5MHz

(at IN_C, OUT_C, OUT_G, and P- Gate, V_{DD} = 5V, V_{NEG} = -10V)



Board Connector and Test Pin Description

CPLD Pin #	Signal	Description
15,26,35	V_{LL}	Logic Power Supply +3.3V.
4,17,25	GND	Logic Power Ground 0V.
2	WAV	Selecting waveform pattern, push button input signal, Active low. See Fig.1 and Note 1.
3	FRE	Selecting frequency: 20,10, 5, 2.5,1.25 and 0.625MHz button input signal, active low.
5	SEL	Selecting waveform to CH1 of oscilloscope, push button input signal, active low.
6	ENABLE	Enable button, Active low, Control OE.
7	PHASE	Button for output waveform phase control.
22	IN_A	Output signal to MD1812 INA.
18	IN_B	Output signal to MD1812 INB.
19	IN_C	Output signal of MD1812 INC.
20	IN_D	Output signal of MD1812 IND.
21	OE	Output signal to MD1812 OE.
32	LED_1	Output signal LED_1, Yellow.
31	LED_2	Output signal LED_2, Yellow.
30	LED_3	Output signal LED_3, Yellow.
28	ENA	Output signal LED, RED, indicates OE = Hi.
29	PWR	Output signal LED, Green, indicates power supply ok.
10	TMS	Test Mode Select of JTAG.
9	TDI	Test Data In of JTAG.
24	TDO	Test Data Out of JTAG.
11	TCK	Test Clock of JTAG.
43	CLK	CPLD clock input.
40	CH1	Output signal to CH1 of oscilloscope, select one of the output signal: IN_A, IN_B, IN_C, IN_D.
39	EXTRG	External trigger signal input to control waveform timing.
12	SENSE	Sense solder jumper pin for MD1812 = Hi or MD1813 = Low, manufacture installation only.
13	N.C.	Reserved for manufacture test only.
36	TEST_A	Test pin reserved.
37	TEST_B	Test pin reserved.
38	TEST_C	Test pin reserved.

Board Connector and Test Pin Description

JTAG Connector Pin Number	Signal	Description
J8-1	TMS	Test Mode Select of CPLD
J8-2	TDI	Test Data In of CPLD
J8-3	TDO	Test Data Out of CPLD
J8-4	TCK	Test Clock of CPLD
J8-5	GND	Logic Power Supply Ground 0V for programming only
J8-6	V_{CC}	Logic Power Supply +3.3V for programming only
Signal / Jumper Pin Number	**Signal**	**Description**
J4	EXCLK	External clock input when on-board oscillator is disabled, or output the clock when it is enabled.
J9	EXTRG	External trigger signal input
J3	CH1	CH1 waveform output signal to oscilloscope or other test equipment, CMOS logic level
J6	XDCR	MD1812 / TC6320s switching waveform output, to user load and/or oscilloscope, high voltage 0 to +/-100V
J7	OSC_EN	Jumper for on-board oscillator enable / disable, open = enabled, short = disable
J5	Load JP	Jumper for on-board RC load to MD1812 high voltage output and XDCR connector
R34	Jumper	Solder jumper open if MD1812 in installed, short to GND if MD1813 is installed
Low Voltage Supply Connector Pin Number	**Signal**	**Description**
J1-1	V_{CC}	+3.3V logic voltage supply for V_{CC} (for CPLD only)
J1-2	V_{NEG}	-5.0 to -12V negative bias supply for V_{NEG} and SUB
J1-3	GND	Power supply ground
J1-4	GND	Power supply ground
J1-5	V_{DD}	+10V positive driver voltage supply for V_{DD} and V_H
J1-6	V_{DD}	+10V positive driver voltage supply for V_{DD} and V_H
High Voltage Supply Connector Pin Number	**Signal**	**Description**
J2-1	V_{PP}	0 to +100V positive high voltage supply with current limiting maximum to 5.0mA
J2-2	GND	High voltage power supply return, 0V
J2-3	V_{NN}	0 to -100V Negative high voltage supply with current limiting maximum to 5.0mA

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