MC14046B

Phase Locked Loop

The MC14046B phase locked loop contains two phase comparators, a voltage–controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self–bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, $PC2_{out}$ and LD, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source–follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage–to–frequency conversion and motor speed control.

Features

- Buffered Outputs Compatible with MHTL and Low–Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin–for–Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive OR Gate and is Duty Cycle Limited
- Phase Comparator 2 Switches on Rising Edges and is not Duty Cycle Limited
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (All Inputs)	−0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C

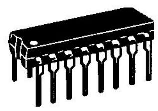
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

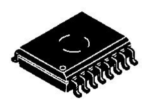
ON Semiconductor®

http://onsemi.com

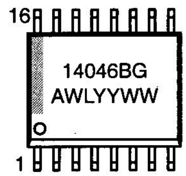
MARKING DIAGRAMS

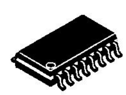


PDIP–16
P SUFFIX
CASE 648

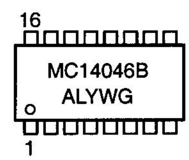


SOIC–16
DW SUFFIX
CASE 751G





SOEIAJ–16
F SUFFIX
CASE 966



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G	=	Pb–Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

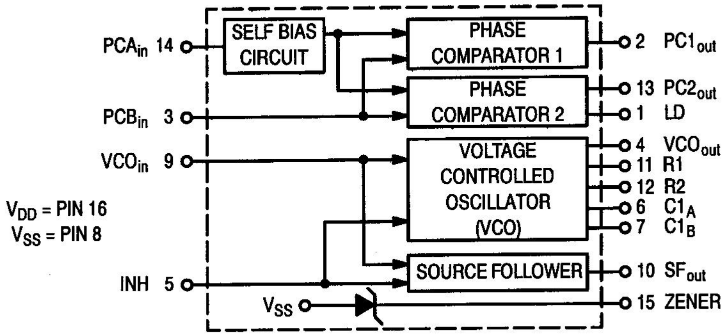
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

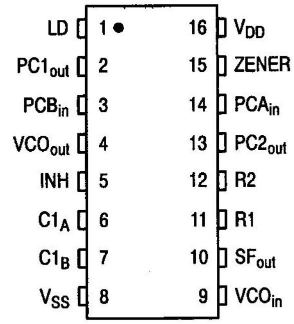
August, 2005 – Rev. 10

Publication Order Number:
MC14046B/D

BLOCK DIAGRAM



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage (Note 2) (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	– – – –	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	– – – –	– 0.7 – 0.14 – 0.35 – 1.1	– – – –	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current		I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	µAdc
Input Capacitance		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) Inh = $PCA_{in} = V_{DD}$, Zener = VCO_{in} = 0 V, $PCB_{in} = V_{DD}$ or 0 V, I_{out} = 0 µA		I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	µAdc
Total Supply Current (Note 3) (Inh = "0", f_o = 10 kHz, C_L = 50 pF, R1 = 1.0 MΩ, R2 = ∞ R_{SF} = ∞, and 50% Duty Cycle)		I_T	5.0 10 15	I_T = (1.46 µA/kHz) f + I_{DD} I_T = (2.91 µA/kHz) f + I_{DD} I_T = (4.37 µA/kHz) f + I_{DD}							mAdc

2. Noise immunity specified for worst-case input combination.
   Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
   2.0 Vdc min @ V_{DD} = 10 Vdc
   2.5 Vdc min @ V_{DD} = 15 Vdc
3. To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD}\left(\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right)^{3/4} + 1.6 \times \left(\frac{VCO_{in} - 1.65}{R_{SF}}\right)^{3/4} + 1 \times 10^{-3}\,(C_L + 9)\,V_{DD}\,f\,+$$

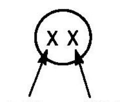
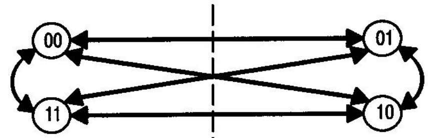
$$1 \times 10^{-1}\,V_{DD}^2\left(\frac{100\%\ \text{Duty Cycle of } PCA_{in}}{100}\right) + I_Q$$

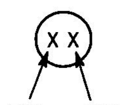
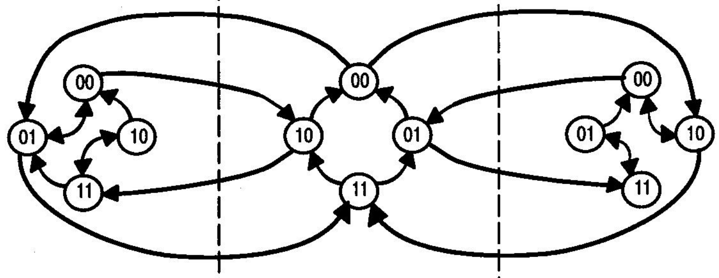
where: I_T in µA, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in kHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS (Note 4) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Minimum Device	Typical	Maximum Device	Units
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	350	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	150	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	110	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	175	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	75	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	37	55	
PHASE COMPARATORS 1 and 2						
Input Resistance – PCA_{in}	R_{in}	5.0	1.0	2.0	–	MΩ
		10	0.2	0.4	–	
		15	0.1	0.2	–	
– PCB_{in}	R_{in}	15	150	1500	–	MΩ
Minimum Input Se-sitivity	V_{in}	5.0	–	200	300	mV p–p
AC Coupled — PCA_{in}		10	–	400	600	
C series = 1000 pF, f = 50 kHz		15	–	700	1050	
DC Coupled – PCA_{in}, PCB_{in}	–	5 to 15	See Noise Immunity			
VOLTAGE CONTROLLED OSCILLATOR (VCO)						
Maximum Frequency	f_{max}	5.0	0.5	0.7	–	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF		10	1.0	1.4	–	
R1 = 5.0 kΩ, and R2 = ∞)		15	1.4	1.9	–	
Temperature – Frequency Stability	–	5.0	–	0.12	–	%/°C
(R2 = ∞)		10	–	0.04	–	
		15	–	0.015	–	
Linearity (R2 = ∞)	–					%
(VCO_{in} = 2.5 V ± 0.3 V, R1 > 10 kΩ)		5.0	–	1.0	–	
(VCO_{in} = 5.0 V ± 2.5 V, R1 > 400 kΩ)		10	–	1.0	–	
(VCO_{in} = 7.5 V ± 5.0 V, R1 ≥ 1000 kΩ)		15	–	1.0	–	
Output Duty Cycle	–	5 to 15	–	50	–	%
Input Resistance – VCO_{in}	R_{in}	15	150	1500	–	MΩ
SOURCE–FOLLOWER						
Offset Voltage	–	5.0	–	1.65	2.2	V
(VCO_{in} minus SF_{out}, RSF > 500 kΩ)		10	–	1.65	2.2	
		15	–	1.65	2.2	
Linearity	–					%
(VCO_{in} = 2.5 V ± 0.3 V, R_{SF} > 50 kΩ)		5.0	–	0.1	–	
(VCO_{in} = 5.0 V ± 2.5 V, R_{SF} > 50 kΩ)		10	–	0.6	–	
(VCO_{in} = 7.5 V ± 5.0 V, R_{SF} > 50 kΩ)		15	–	0.8	–	
ZENER DIODE						
Zener Voltage (I_Z = 50 μA)	V_Z	–	6.7	7.0	7.3	V
Dynamic Resistance (I_Z = 1.0 mA)	R_Z	–	–	100	–	Ω

4. The formula given is for the typical characteristics only.

	PHASE COMPARATOR 1	
Input Stage 		
PC1$_{out}$	0	1

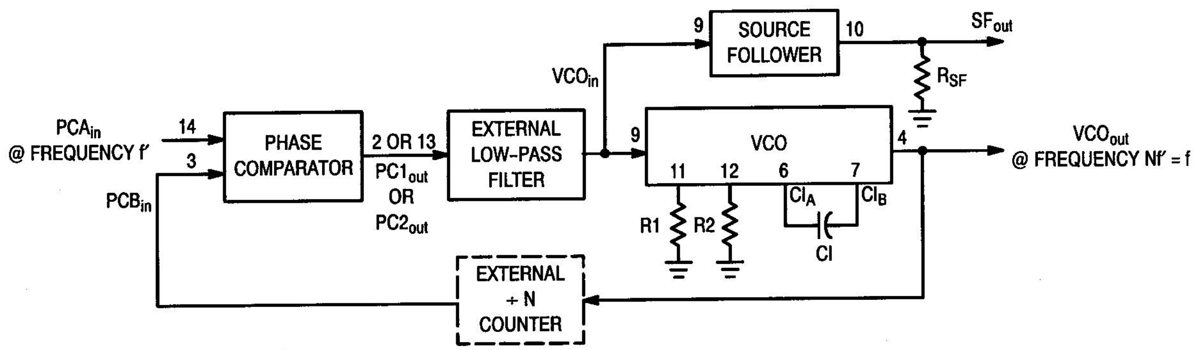
	PHASE COMPARATOR 2		
Input Stage 			
PC2$_{out}$	0	3–State Output Disconnected	1
LD (Lock Detect)	0	1	0

Refer to Waveforms in Figure 3.

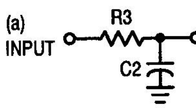
Figure 1. Phase Comparators State Diagrams

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$)	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low–pass filter characteristics (see Figure 3). $f_C \le f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.	$f_{min} = \frac{1}{R_2(C_1 + 32\ pF)}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32\ pF)} + f_{min}$ (V_{CO} input = V_{DD}) Where: $10K \le R_1 \le 1\ M$ $10K \le R_2 \le 1\ M$ $100pF \le C_1 \le .01\ \mu F$	

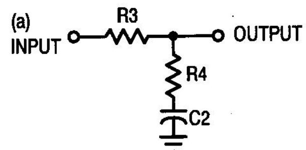
Figure 2. Design Information



Typical Low-Pass Filters



$$2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{R3\,C2}}$$



Typically:

$$R_4\,C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi\Delta f}$$

$$(R_3 + 3,000\Omega)\,C_2 = \frac{100N\Delta f}{f_{max}{}^2} - R_4\,C_2$$

$$\Delta f = f_{max} - f_{min}$$

NOTE: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor C_C is then placed from the midpoint to ground. The value for C_C should be such that the corner frequency of this network does not significantly affect Ω_n. In Figure B, the ratio of R3 to R4 sets the damping, R4 ≅ (0.1)(R3) for optimum results.

Definitions: N = Total division ratio in feedback loop

$K\phi = V_{DD}/\pi$ for Phase Comparator 1

$K\phi = V_{DD}/4\pi$ for Phase Comparator 2

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{V_{DD} - 2\,V}$$

for a typical design $\Omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input)

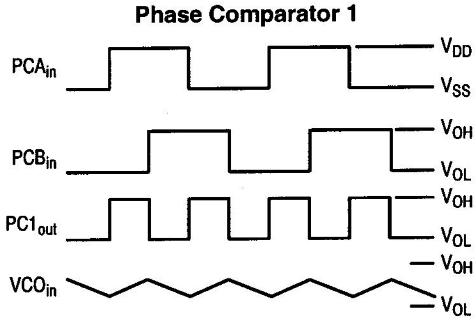
$\zeta \cong 0.707$

LOW-PASS FILTER

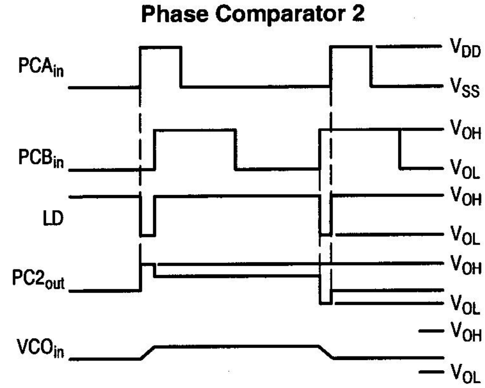
Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{NR_3C_2}}$	$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi K_{VCO}}$	$\zeta = 0.5\,\omega_n\left(R_3C_2 + \frac{N}{K\phi K_{VCO}}\right)$
$F(s) = \frac{1}{R_3C_2S + 1}$	$F(s) = \frac{R_3C_2S + 1}{S(R_3C_2 + R_4C_2) + 1}$

Waveforms

Phase Comparator 1



Phase Comparator 2



Note: for further information, see:

(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
(2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
(3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
(4) A. B. Przedpelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.

Figure 3. General Phase-Locked Loop Connections and Waveforms