National Exams, December 2006

Comp-A2
Digital Systems Design

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.

2. This is CLOSED BOOK exam. Any Casio or Sharp approved calculator is permitted.

3. Any FOUR (4) questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

4. Each question is of equal value. Marks for multipart questions are stated in each part.

Question 1 (25 Marks)

A system must be designed to accept three inputs and a clock and provide three outputs. The three inputs are numbered X1, X2 and X3 respectively. The outputs are Y1, Y2 and Y3. Input X1 has higher priority than X2, which in turn has higher priority than X3. Note that Y1 is associated with X1, Y2 is associated with X2 and Y3 is associated with X3. The system must do the following:

do forever {

1. At the positive edge of the clock, check to see that each input is now the same value as it was just prior to the clock edge.
2. If at least one input has changed state from 0 before the positive clock edge to 1 after the positive clock edge, then
   i. wait for the next positive clock edge
   ii. on the next positive clock edge, pulse the output corresponding to the highest priority input high for one clock cycle

} loop

For example, the following sequence of inputs will yield the corresponding outputs. Note that the bits to the left are the oldest bits, the bits on the right are the most recent. The rightmost column contains the current signals. **Note that each column corresponds to the state of the three inputs and outputs just after the positive clock edge.**

X1	1 0 1 1 0 1 0 1 1 0 0 0 0 0 0 1 0 0 1 1 0 0 0 0 0 1 0 1 0 1
X2	0 0 0 1 1 0 0 0 0 1 0 1 0 1 1 0 0 1 1 0 0 0 0 1 0 1 0 0 1 0
X3	0 0 0 1 0 1 0 1 1 1 0 0 0 1 1 0 1 0 0 1 1 1 0 1 1 0 0 0 0 0
Y1	0 0 0 1 0 0 1 0 1 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 1 0 1 0
Y2	0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0 0 0 1 0 0 0 0 0 1 0 0 0 0 1
Y3	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0

oldest most recent

Design the system. Try to minimize the number of states used and the number of gates and flip-flops used. Use D flip-flops.

Question 2 (25 Marks)

a) **(10 Marks)** What are propagation delay, set-up and hold times. What causes them and what problems do they solve? If a specification sheet for a logic device lists a set-up time of 5nsec and a hold time of 3nsec, what do you do with these values?

b) **(15 Marks)** Binary counters and shift registers can have more than one output change state at every clock pulse. Sometimes the outputs of these counters are combined through combinatorial logic gates and used to trigger external events. What problems can occur

due to set-up time, hold time and propagation time considerations? Answer this question by making specific reference to the circuit of Figure 1.

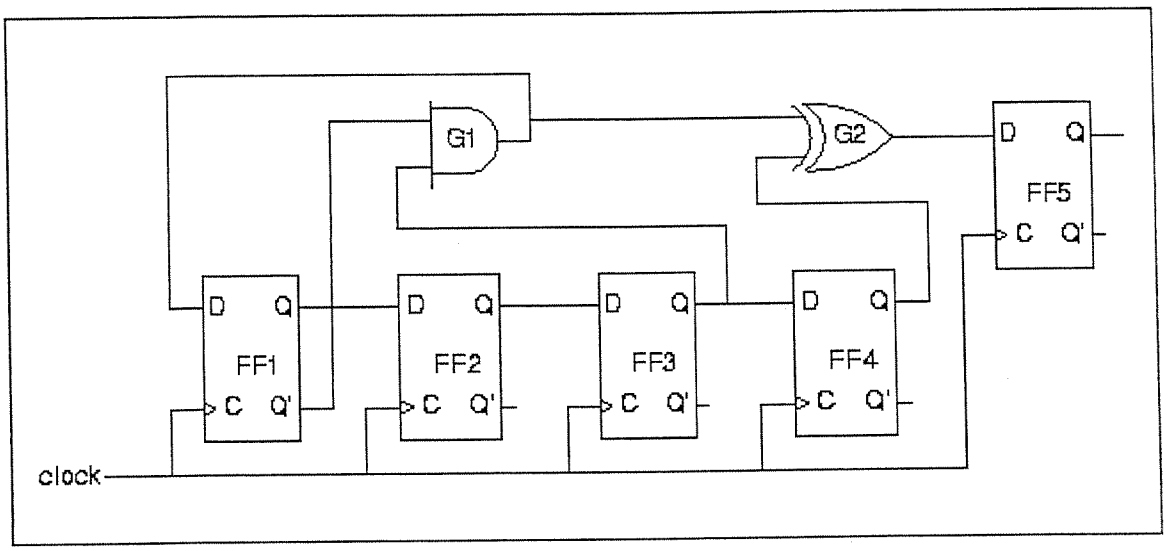

Figure 1: Circuit for part b) of Question 2.

Question 3 (25 Marks)

a) **(15 Marks)** Sketch the data path internal to the CPU for a microprocessor with which you are familiar and describe the cycle-by-cycle flow of signals in the datapath. Your description should commence at the point where the processor is starting to read the next instruction and should end when the processor is about to read the subsequent instruction. Use a table showing the contents of the address bus, the data bus, the flag register (or the flags) and any relevant temporary registers in your explanation. Each row of the table should show the contents of the registers and busses at the end of each clock "tick."

b) **(5 Marks)** What are interrupts used for? How do you incorporate them into the design of your program? How do they differ from subroutines? What are the methods by which the program enter an Interrupt Service Routine?

c) **(5 Marks)** Key issues that must be addressed in the design of a system with multiple interrupt sources include the length of the Interrupt Service Routines, latency and nesting. Briefly explain each issue and why it is important.

Question 4 (25 Marks)

a) **(15 Marks)** You want to connect two embedded computers, machine A and machine B, together, and choose to do it by connecting together their serial ports. Machine A will pass 8-bit bytes to machine B using the UARTs on the two machines. What other control signals are required to ensure that each byte is passed correctly, and is read once and only once by machine B? Note that we do not know when each byte is to be passed to machine B by machine A. Also assume that each machine has other work to do as well.

b) **(10 Marks)** Why is it possible to transfer data synchronously so much faster than asynchronously? Your answer should convey your understanding of the essential issues in both techniques.

Question 5 (25 Marks)

a) **(10 Marks)** An embedded system based on a microprocessor is being designed to have a 24-bit address bus with a linear address range. The memory is not organized in banks. The system must have ROM from addresses $d00000 to $ffffff, RAM from $000000 to $00ffff, and four I/O devices occupying 16 bytes each anywhere in the address range from $100000 to $17ffff. The system will never be expanded.

The ROM is made up of devices that store 512 KBytes x 8-bits each, the RAM consists of parts that store 128 Kbytes each, and the I/O devices occupy 16 consecutive bytes each.

Design an address decoder for this system. Use as few gates as possible. Note that all devices use active-low chip-select inputs.

b) **(10 Marks)** A typical microprocessor has a bus architecture. The two most-often used bus structures are the von Neumann architecture and the Harvard architecture. Briefly describe each of these and explain the strengths and weaknesses of each.

c) **(5 Marks)** What must a microprocessor do when its RESET input is changed from the asserted state to the de-asserted state? Discuss all of the steps at a high level of detail.