

512K x 8 HIGH-SPEED CMOS STATIC RAM

APRIL 2005

FEATURES

- High-speed access times: 10, 12 ns
- · High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with CE and OE options
- CE power-down
- Fully static operation: no clock or refresh required
- · TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
 - 36-pin 400-mil SOJ
 - 36-pin miniBGA
 - 44-pin TSOP (Type II)
- Lead-free available

DESCRIPTION

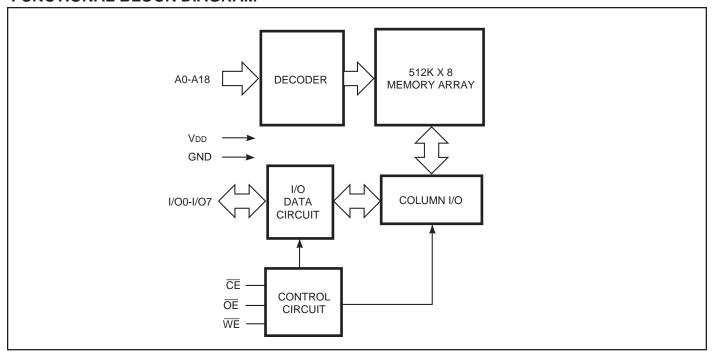
The *ISSI* IS61LV5128AL is a very high-speed, low power, 524,288-word by 8-bit CMOS static RAM. The IS61LV5128AL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 μ W (typical) with CMOS input levels.

The IS61LV5128AL operates from a single 3.3V power supply and all inputs are TTL-compatible.

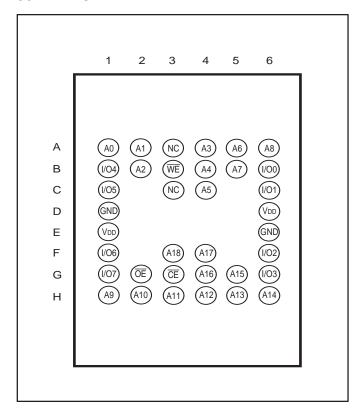
The IS61LV5128AL is available in 36-pin 400-mil SOJ, 36-pin mini BGA, and 44-pin TSOP (Type II) packages.

FUNCTIONAL BLOCK DIAGRAM

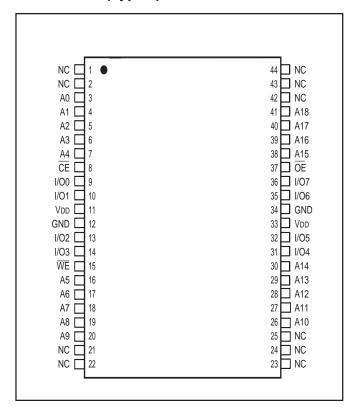




PIN CONFIGURATION 36 mini BGA



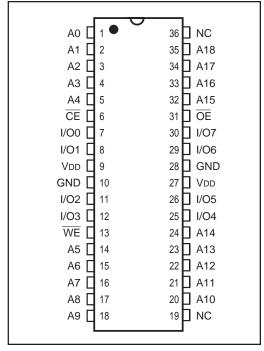
44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
WE	Write Enable Input
1/00-1/07	Bidirectional Ports
VDD	Power
GND	Ground
NC	No Connection

36-Pin SOJ



TRUTH TABLE

Mode	WE	CE	ŌĒ	I/O Operation	V _{DD} Current
Not Selected (Power-down)	Х	Н	Х	High-Z	ISB1, ISB2
Output Disable	d H	L	Н	High-Z	lcc
Read	Н	L	L	D оит	lcc
Write	L	L	Χ	Din	Icc



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to V _{DD} + 0.5	V
Тѕтс	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.0	W

Notes:

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

		VDD		
Range	Ambient Temperature	10ns	12ns	
Commercial	0°C to +70°C	3.3V +10%, -5%	3.3V <u>+</u> 10%	
Industrial	-40°C to +85°C	3.3V +10%, -5%	3.3V <u>+</u> 10%	

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
Cı/o	Input/Output Capacitance	Vout = 0V	8	pF

Notes:

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions: $T_A = 25^{\circ}C$, f = 1 MHz, $V_{DD} = 3.3V$.

IS61LV5128AL



DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
Vон	Output HIGH Voltage	VDD = Min., IOH = -4.0 mA		2.4	_	V
Vol	Output LOW Voltage	VDD = Min., IOL = 8.0 mA		_	0.4	V
VIH	Input HIGH Voltage			2.0	VDD + 0.3	V
VIL	Input LOW Voltage(1)			-0.3	0.8	V
ILI	Input Leakage	GND ≤ Vin ≤ Vdd	Com.	-2	2 5	μA
			Ind.	- 5	5	
ILO	Output Leakage	$GND \leq Vout \leq Vdd, Outputs Disabled$	Com. Ind.	-2 -5	2 5	μΑ

Note:

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Ob. a.l.	Danamatan.	Test Conditions			0	-1: Min		II.a.!t	
Symbol	Parameter	Test Conditions		IVIIN.	Max.	wiin.	Max.	Unit	
Icc	V _{DD} Dynamic Operating	VDD = Max.,	Com.	_	90	_	85	mA	
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	95	_	90		
IsB	TTL Standby Current	VDD = Max.,	Com.	_	40	_	35	mA	
	(TTL Inputs)	$\frac{\text{Vin} = \text{Vih or Vil}}{\overline{\text{CE}}} \geq \text{Vih, f} = \text{fmax.}$	Ind.	_	45	_	40		
IsB1	TTL Standby Current	V _{DD} = Max.,	Com.	_	20	_	20	mA	
	(TTL Inputs)	$\frac{V_{IN} = V_{IH} \text{ or } V_{IL}}{\overline{CE}} \ge V_{IH}, f = 0$	Ind.	_	25	_	25		
IsB2	CMOS Standby	V _{DD} = Max.,	Com.	_	15	_	15	mA	
	Current (CMOS Inputs)	$\label{eq:continuous} \begin{split} \overline{\text{CE}} &\geq \text{V}_{\text{DD}} - 0.2\text{V},\\ \text{V}_{\text{IN}} &\geq \text{V}_{\text{DD}} - 0.2\text{V}, \text{ or}\\ \text{V}_{\text{IN}} &\leq 0.2\text{V}, \text{ f} = 0 \end{split}$	Ind.	_	20	_	20		

Note:

^{1.} $V_{IL} = -3.0V$ for pulse width less than 10 ns.

^{1.} At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.



READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

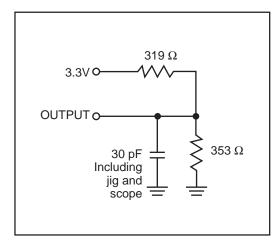
		-10)	-12	2	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
trc	Read Cycle Time	10	_	12	_	ns
t AA	Address Access Time	_	10	_	12	ns
t oha	Output Hold Time	2	_	2	_	ns
tace	CE Access Time	_	10	_	12	ns
t DOE	OE Access Time	_	4	_	5	ns
thzoe(2)	OE to High-ZOutput	_	4	_	5	ns
t LZOE ⁽²⁾	OE to Low-Z Output	0	_	0	_	ns
thzce(2	CE to High-Z Output	0	4	0	6	ns
tLZCE ⁽²⁾	CE to Low-Z Output	3	_	3	_	ns
t PU	PowerUpTime	0	_	0	_	ns
t PD	Power Down Time	_	10	_	12	ns

Notes:

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS



 $\begin{array}{c} 319 \ \Omega \\ 3.3 \text{VO} \\ \hline \\ \text{OUTPUTO} \\ \hline \\ \text{Including} \\ \text{jig and} \\ \text{scope} \end{array} \begin{array}{c} 353 \ \Omega \\ \hline \\ \end{array}$

Figure 1 Figure 2

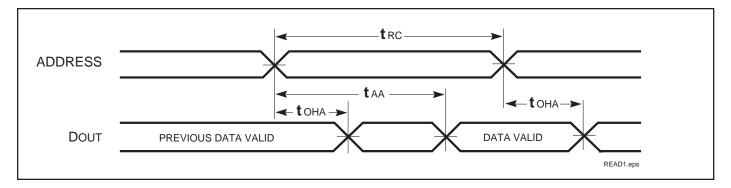
^{1.} Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.

^{2.} Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

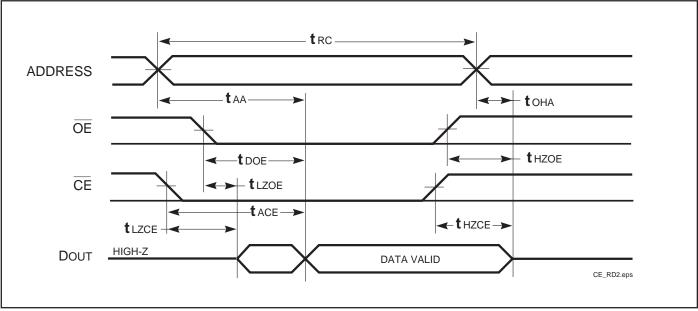


AC WAVEFORMS

READ CYCLE NO. $1^{(1,2)}$ (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) ($\overline{\text{CE}}$ and $\overline{\text{OE}}$ Controlled)



Notes:

- 1. WE is HIGH for a Read Cycle.
- 2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- 3. Address is valid prior to or coincident with $\overline{\textbf{CE}}$ LOW transitions.



WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

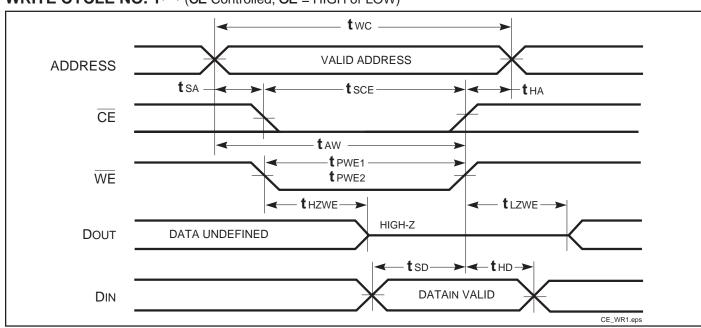
		-1	0	-1:	2	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	10	_	12	_	ns
tsce	CE to Write End	8	_	8	_	ns
taw	Address Setup Time to Write End	8	_	8	_	ns
t ha	Address Hold from Write End	0	_	0	_	ns
t sa	Address Setup Time	0	_	0	_	ns
t PWE1	WE Pulse Width	8	_	8	_	ns
tpwe2	WE Pulse Width (OE = LOW)	10	_	12	_	ns
tsp	Data Setup to Write End	6	_	6	_	ns
t HD	Data Hold from Write End	0	_	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	5	_	6	ns
tLZWE ⁽²⁾	WE HIGH to Low-Z Output	2	_	2	_	ns

Notes:

- 1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
- 2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
- 3. The internal write time is defined by the overlap of $\overline{\textbf{CE}}$ LOW and $\overline{\textbf{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

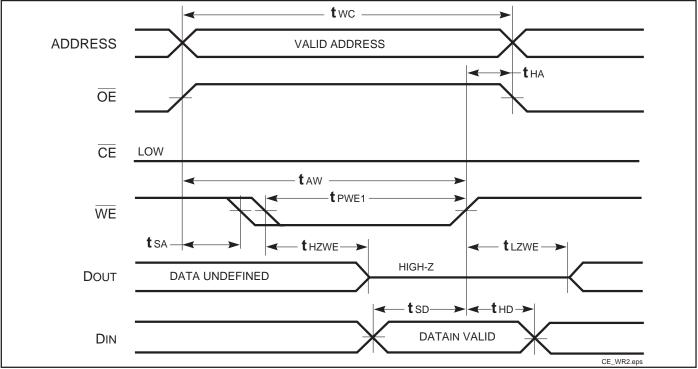
AC WAVEFORMS

WRITE CYCLE NO. $1^{(1,2)}$ (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)





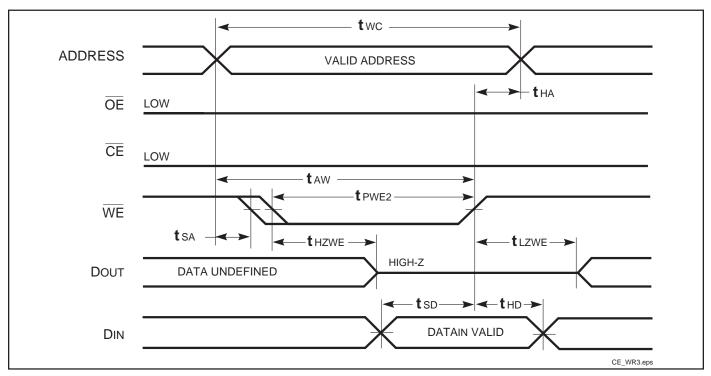
WRITE CYCLE NO. 2^(1,2) (WE Controlled: OE is HIGH During Write Cycle)



Notes:

- 1. The internal write time is defined by the overlap of $\overline{\textbf{CE}}$ LOW and $\overline{\textbf{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- 2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)





ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package	
10	IS61LV5128AL-10K	L-10K 400-mil Plastic SOJ	
10	IS61LV5128AL-10T	TSOP (Type II)	
12	IS61LV5128AL-12K	400-mil Plastic SOJ	
12	IS61LV5128AL-12T	TSOP (Type II)	

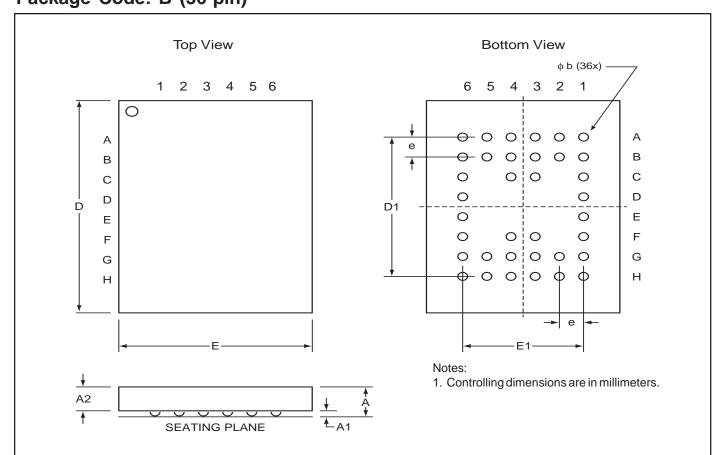
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61LV5128AL-10KI	400-mil Plastic SOJ
10	IS61LV5128AL-10KLI	400-mil Plastic SOJ, Lead-free
10	IS61LV5128AL-10TI	TSOP (Type II)
10	IS61LV5128AL-10TLI	TSOP (Type II), Lead-free
10	IS61LV5128AL-10BI	mini BGA (8mmx10mm)
10	IS61LV5128AL-10BLI	mini BGA (8mmx10mm), Lead-free
12	IS61LV5128AL-12TI	TSOP (Type II)

PACKAGING INFORMATION



Mini Ball Grid Array Package Code: B (36-pin)



mBGA - 6mm x 8mm

	MILI	IMET	ERS	INCHES					
Sym.	Min.	Тур.	Max.	Min. Typ. Max.					
N0. Leads		36		36					
Α	_	_	1.20	— — 0.047					
A1	0.24	_	0.30	0.009 — 0.012					
A2	0.60	_	_	0.024 — —					
D	7.90	8.00	8.10	0.311 0.315 0.319					
D1	5	.25BS	3	0.207BSC					
E	5.90	6.00	6.10	0.232 0.236 0.240					
E1	3	.75BS	C	0.148BSC					
е	0	.75BS	С	0.030BSC					
b	0.30	0.35	0.40	0.012 0.014 0.016					

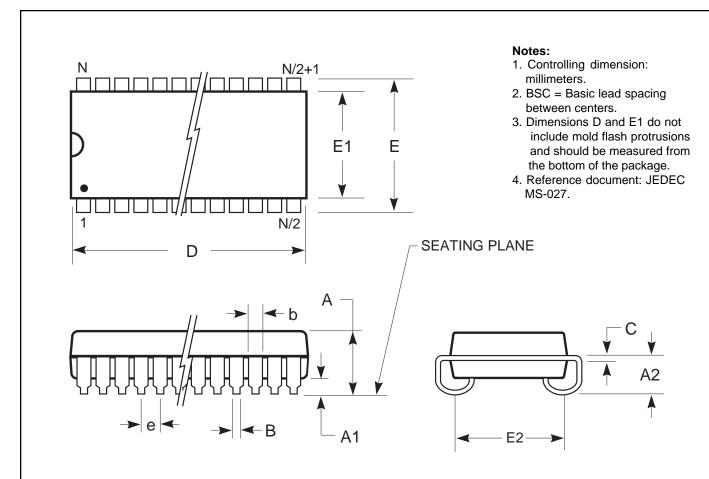
mBGA - 8mm x 10mm

	MIL	LIMET	ER	INCHES
Sym.	Min.	Тур.	Max.	Min. Typ. Max.
N0. Leads		36		36
Α	_	_	1.20	— — 0.047
A1	0.24	_	0.30	0.009 — 0.012
A2	0.60	_	_	0.024 — —
D	9.90	10.00	10.10	0.390 0.394 0.398
D1	5	.25BSC)	.207BSC
E	7.90	8.00	8.10	0.311 0.315 0.319
E1	3	3.75BSC)	0.148BSC
е	0	.75BSC)	0.030BSC
b	0.30	0.35	0.40	0.012 0.014 0.016

PACKAGING INFORMATION



400-mil Plastic SOJ Package Code: K



Millimeters		Inches		Millim	Millimeters		Inches		Millimeters		es	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads	(N)	28				32	2				36	
Α	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40	BSC	0.370) BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370	BSC
е	1.27	BSC	0.05	0 BSC	1.27 E	BSC	0.050) BSC	1.27	BSC	0.050) BSC



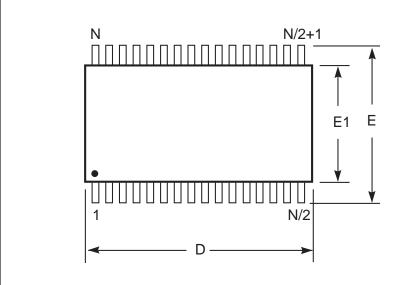
	Millimeters		Inches		Millim	Millimeters		Inches		Millimeters		es	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
No. Leads (N) 4			0			42				44			
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_	
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_	
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130	
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	
E2	9.40 BSC		0.370	70 BSC 9.40 BSC		BSC	0.370 BSC		9.40	9.40 BSC		0.370 BSC	
е	1.27	BSC	0.050	BSC	1.27 E	3SC	0.050	BSC	1.27	BSC	0.050) BSC	

PACKAGING INFORMATION



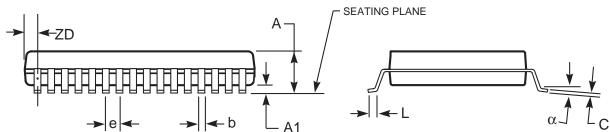
Plastic TSOP

Package Code: T (Type II)



Notes:

- Controlling dimension: millimieters, unless otherwise specified.
- 2. BSC = Basic lead spacing between centers.
- Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
- Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)													
	Millimeters		Inches		Millim	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Ref. Std.													
No. Leads (N) 32						44	ļ			50			
Α	_	1.20	_	0.047	_	1.20	_	0.047	_	1.20	_	0.047	
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018	
С	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830	
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	
Е	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471	
е	1.27	BSC	0.050	BSC	0.80	0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024	
ZD	0.95	REF	0.03	7 REF	0.81	REF	0.03	2 REF	0.88	REF	0.035	REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	