design ideas

Edited by Brad Thompson

Enhanced battery "gas gauge" keeps its data through glitches

Herbert Seidenberg, Costa Mesa, CA

Texas Instruments' BQ2010 battery-"gas-gauge" IC offers a convenient method for recording available charge stored in a nickel-cadmium or nickel-metal-hydride battery. However, even though plenty of charge remains available, under certain circumstances, transient-current spikes can fool the BQ2010 into registering a discharged battery. For example, spikes can occur when you connect a heating element or a switched-mode regulator containing a high-value input capacitor, or if you momentarily short-circuit the battery's terminals while making a connection.

During a current spike, the battery voltage decreases by the voltage drop across the battery's internal resistance plus the voltage drop across the circuit's current-sense resistor. The BQ2010 misinterprets the voltage decrease as a low-cell voltage condition normally seen during discharge. The device then loses data on the remaining battery capacity, and, depending on the application, of the BQ2010's Empty output, the load may inadvertently disconnect. Finally, the battery must contain a partial charge to un-

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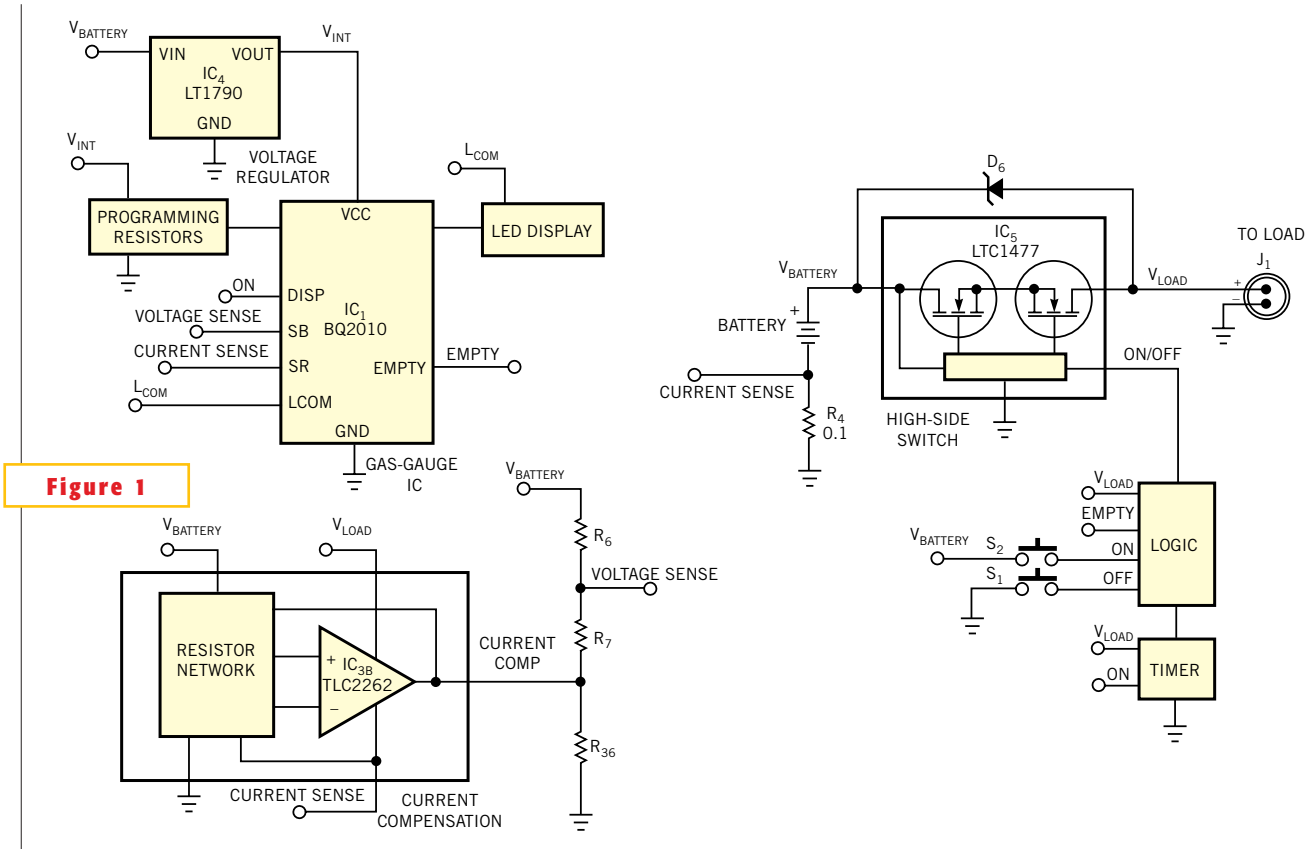
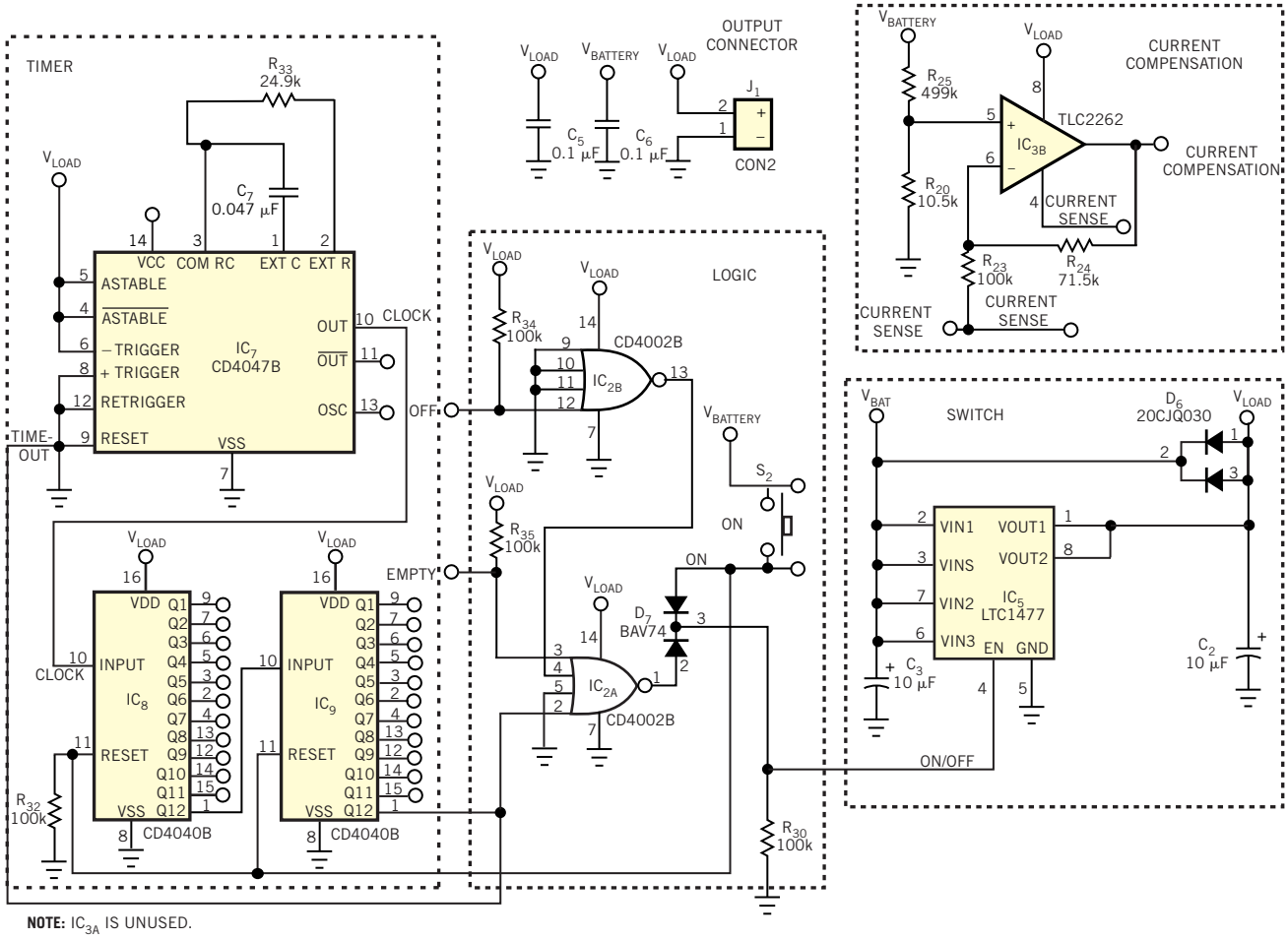


Figure 1

This circuit improves the BQ2010's current-spike immunity in several ways and adds several useful features.



NOTE: IC_{3A} IS UNUSED.

Figure 2 You can customize this circuit for a battery's chemistry, capacity, internal resistance, cell count, and timer and display options.

latch the BQ2010's Empty output.

The circuit in **Figure 1** improves the BQ2010's current-spike immunity in several ways and adds several useful features. First, a 3.3V, current-limited low-dropout voltage regulator, IC_4, supplies power to IC_1, the BQ2010. Second, an LTC1477 short-circuit-protected, high-side FET switch, IC_5, limits battery-to-load current to a maximum of 2A. To prevent IC_1's SB (single-cell voltage) monitor pin from sensing an invalid Empty state, current-compensation amplifier IC_{3B} makes the voltage to the SB pin current-independent. The negative rail of IC_{3B} connects to the active side of the ground-referenced current-sense resistor, R_4. With no load current, op amp IC_{3B}'s output should rest at 0V, but few rail-to-rail op amps provide outputs that go to 0V. The solution is to bias the positive side of the op amp enough to set the output above V_{OL} and compensate by lowering the gas-gauge-voltage sense-resistor ratio.

Additional features include a short-circuited load shutoff to prevent IC_5 from going into thermal-protection mode (**Figure 2**). Also, the entire circuit shuts off when the battery provides no current to the load or when the battery is discharged. A timer circuit consisting of IC_7, IC_8 and IC_9 provides an additional shutoff option. You can set the turnoff delay from minutes to days by changing R_{33} and C_7 to reduce the clock frequency, or by selecting other taps on binary ripple counters IC_8 and IC_9. Pressing switch S_2 or starting a recharging cycle turns the controller back on. The parallel-connected sections of Schottky diode D_6 provide a current path for recharging the battery.

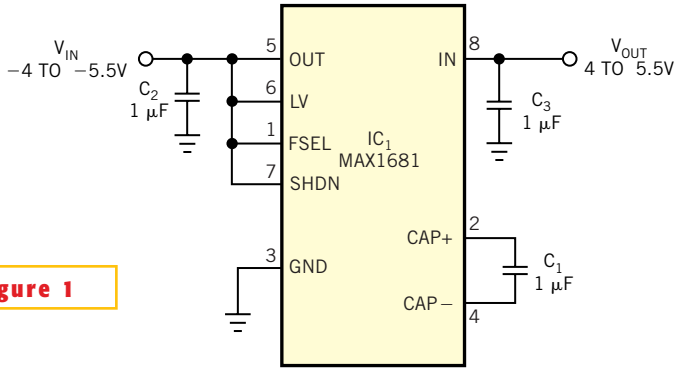
Although the resistor values shown in **Figure 2** apply to a specific application, you can customize the circuit for a battery's chemistry, capacity, internal resistance, cell count, and timer and display options. You can calculate component values via a Microsoft Excel 2002 spreadsheet in the Web version of this Design Idea at www.edn.com. All of the circuit's low-profile, surface-mounted components fit on one side of a 1.8-sq-in., four-layer board. The switches and LED readout connect to the pc board's underside.□

Charge pump converts −5V to 5V

Ken Yang, Maxim Integrated Products Inc, Sunnyvale, CA

Versatile switched-capacitor charge-pump voltage converters can provide a negative supply voltage from a positive-voltage source or double a positive source's voltage. However, certain applications that consist entirely of ECL (emitter-coupled-logic) circuits provide only a negative-voltage supply—for example, −5.2V. **Figure 1** shows how you can use a switched-capacitor converter to obtain a positive power-supply voltage suitable for powering ECL-to-TTL (transistor-to-transistor-logic)-level translators and other circuits.

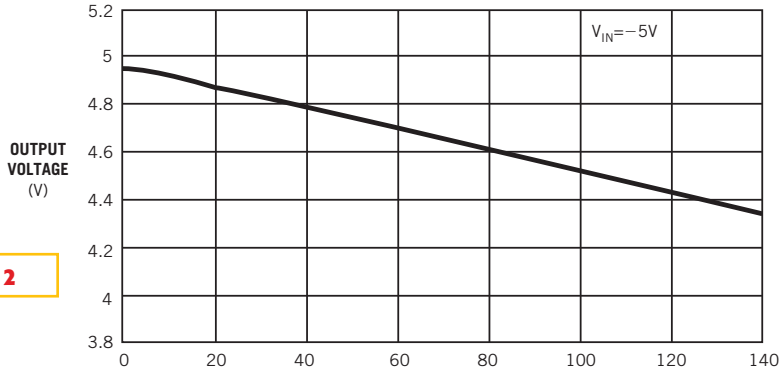
Figure 1



The "backwards" switched-capacitor converter converts −5V to 5V.

Although connections to IC_1 may appear to be reversed, the bilateral characteristics of IC_1's internal switches allow use of IC_1's output pin as its power input. Capacitor C_1 acquires a charge when IC_1's internal switches connect the CAP+ pin to ground and CAP− to the negative-voltage power source via the output pin, OUT. During the next half-cycle, IC_1 connects CAP− to ground and CAP+ to IN (normally used as the input), transferring C_1's positive charge to output capacitor C_3 and the load. With FSEL connected to OUT, an internal oscillator sets the charge-discharge cycle's frequency to approximately 1 MHz.

Figure 2



This load-voltage-versus-current graph shows the effects of the converter's nonzero output impedance on output regulation.

As **Figure 2** shows, IC_1's switches present internal resistances that affect the output voltage's magnitude, which is lower than the input voltage and subject to less-than-ideal regulation as output-load current increases. For optimum performance, use low-ESR capacitors for C_1, and input and output bypass capacitors C_2 and C_3.□

JFETs offer LC oscillators with few components

Herminio Martínez, Joan Domingo, Juan Gámiz, and Antoni Grau, Technical University of Catalonia, Barcelona, Spain

By using JFETs in unusual configurations, you can design simple, high-frequency LC oscillators with few passive components. The structure for implementing the amplifier stage comprises a JFET transistor that you configure as a common drain (**Figure 1**).

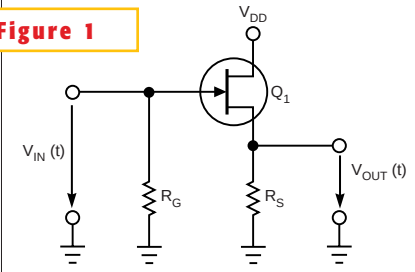
When the JFET transistor works in the saturation zone, the drain current, I_D, is:

$$I_D = \frac{I_{DSS}}{V_P^2} \times (v_{GS} - V_P)^2 = I_{DSS} \times \left(1 - \frac{v_{GS}}{V_P}\right)^2,$$

where I_{DSS} is the maximum saturation current and V_P is the pinch-off voltage. You can model the JFET in this saturation zone in the small-signal regime using an infinite input impedance and a current source that the gate-source voltage controls. The following **equation** determines the small-signal transconductance of the transistor:

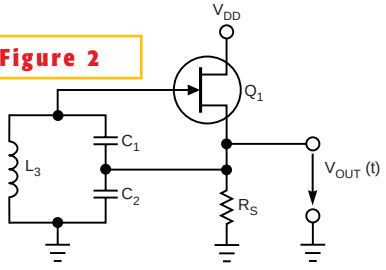
$$g_m = \frac{2I_{DSS}}{|V_P|} \times \left(1 - \frac{v_{GS}}{V_P}\right).$$

Figure 1



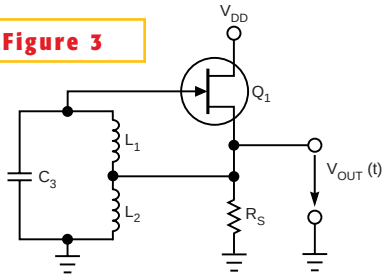
You can configure an amplifier stage, based on a JFET transistor, as a common drain.

Figure 2



To complete the oscillator circuit, you add an LC-resonant tank to the amplifier stage; the result is a Colpitts oscillator.

Figure 3



You can develop a Hartley oscillator based on a JFET transistor.

Gate resistance R_G provides the necessary connection from the gate to ground. Its typical value is in the low-megaohm range to provide the needed high impedance of the amplifier structure. Resistance R_S biases the transistor; the following **equation** determines resistance:

$$R_S = -\frac{V_{GSQ}}{I_{DQ}}.$$

To complete the oscillator circuit, you add an LC-resonant tank to the amplifier stage (**Figure 2**); the result is a Colpitts oscillator. The connection from the gate to ground for dc exists because of the inductance of the LC-resonant tank, removing the gate resistance of the amplifier.

Analyzing the circuit using the Barkhausen criterion, the frequency of oscillation f_O of the circuit is:

$$\omega_O = \frac{1}{\sqrt{L_3 \times \frac{C_1 \times C_2}{C_1 + C_2}}} \Rightarrow f_O = \frac{1}{2\pi\sqrt{L_3 \times \frac{C_1 \times C_2}{C_1 + C_2}}}.$$

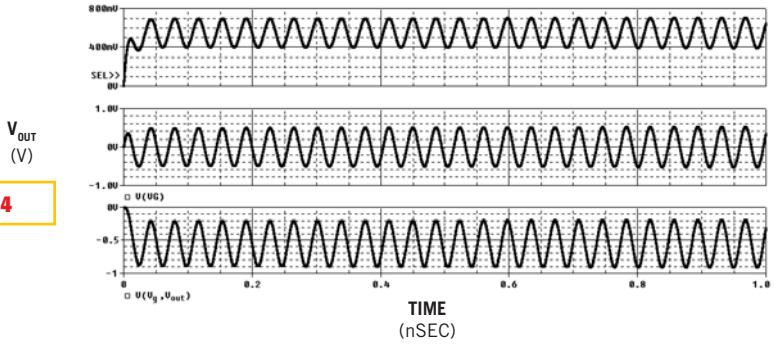
The necessary condition on the capacitors so that the circuit can oscillate is:

$$g_m \times R_S \geq \frac{C_1}{C_2},$$

or, equivalently, the voltage gain, A_V, of the amplifier stage, $V_{OUT}(t)/V_G(t)$, is:

$$A_V \geq \frac{C_1}{C_1 + C_2},$$

Figure 4



With C_1 having a value of 50 nF and C_2 having a value of 114 nF, the circuit oscillates.

where voltage gain of the common drain stage is:

$$A_V = \frac{g_m \times R_S}{1 + g_m \times R_S},$$

which demonstrates that the voltage gain in always lower than one.

Similarly, you can develop a Hartley oscillator based on a JFET transistor (**Figure 3**). The simulation and experimental results for the Colpitts oscillator circuit uses a 2N3819, an n-channel device, for the JFET. The PSpice parameters for this transistor are I_{DSS} of 12 mA and V_P of −3V. Simulation shows the voltage gain of the amplifier circuit is 0.3064V, and, with C_1 having a value of 50 nF and C_2 having a value of 114 nF, then

$$A_V = 0.3064 > \frac{C_1}{C_1 + C_2} = \frac{50}{164} = 0.3049,$$

and the circuit oscillates (**Figure 4**), which also shows the start-up process of the oscillator. The voltage gain also shows that the design meets the start-up conditions on the capacitors:

$$A_V = \frac{g_m \times R_S}{1 + g_m \times R_S} = 0.3064 \Rightarrow g_m \times R_S = 0.4417 > \frac{C_1}{C_2} = \frac{50}{114} = 0.4386.$$

Note that transconductance of the transistor is equal to the value of the slope of the curve $i_D = f(V_{GS})$ at this operating point. Depending on this point, the actual value of the transconductance will be larger or smaller. Confirming this value, when oscillations start up, the curve $i_D = f(V_{GS})$ restricts the amplitude of the output signal due to the reduction of the transconductance when V_{GS} decreases to values close to the pinch-off voltage; in this zone of the curve, its slope and, therefore, the transconductance is smaller. The intrinsic nonlinearity of the JFET transistor limits the gain of the amplifier stage, and no additional circuit stabilizing the amplitude of the output signal is necessary.□

Autostart circuit helps ATX motherboards resume operation after power interruptions

William Mohat , Ameritech, Cleveland, OH

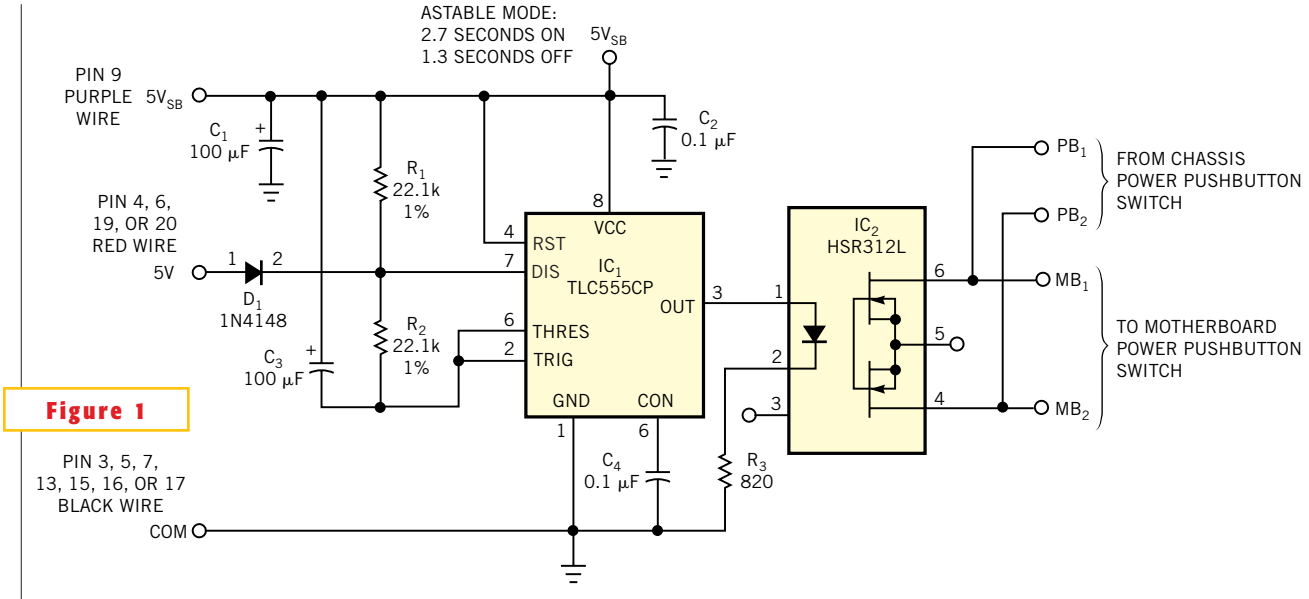


Figure 1

An inexpensive CMOS 555 timer generates power-on-switch closures upon restoration of ac power.

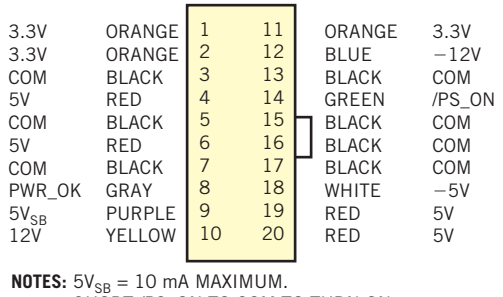
Unlike legacy PC motherboards, an ATX-style motherboard controls its power supply's on/off state. If ac power fails, many ATX motherboards do not automatically restart when power returns, and that behavior is unacceptable for a server system that must provide near-continuous service. Although some PCs provide BIOS configuration selections for "wake-on-LAN" or "wake-on-modem" operation, these options depend on another computer to provide the wake-up call. A few ATX motherboard chip sets offer an "always-on" BIOS option, but chances are, the motherboard that's available for your server system isn't one of these.

The circuit design in **Figure 1** offers a reliable method of recovery from a power interruption. Upon restoration of ac power, an ATX power supply delivers a standby voltage of 5V dc at a maximum of 10 mA via Pin 9 of its power connector (**Figure 2**). With standby power available, low-power CMOS timer TLC555 CP IC$_1$ functions as an astable oscillator and delivers pulses at approximately 4-sec intervals to MOSFET-output optoisolator IC$_2$. The output of IC$_2$ connects in parallel with the PC's front-panel power-on switch and in effect "pushes the power switch" every 4 sec.

In most astable-oscillator designs based on the generic 555 timer, timing capacitor C$_3$ connects from pins 2 and 6 to ground. Upon initial application of power, IC$_1$'s output goes low, activating IC$_2$ and generating an immediate power-on signal. Depending on the motherboard's design, an immediate start-up signal may cause the motherboard to lock up. Connecting C$_3$ as shown eliminates the initial start-up pulse.

When the power supply switches on, primary 5V power becomes available at pins 4, 6, 19, and 20, driving diode D$_1$ into conduction and biasing Pin 7 of IC$_1$ to a level that stops oscillation. Although IC$_1$'s output (Pin 3) can directly drive a motherboard's power-on input, MOSFET-output optoisolator IC$_2$ removes the need to trace the polarity of the power-on switch's connections. In addition, IC$_2$ eliminates any possibility of incompatible logic levels that some 3.3V motherboards impose.

You can assemble the start-up circuit on a small section of prototyping board and splice its connections into the power supply's wiring harness and power-on pushbutton wiring. Variants of ATX connectors exist, so verify wiring before connecting the start-up circuit.□



NOTES: 5V$_{SB}$ = 10 mA MAXIMUM.
SHORT /PS_ON TO COM TO TURN ON.

Figure 2 **This view of an ATX power supply's connector shows color codes. Pinouts may differ slightly from manufacturer to manufacturer.**