Power-supply interrupter fights ESD-induced device latch-up

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Under certain conditions, ESD events can damage digital circuits by causing latch-up. For example, when ESD triggers them, parasitic transistors normally formed as parts of a CMOS device can behave as an SCR (silicon-controlled rectifier). Once ESD triggers, the SCR presents a low-resistance path between portions of the CMOS device and conducts heavily. Damage to the device can result unless you immediately remove power from the circuit. ESD from human interaction presents a significant problem for mobile industrial and medical devices. For adequate ESD protection, most medical and industrial devices require a grounded return path for ESD currents. In the real world, mobile devices may serve in environments in which properly grounded power outlets are unavailable.

To protect expensive equipment from latch-up failures even when no ESD ground is present, you can add the power-interruption circuit shown in **Figure 1** to prevent damage when ESD-induced latch-up occurs. Under normal conditions, current drawn by ESD-susceptible devices develops a small voltage across sense resistor R_6. A voltage divider formed by R_4 and R_5 defines a reset-current threshold for the LED portion of optoisolator IC_1, and, under normal operational current consumption, the LED remains dark.

The output of IC_1 controls the gate bias applied to MOSFET Q_1, which is normally on. When latch-up occurs, power-supply current drain rapidly increases by an order of magnitude or more. The large voltage drop developed across R_6 forward-biases IC_1's LED, which in turn drives IC_1's phototransistor into conduction and shuts off Q_1, interrupting dc power to ESD-susceptible devices for several milliseconds. In addition, the system's firmware design must allow for automatic recovery from a power interruption.

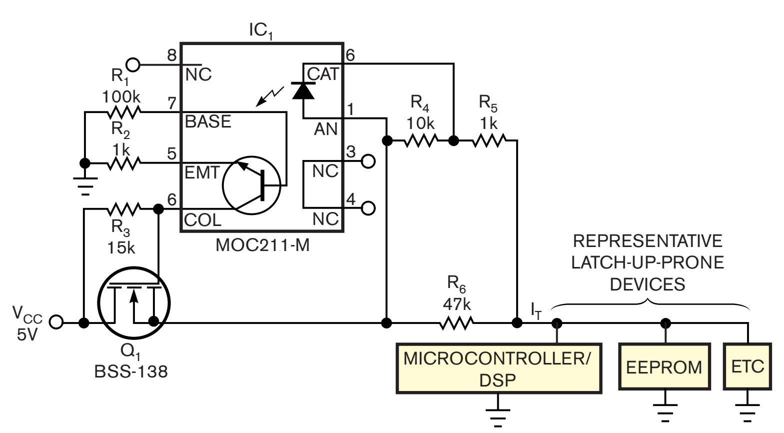

Figure 1 Upon sensing an overcurrent spike, this circuit interrupts power and enables the circuit's recovery from ESD-induced latch-up.

The following describes the relationship between the reset-current threshold and the values of R_4 and R_5: $(R_4+R_5)/R_4=(I_T \times R_6)/V_{LED}$, in which $I_T \geq (V_{LED})/R_6$, and $V_{CC}>V_{LED}$.

The ESD-induced fault threshold current, I_T, is greater than or equal to the optoisolator LED's conducting forward-voltage drop divided by the value of sense resistor R_6. Also, the raw power-supply voltage must exceed the LED's forward-voltage drop. Resistor R_1 provides a path for IC_1's base-leakage current, and resistors R_3 and R_2 determine Q_1's gate-shutoff bias.

In **Figure 1**, the optoisolator presents an LED forward-voltage drop of 1.2V. For the component values shown, the circuit momentarily interrupts V_{CC} when ESD-induced power-supply current exceeds approximately 300 mA. Total cost of the six resistors, one MOSFET, and one optoisolator is approximately $1 (production quantities). EDN

High-impedance FET probe extends RF-spectrum analyzer's usable range

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Current models of spectrum analyzers routinely offer frequency responses that begin as low as 10 Hz. When you combine them with 1-Hz or narrower band FFT software, expanded low-frequency performance makes the modern spectrum analyzer an invaluable tool for designing and debugging high-performance analog circuits. Unfortunately, a spectrum analyzer that's primarily for RF typically presents an input impedance of 50Ω, a heavy load when you apply it to most high-impedance analog circuits. You can improvise a somewhat higher impedance probe by adding a 953Ω resistor in series with the 50Ω input, but this approach provides only a 1-kΩ input impedance and reduces the measured signal by 26 dB.

In addition, most RF-spectrum analyzers lack ac coupling, and, thus, any dc-input component directly reaches either the internal terminating resistor or the front-end mixer. To maintain a 10-Hz, low-frequency response, you must connect a coupling capacitor with a value of at least 2 μF in series with the 953Ω input probe. Although oscilloscopes' input circuits can withstand accidental probe contacts and capacitive-transient overloads, using a low-impedance, ac-coupled probe with a spectrum analyzer can lead to destruction of the analyzer's expensive and possibly hard-to-replace front-end mixer.

Although high-impedance probes are commercially available, they're expensive to purchase and repair. This Design Idea offers an alternative: an inexpensive and well-protected unity-gain probe that presents the same input impedance as a basic bench oscilloscope and can drive the spectrum analyzer's 50Ω input impedance. The probe has a gain of 0±0.2 dB at 100 kHz. Input impedance is 1 MΩ, 15 pF, and maximum input is 0.8V p-p. Load impedance is 50Ω, and frequency response is 10 Hz to 200 MHz at −3 dB. Passband ripple is less than 1 dB p-p. Input noise at 1 MHz is less than 10 nV/$\sqrt{\text{Hz}}$. Distortion for 0.5V p-p input at 10 MHz is less than −75 dBc for second-order distortion and less than −85 dBc for third order. Power requirements are ±5V at 16 mA.

You can assemble the circuit in **Figure 1** in an afternoon from readily available and inexpensive components. The circuit's input presents the same characteristics as a bench oscilloscope—a 1-MΩ resistance in parallel with 15 pF of capacitance. You can also use this active probe in place of standard 1-to-1 or 10-to-1 oscilloscope probes, thus extending the design's applicability. The back-to-back silicon diodes in the D_1 clamp the input signal to plus or minus one forward-voltage drop, which limits signal excursions you apply to the spectrum analyzer's front end, thus protecting the input mixer from damage due to overloads and ESD. Because most users employ the probe and spectrum analyzer to measure small-amplitude signals and noise,

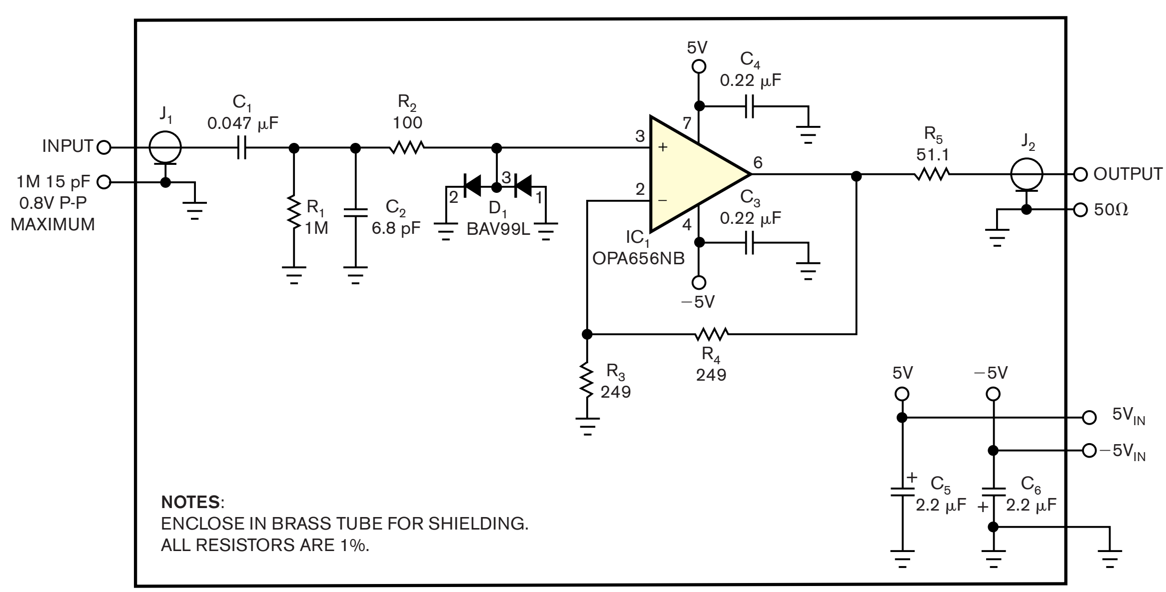

Figure 1 Just a handful of parts can help extend a spectrum analyzer's performance. This unity-gain probe emulates a standard oscilloscope probe's 1-MΩ and 15-pF input characteristics and easily drives 50Ω loads.

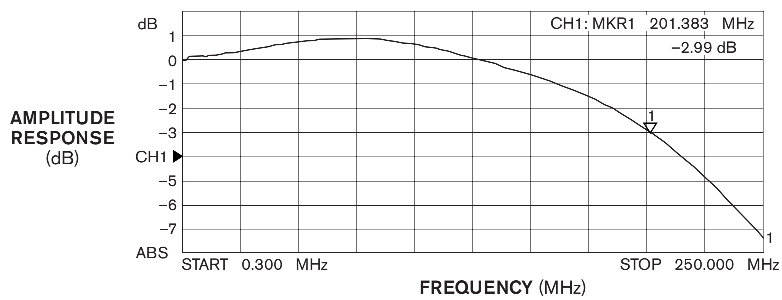

Figure 2 The probe's measured −3-dB frequency response extends from 10 Hz to 200 MHz with slightly less than 1-dB passband ripple, which compares favorably with the ±2-dB response of many commercial active-FET probes.

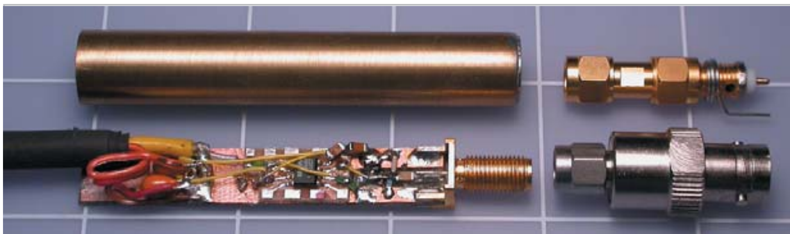

Figure 3 You can assemble the probe on a piece of breadboard that fits into a section of brass tubing from model and hobby shops. An SMA input connector matches a multitude of adapters and probe tips, a few of which are shown. Use a rubber grommet to close the probe's output end.

the limited large-signal response does not affect most applications.

High-performance FET input operational amplifier IC_1, a Texas Instruments OPA656, provides a voltage gain of two. This configuration yields a bandwidth of approximately 200 MHz (**Figure 2**). The OPA656 can drive 50Ω back-matched loads for a total load of 100Ω, which results in a 6-dB gain loss for which IC_1's gain of two compensates for a net gain of unity. The OPA656 also introduces lower noise and distortion than that of most commercially available, active FET-based probes.

The probe in **Figure 3** fits into a small section of brass hobby tubing. The input connector comprises a small SMA edge-launch connector that you can easily adapt to other connectors, including the BNC and its many accessories. The probe requires 5 and −5V at approximately 18 mA each, which you can obtain from an instrument's probe-power connector if available or from a linear supply designed around an ac wall transformer. For best results, use 78L05 and 79L05 voltage regulators to stabilize the supply voltages.

Standard miniature 50Ω coaxial cable connects the probe to the measuring instrument. For the flattest frequency response and uniform gain, terminate the probe's output with 50Ω; the circuit requires no dc-output-blocking capacitor. EDN

Watchdog circuit protects against loss of battery charger's control signals

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Recharging a mobile phone's internal battery usually occurs under control of a proprietary charging algorithm that resides in the baseband controller. The charger connects to the internal battery through a P-channel-MOSFET switch of low on-resistance (**Figure 1**). A baseband controller supplies a PWM signal that drives the switch. To minimize power dissipation and consequent thermal problems in the phone, the charging supply—usually a plug-in transformer assembly—features internal current limiting and has specifications that correspond to the battery's chemistry and charge-recovery requirements.

However, if the baseband processor stalls for any reason, the nearly direct charger-to-battery connection could damage the battery. To circumvent the problem, another circuit monitors the charger's PWM input and disables the series power switch after a predetermined delay interval (**Figure 2**). The circuit operates independently of the baseband unit's processor and allows charging to resume when the PWM signal returns.

In this circuit, microprocessor supervisor IC_1, a Maxim MAX6321 that includes a watchdog circuit that can monitor software execution, drives IC_2, a normally open SPST analog switch. Components R_4, D_2, and C_1 protect IC_1 and IC_2 by limiting V_{CC} to a maximum of 5.1V. Resistor R_4's value isn't critical because the protection circuit's quiescent current is low at approximately 30 μA. Select R_4 to provide just enough current—for example, 0.5 mA—to bias zener diode D_1 into the "knee" of its characteristic V-I curve.

(continued on pg 76)

The protection circuit consumes no power except when the battery undergoes charging and therefore doesn't burden the battery. Supervisor IC_1 provides a $\overline{\text{RESET}}$ output that can serve as a charger-ready interrupt input to the baseband-controller CPU. The $\overline{\text{RESET}}$ output's open-drain structure allows its connection to other circuits that operate from different supply voltages. Supplying power to the watchdog and PWM circuits only during charging also prevents reverse current from flowing into the IC_1's $\overline{\text{RESET}}$ output and discharging the battery via a sneak path.

The timing diagram illustrates the circuit's operation when an active

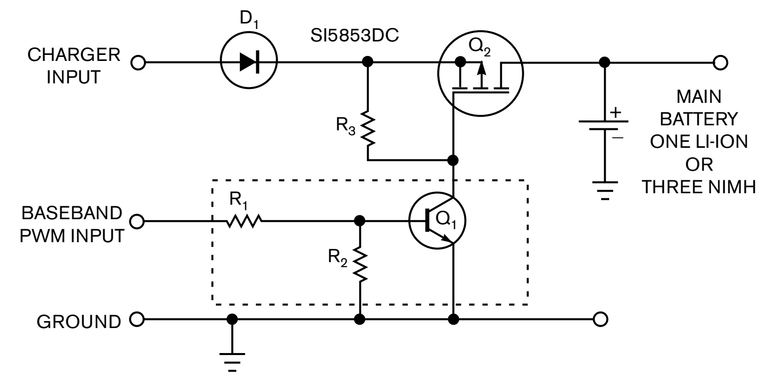

Figure 1 A typical mobile phone's battery-charger input circuit comprises a series switch controlled by a PWM signal.

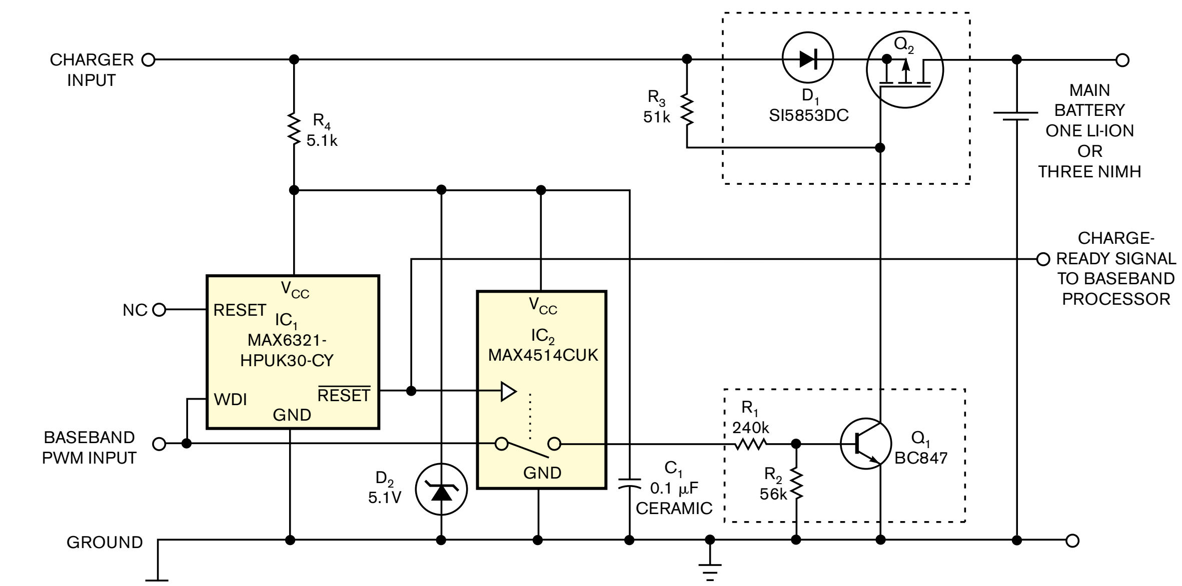

Figure 2 Adding watchdog protection to the circuit of Figure 1 guards against battery damage when the baseband processor stalls or ceases software execution.

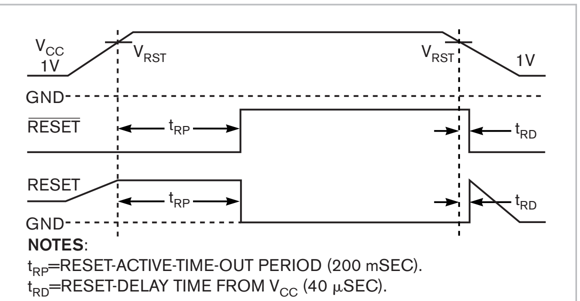

Figure 3 Reset-timing relationships for the circuit of Figure 2 illustrates its power-on behavior.

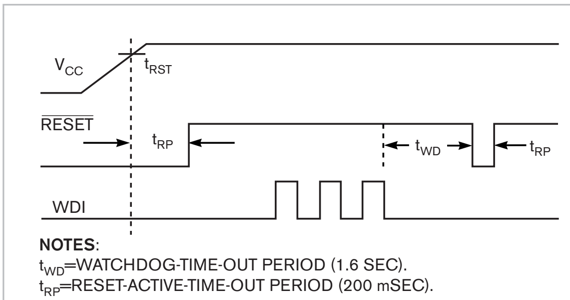

Figure 4 When PWM pulses cease, the watchdog circuit disables the charger after a 1.6-sec interval.

charger connects to the phone's charger-input socket (**Figure 3**). In this example, the MAX6321-HPUK30-CY that IC_1 uses is factory-trimmed for a 3V reset threshold, and the -CY suffix indicates complementary reset outputs and a 1.6-sec delay interval. The reset interval begins when V_{CC} reaches 3V±45 mV. After 200 msec, RESET goes low, and $\overline{\text{RESET}}$ goes high.

The $\overline{\text{RESET}}$ output releases the SPST analog switch, IC_2, which enables the PWM input. Meanwhile, the active WDI (watchdog input) monitors the PWM input signal. If no signal transitions occur within 1.6 sec, the RESET and $\overline{\text{RESET}}$ outputs become active, disabling the PWM input and pausing the charger algorithm using a CPU interrupt that the charger-ready signal conveys (**Figure 4**). All active and passive components for the circuit are available in surface-mount packages. Pass transistor Q_2, a Siliconix-Vishay SiS5853, includes an integrated Schottky diode, D_1. **EDN**

Circuit adds foldback-current protection

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For many applications that require power-supply currents of a few amperes or less, three-terminal adjustable-output linear voltage regulators, such as National Semiconductor's LM317, offer ease of use, low cost, and full on-chip overload protection. The addition of a few components can provide a three-terminal regulator with high-speed short-circuit current limiting for improved reliability. The current limiter protects the regulator from damage by holding the maximum output current at a constant level, I_{MAX}, that doesn't damage the regulator (**Reference 1**). When a fault condition occurs, the power dissipated in the pass transistor equals approximately $V_{IN} \times I_{MAX}$. Designing a regulator to survive an overload requires conservatively rated—and often overdesigned—components unless you can reduce, or fold back, the output current when a fault occurs (**Reference 2**).

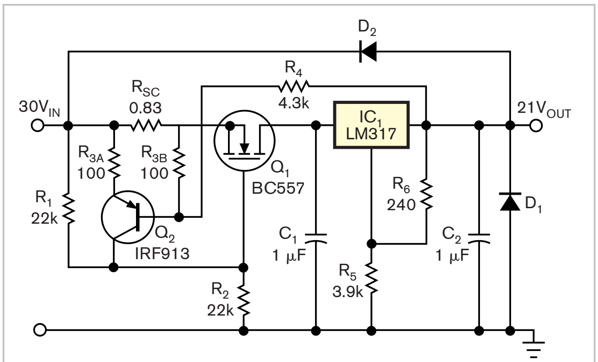

Figure 1 This circuit adds foldback-overcurrent protection to a linear regulator.

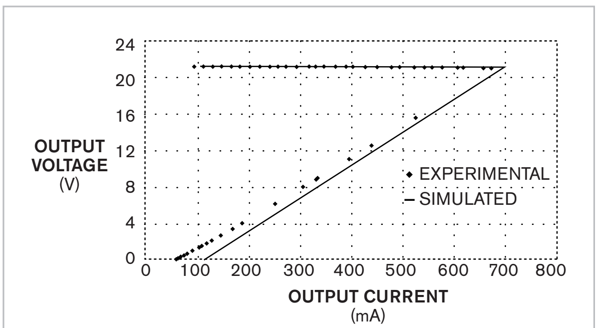

Figure 2 Simulated and measured foldback-current responses to a load resistance that varies from 200 to 0.01Ω show close agreement.

The circuit in **Figure 1** incorporates foldback-current limiting to protect the pass transistor by adding feedback resistor R_4. Under normal conditions, transistor Q_2 doesn't conduct, and resistors R_1 and R_2 bias MOSFET Q_1 into conduction. When an output overload occurs, Q_2 conducts, reducing the on-state bias applied to Q_1 and thus increasing its drain-source resistance and limiting the current flowing into regulator IC_1, an LM317. Adding R_4 makes Q_2's bias current dependent on the output voltage, V_{OUT}, which decreases under overload conditions.

For the circuit in **Figure 1**, you can calculate the maximum foldover and short-circuit currents, I_{KNEE} and I_{SC}, respectively, as follows:

$$I_{KNEE} = \frac{(R_3+R_4)\times V_{SENSE}}{R_{SC}\times R_4} - (V_{IN}-V_{OUT})\times\frac{R_3}{R_{SC}\times R_4}. \quad (1)$$

$$I_{SC} = \frac{(R_3+R_4)\times V_{SENSE}}{R_{SC}\times R_4} - V_{IN}\times\frac{R_3}{R_{SC}\times R_4}. \quad (2)$$

In a practical design, you select values for I_{KNEE} and I_{SC} and equal values for R_{3A} and R_{3B} and then use **equations 1** and **2** to calculate resistors R_{SC} and R_4. For the circuit in **Figure 1**, the output's maximum and short-circuit currents are fixed at 0.7 and 0.05A, respectively. With R_{3A} and R_{3B} set to 100Ω, solving the equations yields values of 0.73Ω for R_{SC} and 4.3 kΩ for R_4. You can demonstrate the circuit's performance by applying a variable-load resistor that's adjustable from 0 to 200Ω. As **Figure 2** shows, the output's simulated and measured voltage-versus-current characteristics, V_{OUT} and I_{OUT}, respectively, are in close agreement. **EDN**

REFERENCES

1. Hulseman, Herb, "MOSFET enhances voltage regulator's overcurrent protection," *EDN*, March 3, 2005, pg 74.
2. Galinski, Martin, "Circuit folds back current during fault conditions," *EDN*, Nov 28, 2002, pg 102.