LESSON 27:
MOS AND CMOS LOGIC

In this lecture you will study about unipolar logic families i.e., PMOS , NMOS and CMOS logic families.

On completion of this lecture you should be able to explain the following:

- MOS inverter.
- MOSFET NAND and NOR gates.
- Characteristics of MOS devices.
- CMOS Inverter.
- CMOS NAND and NOR gates.
- CMOS Transmission gate.
- Characteristics of CMOS devices.

27.1. MOS Logic

MOSFETs have become very popular for logic circuits due to high density of fabrication and low power dissipation. When MOS devices are used in logic circuits, there can be circuits in which either only p- or only n-channel devices are used. Such circuits are referred to as PMOS and NMOS logic respectively. It is also possible to fabricate enhancement mode p-channel and n-channel MOS devices on the same chip. Such devices are referred to as complementary MOSFETs and logic based on these devices is known as CMOS logic. The power dissipation is extremely small for CMOS and hence CMOS logic has become very popular.

The basic MOS gate is an inverter as shown in the figure 27.1, in which T_1 is an enhancement MOSFET which acts as driver and T_2 may be an enhancement (Fig. a) or depletion (Fig. b) MOSFET, which acts as load.

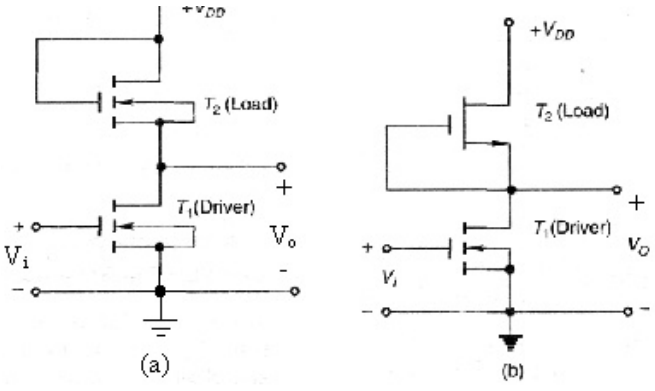

Fig 27.1: A MOS inverter with (a) Enhancement load (b) Depletion load.

Instead of fabricating diffusion resistor for load, which usually occupies an area, about 20 times that of a MOS device, MOSFET itself is used as the load. This makes possible high density of fabrication and therefore MOS logic made large-scale integration possible.

The logic levels for the MOS circuits are

$V(0) \approx 0$

$V(1) \approx V_{DD}$

Although the MOS logic circuits are identical in configuration to bipolar DCTL, the problem of current hogging is not present.

MOS logic is mainly used for LSI and VLSI ICs and not for SSI and MSI ICs. Most of the microprocessors, memories, and peripheral devices are available in NMOS.

27.1.1. MOSFET NAND and NOR Gates

NOR gates can be obtained by using multiple drivers in parallel, whereas for NAND gates the drivers are to be connected in series. A two-input NOR gate and a two-input NAND gate are shown in the figure 27.2.

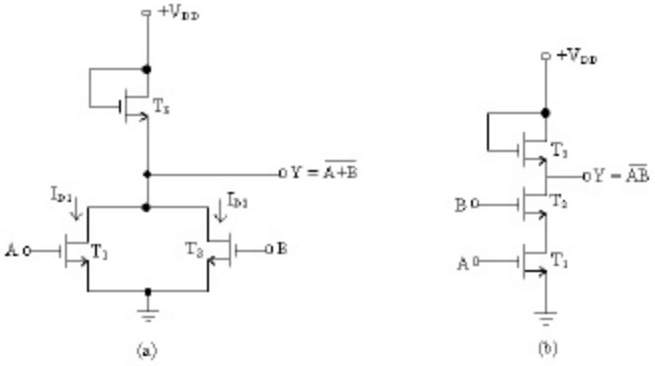

Fig 27.2: 2-input NMOS gates (a) NOR (b) NAND.

In the gate of Fig 27.2 (a), if both inputs are 0, both transistors T_1 and T_2 are OFF ($I_{D1} = I_{D2} = 0$), hence the output is V_{DD}. If either one or both of the inputs are $V(1) = V_{DD}$, the corresponding FETs will be ON and the output is 0 V. Its truth table is given in the table 27.1, which obviously shows NOR operation.

Inputs		Output
A	B	Y
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	0

Table: 27.1 Truth table of Fig: 35.2 (a)

In the gate of Fig 27.2 (b), if either one or both the inputs are V(0) = 0, the corresponding FETs will be OFF, the voltage across the load FET will be 0, hence the output is V_{DD}. If both inputs are V(l) = V_{DD}, both T_1 and T_2 are ON and the output is 0. Its truth table is given in the table 27.2, which shows NAND operation.

Inputs		Output
A	B	Y
0	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	0	V_{DD}
V_{DD}	V_{DD}	0

Table: 27.2 Truth table of Fig: 27.2 (b)

27.1.2. Fan-Out

Since MOS devices have very high input impedance, therefore, the fan-out is large. But driving a large number of MOS gates increases the capacitance at the output of the driving gate, which reduces, considerably, the speed of MOS gates.

The voltage and current parameters for 8085, 8086 microprocessors and other NMOS devices are:

V_{CC} = 5V, V_{IL} = 0.8V, V_{IH} = 2V, V_{OL} = 0.45V, I_{OL} = 2mA, V_{OH} = 2.4V,

I_{OH} = -400μA.

The input and output leakage currents are ±10mA.

These voltages are directly compatible with TTL ICs. Usually, NMOS devices are available with higher sink currents, which are directly compatible with TTL ICs. This helps in easy interfacing between NMOS devices and TTL devices.

27.1.3. Propagation Delay Time

The propagation delay time is large in MOS devices because of large capacitances present at the input and output of these devices. Also, the resistance through which these capacitors get charged and discharged is high.

In MOS devices, the phenomenon of minority charge storage is not present, and the speed of operation is mainly determined by the speed with which the capacitors get charged and discharged.

Due to the developments in the technology of MOS fabrication, it has become possible to obtain speeds, which are comparable to TTL.

27.1.4. Power Dissipation

In the NAND gate of Fig 27.2 (b), current is drawn from the power supply only during one of the four possible input conditions, whereas in the NOR gate of Fig 27.2 (a), power is drawn during three out of four input conditions. Therefore, the power consumption in MOS circuits is small which is very useful for large-scale integration.

27.1.5. Unconnected Inputs

MOS devices have very high input impedance and even a very small static charge flowing into this high impedance can develop a dangerously high voltage. This may cause damage to the device by rupturing the insulation layer and also to the persons handling such devices. Therefore, MOS ICs inputs must not be left unconnected. Even for storage of such devices, conductive foam or aluminium foil should be used which will ensure shorting of 1C pins together so that no voltage can be developed between the pins. Necessary precautions must be taken while handling such devices.

27.2. CMOS Logic

A complementary MOSFET (CMOS) is obtained by connecting a p-channel and an n-channel MOSFET in series, with drains tied together and the output is taken at the common drain. Input is applied at the common gate formed by connecting the two gates together (Fig. 27.3). In a CMOS, p-channel and n-channel enhancement MOS devices are fabricated on the same chip, which makes its fabrication more complicated and reduces the packing density. But because of negligibly small power consumption, CMOS is ideally suited for battery-operated systems.

Its speed is limited by substrate capacitances. To reduce the effect of these substrate capacitances, the latest technology known as silicon on sapphire (SOS) is used in microprocessor fabrication, which employs an insulating substrate (sapphire). CMOS has become the most popular in MSI and LSI areas and is the only possible logic for the fabrication of VLSI devices.

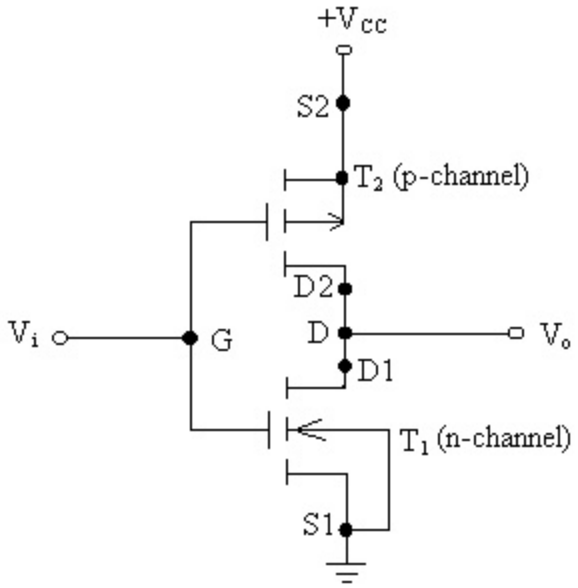

Fig: 27.3: A CMOS switch.

27.2.1. CMOS Inverter

The basic CMOS logic circuit is an inverter shown in Fig. 27.3. For this circuit the logic levels are 0V (logic 0) and V_{CC} (logic 1). When $V_i = V_{CC}$, T_1 turns ON and T_2 turns OFF. Therefore $V_o \approx 0V$ and since the transistors are connected in series the current I_D is very small. On the other hand, when V_i = 0V, T_1 turns OFF and T_2 turns ON giving an output voltage $V_o \approx V_{CC}$ and I_D is again very small. In either logic state, T_1 or T_2 is OFF and the quiescent power dissipation which is the product of the

OFF leakage current and V_{CC} is very low. More complex functions can be realized by combinations of inverters.

27.2.2. CMOS Nand and Nor Gates

A 2-input CMOS NAND gate is shown in Fig. 27.4 and NOR gate in Fig. 27.5. In the NAND gate, the NMOS drivers are connected in series, where as the PMOS loads are connected in parallel. On the other hand, the CMOS NOR gate is obtained by connecting the NMOS drivers in parallel and PMOS loads in series. The operation of NAND gate can be understood from Table 27.3. The operation of the NOR gate can be verified in the similar manner.

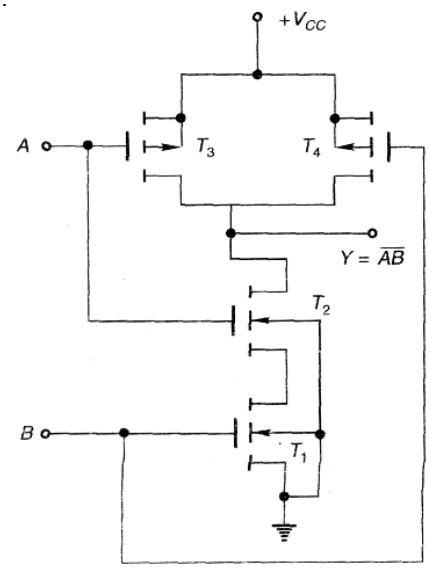

Fig: 27.4. A 2-input CMOS NAND Gate.

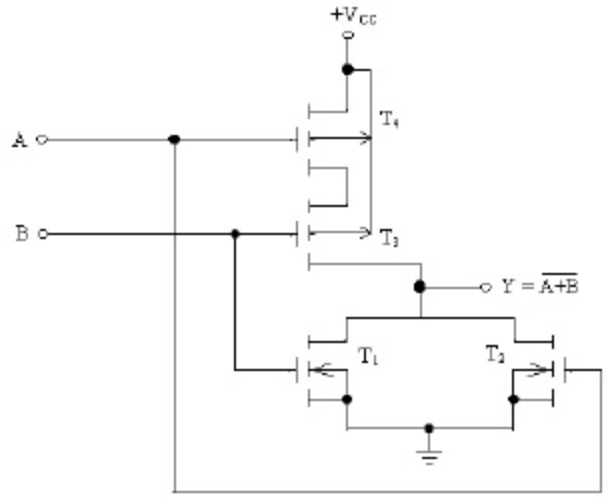

Fig: 27.5. A 2-input CMOS NOR Gate.

Table: 27.3. Operation of CMOS NAND Gate.

Inputs		State of MOS devices			Output
A	B	T_2	T_3	T_4	Y
0	0	OFF	ON	ON	V_{CC}
0	V_C	OFF	ON	OFF	V_{CC}
V_{CC}	0	ON	OFF	ON	V_{CC}
V_{CC}	V_C	ON	OFF	OFF	0

27.2.3. CMOS Transmission Gate

A CMOS transmission gate controlled by gate voltages C and $\overline{C}$ is shown in Fig. 27.6. Assume C = 1. If A = V(l), then T_1 is OFF and T_2 conducts in the ohmic region because there is no voltage applied at the drain. Therefore, T_2 behaves as a small resistance connecting the output to the input and B = A = V(l}. Similarly, if A = V(0), then T_2 is OFF and T_1 conducts, connecting the output to the input and B = A = V(0). This means the signal is transmitted from A to B when C = 1.

In a similar manner, it can be shown that if C = 0, transmission is not possible.

In this gate the control C is binary, whereas the input at *A* may be either digital or analog [the instantaneous value must lie between V(0) and V(l)].

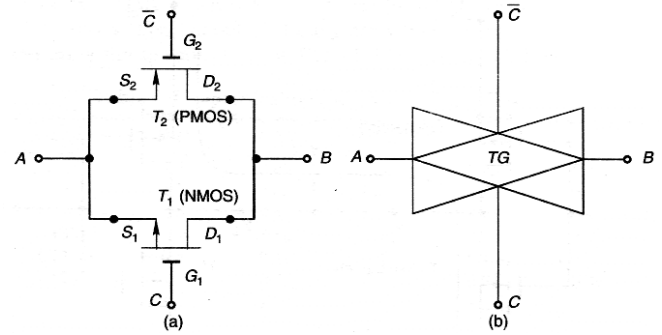

Fig: 27.6. (a) A CMOS Transmission Gate (b) Its symbol.

27.2.4. Noise Margin

Noise margin of CMOS logic ICs is considerably higher than that of TTL ICs. CMOS devices have wide supply voltage range and the noise margin increases with the supply voltage V_{CC}. Typically, it is 0.45 V_{CC}.

27.2.5. Unconnected Inputs

The unconnected CMOS ICs inputs behave in a way similar to MOS devices. Therefore, the unused inputs must be connected to either the supply voltage terminal or one of the used inputs provided that the fan-out of the signal source is not exceeded. This is highly unlikely for CMOS circuits because of their high fan-out.

Some CMOS ICs have Zener diodes connected at the inputs for protection against high input voltages.

27.2.6. Wired-logic

Figure 27.7 shows two CMOS inverters with their outputs connected together.

In this circuit,

(i) When A = B = V(0)

T_1 and T_1^1 are cut-off and Y = V(1) = V_{CC}

(ii) When A = B = V(1)

T_1 and T_1^1 are ON and Y = V(0) = 0

(iii) When A = V(1) and B = V(0)

T_1 and T_2^1 are ON whereas T_1^1 and T_2 are OFF.

Therefore, a large current I will flow as shown in Fig. 27.7.

This will make voltage at Y equal to V_{CC} /2 which is neither in the range of logic 0 nor in the range of logic 1. Therefore, the circuit will not operate properly. Also because of large current I, the transistors will be damaged.

Similarly, corresponding to A = V(0) and B = V(1) the operation will not be proper. Therefore, wired-logic must not be used for CMOS logic circuits.

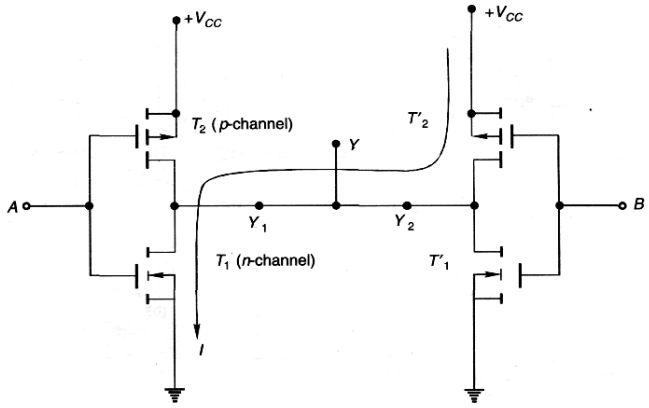

Fig: 27.7. CMOS inverters with outputs connected.

27.2.7. Open-drain Outputs

CMOS gates with open-drain output are available which are useful for wired-AND operation. In this the drain terminal of the output transistor (n-channel) is available outside and the load resistor is to be connected externally since p-channel load does not exist.

27.2.8. 54COO/74COO CMOS SERIES

There are two commonly used CMOS series ICs. These are the 4000 series and 54C/74C series. 54C/74C CMOS series is pin-for-pin, function-for-function equivalent to the 54/74 TTL family and has, therefore, become very popular. The temperature range for 54C series is -55 °C to + 125 °C and for 74C series is -40 °C to 85 °C. It has a wide supply voltage range, 3 V to 15 V. A person can take full advantage of his knowledge of the 54/74 TTL series for the effective use of 54C/74C series.

There have been significant improvements in 54C/74C series. The 74HC/74HCT have higher speed and better current capabilities. 74HC is known as high-speed CMOS and 74HCT is known as high-speed, TTL compatible CMOS series. 74AC/74ACT are very fast and have very high current sinking capabilities. These are known as advanced CMOS and advanced, TTL compatible CMOS, respectively. The 74 HC/74HCT/74AC/74ACT series can be operated at supply voltages in the range of 2-6 volts.

Table: 27.4. Specifications of CMOS IC Families.

Parameter	Load	74C	74HC	74HCT	74AC	74ACT	Units
V_{IH}		3.5	3.85	2.0	3.85	2.0	Volts
V_{IL}		1.5	1.35	0.8	1.35	0.8	Vo
V_{OH}	CMO	4.5	4.4	4.4	4.4	4.4	Vo
V_{OH}	TTL		3.84	3.84	3.76	3.7	Vo
V_{OL}	CMO	0.5	0.1	0.1	0.1	0.1	V
	TTL		0.33	0.33	0.37	0.3	V
I_{IH}		1	1	1	1	1	μ
I_{IL}		- 1	- 1	- 1	- 1	- 1	μ
I_{OH}	CMO	-0.1	-0.02	-0.02	-0.05	-	m
I_{OH}	TTL		-4.0	-4.0	-24.0	-24.0	m
I_{OL}	CMO	0.36	0.02	0.02	0.05	0.0	m
	TTL		4.0	4.0	24.0	24.0	m

The voltage and current parameters of various 74 CMOS series with 5 V supply voltage are given in Table 27.4. From the table, we observe that the output currents and voltages for 74HC/74HCT/74AC/74ACT are different when gates of these series are driving CMOS circuits and TTL circuits. 74 HCT and 74 ACT series are compatible with TTL series for input as well as output and therefore, can easily be used along with TTL ICs for optimum system design from the point of view of speed, power dissipation, noise margins, cost, etc.

The fan-out of 74 HC/74HCT series is 20, whereas for 74AC/74ACT series it is 50 while driving these CMOS series. The fan-out of these gates while driving various TTL series gates can be determined using the specifications of TTL (Table 25.1) and CMOS (Table 27.4).

With this we complete our topic of discussion **Logic Families**.

References

Modern Digital Electronics – R P Jain.