JFET 101, a Tutorial Look at the Junction Field Effect Transistor

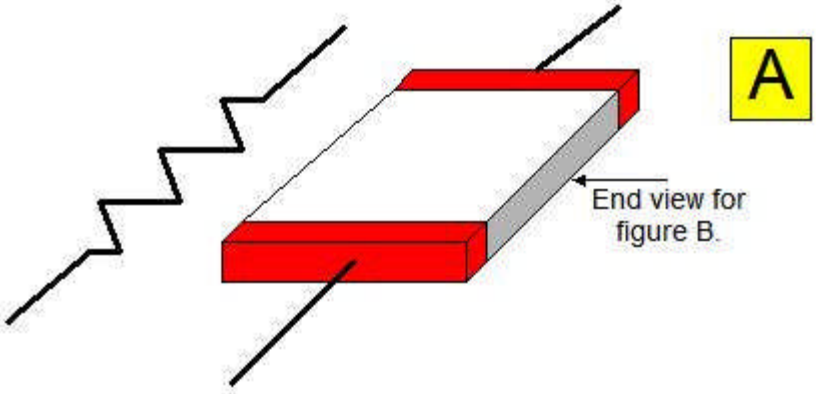
8May 2007, Wes Hayward, w7zoi

FETs are popular among experimenters, but they are not as universally understood as the bipolar transistor. This discussion presents a brief look at the junction field effect transistor, or JFET. The example we consider is a depletion mode, N-channel part. P channel parts represent an "obvious" extension.

An interesting, highly readable reference for this material is a short text by Thomas M. Frederiksen, "**Intuitive IC Electronics: A Sophisticated Primer for Engineers and Technicians**," McGraw-Hill, 1982. (ISBN 0-07-021923-0) He considers both bipolar and unipolar devices (FETs), although he emphasizes the former.

Basics

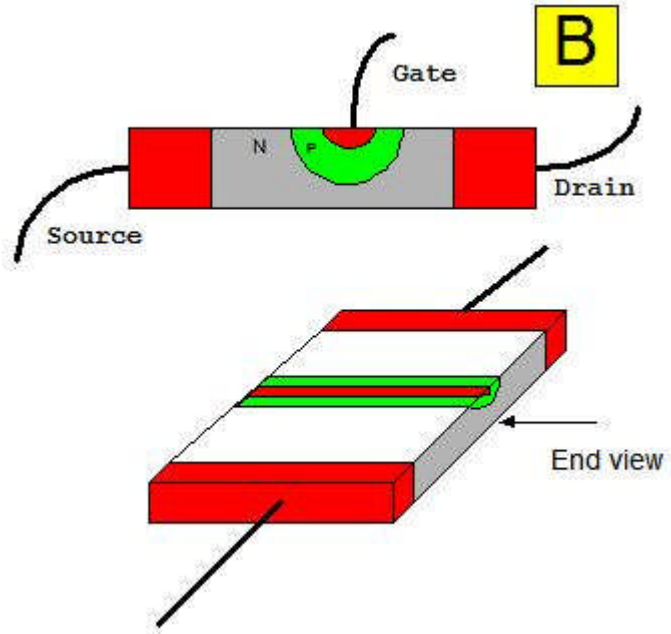
We begin our examination of the JFET with a look at Fig A, the basis for the part, which is a thin slab of N type semiconductor, usually silicon. Note that this, and the other sketches that follow represent simplified models. They do not really represent the real parts, but retain the vital characteristics.



The semiconductor is modified with "Ohmic" contacts, metalization that forms an interface between the semiconductor and wires leading to the outside world. Applying a voltage to this slab would show us that it is nothing more than a resistor. The current increases in direct proportion to the voltage, following Ohm's Law and justifying the resistor schematic model to the left of the sketch.

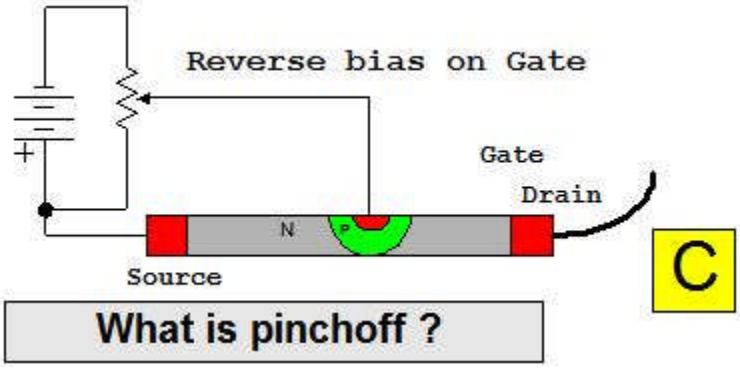
We now diffuse additional material into the slab, doping part of the structure

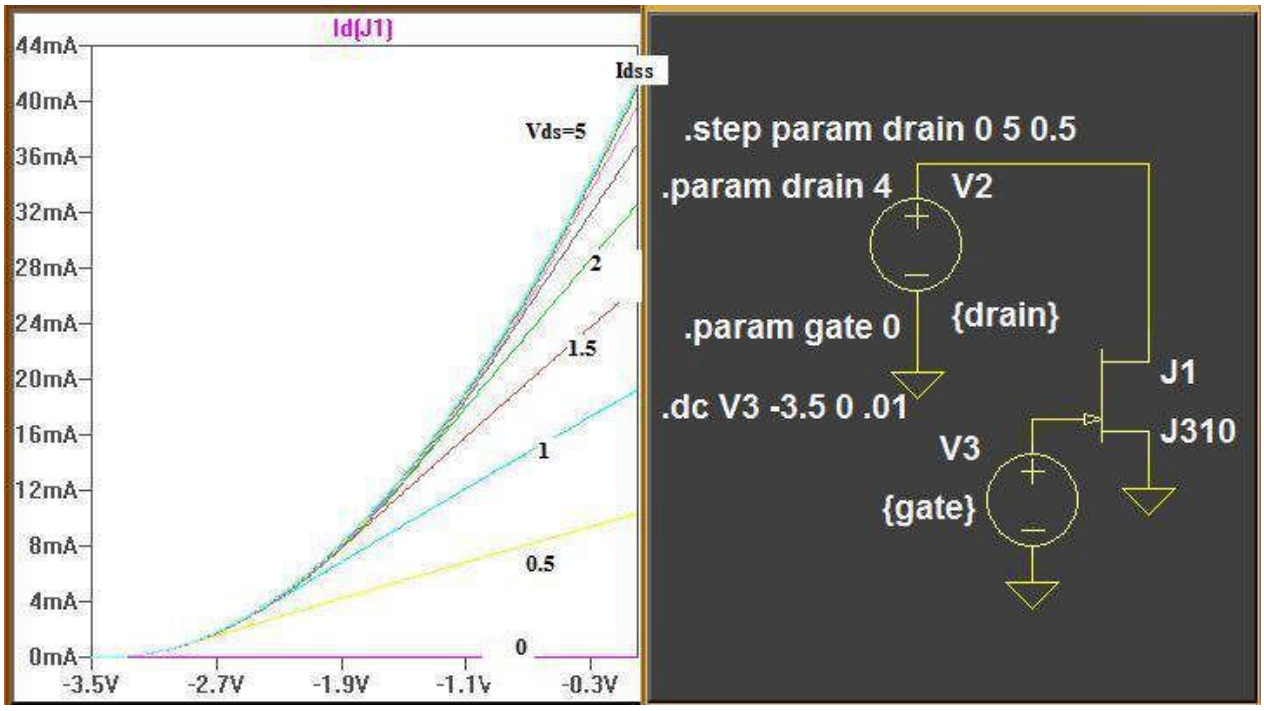
with a P type semiconductor. An additional Ohmic contact is applied, allowing us to attach a gate lead. This is shown with an end view detail and another sketch in Fig B below. As before, the red represents an Ohmic contact where a bond wire can be attached and eventually routed to a lead to the outside world.



Examination of the gate with either the source or the drain lead will show classic silicon diode action.

This structure is a three terminal device and we might expect, or at least hope that it has some triode-like properties. To tell, we attach a positive voltage source to the drain while the source is grounded. We then apply voltage to the gate lead. The results of this experiment are shown in the following Fig C. A graph and schematic (from a computer simulation) are below Fig C.





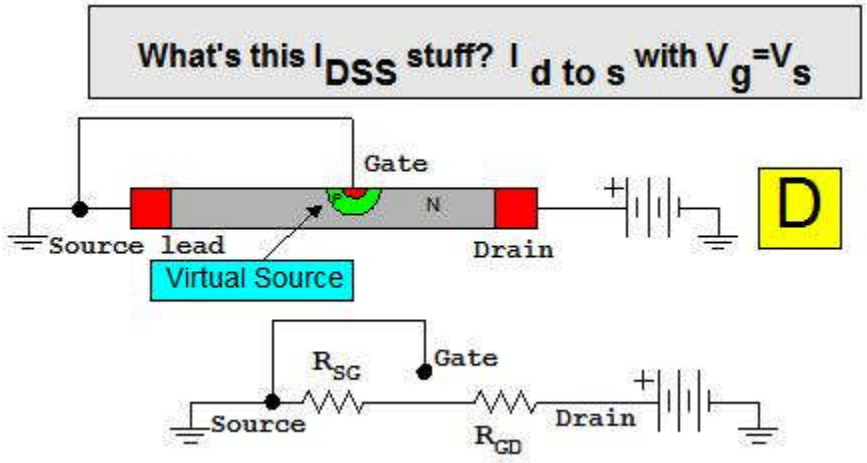
The drain current is plotted versus gate voltage for drain voltages from 0 to 5 volts.

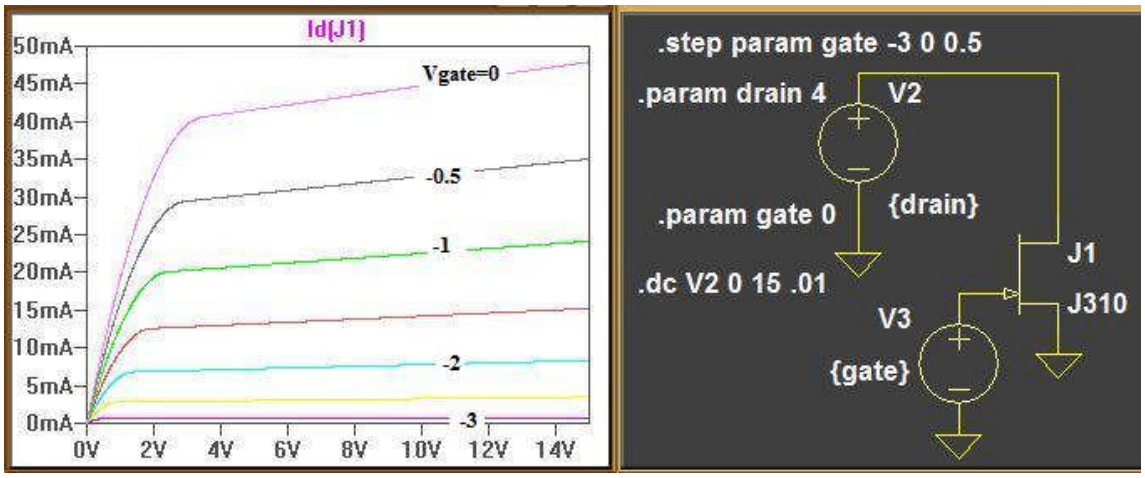
Once the drain is at 2.5 volts, the curves are essentially identical. The gate voltage where drain current drops essentially to zero is the ***pinchoff***. ***Idss*** is the maximum drain current observed when the gate voltage is zero with respect to the source. A positive voltage on the gate with respect to the source does little, for the diode action clamps the gate at 0.7 volts above the source. The pinchoff voltage is about -3.3 volts for the J310 used in this example. Remember that pinchoff is a negative voltage (for this J310 N-channel example), an important detail in equations that will follow.

Fig C shows the green diode depletion region touching the bottom of the channel between source and drain. Recall that the diode depletion region is that part of a junction diode where there are no carriers, P or N type. They have all been forced away by the electric field related to the diode reverse bias. As the gate bias increases above pinchoff, becoming less negative, the depletion region shrinks to allow conduction along the lower surface of the channel.

We mentioned above that positive gate bias did little to produce greater current. (Slight positive gate signals are allowed and often useful.) We then ask the question: What is the behavior with drain voltage, particularly with the gate lead attached to the source? Fig D below shows this state and includes some

characteristic drain curves.





Drain curves for the J310. The various curves are for a variety of gate bias values.

It is instructive to examine the graphics of D above while asking the question: Why is current approximately constant (at Idss) with a few volts of bias on the drain with Vgs=0?

Recall the initial graphic, A, where the FET channel was just a slab of semiconductor that behaved as a simple resistor. With drain bias, current flows through the N Channel semiconductor. Now consider the sketch of Fig D above. Current still flows and we still have a resulting voltage drop between the point labeled as the ***virtual source*** and the source terminal connecting to the external world. The gate voltage is set equal to that of the source. Hence, there is a negative bias applied to the diode which increases the size of the depletion region and reduces the FET current. An increase in drain voltage would "try" to make the drain current increase. But that would only produce greater bias that tries to reduce current. This is negative feedback that is

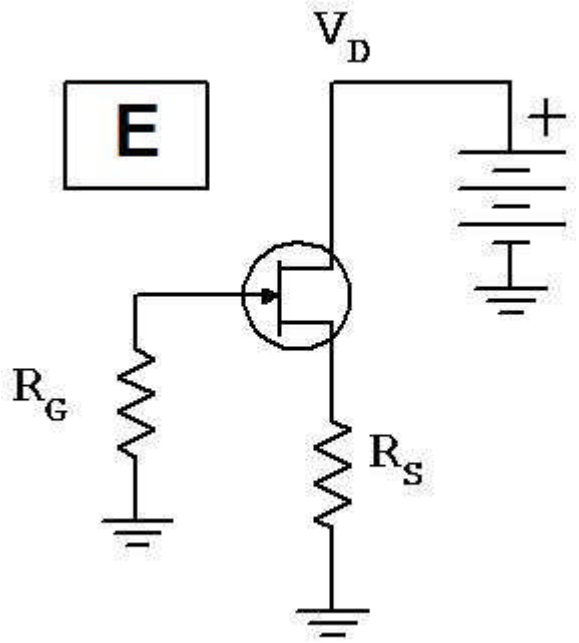
exactly the same as the emitter degeneration we use to stabilize the emitter current in a bipolar transistor. However, it is built into the JFET.

We see from the curves that the drain current reaches a magnitude close to Idss when Vds is approximately equal to or above the magnitude of the pinchoff. That is, our J310 with a -3.3 volt pinchoff is virtually at Id=Idss (about 42 mA) when Vd exceeds 3.3 volts. This behavior is typical of all JFETs.

The model presented here depicting the FET as a simple slab of semiconductor with a linear diode across it is highly simplified. The FETs we usually encounter have a more complicated shape and more complicated electric fields. The reader is referenced to the outstanding text by Gray and Meyer, **Analysis and Design of Analog Integrated Circuits**, 2nd Edition, Wiley, 1984, pp46-53, where a P-Channel JFET is analyzed. The parabolic curve shape that we saw in Fig C above is derived in that discussion. The internal voltage drop through the channel is shown to contribute to the FET behavior.

Designing with the JFET

The predominant method used to bias a JFET is implied from the discussion above and is shown in Fig E below. Resistance is added in series with the source. The voltage developed across this resistance causes the source voltage to increase with respect to the grounded gate. A positive voltage on the source has the same consequence as a negative one applied to the gate. There is negligible gate current because the gate is a reverse biased diode.



A source resistor Rs biases the FET. See text. The gate resistor Rg can be about any value, for DC gate current is extremely low.

A drain current value less than Idss should be chosen. We know that if Rs is set to zero, the drain current will be Idss, but the current will drop to zero when the source is above the gate by Vp, the pinchoff. The following experimental procedure is suggested: Install a large value Rs, perhaps 10K or more. Measure the voltage on the source; this will approximately equal the magnitude of the pinchoff. Then, short circuit the source to ground through a milliampmeter. That result will be Idss. The current value may not be very stable in time, for FET heating will cause changes, so be quick. If we performed this experiment with the J310, we would obtain values of -3.3 Volts for Vp and 42 mA for Idss.

The described experiment provides Vp and Idss values that will then let us bias the FET. A desired drain current Id<Idss is picked. The required source resistance value is then

$$R_S = \frac{V_p}{I_D} \cdot \left(\sqrt{\frac{I_D}{I_{DSS}}} - 1 \right)$$

At one time we measured some FETs with the procedure outlined and used it to determine biasing. This discussion is found on the VE7BPO web site,

http://www.qrp.pops.net. Further discussion appears in Introduction to RF Design, Chapter 1.

Rs established a drain current. To use the JFET as an amplifier, we need to know the transconductance. This is a gain figure of merit that tells us how much the drain current will change for a small change in gate voltage. The curve of Fig C above showed drain current as a function of gate voltage. The curve is not a straight line, but a parabola. When the FET is biased close to pinchoff with low DC drain current, the transconductance is low. There will be very little change in drain current if we "tickle" the gate with, for example, 1 millivolt of drive. The curve becomes steeper as the gate-source bias decreases from pinchoff with higher DC drain current. Transconductance is the slope of the curve of Fig C, evaluated at the DC bias point. gm is given by the following expression relating to the bias current, Id, the FET parameters Idss and Vp, and the source bias resistor Rs:

$$g_m = \frac{-2 \cdot I_{DSS}}{V_p} \cdot \left(1 + \frac{I_D \cdot R_s}{V_p}\right)$$

The usual JFET data sheet may well list transconductance. gm is NOT a characteristic of the FET, but rather is a parameter that is controlled by the biasing. The transconductance (gm) given in a FET specification sheet is a maximum value obtained when the FET is biased to Idss.

Consider an amplifier using a J310 that is to be biased at 10 mA. The calculations are shown below:

Remember that Vp is a negative number!

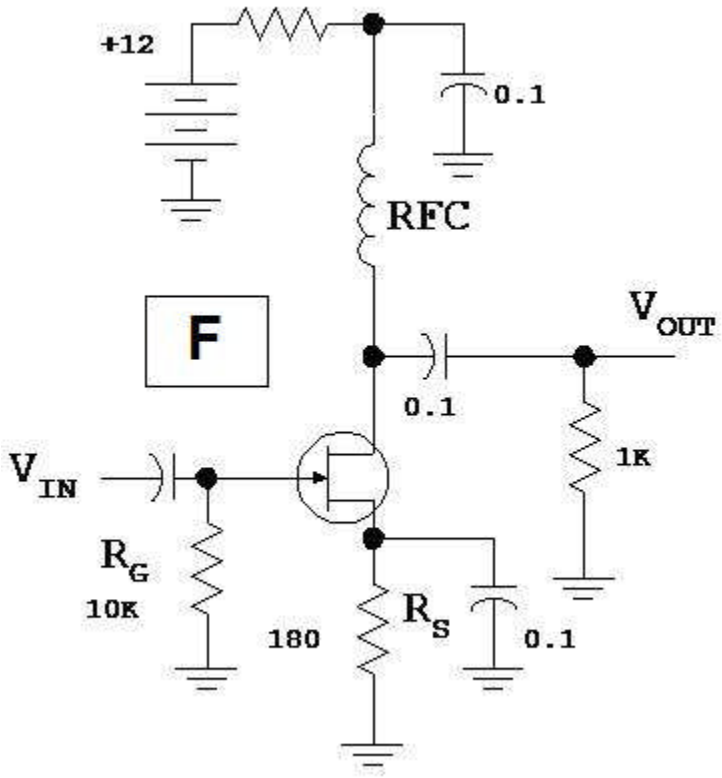
$$V_p := -3.3 \qquad I_{DSS} := .042 \qquad I_D := .01$$

$$R_s := \frac{V_p}{I_D} \cdot \left(\sqrt{\frac{I_D}{I_{DSS}}} - 1\right) \qquad R_s = 168.976$$

$$g_m := \frac{-2 \cdot I_{DSS}}{V_p} \cdot \left(1 + \frac{I_D \cdot R_s}{V_p}\right) \qquad g_m = 0.012$$

In practice we might pick standard Rs values of either 160 or 180 Ohms.

An RF amplifier based upon this analysis is shown below.



A small signal RF amplifier using a JFET. The source is bypassed with a 0.1 uF capacitor. This places the source at ground for RF signals, but does not compromize the bias stabilizing effect of Rs at DC.

Assume that this circuit is biased at 10 mA and that it is driven with a signal of 0.5 volts, peak-to-peak. We use a 100 Ohm decoupling resistor from the 12 volt supply. With 10 mA, there will be a 1 volt drop across the resistor, leaving an 11 volt supply on the FET drain. The amplifier design is shown below.

$V_{in} := 0.5$ $R_L := 1000$

$I_{sig} := g_m \cdot V_{in}$ $I_{sig} = -6.21 \times 10^{-3}$

$V_{out} := I_{sig} \cdot R_L$

$V_{out} = -6.21$

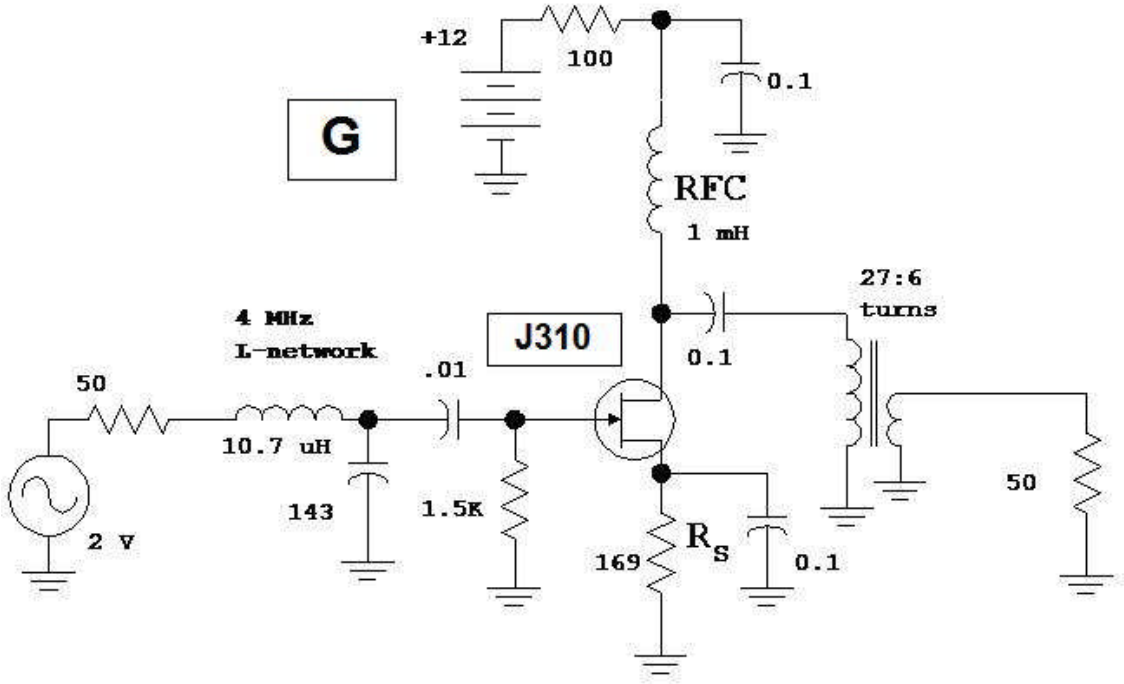
We see that the half volt signal will produce a drain current signal of 6.2 mA pk-pk, or 3.1 mA peak. The 6.2 mA is peak-to-peak, so the actual drain current excursion is from the DC value of 10 mA up to 13.1 mA, down to 6.9 mA, and back to 10 mA. The 1K load resistance is AC coupled to the drain. The drain is attached to the power supply with a Radio Frequency Choke, marked merely as RFC. An inductor is a component that resists an instantaneous change in current. Hence, the signal current from the drain will mostly flow in the 1K load resistor rather than in the inductor. This means that a 6.21 volt peak to peak signal will appear across the 1K resistor. The drain will go from 11 volts up to 14.1, down to 7.9, and back to 11 volts. The negative sign on the output voltage shows that the amplifier is inverting.

This is a simple analysis that does not take any FET capacitance into account. Still, this would be a practical circuit in the HF spectrum and lower.

An input of 0.5 volt produces an output voltage of 6.21 volts for a voltage gain of 12.4. Some folks might apply 20Log(Gv) to this to infer a gain of 21.9 dB. **This is WRONG!** The dB construct relates to the comparison of two power levels. The power is well established at the output because we have a known termination of 1000 Ohms. But the available input power is unknown, for the input source impedance is not even specified.

Let's modify this amplifier to have well defined impedances so we can actually calculate a meaningful power gain. We wish to measure the performance with our usual 50 Ohm instruments, so we will add networks at the input and output that will provide a 50 Ohm interface. The Rs resistor is set exactly to 169 Ohms to guarantee 10 mA for Id. Just to keep things stable (free from oscillation) and well defined, we pick a gate resistor of 1500 Ohms. An input matching circuit is then designed for operation at 4 MHz that uses the low pass form of an L-network. Wishing to measure output in a 50 Ohm load, we replace the 1K output load resistor with a transformer that makes a 50 Ohm load appear as 1K at the drain. Because impedance transforms in proportion to the square of a turns ratio, we need a turns ratio equaling the square root of 20, which is the impedance ratio. The turns ratio is then 4.47. An approximation would be a transformer with a 27 turn primary and a 6 turn secondary. This turns ratio is then 4.5 for a 20.25 impedance ratio. This would present an impedance of 1013 Ohms to the drain. A FB43-2401 ferrite bead might be a good choice for a transformer core. I measure these as having a single turn inductance of 370 nH, so the primary inductance would increase this value by 27 squared to 270 uH. The 6 turn output will have an inductance of 13.3 uH. Our amplifier circuit is shown in Fig G. We have included an

input source that is labeled as 2 volts. This is NOT a practical input value, but that won't hurt us so far as gain calculations are concerned.

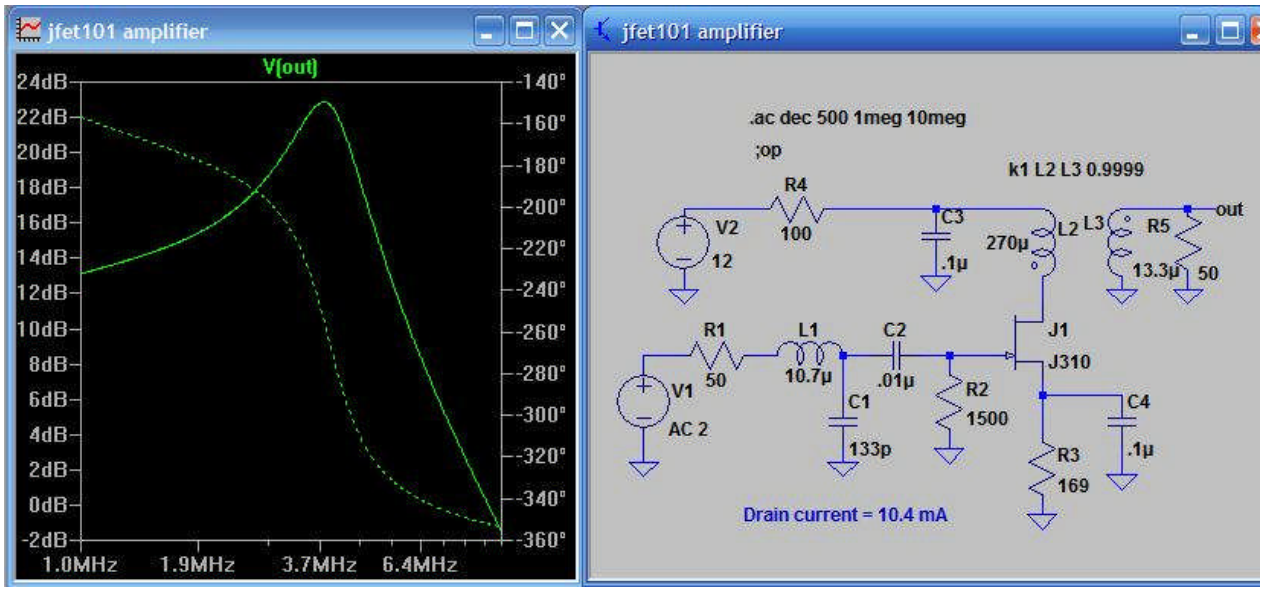


Let's now work our way through a gain calculation. First, consider the input. The 1.5K gate resistor terminates the L-network, causing an impedance of 50 Ohms to appear at the input side of the 10.7 uH inductor. The 50 Ohm generator with a 2 volt open circuit magnitude is properly terminated with 50 Ohms. Hence the input voltage to the matched amplifier is 1 volt. This is increased by the square root of the impedance ratio of 1500/50, resulting in 5.477 volts at the FET gate. (Again, don't worry about this being an impractical value.) Recall the transconductance value of .012 for the FET. So the 5.477 volts yields a drain current of .0657 Amps. The output transformer alters voltage and current in proportion to the turns ratio. If we apply the turns ratio to the drain current of .0657 A, a higher value by the ratio 27/6 will flow in the 50 Ohm resistor. The current in the load will then be 0.2958 A. The resulting voltage across the load will be IR, or 14.79 volts. The transducer power gain is then 20 Log (14.79) = 23.4 dB. We can now apply the dB construct with validity, for the impedances are well defined and equal at 50 Ohms.

The voltages are completely impractical. If this is a conceptual problem, use a 2 millivolt value for the input source to perform the calculations. The gain

results will be the same.

It is interesting to compare this calculation with a computer simulation in SPICE. These results are shown below.



The L-network capacitor was reduced by 10 pF to account for FET input C. Even with this adjustment, the peak response is at 3.78 MHz instead of 4 MHz. The peak gain is 22.86 dB while the SPICE predicted drain current was 10.4 instead of 10.0 mA.

The next logical step, which we will forgo at this time, is to build and actually measure this amplifier.