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How do ADCs work?

Martin Rowe, Senior Technical Editor -- 7/1/2002
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If you asked me to nominate one electronic component as the workhorse inside test-and-measurement equipment, I'd nominate the analog-to-digital converter (ADC). ADCs convert voltages that represent real-world signals into bits that microprocessors and software use to manipulate test data and control test equipment. Even if you work on digital signals exclusively, you probably use an ADC in an oscilloscope to look at the analog characteristics of your signals.

ADCs come in several basic architectures, although many variations exist for each type. Different types of test equipment need different types of ADCs. For example, a digital oscilloscope needs high digitizing speeds but can sacrifice resolution. Some PC-plug-in digitizers and RF test equipment use subranging ADCs, which provide better resolution than flash converters, but at the expense of speed. General-purpose data-acquisition equipment usually falls between scopes and DMMs for sample speed and resolution. This type of equipment uses successive-approximation register (SAR) or sigma-delta converters. A digital multimeter (DMM) needs fine resolution and can sacrifice high measurement speeds.

Figure 1 provides a graph of resolution versus sample rate and shows where the basic ADC types fit on the graph. I'll explain how each ADC works, starting with the fastest ADCs—flash converters—and proceeding toward the slow, high-resolution integrating dual-slope converter.

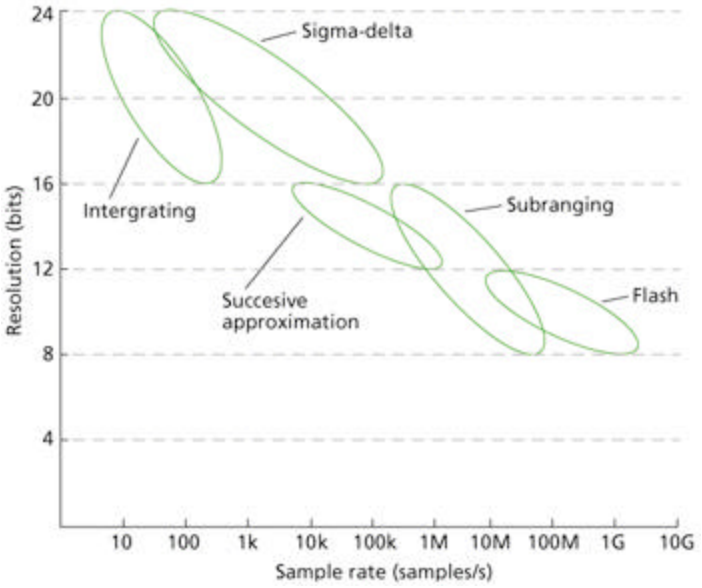

Figure 1. ADC architectures cover differing ranges of sample rate and resolution.

Flash converters

Most high-speed oscilloscopes and some RF test instruments use flash ADCs because of their fast digitizing rate, which now reaches 5 Gsamples/s for off-the-shelf devices and 20 Gsamples/s for proprietary designs. The typical flash converter resolves analog voltages to 8 bits, although some flash converters can resolve 10 bits.

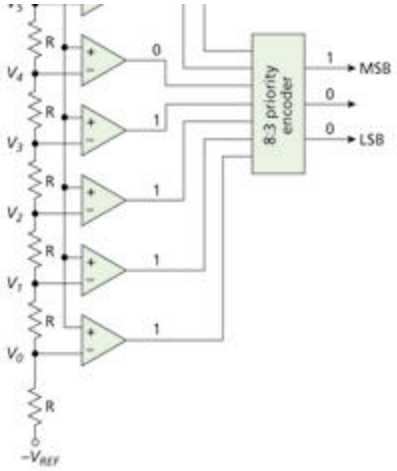

Figure 2. A parallel flash ADC requires 2^N–1 comparators for *N* bits of resolution.

Figure 2 shows a simplified block diagram for a parallel flash converter. For simplicity, I've depicted a 3-bit converter, but the concept extends to other resolutions. Parallel flash converters use a bank of comparators that compare the input voltage to a set of reference voltages across a resistor network. The voltages start at a value equal to that for one-half the least-significant bit (LSB) and increase in equal voltage increments equivalent to one LSB for each comparator. As a result, a 3-bit flash ADC requires 2^3–1, or seven, comparators. Each comparator's output represents one LSB. An 8-bit flash converter uses 255 (2^8–1) comparators.

As the input voltage increases, the comparators set their outputs to logic 1 starting with the lower-most comparator. Think of the converters as being like a mercury thermometer. As temperature increases, the mercury rises (Ref. 1). Likewise, as the input voltage increases, comparators referenced to higher voltages set their outputs from 0 to 1. In Figure 2, the input voltage falls between V_3 and V_4, so the four lower comparators have logic-1 outputs while the upper three comparators have logic-0 outputs. A digital encoder circuit converts the comparator outputs into a 3-bit binary-weighted code.

Flash converters are fast, but they have drawbacks. Because they require so many comparators, flash ADCs consume considerable power, making them impractical for battery-powered equipment.

Subranging ADCs

A subranging ADC uses fewer comparators than parallel flash ADCs. Instead of using one comparator per LSB like a flash converter does, a subranging ADC uses fewer comparators, draws less power, has lower input capacitance, and can attain higher resolutions.

Although not as fast as a parallel ADC, subranging (also called pipelined) ADCs can digitize at speeds greater than 100 Msamples/s at 8-bit resolution. They can resolve signals to 16 bits at slower speeds. Subranging ADCs often find use in RF test equipment, lower-speed digitizing oscilloscopes, and high-end PC plug-in digitizer cards and PC-external data-acquisition systems.

Figure 3 shows a block diagram of an 8-bit subranging ADC that uses two 4-bit stages to digitize the analog input signal. The first ADC converts the upper 4 bits while the second stage converts the lower 4 bits. This design uses 30 comparators (15 for each ADC) rather than the 255 comparators required by an 8-bit flash converter. A 12-bit subranging ADC may use two 6-bit stages, three 4-bit stages, or four 3-bit stages.

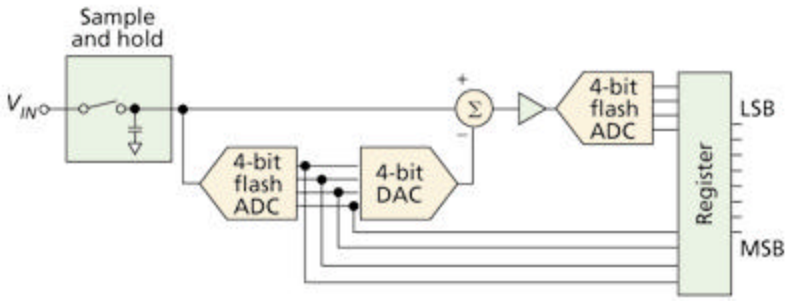

Figure 3. A subranging ADC uses two or more flash converters and a DAC following all but the last flash converter.

When the sample-and-hold amplifier stores a sample, the first stage's 4-bit flash ADC digitizes the signal and sends its output to a 4-bit digital-to-analog converter (DAC). A summing junction subtracts the DAC's output from the sampled input voltage. An amplifier boosts the remaining analog voltage and sends it to the next stage. (Ref. 2).

Subranging ADCs generally use extra bits in the latter stages to correct errors made in earlier stages. For instance, a 12-bit ADC might comprise three stages: 4-bits, 5-bits, and 5-bits. Buffer registers store the results from the early conversions, and appropriate logic is used to combine the bits from each stage at the output.

SAR converters

When you need resolution from 12, 14, or 16 bits, but you don't need the speed of a subranging ADC and you want to use a lower cost device that draws less power, look for equipment that contains an SAR. SAR converters are by far the most popular ADCs in measurement products. If you use a PC plug-in data-acquisition board or PC-external data-acquisition system, you probably use an SAR converter. Some SAR converters have less than 12 bits of resolution, but they're generally not used in test equipment.

Currently, SAR converters resolve voltages to 16 bits with sampling speeds of about 100 ksamples/s (Ref. 3). Some 12-bit SAR converters digitize at speeds faster than 1 Msamples/s.

At the start of a conversion, the SAR converter sets its successive-approximation register's output so that all bits except the MSB produce logic 0. That sets the DAC's output (**Figure 4**) to one-half of the device's full-scale input. The comparator sets its output based on the difference between the DAC's output and the sampled voltage.

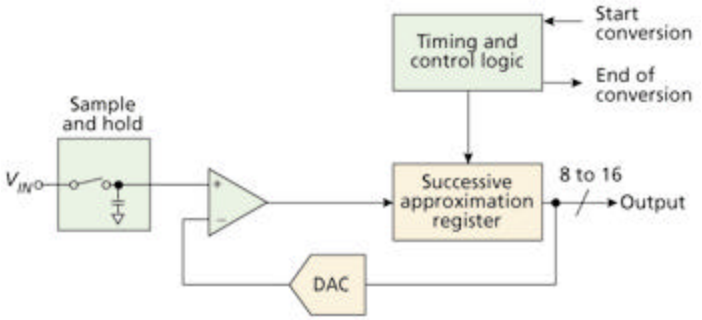

Figure 4. Successive approximation register (SAR) converters use a comparator and a DAC to close in on V_{IN}.

For example, consider an 8-bit SAR converter (**Figure 5**). The register's output starts at 10000000. If the input voltage is less than one-half of the ADC's full range, then the comparator's output goes (or stays) low. That forces the register's output to 01000000, which changes the DAC's output voltage to the comparator. If the comparator's output stays low, then the register's output changes to 00100000, and so on. SAR converters, therefore, need one cycle for each output bit, or *N* cycles for an *N*-bit converter. A 16-bit SAR converter takes longer than twice the conversion time of an 8-bit SAR converter, because the output must settle to one bit in 65,536, where an 8-bit ADC needs to settle to one bit in 256.

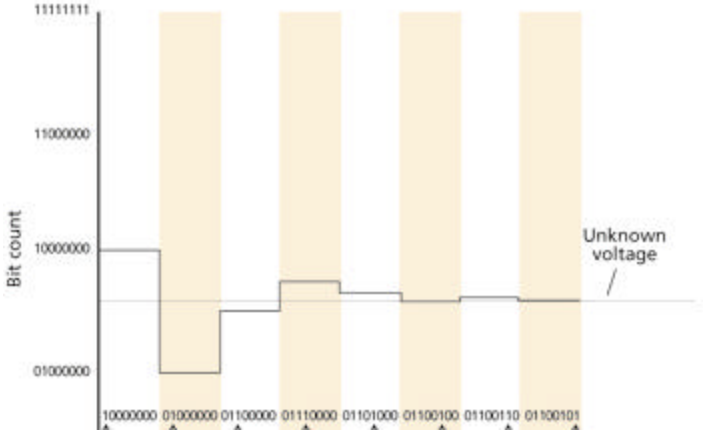

Figure 5. SAR converters approximate an unknown voltage starting from half of full scale, moving in on the final output by decreasing steps until reaching the LSB.

Sigma-delta converters

Many measurement applications don't need the conversion rates possible with SAR converters, but the applications need finer resolution. Sigma-delta ADCs can provide resolution as fine as 24 bits and they can trade resolution for speed. At 16 bits, you can get sample rates up to about 100 ksamples/s. At 24 bits, the ADC's speed drops to around 100 samples/s or lower, depending on the device.

Sigma-delta ADCs find use in digitizing audio-frequency signals. You'll find them in some PC-external data-acquisition systems and in vibration test equipment. Sigma-delta ADCs also find widespread use in weighing systems and temperature-measurement applications, which don't need high-speed sampling but often need resolution finer than 16 bits. Many chart recorders and dataloggers also use sigma-delta ADCs.

Sigma-delta ADCs are far more complex than other ADC types. The block diagram in **Figure 6** shows the basic components of a sigma-delta ADC. A sigma-delta ADC with a 100-ksamples/s conversion rate that uses 128X oversampling will sample the incoming analog signal at 12.8 Msamples/s.

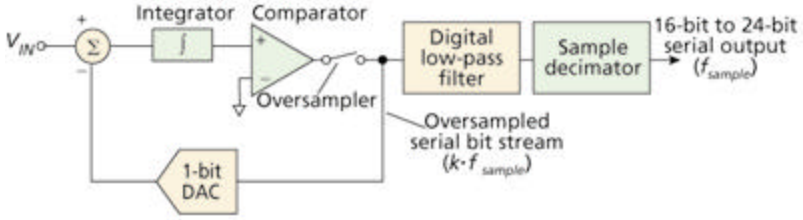

Figure 6. Sigma-delta ADCs use a comparator and 1-bit DAC followed by digital filters to remove unwanted frequencies and to reduce the sample rate.

The oversampled analog signal goes through an integrator whose output drives a comparator (a 1-bit ADC) that, in turn, drives a 1-bit DAC in the feedback loop. Through a series of iterations, the integrator, comparator, DAC, and summing junction produce a serial bit stream that represents the oversampled input voltage.

Once digitized, the oversampled signal goes through a digital filter to remove frequency components at or above the Nyquist frequency, which is one-half of the ADCs output-sampling rate (Ref. 4). A digital low-pass filter removes those high-frequency components, and a data decimator removes the oversampled data. In an ADC with 128X oversampling, the decimator will retain 1 bit for every 128 bits that it receives. The final output is a serial bit stream.

Because the internal digital filter in the sigma-delta ADC is an integral part of the conversion process, its settling time becomes a factor when you want to measure step functions. You may lose some important information because of the ADC's sample rate. This settling time, or "latency," may be several clock cycles at the final output data rate. The latency also limits the scan rate of multiplexed data-acquisition instruments.

Integrating ADCs

So far, I've described ADCs used in oscilloscopes, data-acquisition cards, and data-acquisition systems. Most DMMs, from handheld units to metrology-grade meters, use yet another ADC architecture called integrating type or dual-slope ADCs. DMMs use integrating ADCs because these instruments require high resolution with superior noise rejection.

The concept behind the integrating ADC is far less complex than the sigma-delta ADC. **Figure 7** shows how the integrating ADC works. The sampled signal charges a capacitor for a fixed amount of time, usually one power-line cycle (50 Hz or 60 Hz). By integrating over one line cycle, any power-line noise integrates out of the conversion.

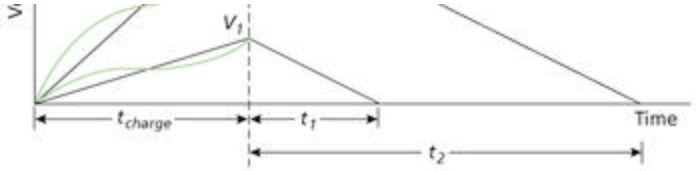

Figure 7. Integrating ADCs charge a capacitor for a fixed amount of time, then discharge while counting output bits.

When the charging time ends, the ADC discharges the capacitor at a fixed rate while a counter counts the ADC's output bits. A longer discharge time results in a higher count. As a result, V_2 in Figure 7 produces a larger digital output value than V_1 does.

Integrating ADCs work best in high-accuracy, fine-resolution systems because they remove any power-line frequency noise from the input signal. But removing that noise limits the converter's sample rate to about 30 samples/s for 60-Hz equipment. Integrating ADCs can run at higher sample rates, but as speed increases, noise immunity decreases.

Today, most DMMs use proprietary integrating ADC designs. Handheld DMMs with up to 20,000-count resolution (14-bits) often use off-the-shelf integrating ADCs.

For more information

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