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READERS SOLVE DESIGN PROBLEMS

Microprocessor generates programmable clock sequences

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To produce trains of pulses suitable for keying transmitters, testing circuits, and debugging data links, designers requiring continuous or event-driven pulse sequences have traditionally relied on pulse generators or collections of simple circuits. Today's inexpensive microprocessors make it possible to design and build low-cost, dedicated pulse-sequence generators with a minimum of resources. In a small, SOT-23-packaged, 10F200 controller from Microchip (www.microchip.com), the design in Figure 1 uses a code-based embedded table algorithm to generate an application-settable period and table-based PWM (pulse-width-modulation) sequence. The application produces a continuously pulsed sequence and requires only three constants and a pulse-width profile table that it copies into the microprocessor's assembler-based code before compiling (Figure 2).

All code branches undergo equalization to produce a group of 29 constant instruction times. During software development, you can use coded constants and a table-based approach as a flexible method of modifying the pulse sequence. The three parameters that Figure 2 highlights include the number of PWM cycles that execute between tabled steps, which the algorithm passes as "temp_cntK." This parameter defines how many PWM periods of a range from one to 255 repeat within each tabled step. For three cycles per table step, you use #define temp_cntK .3. The next parameter is the number of 29-instruction loops that execute during each PWM period. All branches of the coded instructions equalize to constant 29-instruction periods. When you copy this parameter as "loopsK," it can range from one to 255. Using the 10F200's internal 4-MHz clock and an 8-bit counter to generate 1-µsec instruction periods, you can generate a PWM period range of 58 to 7395 µsec, which corresponds to a frequency range of 17,241 to 135 Hz. For a 1-msec PWM-cycle period and the sequence in Figure 2, you require 31 base loops per cycle, which you obtain by dividing 1 msec by the 29-µsec instruction period: #define loopsK .31.

You then equate the total number of table profile steps to "table_maxK." The total number of profile steps that a look-up table includes and that you copy into the code may vary from one to 252. In this application, five tabled steps correspond to pulse duty cycles of 25, 50, 87.5, 12.5, and 75%. These val-

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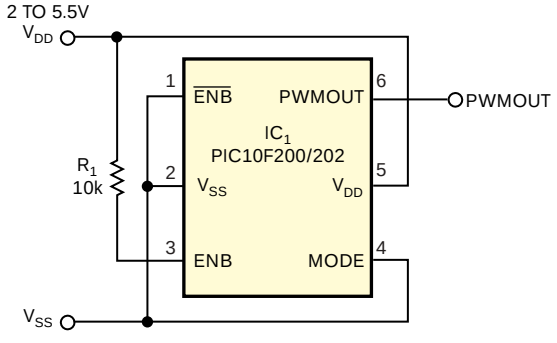

Figure 1 A microcontroller and a resistor can deliver a complex PWM output.

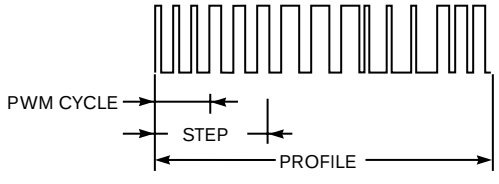

Figure 2 This waveform profile comprises five steps, each using one of three PWM cycles. In continuous mode, the circuit's output repeats indefinitely.

ues undergo scaling according to the following equation: Duty cycle=INT ($\%T_{DTY}/100 \times loopsK+0.5$), in which INT is the integer value and $\%T_{DTY}$ is the percentage of the total duty cycle. In this example, loopsK=31. The number of steps in the table passes to the program as #define loop_maxK .5.

The pulse-duty cycle can vary only in increments of a single 29-instruction base loop, and, as a consequence, the pulse duty cycle's resolution varies as the number of basic loops for the waveform's desired period, which you define as loopsK=31 loops. Thus, the duty-cycle resolution equals 1/(loopsK), or 1/(31)=3.22% for this application.

You can use a spreadsheet or manually calculate the translated and scaled duty-cycle values and store them in the data-profile table. For example, you calculate the value for a 25% duty cycle as INT(25/resolution+0.5)=INT(25/3.22+0.5), where INT represents extraction of the integer value of the computed quantity. For required duty cycles of 25, 50, 87.5, 12.5, and 75%, the values that pass to the data-profile table are retlw_8, 16, 27, 4, and 23, respectively. The assembly-language program available for downloading from the online version of this Design Idea at www.edn.com/060720di1 includes these duty-cycle values and the three other parameters.

The program includes two additional features: Connecting Pin 1 to ground enables a continuous-output mode. Connecting Pin 1 to $+V_{DD}$ evokes a single output waveform. Pin 3 serves as a high true-output enable when you connect it to $+V_{DD}$ or as a positive-edge trigger input when you pull the pin to ground and release it. Note that the program currently includes no contact-debounce routines for either input.

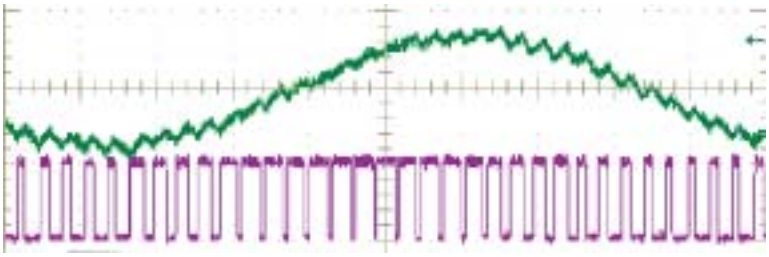

Figure 3 After undergoing lowpass-filtering, the controller's pulse-width-modulated output (lower trace) reveals its sine-wave origin.

In the example in Figure 3, the controller delivers a pulse-width-modulated output (lower trace), which, after processing by a single-pole lowpass filter, corresponds to a sine wave (upper trace). Using another version of the circuit, you can evaluate how a critical midword error affects a serial link's characteristics, system timing, and response latency.

The waveform in Figure 4 comprises 100 pulses, 99 of which exhibit a nominal duty cycle that varies from 48 to 51%, and a single error pulse with a 75% duty cycle. The waveform-table entries use values of loopsK=100, temp_cntK=1, and table_maxK=100 to produce a pulse sequence comprising 74 pulses with nominal duty cycles, a single pulse with a 75% duty cycle, and a final sequence of 25 clocks with nominal duty cycles. The entire sequence repeats at a 345-Hz rate.

Using a 4-MHz-clock-rate version of Microchip's 10F220 controller constrains the basic software-timing loop to a 29-μsec period. You can compile the program into an 8-MHz 10F220 to reduce the timing loop to 14.5 μsec and extend the output's usable bandwidth. You can modify the code in the listing to suit other compatible microprocessors to obtain greater bandwidth and integrate additional functions. As is, the circuit requires only 155 bytes of internal EEPROM and occupies an SOT-23 pc-board footprint—not bad for a processor that costs less than $1. EDN

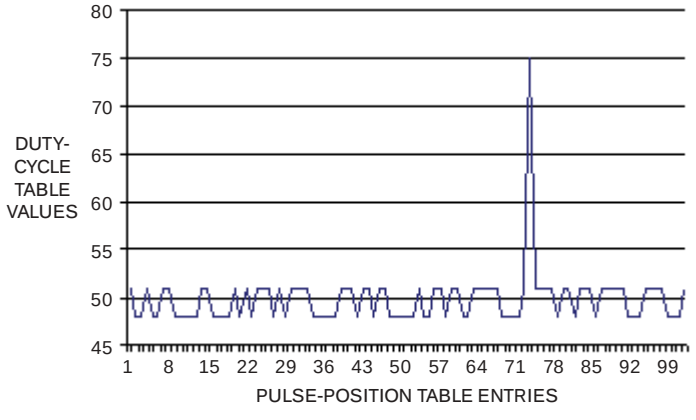

Figure 4 Devised for testing a serial link's error response, this waveform plot displays pulses' locations within the waveform (horizontal axis) versus the duty cycle for each pulse (vertical axis). The waveform cycle repeats after pulse 100 ends.

Ceramic output capacitors enhance internally compensated switchers

Robert Kollman, Texas Instruments, Dallas, TX

Integrating compensation components with a power-supply controller and buck regulator's power switches can minimize pc-board area, improve reliability, and eliminate assembly errors by reducing the number of components and solder joints. However, integration also limits a designer's range of choices in the selection of output-filter components. Figure 1a presents a typical switching regulator based on Texas Instruments' (www.ti.com) TPS5430. The boxed area in Figure 1b shows a simplified version of the IC's internal small-signal-equivalent circuit, which includes an error amplifier, E_1; passive-compensation components; and a voltage-controlled voltage-source, E_2, which represents the modulator and the power switches. Support components external to the IC include output-filter components and their parasitic resistances, a resistor representing an external load, and a divider comprising R_1 and R_2 that sets the output voltage. The compensation-circuit design accommodates a certain range of output-filter inductance and capacitance and their associated parasitics.

Figure 2 shows Bode diagrams for the error-amplifier and modulator-gain blocks (2a) and the entire regulator system (2b). Envisioning that end users would specify aluminum electrolytic capacitors for the output-filter circuit, the IC's designer includes a Type 3 compensation circuit to optimize the IC's performance for aluminum capacitors' characteristics. Note that a Type 3 compensation circuit includes a pole at the origin of the circuit's pole-zero plot to provide high gain at dc and an integratorlike high-frequency roll-off augmented with pairs of poles and zeros to provide phase and gain margins at certain frequencies (Reference 1).

The regulator's LC-output modulator/filter's amplitude-response curve peaks at the resonant frequency set by the filter's inductor and output capacitor, and then it decreases at a −40-dB/decade rate until it reaches a zero at a frequency set by the output capacitor and its ESR (equivalent series resistance). Beyond that frequency, the output inductor's and the capacitor's ESRs determine the attenuation curve's slope, resulting in a −20-dB/decade rate.

For good regulation, the error amplifier provides a high dc gain at low frequencies. However, to ensure stability, the loop gain must decrease as frequency increases. The goal is to approximate a −20-dB/decade roll-off at all frequencies. Placing two zeros at the output filter's resonant frequency helps cancel the two poles representing the resonance. Adding a pole to the error-amplifier response cancels the zero that the output capacitor and its ESR introduce. Adding a final pole above the power supply's crossover frequency helps further increase the regulator loop's stability. Figure 2b shows the sum of the gains of the error amplifier and modulator/filter gain. The power supply's characteristics show a 30-kHz bandwidth and a 60° phase margin that ensures stable operation.

The power-supply-control-

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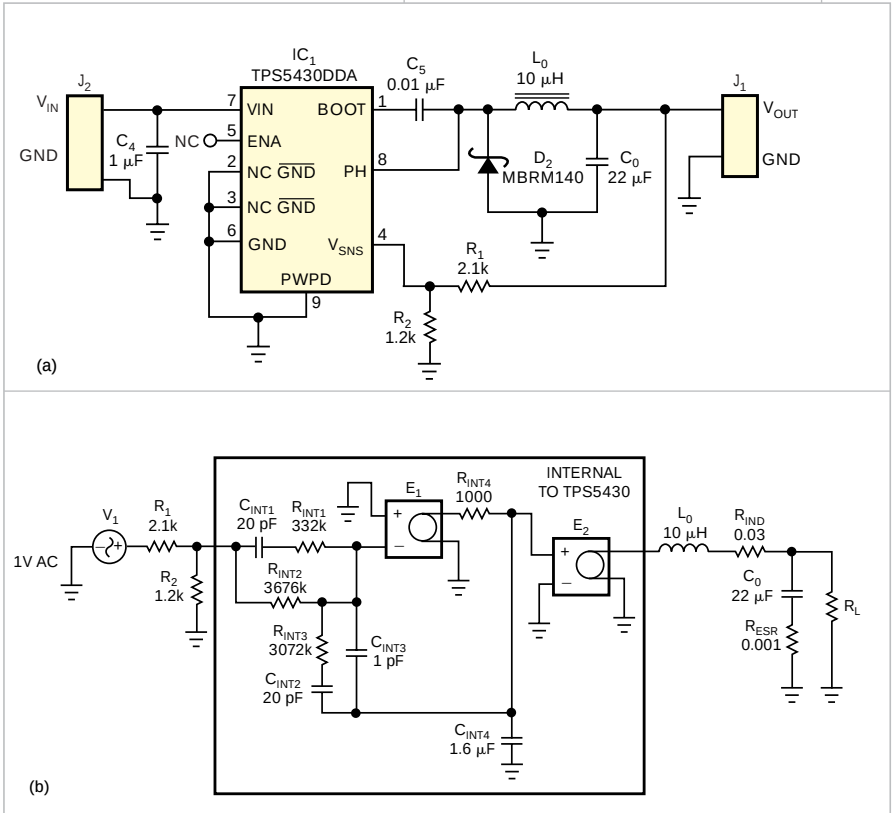

Figure 1 This TPS5430 power-supply design includes an aluminum electrolytic output-filter capacitor, C_0 (a). A circuit model includes parasitic resistances associated with output-filter components L_0 and C_0 (b).

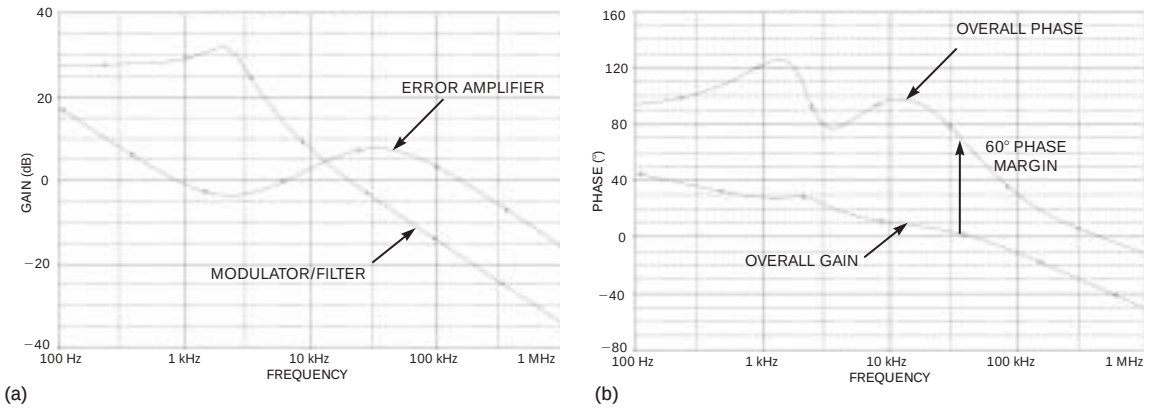

Figure 2 Gain (a) and phase (b) plots show that the circuit of Figure 1a includes adequate compensation and phase-angle margin for an aluminum electrolytic output-filter capacitor.

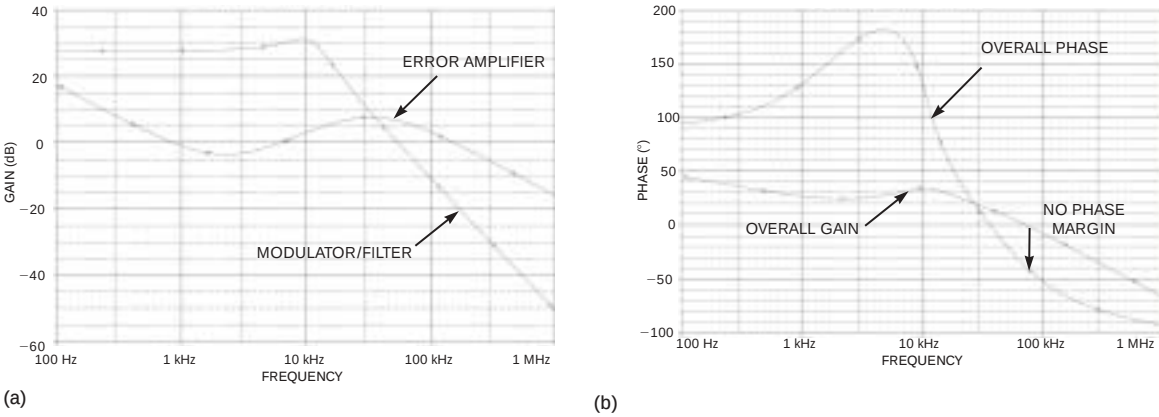

Figure 3 Gain (a) and phase (b) plots show that using a ceramic-dielectric output-filter capacitor erodes the phase-angle margin and pushes the circuit dangerously close to oscillation.

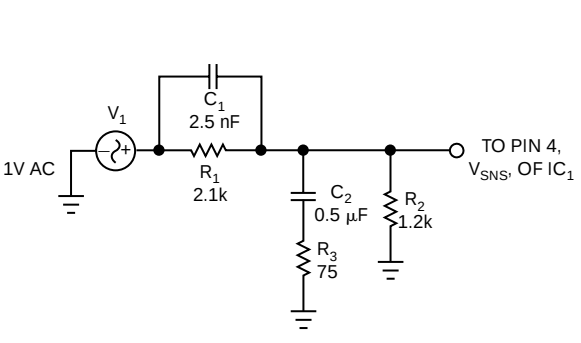

Figure 4 A few passive components supplement R_1 and R_2 and stabilize the circuit for use with a ceramic-dielectric output-filter capacitor.

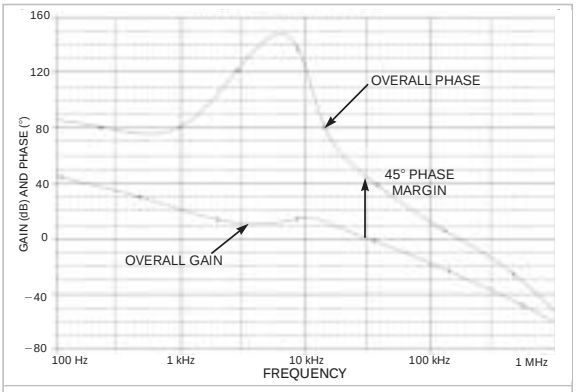

Figure 5 The phase-angle plot for the circuit of Figure 4 shows a sufficient phase-angle margin to allow stable operation with a ceramic output-filter capacitor.

loop response (Figure 3) illustrates the circuit's behavior when the design includes ceramic-dielectric output-filter capacitors and the same integrated-compensation components in Figure 1. Ceramic capacitors present a much lower ESR than do aluminum electrolytic capacitors, and their capacitance determines the filter's attenuation rather than their ESR. Consequently, at high frequencies, the LC filter's characteristics include a double pole and a steeper, −40-dB/decade slope. In addition, filter attenuation increases at the desired crossover frequency, degrading phase and gain margins. Figure 3b indicates that the power supply is unstable and, with no phase margin, will likely oscillate.

Replacing the divider network, R_1 and R_2 in Figure 1 with the passive network in Figure 4 stabilizes the regulation loop and allows an internally compensated controller to use ceramic output capacitors. The network's components add two sets of poles and zeros to the compensation network to cancel the consequences of using ceramic output capacitors. For example, C_2 and R_3 provide attenuation that reduces the crossover frequency. You select C_2 to provide attenuation at frequencies much lower than the crossover frequency. Unfortunately, C_2 adds a negative-phase shift that R_3 returns to nearly zero at the design's crossover frequency. Adding C_1 introduces a phase lead that compensates for the ceramic capacitors' negative effects. Without C_1, the filter's 180° phase shift would reduce the regulator's phase margin to nearly zero.

The phase angle starts increasing at a frequency that C_1 and R_1 determine, and they introduce a zero in the phase-plane plot at that frequency (Figure 5). At a frequency that C_1 and R_3 determine, a pole in the phase-plane plot terminates the phase angle's increase. The geometric mean of the pole and zero frequencies determines the maximum phase-angle boost.

As a starting point, you can place the first pole, which C_2 and the parallel combination of R_1 and R_2 determine, at a low frequency, such as 100 Hz. Next, adjust the values of C_2 and R_3 to set the first zero's frequency at 1 kHz, which is much less than the gain curve's 0-dB crossover frequency. Finally, set the zero that C_1 and R_1 introduce to a frequency that's at least a factor of two below the zero-gain crossover frequency to ensure a 45° phase margin at the crossover frequency. The Bode plot in Figure 5 features a 30-kHz regulation-loop bandwidth that provides good transient response and more than 45° of phase margin to ensure good stability. EDN

REFERENCE

1. "Optimal Feedback Amplifier Design For Control Systems," Venable Industries, www.venable.biz/tp-03.pdf.

Tapped inductor, boost regulator deliver high voltage

David Ng and Adam Huff, Linear Technology Corp, Milpitas, CA

When you face the task of generating a regulated voltage that's higher than the available power-supply voltage, you may consider a boost regulator. Although a boost converter can in theory generate almost any voltage that's higher than its input, practical considerations limit the output to approximately eight times its applied voltage. To generate an even higher voltage, consider using a tapped-inductor boost topology. Figure 1 shows an implementation of a converter that boosts a 3V input to 100V dc. The connections to the regulator chip are similar to those of a traditional boost converter, but, to achieve the high boost ratio, this design uses L_1, a 1-to-6-turns-ratio, tapped inductor.

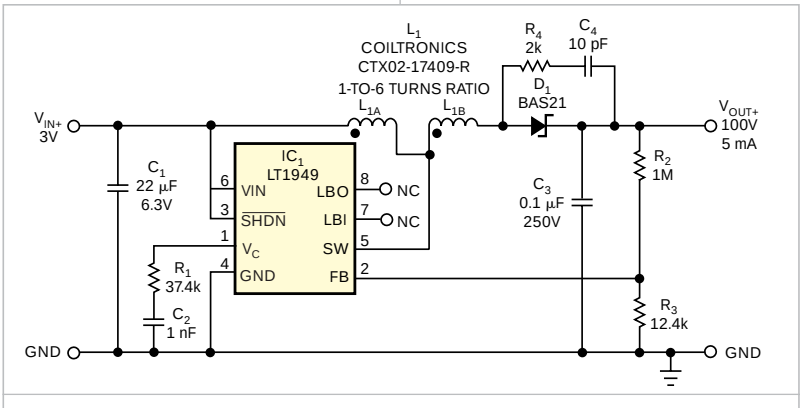

Figure 1 Using a tapped inductor extends a boost-topology switching regulator's practical output-voltage range.

The waveforms in Figure 2 show the input voltage, the voltage at power-switch IC_1's output, Pin 5, and rectifier diode D_1's anode voltage. As in any boost circuit, inductor L_1's core stores energy when IC_1's internal output switch conducts. When the switch turns off, the voltage across its terminals and L_{1A} goes higher than the input voltage. Due to inductive coupling and the larger number of turns that make up L_{1B}, the voltage at rectifier diode D_1's anode and hence the output voltage goes much higher. Resistors R_2 and R_3 form a feedback-voltage divider that closes the regulation loop. The R_4-C_4 network forms a snubber circuit that suppresses the impact of diode D_1's small parasitic capacitance. Without the network,

Figure 2 For a 3V-dc input (lower trace, horizontal line), the voltage at regulator IC_1's SW pin reaches a peak of approximately 18V (lower trace, pulsed waveform). The 1-to-6 step-up turns ratio of inductor L_1 further increases the peak output voltage to 160V (upper trace) to produce 100V dc. The upper trace's lower limit goes to $-6\times V_{IN}(-18V)$ due to the tapped inductor.

power switch IC_1 "sees" a capacitance that's 36 times larger due to the multiplicative effect of the tapped inductor's turns ratio.

Measuring only 5.6×6×3.4 mm, Coiltronics' (www.coiltronics.com) CTX02-17409 tapped inductor, L_1, and Linear Technology's (www.linear.com) LT1949 monolithic regulator, IC_1, available in an eight-lead MSOP package, present small pc-board footprints. When you implement the circuit on a single-layer pc board, the entire circuit occupies less than 1.9 cm^2 of board space (Figure 3). For best results, review the board-layout suggestions in the device's data sheet (Reference 1) and use multilayer-ceramic capacitors for C_1 and C_3.EDN

Figure 3 The entire boost-converter circuit occupies a footprint of less than 1.5×1.25 cm on a single-sided pc board.

REFERENCE

1 www.linear.com/pc/productDetail.do?navId=H0,C1,C1003,C1042,C1031,C1061,P1958.