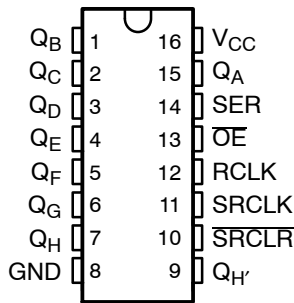


SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

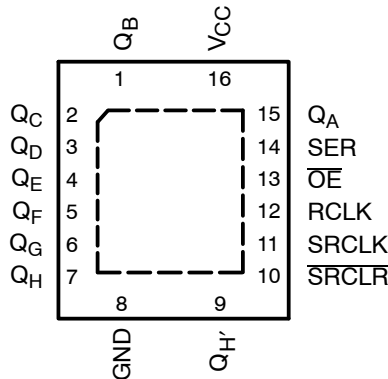
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 7.1 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift
- I_{off} Supports Partial-Power-Down Mode Operation
- Shift Register Has Direct Clear
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

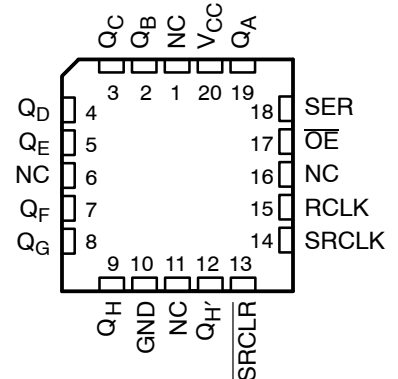
SN54LV595A . . . J OR W PACKAGE
SN74LV595A . . . D, DB, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV595A . . . RGY PACKAGE
(TOP VIEW)



SN54LV595A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'LV595A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LV595ARGYR | LV595A |
| | | Tube of 40 | SN74LV595ADG3 | LV595A |
| | SOIC – D | Reel of 2500 | SN74LV595ADR | |
| | | Reel of 2000 | SN74LV595ANSR | 74LV595A |
| | SSOP – DB | Reel of 2000 | SN74LV595ADBR | LV595A |
| –55°C to 125°C | TSSOP – PW | Tube of 90 | SN74LV595APW | LV595A |
| | | Reel of 2000 | SN74LV595APWRG3 | |
| | | Reel of 250 | SN74LV595APWT | |
| | CDIP – J | Tube of 25 | SNJ54LV595AJ | SNJ54LV595AJ |
| | CFP – W | Tube of 150 | SNJ54LV595AW | SNJ54LV595AW |
| | LCCC – FK | Tube of 55 | SNJ54LV595AFK | SNJ54LV595AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LV595A, SN74LV595A

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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description/ordering information (continued)

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs except Q_H are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

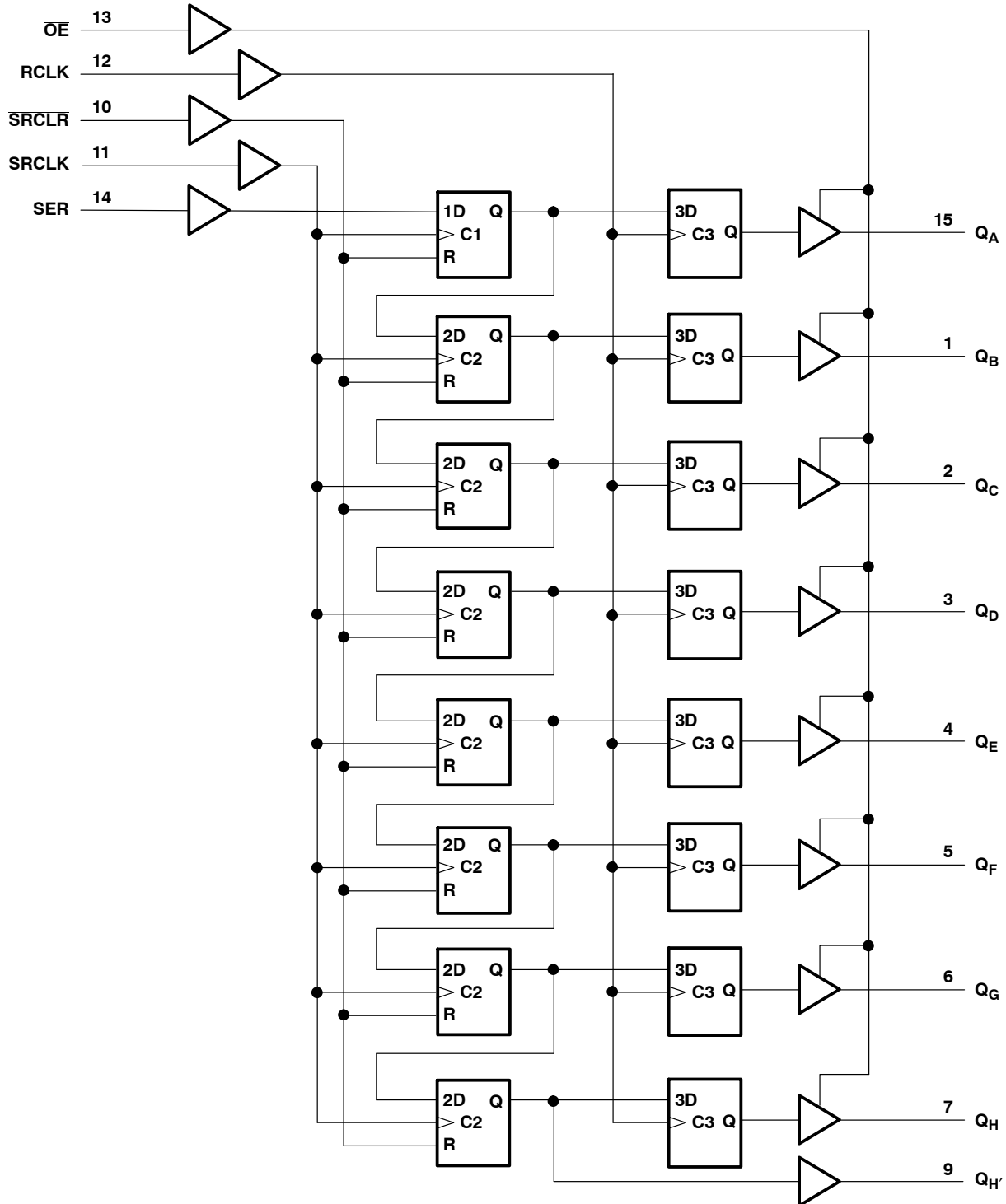
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

| INPUTS | | | | | FUNCTION |
|--------|-------|-------|------|----|--|
| SER | SRCLK | SRCLR | RCLK | OE | |
| X | X | X | X | H | Outputs Q_A – Q_H are disabled. |
| X | X | X | X | L | Outputs Q_A – Q_H are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | X | X | ↑ | X | Shift-register data is stored in the storage register. |

logic diagram (positive logic)

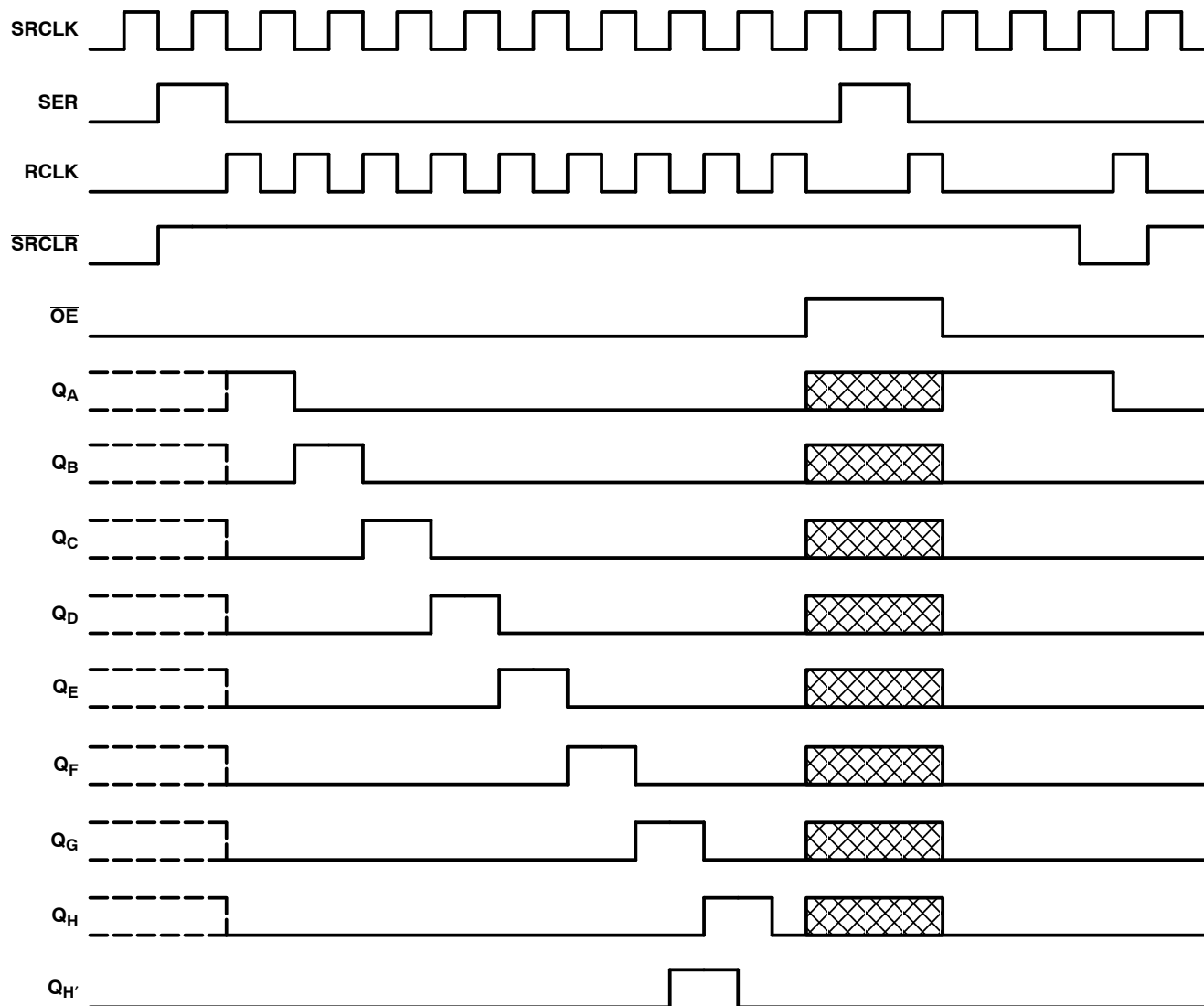



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

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timing diagram



NOTE:  implies that the output is in 3-State mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Output voltage range applied in the high or low state, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±35 mA |
| Continuous current through V_{CC} or GND | ±70 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 73°C/W |
| (see Note 3): DB package | 82°C/W |
| (see Note 3): NS package | 64°C/W |
| (see Note 3): PW package | 108°C/W |
| (see Note 4): RGY package | 39°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV595A, SN74LV595A

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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recommended operating conditions (see Note 5)

| | | | SN54LV595A | | SN74LV595A | | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------|-----------------------|-----------------|------|
| | | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | 1.5 | | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.7 | | V _{CC} × 0.7 | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.7 | | V _{CC} × 0.7 | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.7 | | V _{CC} × 0.7 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | 0.5 | | 0.5 | | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.3 | | V _{CC} × 0.3 | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.3 | | V _{CC} × 0.3 | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.3 | | V _{CC} × 0.3 | | |
| V _I | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | High or low state | 0 | V _{CC} | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 2 V | −50 | | −50 | | μA |
| | | V _{CC} = 2.3 V to 2.7 V | −2 | | −2 | | mA |
| | | V _{CC} = 3 V to 3.6 V | −8 | | −8 | | |
| | | V _{CC} = 4.5 V to 5.5 V | −16 | | −16 | | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | 50 | | 50 | | μA |
| | | V _{CC} = 2.3 V to 2.7 V | 2 | | 2 | | mA |
| | | V _{CC} = 3 V to 3.6 V | 8 | | 8 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 16 | | 16 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 2.3 V to 2.7 V | 200 | | 200 | | ns/V |
| | | V _{CC} = 3 V to 3.6 V | 100 | | 100 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 20 | | 20 | | |
| T _A | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | SN54LV595A | | | SN74LV595A | | | UNIT |
|------------------|--------------------------------|--|-----------------|----------------------|-----|-----|----------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OH} | | I _{OH} = -50 μA | 2 V to 5.5 V | V _{CC} -0.1 | | | V _{CC} -0.1 | | | V |
| | | I _{OH} = -2 mA | 2.3 V | 2 | | | 2 | | | |
| | Q _{H'} | I _{OH} = -6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | Q _A -Q _H | I _{OH} = -8 mA | | 2.48 | | | 2.48 | | | |
| | Q _{H'} | I _{OH} = -12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| | Q _A -Q _H | I _{OH} = -16 mA | | 3.8 | | | 3.8 | | | |
| V _{OL} | | I _{OL} = 50 μA | 2 V to 5.5 V | 0.1 | | | 0.1 | | | V |
| | | I _{OL} = 2 mA | 2.3 V | 0.4 | | | 0.4 | | | |
| | Q _{H'} | I _{OL} = 6 mA | 3 V | 0.44 | | | 0.44 | | | |
| | Q _A -Q _H | I _{OL} = 8 mA | | 0.44 | | | 0.44 | | | |
| | Q _{H'} | I _{OL} = 12 mA | 4.5 V | 0.55 | | | 0.55 | | | |
| | Q _A -Q _H | I _{OL} = 16 mA | | 0.55 | | | 0.55 | | | |
| I _I | | V _I = 5.5 V or GND | 0 to 5.5 V | ±1 | | | ±1 | | | μA |
| I _{OZ} | | V _O = V _{CC} or GND, Q _A -Q _H | 5.5 V | ±5 | | | ±5 | | | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | 20 | | | 20 | | | μA |
| I _{off} | | V _I or V _O = 0 to 5.5 V | 0 | 5 | | | 5 | | | μA |
| C _i | | V _I = V _{CC} or GND | 3.3 V | 3.5 | | | 3.5 | | | pF |

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

| | | | T _A = 25°C | | SN54LV595A | | SN74LV595A | | UNIT |
|-----------------|----------------|-------------------------------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration | SRCLK high or low | 7 | | 7.5 | | 7.5 | | ns |
| | | RCLK high or low | 7 | | 7.5 | | 7.5 | | |
| | | SRCLR low | 6 | | 6.5 | | 6.5 | | |
| t _{su} | Setup time | SER before SRCLK↑ | 5.5 | | 5.5 | | 5.5 | | ns |
| | | SRCLK↑ before RCLK↑† | 8 | | 9 | | 9 | | |
| | | SRCLR low before RCLK↑ | 8.5 | | 9.5 | | 9.5 | | |
| | | SRCLR high (inactive) before SRCLK↑ | 4 | | 4 | | 4 | | |
| t _h | Hold time | SER after SRCLK↑ | 1.5 | | 1.5 | | 1.5 | | ns |

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SN54LV595A, SN74LV595A

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | SN54LV595A | | SN74LV595A | | UNIT |
|-----------------|----------------|-------------------------------------|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration | SRCLK high or low | | 5.5 | | 5.5 | | ns |
| | | RCLK high or low | | 5.5 | | 5.5 | | |
| | | SRCLR low | | 5 | | 5 | | |
| t _{su} | Setup time | SER before SRCLK↑ | | 3.5 | | 3.5 | | ns |
| | | SRCLK↑ before RCLK↑† | | 8 | | 8.5 | | |
| | | SRCLR low before RCLK↑ | | 8 | | 9 | | |
| | | SRCLR high (inactive) before SRCLK↑ | | 3 | | 3 | | |
| t _h | Hold time | SER after SRCLK↑ | | 1.5 | | 1.5 | | ns |

[†] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| | | $T_A = 25^{\circ}\text{C}$ | | SN54LV595A | | SN74LV595A | | UNIT |
|----------|----------------|-------------------------------------|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | SRCLK high or low | 5 | 5 | 5 | 5 | 5 | ns |
| | | RCLK high or low | 5 | 5 | 5 | 5 | 5 | |
| | | SRCLR low | 5.2 | 5.2 | 5.2 | 5.2 | 5.2 | |
| t_{su} | Setup time | SER before SRCLK↑ | 3 | 3 | 3 | 3 | 3 | ns |
| | | SRCLK↑ before RCLK↑† | 5 | 5 | 5 | 5 | 5 | |
| | | SRCLR low before RCLK↑ | 5 | 5 | 5 | 5 | 5 | |
| | | SRCLR high (inactive) before SRCLK↑ | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | |
| t_h | Hold time | SER after SRCLK↑ | 2 | 2 | 2 | 2 | 2 | ns |

[†] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV595A | | SN74LV595A | | UNIT |
|------------------|-----------------|--------------------------------|------------------------|------------------------|-------|------|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | C _L = 15 pF | 65* | 80* | | 45* | | 45 | | MHz |
| | | | C _L = 50 pF | 60 | 70 | | 40 | | 40 | | |
| t _{PLH} | RCLK | Q _A –Q _H | C _L = 15 pF | 8.4* | 14.2* | | 1* | 15.8* | 1 | 15.8 | ns |
| t _{PHL} | | | | 8.4* | 14.2* | | 1* | 15.8* | 1 | 15.8 | |
| t _{PLH} | SRCLK | Q _{H'} | | 9.4* | 19.6* | | 1* | 22.2* | 1 | 22.2 | |
| t _{PHL} | | | | 9.4* | 19.6* | | 1* | 22.2* | 1 | 22.2 | |
| t _{PHL} | SRCLR | Q _{H'} | | 8.7* | 14.6* | | 1* | 16.3* | 1 | 16.3 | |
| t _{PZH} | OE | Q _A –Q _H | | 8.2* | 13.9* | | 1* | 15* | 1 | 15 | |
| t _{PZL} | | | | 10.9* | 18.1* | | 1* | 20.3* | 1 | 20.3 | |
| t _{PHZ} | OE | Q _A –Q _H | | 8.3* | 13.7* | | 1* | 15.6* | 1 | 15.6 | |
| t _{PLZ} | | | | 9.2* | 15.2* | | 1* | 16.7* | 1 | 16.7 | |
| t _{PLH} | RCLK | Q _A –Q _H | | C _L = 50 pF | 11.2 | 17.2 | | 1 | 19.3 | 1 | |
| t _{PHL} | | | 11.2 | | 17.2 | | 1 | 19.3 | 1 | 19.3 | |
| t _{PLH} | SRCLK | Q _{H'} | 13.1 | | 22.5 | | 1 | 25.5 | 1 | 25.5 | |
| t _{PHL} | | | 13.1 | | 22.5 | | 1 | 25.5 | 1 | 25.5 | |
| t _{PHL} | SRCLR | Q _{H'} | 12.4 | | 18.8 | | 1 | 21.1 | 1 | 21.1 | |
| t _{PZH} | OE | Q _A –Q _H | 10.8 | | 17 | | 1 | 18.3 | 1 | 18.3 | |
| t _{PZL} | | | 13.4 | | 21 | | 1 | 23 | 1 | 23 | |
| t _{PHZ} | OE | Q _A –Q _H | 12.2 | | 18.3 | | 1 | 19.5 | 1 | 19.5 | |
| t _{PLZ} | | | 14 | | 20.9 | | 1 | 22.6 | 1 | 22.6 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

SN54LV595A, SN74LV595A

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV595A | | SN74LV595A | | UNIT |
|------------------|-----------------|--------------------------------|------------------------|-----------------------|-------|-----|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | C _L = 15 pF | 80* | 120* | | 70* | | 70 | | MHz |
| | | | C _L = 50 pF | 55 | 105 | | 50 | | 50 | | |
| t _{PLH} | RCLK | Q _A –Q _H | C _L = 15 pF | 6* | 11.9* | | 1* | 13.5* | 1 | 13.5 | ns |
| t _{PHL} | | | | 6* | 11.9* | | 1* | 13.5* | 1 | 13.5 | |
| t _{PLH} | SRCLK | Q _H ' | | 6.6* | 13* | | 1* | 15* | 1 | 15 | |
| t _{PHL} | | | | 6.6* | 13* | | 1* | 15* | 1 | 15 | |
| t _{PHL} | SRCLR | Q _H ' | | 6.2* | 12.8* | | 1* | 13.7* | 1 | 13.7 | |
| t _{PZH} | OE | Q _A –Q _H | | 6* | 11.5* | | 1* | 13.5* | 1 | 13.5 | |
| t _{PZL} | | | | 7.8* | 11.5* | | 1* | 13.5* | 1 | 13.5 | |
| t _{PHZ} | OE | Q _A –Q _H | | 6.1* | 14.7* | | 1* | 15.2* | 1 | 15.2 | |
| t _{PLZ} | | | | 6.3* | 14.7* | | 1* | 15.2* | 1 | 15.2 | |
| t _{PLH} | RCLK | Q _A –Q _H | C _L = 50 pF | 7.9 | 15.4 | | 1 | 17 | 1 | 17 | ns |
| t _{PHL} | | | | 7.9 | 15.4 | | 1 | 17 | 1 | 17 | |
| t _{PLH} | SRCLK | Q _H ' | | 9.2 | 16.5 | | 1 | 18.5 | 1 | 18.5 | |
| t _{PHL} | | | | 9.2 | 16.5 | | 1 | 18.5 | 1 | 18.5 | |
| t _{PHL} | SRCLR | Q _H ' | | 9 | 16.3 | | 1 | 17.2 | 1 | 17.2 | |
| t _{PZH} | OE | Q _A –Q _H | | 7.8 | 15 | | 1 | 17 | 1 | 17 | |
| t _{PZL} | | | | 9.6 | 15 | | 1 | 17 | 1 | 17 | |
| t _{PHZ} | OE | Q _A –Q _H | | 8.1 | 15.7 | | 1 | 16.2 | 1 | 16.2 | |
| t _{PLZ} | | | | 9.3 | 15.7 | | 1 | 16.2 | 1 | 16.2 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV595A | | SN74LV595A | | UNIT |
|------------------|-----------------|--------------------------------|------------------------|-----------------------|------|------|------------|------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | C _L = 15 pF | 135* | 170* | | 115* | | 115 | | MHz |
| | | | C _L = 50 pF | 120 | 140 | | 95 | | 95 | | |
| t _{PLH} | RCLK | Q _A –Q _H | C _L = 15 pF | | 4.3* | 7.4* | 1* | 8.5* | 1 | 8.5 | ns |
| t _{PHL} | | | | | 4.3* | 7.4* | 1* | 8.5* | 1 | 8.5 | |
| t _{PLH} | SRCLK | Q _{H'} | | | 4.5* | 8.2* | 1* | 9.4* | 1 | 9.4 | |
| t _{PHL} | | | | | 4.5* | 8.2* | 1* | 9.4* | 1 | 9.4 | |
| t _{PHL} | SRCLR | Q _{H'} | | | 4.5* | 8* | 1* | 9.1* | 1 | 9.1 | |
| t _{PZH} | OE | Q _A –Q _H | | | 4.3* | 8.6* | 1* | 10* | 1 | 10 | |
| t _{PZL} | | | | | 5.4* | 8.6* | 1* | 10* | 1 | 10 | |
| t _{PHZ} | OE | Q _A –Q _H | | | 2.4* | 6* | 1* | 7.1* | 1 | 7.1 | |
| t _{PLZ} | | | | | 2.7* | 5.1* | 1* | 7.2* | 1 | 7.2 | |
| t _{PLH} | RCLK | Q _A –Q _H | C _L = 50 pF | | 5.6 | 9.4 | 1 | 10.5 | 1 | 10.5 | ns |
| t _{PHL} | | | | | 5.6 | 9.4 | 1 | 10.5 | 1 | 10.5 | |
| t _{PLH} | SRCLK | Q _{H'} | | | 6.4 | 10.2 | 1 | 11.4 | 1 | 11.4 | |
| t _{PHL} | | | | | 6.4 | 10.2 | 1 | 11.4 | 1 | 11.4 | |
| t _{PHL} | SRCLR | Q _{H'} | | | 6.4 | 10 | 1 | 11.1 | 1 | 11.1 | |
| t _{PZH} | OE | Q _A –Q _H | | | 5.7 | 10.6 | 1 | 12 | 1 | 12 | |
| t _{PZL} | | | | | 6.8 | 10.6 | 1 | 12 | 1 | 12 | |
| t _{PHZ} | OE | Q _A –Q _H | | | 3.5 | 10.3 | 1 | 11 | 1 | 11 | |
| t _{PLZ} | | | | | 3.4 | 10.3 | 1 | 11 | 1 | 11 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

| PARAMETER | | SN74LV595A | | | UNIT |
|-------------|--|------------|------|-----|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.3 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.2 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 2.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.99 | | V |

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | V_{CC} | TYP | UNIT |
|-----------|-------------------------------|--|--|----------|-----|------|
| C_{pd} | Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | | 3.3 V | 111 | pF |
| | | | | 5 V | 114 | |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

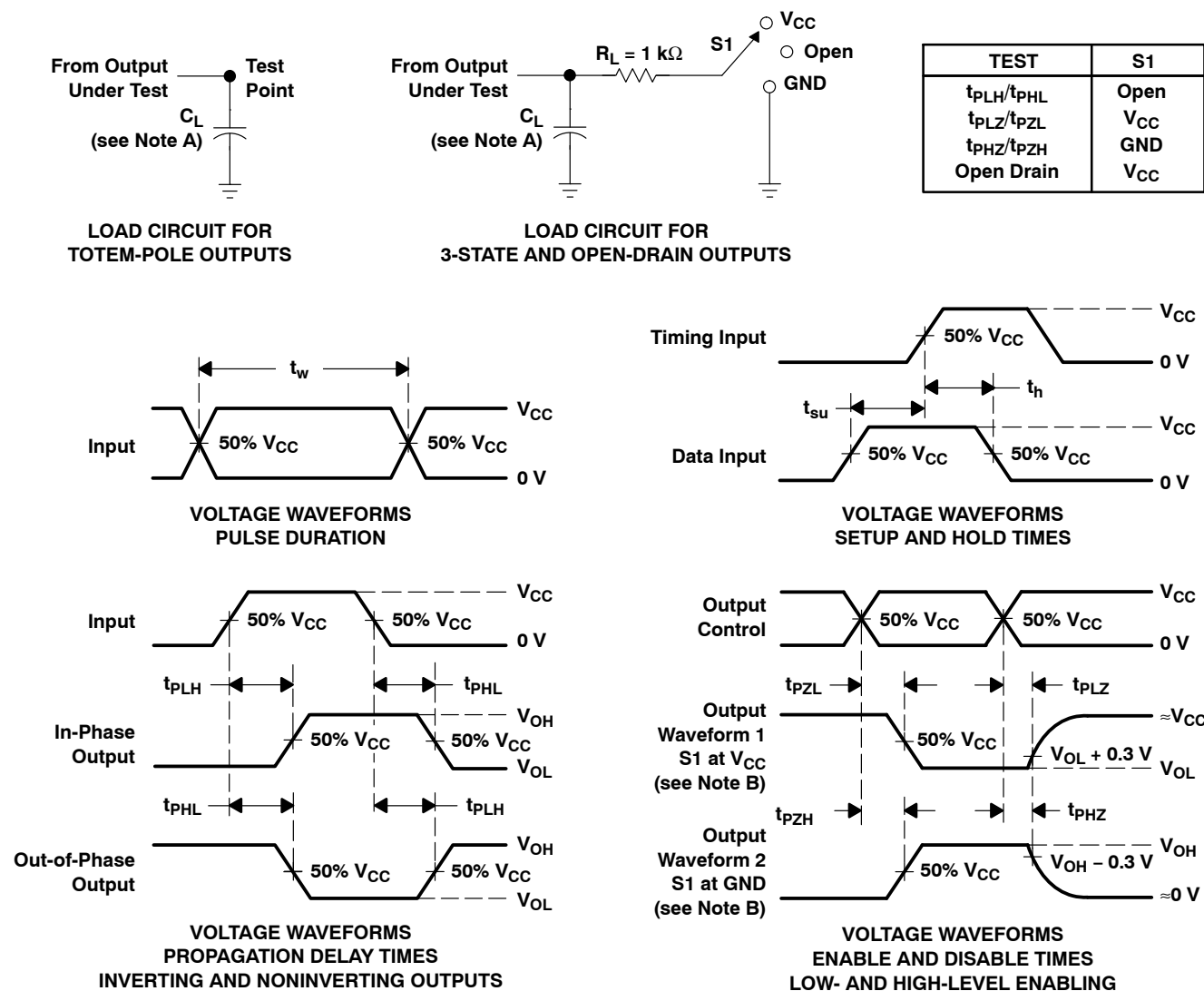


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS4140 – APRIL 1998 – REVISED JANUARY 2011

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LV595AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ADRG3 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV595A | Samples |
| SN74LV595ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV595A | Samples |
| SN74LV595ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV595A | Samples |
| SN74LV595APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595APWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595APWRG3 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595APWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595APWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |
| SN74LV595APWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV595A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LV595ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LV595A | Samples |
| SN74LV595ARGYRG4 | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LV595A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV595A :

- Automotive: [SN74LV595A-Q1](#)

- Enhanced Product: [SN74LV595A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV595ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ADRG3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV595APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWRG3 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV595ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV595ADRG3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV595ADRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LV595ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV595APWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV595APWRG3 | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV595APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV595APWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |
| SN74LV595ARGYR | VQFN | RGY | 16 | 3000 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

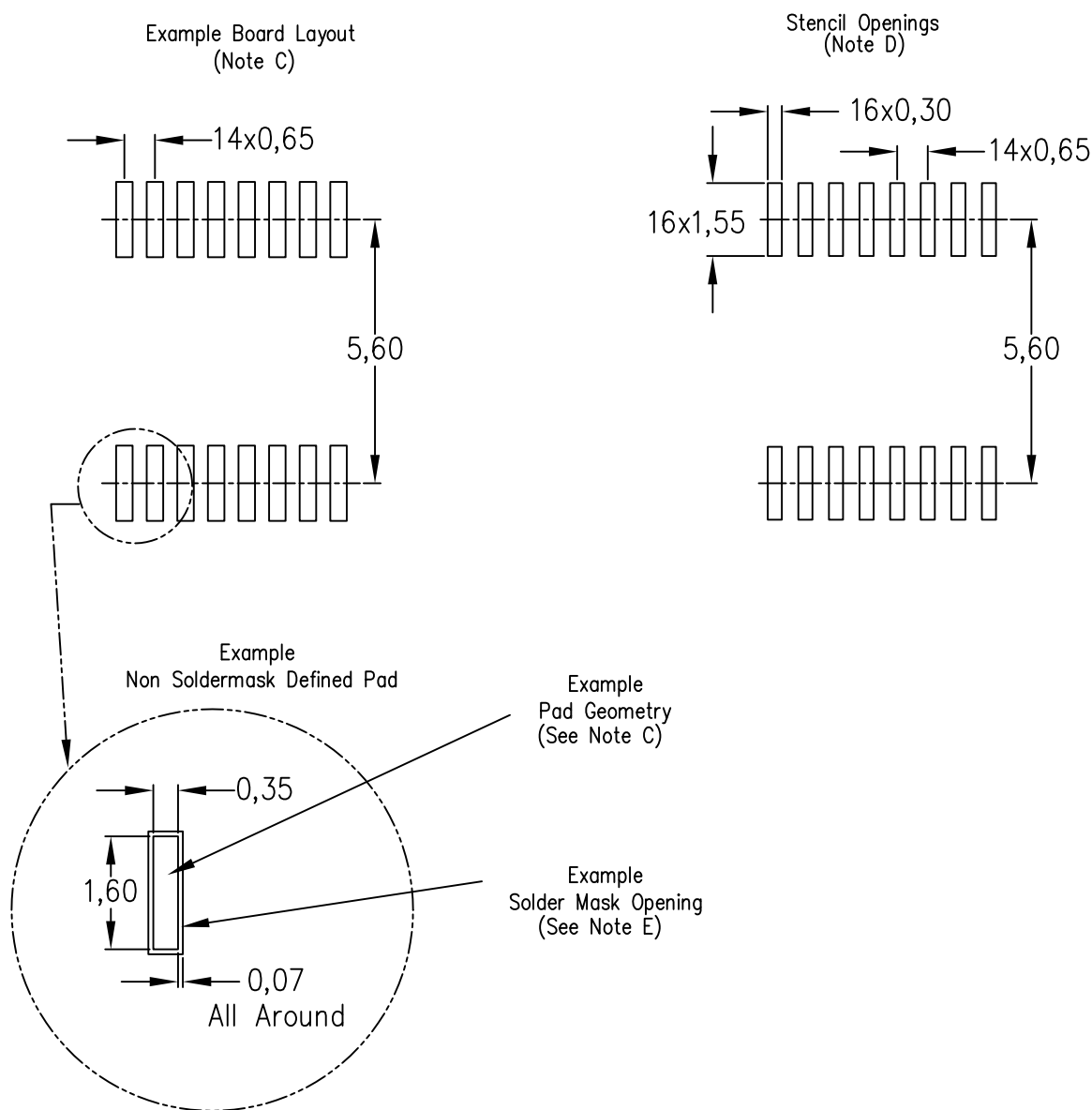


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

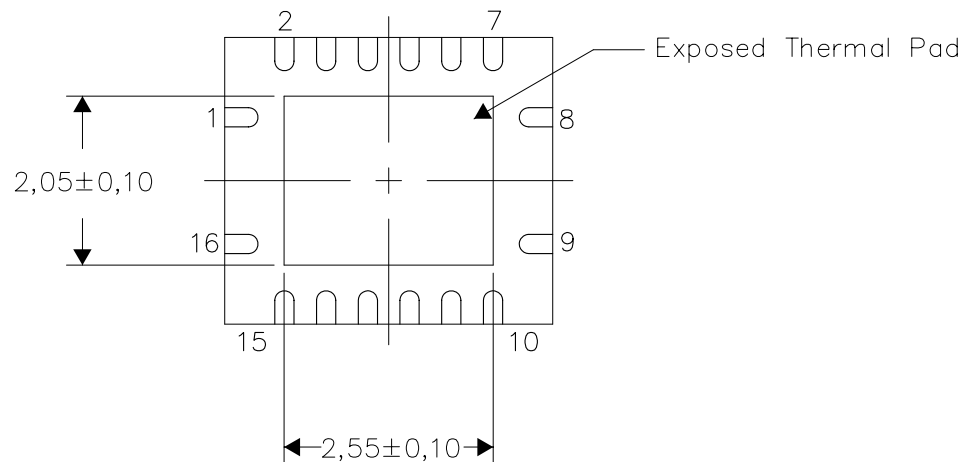
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

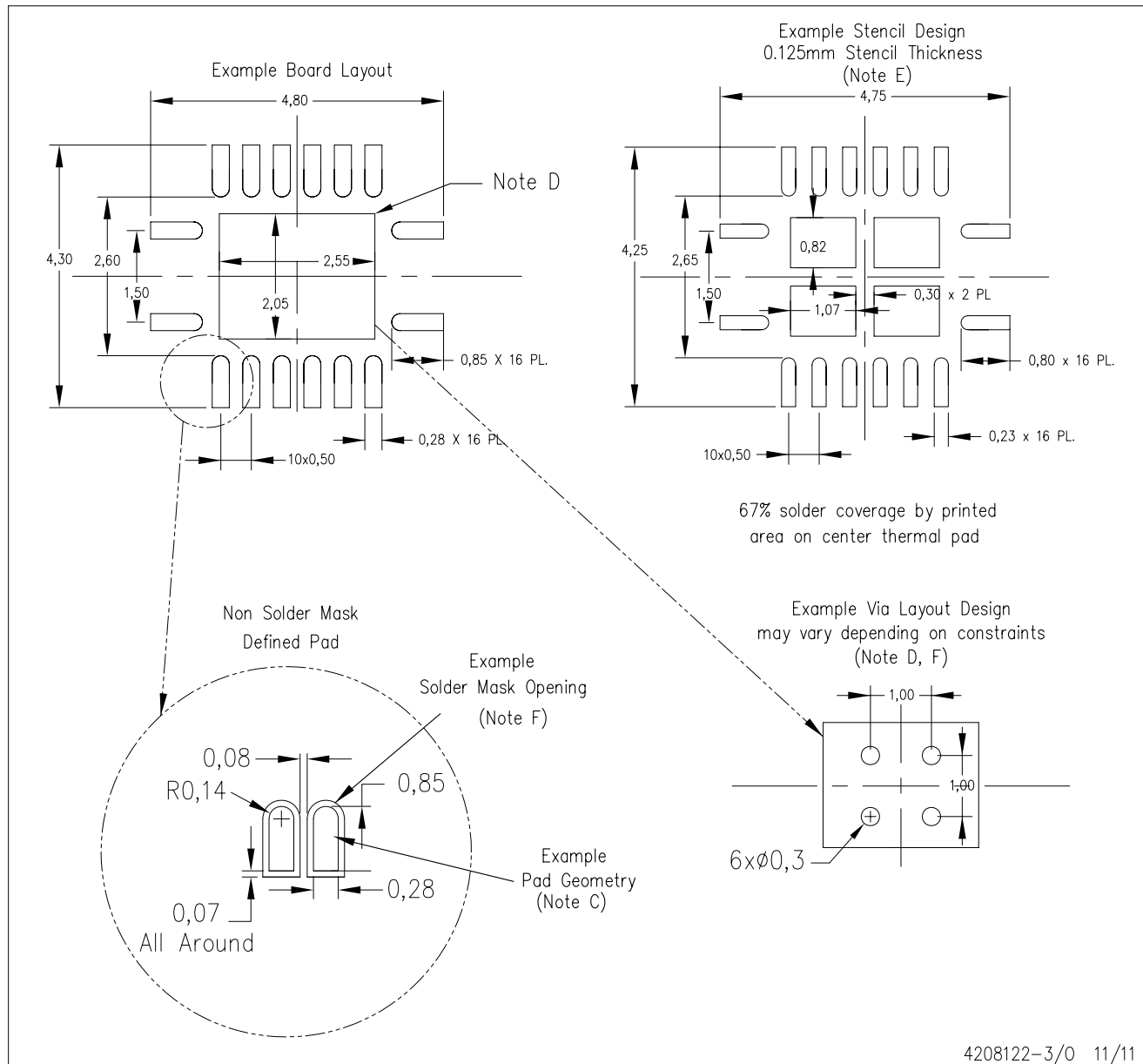
Exposed Thermal Pad Dimensions

4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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