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Analysis of Avalanche Behaviour for Paralleled MOSFETs

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I: Abstract:

In this study, an avalanche extension to existing quasi-dynamic thermal model is developed. And the current and thermal distribution among paralleled devices under avalanche condition is investigated. The statistic distribution of breakdown voltage, terminal stray inductance and thermal coupling all affect final electrical and thermal balance of paralleled devices. Without careful design consideration, it may cause reliability problem. So conclusions in this paper could provide useful guidelines for high power discrete or module applications with paralleled power devices.

II: Introduction:

Parallel MOSFET devices are now commonly used in both module and discrete automotive application where high current must be processed, for example electric power steering. Paralleling power devices has several benefits, such as reducing the conduction losses, spreading the thermal load on the heat sink, and increasing the bond wire opportunity, and is also a cost effective approach relative to a single larger device. However, some problems may arise because of device parameter variation and package parasitics.

Previously, most concerns related to parallel MOSFETs focused on load current balancing affected by stray inductance and gate characteristics [1]. One assumption is that MOSFETs never reach avalanche, which means MOSFETs are selected with a break down voltage much higher than the DC supply voltage. This assumption rarely holds true for automotive applications. As a MOSFET's $R_{ds(on)}$ is proportional to its break down voltage, a MOSFET optimised for higher $V_{(BR)DSS}$ will certainly exhibit higher conduction loss per unit area than a similar technology device with lower $V_{(BR)DSS}$. When the application objective is to make efficient use of the silicon at lowest practical cost, as most automotive applications will typically demand, it is desirable to select a device with $V_{(BR)DSS}$ such that the device will avalanche on switching transitions as a feature of normal operation of the circuit. This is a secondary reason for intentional avalanche in that it provides an inherent voltage clamp.

When parallel devices are operated into avalanche, the statistical normal distribution of $V_{(BR)DSS}$ can cause each device in a parallel configuration to experience different electrical and thermal stresses. If the parallel device circuit needs to operate reliably, it is important that the worst-case load current distribution and the temperature difference among paralleled devices be understood during a switching cycle including avalanche.

However, to our best knowledge, there is no publication directly related to this topic yet. So a study of this phenomenon would provide circuit designers with useful guidelines and an analytical tool for understanding parallel MOSFETs under avalanche operation.

1: Theoretical Analysis:

Let's use a low side hard switching circuit shown in Figure 1-a as an example. When paralleled devices avalanche, the device with lowest breakdown voltage will clamp the Vds and provide a low resistance path for the load. Therefore, nearly all load current tends to flow through this device, which would cause much higher loss than other paralleled devices. Figure 1-b shows the load and temperature changes. However, this is typically not the case, since breakdown voltage has positive temperature coefficient. When the lowest breakdown voltage MOSFET avalanches and dissipates avalanche energy, the die temperature will typically increase until its breakdown voltage equals the breakdown voltage of another paralleled devices. A thermal and electrical dynamic process will normally converge on a balance of the load current among devices. Figure 1-c illustrate the "re-balancing". And finally the FET turns off as shown in Figure 1-d ending the process. So the avalanche process would cause transient and steady state difference on the device thermal and electrical characteristics for paralleled devices.

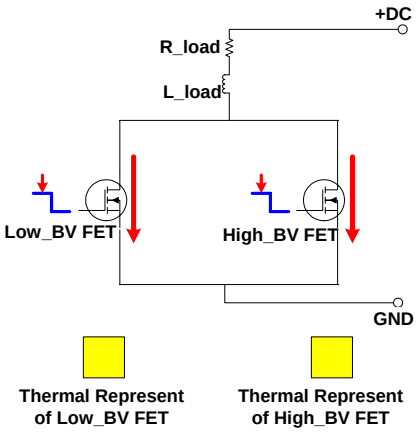

Figure 1-a: Current and thermal distribution during conduction

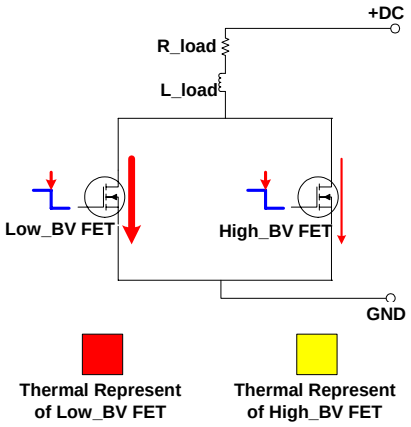

Figure 1-b: Response at the start of turn-off

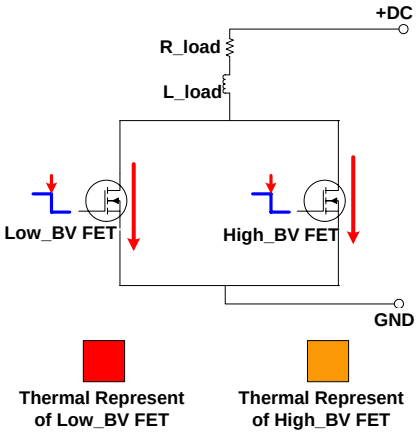

Figure 1-c: The rest of the turn-off process

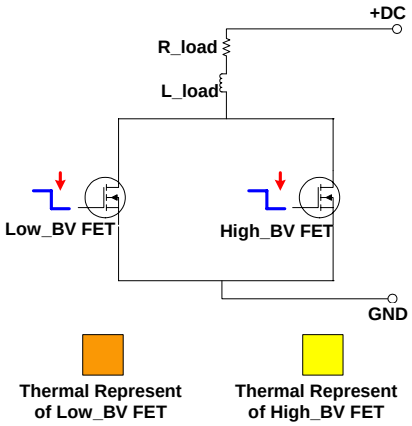

Figure 1-d: MOSFET off

2: Avalanche Modelling based on Quasi-dynamic MOSFET model:

Standard MOSFET model doesn't include the thermal effect. To reflect parameter thermal dependency, quasi-dynamic model is proposed by James C. Bach [2].

Quasi-dynamic thermal model: model equations are written such that the temperature is calculated from the resulting power dissipation. However, the temperature does not affect any or some of model characteristics. Only the external connected components change with the temperature change.

The reason for this approach is mainly from the following. The FET model defines its coefficients using the parameter section in MAST. And parameters (i.e. $R_{ds(on)}$, breakdown voltage) cannot be changed dynamically during simulation. Although a unique MOSFET model could be developed, the coding effort and simulation speed make it the last choice for designer to refine their design. On the other hand, it is of advantage to be able to use widely available MOSFET models with only minor change.

Initial quasi-dynamic model includes only $R_{ds(on)}$ and Vth temperature dependency. In this study, the avalanche behaviour is added to the quasi-dynamic model. To allow this to happen the value of the intrinsic $V_{(BR)DSS}$ constant is changed to an arbitrarily large value to defeat the internal static avalanche model from operation. An external equivalent circuit of the device quasi-thermal avalanche characteristic is then added in parallel with the MOSFET model as shown in Figure 2.

The equivalent circuit for the quasi-thermal avalanche characteristic is comprised of one diode and a temperature dependent serial voltage source BV(Tj). When the Vds is smaller than BV(Tj), the diode blocks the current. So the MOSFET works by itself. As the Vds becomes higher than BV(Tj), the diode conducts and most of the current will flow through the diode. At the

same time, the drain to source voltage is clamped by the BV(Tj). This process can be employed to emulate MOSFET avalanche and is easy to implement through MAST in SABER.

On MOSFET datasheet, $\Delta V_{(BV)DSS} / \Delta T_J$ is given assuming $V_{(BR)DSS}$ is a linear function of junction temperature (Tj). Equation 1 shows the relationship.

$$BV(Tj) = V_{(BV)DSS}(25^{\circ}C) + \Delta V_{(BV)DSS} / \Delta T_J * (T_J - 25) \quad (1)$$

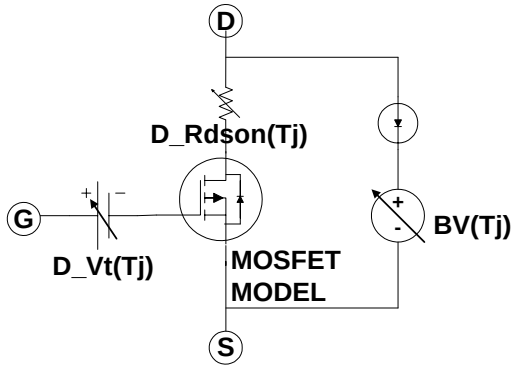

Figure 2: Avalanche model based on Quasi-dynamic model of IRF1404

III: Simulation and Results:

Half-bridge is a typical topology in motor drive and converter applications. So in this study, it is chosen to investigate the avalanche characteristics of paralleled MOSFETs.

For simplicity, term “BV” would be used through the rest of this paper to represent “Breakdown Voltage”.

1: Avalanche Behaviour of two MOSFETs in parallel

Circuit schematic of a half bridge low-side drive passive load system is shown in Figure 3. Two MOSFETs are paralleled as low-side switch. A 10Khz 50% duty cycle signal is applied to the gates of both FETs. When they turn on, voltage source would charge the load inductor and resistor. When they turn off, load current would flow through the free wheeling diode. A simple heatsink thermal RC is applied with device internal thermal networks written in MAST representing thermal impedance from junction to case to calculate junction temperature through its power losses. Ambient temperature is set to 25C. The PCB and harness inductance is lumped to one 200nH inductance.

From one lot measurement of IRF1404, at $25^{\circ}C$, BV average=42.24V. With 6 sigma guard band, BVmax=42.62V, BVmin=41.86V. Under worst case, the initial breakdown voltages of the two MOSFETs are set to Bvmax and Bvmin respectively.

As a base analysis, the stray inductances of the terminal connection of the paralleled MOSFETs are assumed to be zero. The stray inductance related to PCB and passive component is lumped as 200nH. Simulation results are shown in Figure 4, 5 and 6.

In Figure 4, at the beginning of the turn-off, the low BV MOSFET avalanches first, which presents a path with lower resistance than the high BV device. So it draws nearly all the load current and generates much higher dissipation. Its junction temperature increases, in turn making its BV higher, as shown in Figure 5. When the low BV FET catches up with the BV of the other FET, the resistivity of the two FETs is balanced again and the load current is evenly distributed. After that, breakdown voltages of the two FETs are aligned till the end of the turn-off. During the avalanche, the junction temperature of the low BV FET is higher than the high BV FET as shown in Figure 6.

So this is a thermal and electrical dynamic process. The low BV FET dissipates more (higher junction temperature) to gain balanced load current. However, from the application point of view, this behaviour means the low BV FET and FET bond wires will see higher thermal stress, which can be a reliability issue.

2: Different stray inductances

In the base analysis, the avalanche process of paralleled devices during the turn-off is revealed. However, for simplicity, the terminal stray inductances are set to be zero. To make a more realistic simulation, in this section, different stray inductances relevant to typical device terminal connection are considered.

This approach can also be seen as an investigation of the different characteristics between discrete device and module implementation of the same circuit in avalanche operation, because the terminal stray inductance are the most important parameter difference between them.

Figure 7 shows the circuit schematic. Red circles are used to mark the terminal stray inductances. Two cases with stray inductances Ls=4nH and 10nH are compared. All other conditions are the same as in case 1.

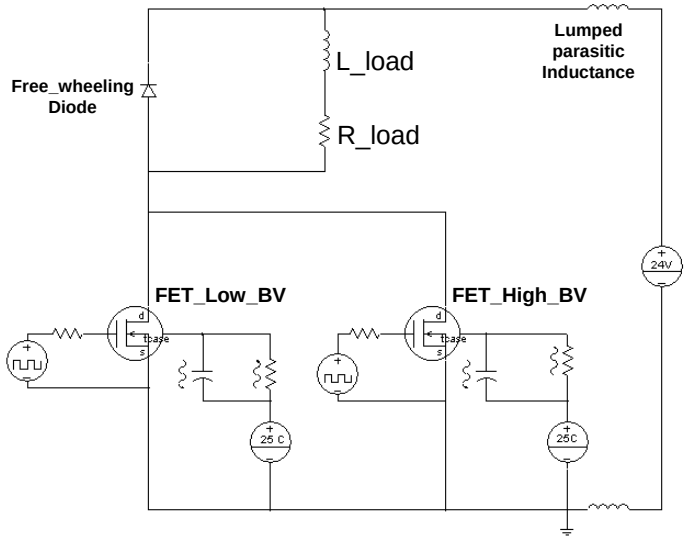

Figure 3: Circuit Schematic of two FETs in Parallel

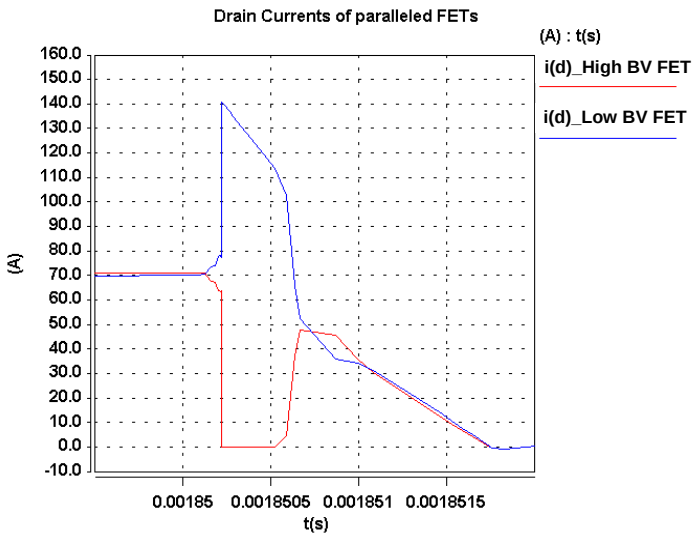

Figure 4: Drain Current of paralleled FETs

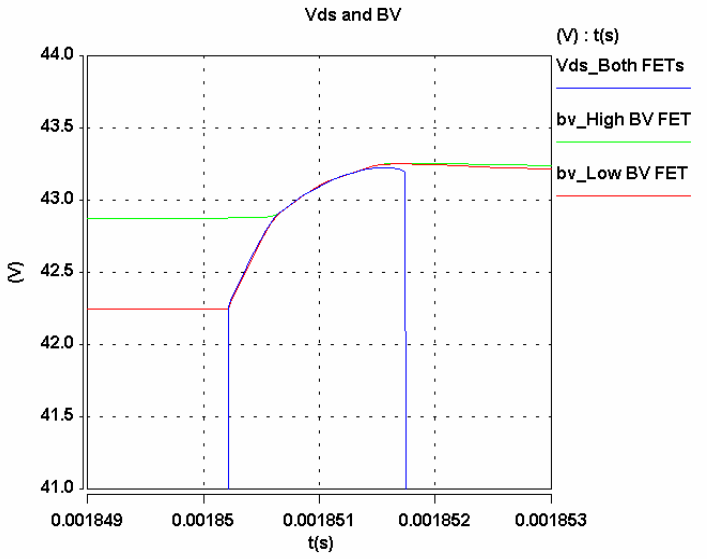

Figure 5: Vds and BV

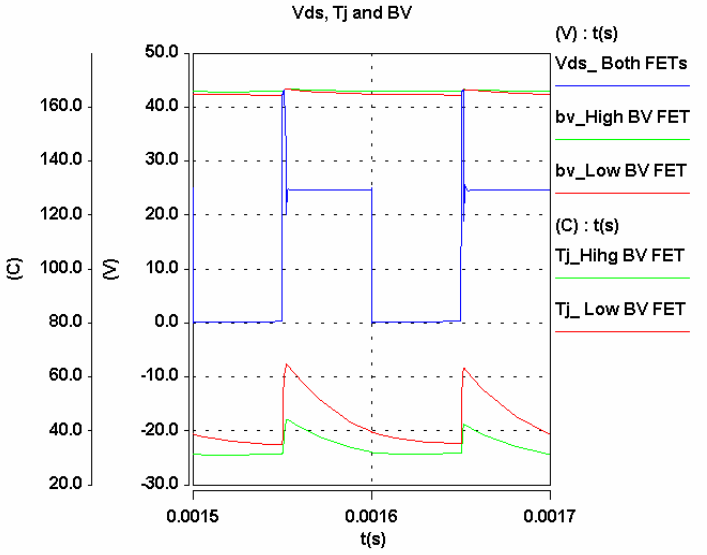

Figure 6: Vds, Tj and BV

In Figure 8, the drain current of the low BV FET is lower under high Ls than low Ls, while Id of the high BV FET is higher under high Ls than low Ls. In Figure 9, Vds of the low BV FET is lower under high Ls than low Ls, and the Vds of the high BV FET is higher under high Ls than low Ls. This means that with higher Ls, the BVs of the two paralleled FETs don't need to be closer as the voltages developed across the stray inductances already adjusts to help the thermal balance. This can also be seen from Figure 10. In Figure 11, it is clear that the temperature difference of the paralleled FETs is smaller under high Ls than low Ls.

So bigger terminal stray inductances can help balance the stresses on two paralleled devices.

3: Breakdown voltage parametric study

Another concern in this study is to investigate the effect of breakdown voltage variation on avalanche characteristics.

In the following simulation, initial breakdown voltage of one FET is set to BVmax=42.62V, initial BV of the other FET is changed from BVmin=41.86 to Bvmax=42.62 with five even steps Note: Ls=4nH.

Figure 12 to 15 show the variations of Id, Vds, Tj and BV. The closer the BVs of the two paralleled FETs, the closer the distribution of the load currents, Vds, and junction temperature.

4: Thermal coupling effect

All above simulations assume that there is no thermal coupling between the two paralleled devices. This may be nearly true for paralleled discrete devices, but is not typically true for module. Normally, in a module, the paralleled dies sit on the same copper etch of the DBC, which provide excellent lateral thermal transfer. In this simulation, a small thermal resistance (0.04C/W) is put between the die junctions of the two paralleled devices, as shown in Figure 16. Note: all stray inductances are kept 4nH.

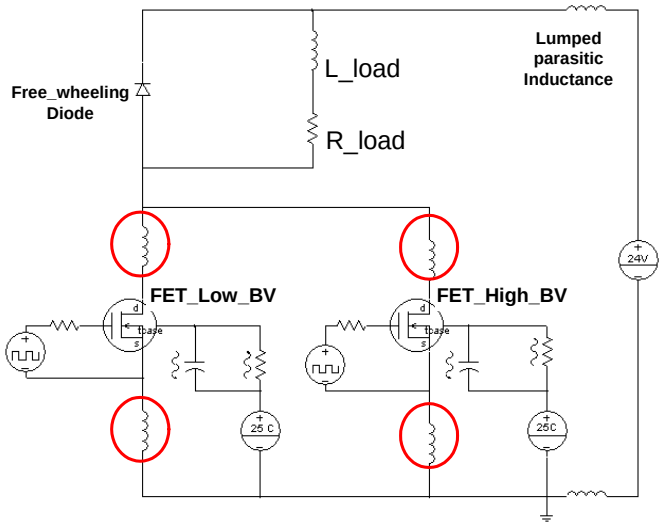

Figure 7: Circuit schematic for different terminal stray inductance

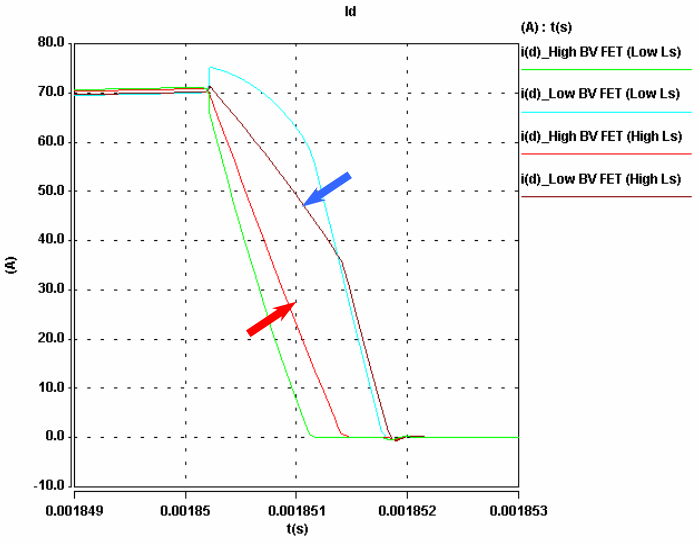

Figure 8: Id

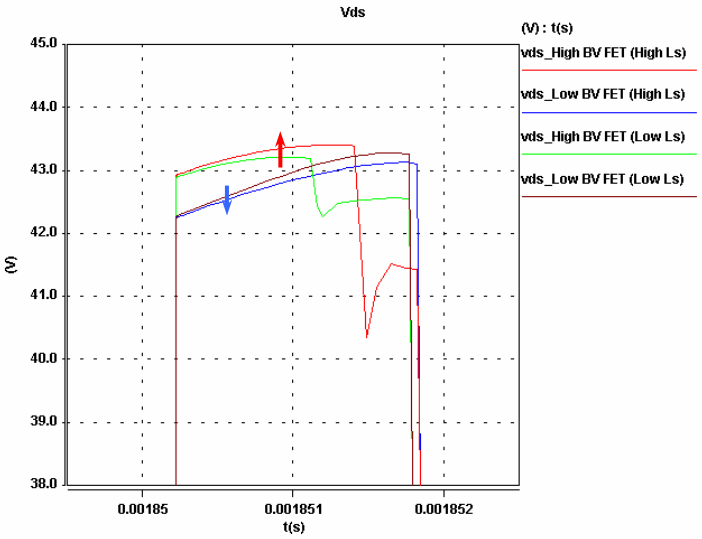

Figure 9: Vds

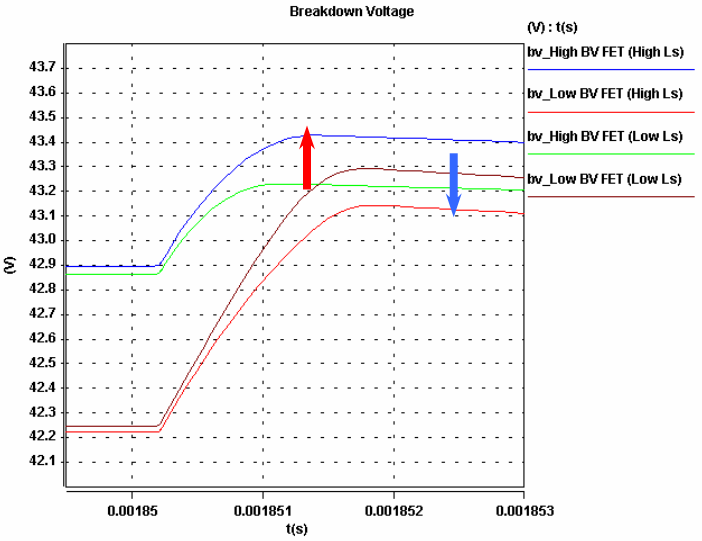

Figure 10: Breakdown Voltage (BV)

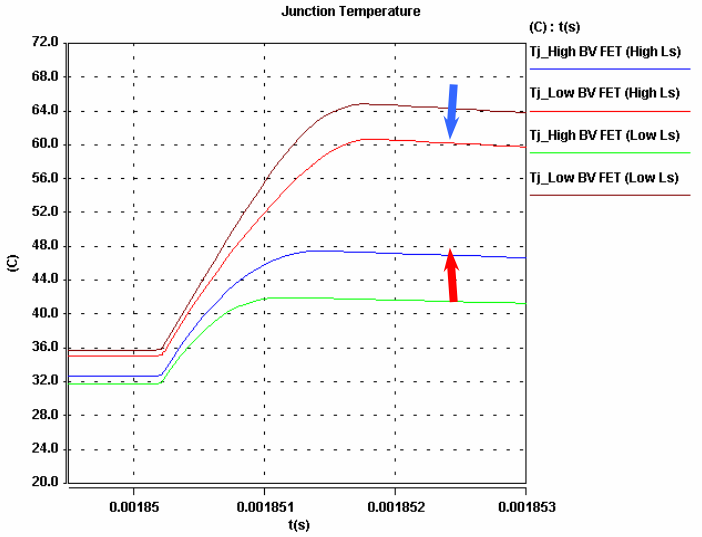

Figure 11: Junction Temperature (Tj)

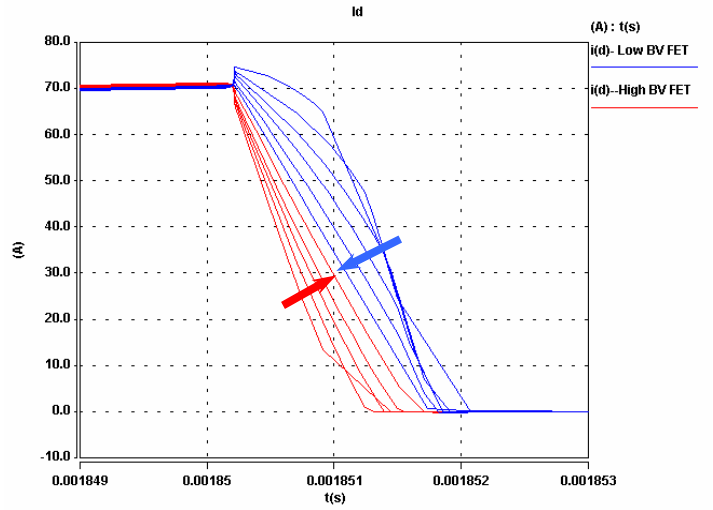

Figure 12: Id

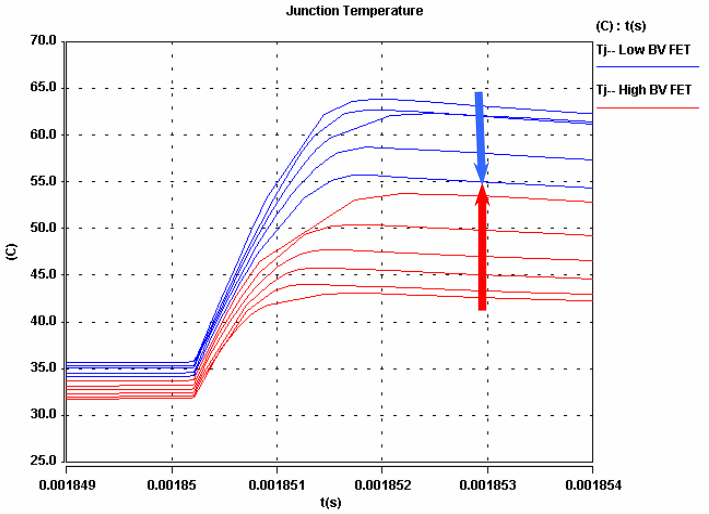

Figure 14: Tj

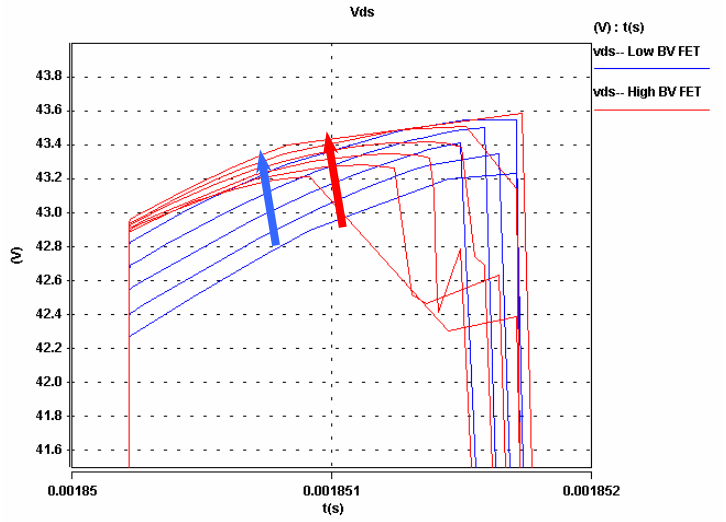

Figure 13: Vds

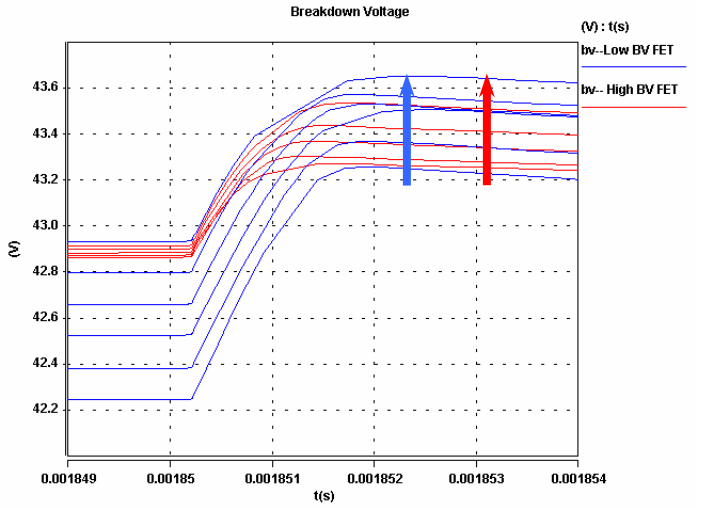

Figure 15: BV

Figure 17 shows Id. There is very small difference between them with and without thermal coupling. Junction temperatures in Figure 18 indicate that with thermal coupling, two paralleled devices demonstrate a smaller temperature difference. As a result, the Vds and BV shown in Figure 18 and 19 can be further apart under thermal coupling.

This means that with thermal coupling, the low BV FET transfers its heat to the high BV device. It makes the BV of the high BV device increase and that of the low BV device decrease compared to the low BV device under no thermal coupling condition, and the Vds difference is compensated by the terminal stray inductances.

So with thermal coupling, the thermal stress for the low BV FET is eased and that for the high BV FET is increased. The thermal conditions of the two paralleled FETs are further balanced.

However, the stray inductance would be under higher electrical stress, which could cause potential wire bond failure.

5: Three or more MOSFETs in parallel

In real high power applications, more than two power devices can be paralleled to share the high load current. So under worst case, the FET with lowest BV could take most of the load current and be quickly damaged.

Note: this is worst case condition. One device's BV at one extreme, all other devices have BVs at the other extreme. However, in reality, when more devices are paralleled, statistically, there is more possibility for these devices to have even BV distribution. So statistic analysis may provide different conclusion, which will be next step following this study.

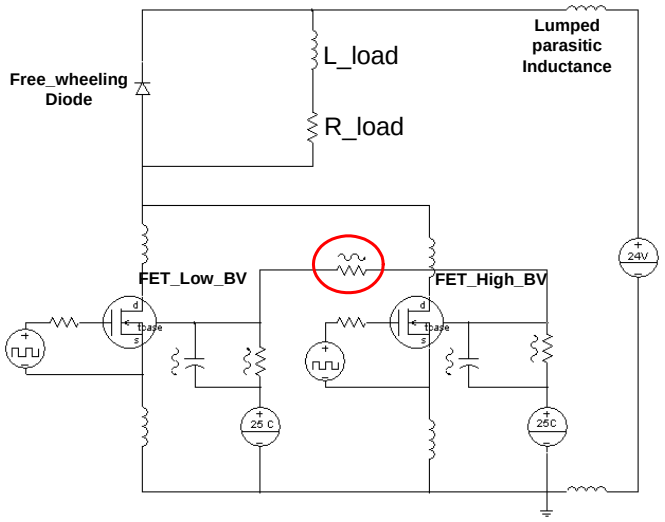

Figure 16: Circuit Schematic

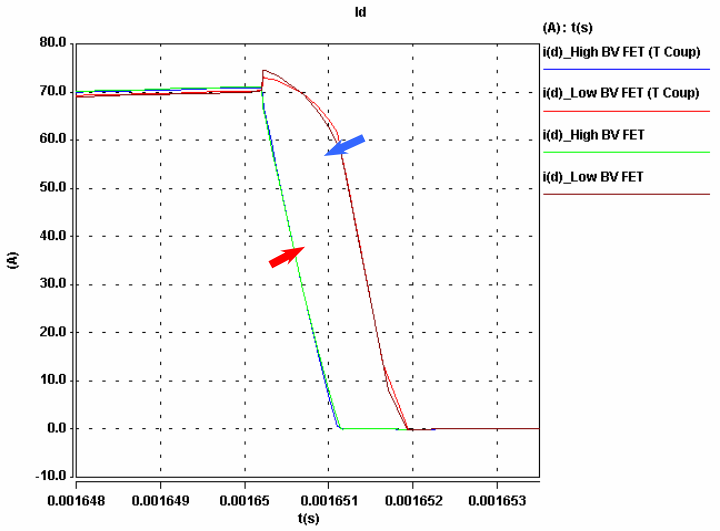

Figure 17: Id

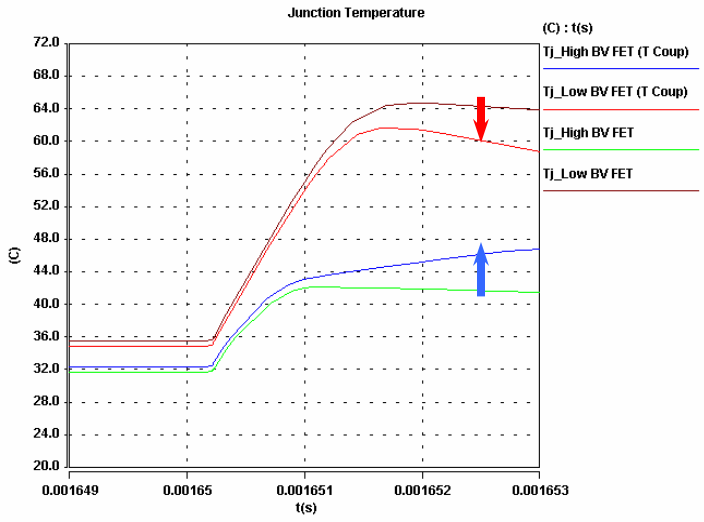

Figure 18: Junction Temperature (Tj)

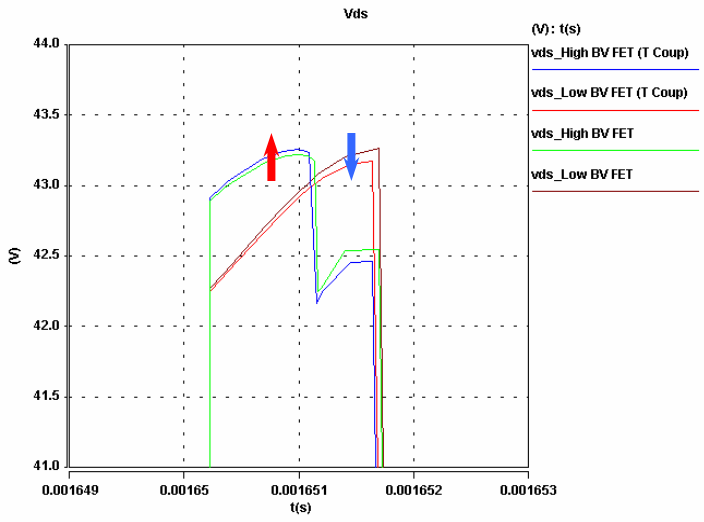

Figure 19: Vds

IV: Conclusions:

1: A quasi-dynamic MSFET model with temperature dependent breakdown voltage is established in this study. It can be used to represent the device avalanche characteristics.

2: Paralleled devices with varied breakdown voltages work under different electrical and thermal stresses. The lower BV device experiences higher stresses.

3: Under the same condition, paralleled devices with higher terminal stray inductances have more balanced load and more evenly distributed junction temperature.

4: Good thermal coupling among paralleled devices can help ease the electrical stress and balance the load.

3 and 4 suggest that in module solution of paralleling power devices, its good thermal coupling can help balance the load, but the small terminal stray inductances may not be very helpful from avalanche standpoint. This conclusion is only valid if devices in module definitely work under avalanche.

References:

[1]: Paralleling HEXFET Power MOSFETs. AN941 www.irf.com. Application Note of International Rectifier Co.

[2]: James C. Bach, “Development of an Electro-Thermal Power MOSFET Macro-Model”, Saber Asssure2000 users conference, May 10-12, 2000