Data sheet acquired from Harris Semiconductor
SCHS167A

November 1997 - Revised May 2000

CD54/74HC240, CD54/74HCT240, CD74HC241, CD54/74HCT241, CD54/74HC244, CD54/74HCT244

High Speed CMOS Logic Octal Buffer/Line Drivers, Three-State

Features

- **HC/HCT240 Inverting**
- **HC/HCT241 Non-Inverting**
- **HC/HCT244 Non-Inverting**
- **Typical Propagation Delay = 8ns at V_{CC} = 5V, C_L = 15pF, T_A = 25^{O}C for HC240**
- **Three-State Outputs**
- **Buffered Inputs**
- **High-Current Bus Driver Outputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC240 and ’HCT240 are inverting three-state buffers having two active-low output enables. The CD74HC241, ’HCT241, ’HC244 and ’HCT244 are non-inverting three-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD54HC240F3A	-55 to 125	20 Ld CERDIP
CD74HC240E	-55 to 125	20 Ld PDIP
CD74HC240M	-55 to 125	20 Ld SOIC
CD54HCT240F3A	-55 to 125	20 Ld CERDIP
CD74HCT240E	-55 to 125	20 Ld PDIP
CD74HCT240M	-55 to 125	20 Ld SOIC
CD74HC241E	-55 to 125	20 Ld PDIP
CD54HCT241F3A	-55 to 125	20 Ld CERDIP
CD74HCT241E	-55 to 125	20 Ld PDIP
CD74HCT241M	-55 to 125	20 Ld SOIC
CD54HC244F	-55 to 125	20 Ld CERDIP
CD54HC244F3A	-55 to 125	20 Ld CERDIP
CD74HC244E	-55 to 125	20 Ld PDIP
CD74HC244M	-55 to 125	20 Ld SOIC
CD54HCT244F	-55 to 125	20 Ld CERDIP
CD54HCT244F3A	-55 to 125	20 Ld CERDIP
CD74HCT244E	-55 to 125	20 Ld PDIP
CD74HCT244M	-55 to 125	20 Ld SOIC

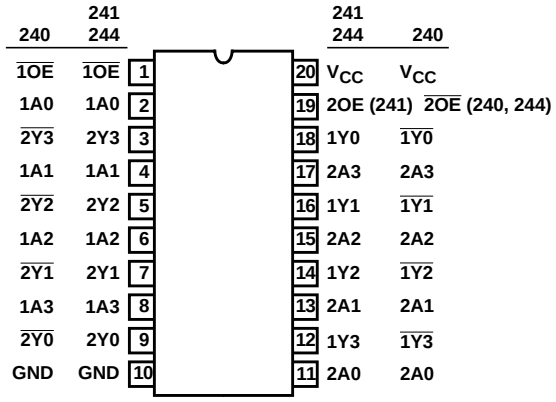
NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

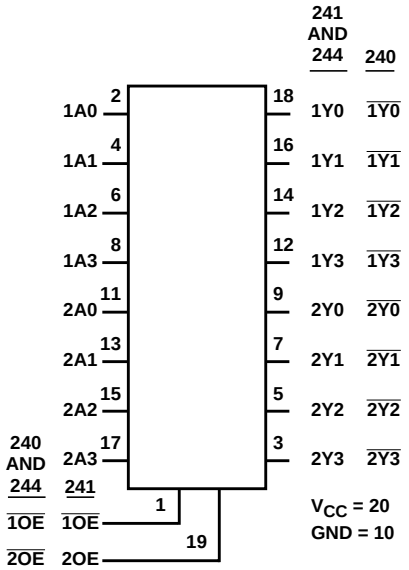
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Pinout

**CD54HC240, CD54HCT240, CD54HCT241,
CD54HC244, CD54HCT244
(CERDIP)
CD74HC240, CD74HCT240, CD74HC241, CD74HCT241,
CD74HC244, CD74HCT244
(PDIP, SOIC)**
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V. . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±70mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	125
SOIC Package	120

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	-	6	-	-	±0.5	-	±0.5	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	-	5.5	-	-	±0.5	-	±5	-	±10	µA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
HCT240	
nA0-A3	1.5
$\overline{1OE}$	0.7
$\overline{2OE}$	0.7
HCT241	
nA0-A3	0.7
$\overline{1OE}$	0.7
2OE	1.5
HCT244	
nA0-A3	0.7
$\overline{1OE}$	0.7
$\overline{2OE}$	0.7

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES													
Propagation Delay Data to Outputs HC240	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	100	-	-	125	-	-	150	ns
			4.5	-	-	20	-	-	25	-	-	30	ns
		C_L = 15pF	5	-	8	-	-	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	17	-	-	21	-	-	26	ns
Data to Outputs HC241	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	110	-	-	140	-	-	165	ns
			4.5	-	-	22	-	-	28	-	-	33	ns
		C_L = 15pF	5	-	9	-	-	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	19	-	-	24	-	-	28	ns
Data to Outputs HC244	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	110	-	-	140	-	-	165	ns
			4.5	-	-	22	-	-	28	-	-	33	ns
		C_L = 15pF	5	-	9	-	-	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	19	-	-	24	-	-	28	ns
Output Enable and Disable Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	150	-	-	190	-	-	225	ns
			4.5	-	-	30	-	-	38	-	-	45	ns
			5	-	12	-	-	-	-	-	-	-	ns
			6	-	-	26	-	-	33	-	-	38	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	60	-	-	75	-	-	90	ns
			4.5	-	-	12	-	-	15	-	-	18	ns
			6	-	-	10	-	-	13	-	-	15	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	-	10	-	-	10	pF
Three-State Output Capacitance	C_O	C_L = 50pF	-	-	-	20	-	-	20	-	-	20	pF
Power Dissipation Capacitance (Notes 5, 6) HC240	C_{PD}	C_L = 15pF	5	-	38	-	-	-	-	-	-	-	pF
HC241			5	-	34	-	-	-	-	-	-	-	pF
HC244			5	-	46	-	-	-	-	-	-	-	pF
HCT TYPES													
Propagation Delay Data to Outputs HCT240	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	22	-	-	28	-	-	33	ns
		C_L = 15pF	5	-	9	-	-	-	-	-	-	-	ns
Data to Outputs HCT241	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	25	-	-	31	-	-	38	ns
		C_L = 15pF	5	-	10	-	-	-	-	-	-	-	ns
Data to Outputs HCT244	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	25	-	-	31	-	-	38	ns
		C_L = 15pF	5	-	10	-	-	-	-	-	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Enable and Disable Times	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	30	-	-	38	-	-	45	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	4.5	-	-	12	-	-	15	-	-	18	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	-	10	-	-	10	pF
Power Dissipation Capacitance (Notes 5, 6))	C_{PD}												
HCT240		-	5	-	40	-	-	-	-	-	-	-	pF
HCT241		-	5	-	38	-	-	-	-	-	-	-	pF
HCT244		-	5	-	40	-	-	-	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per channel.
6. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

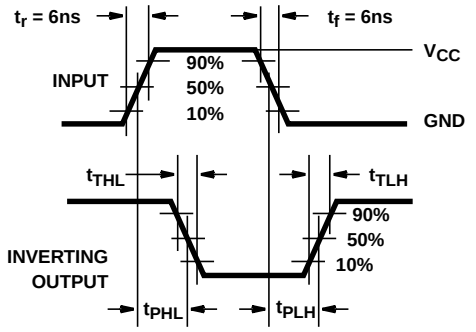


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

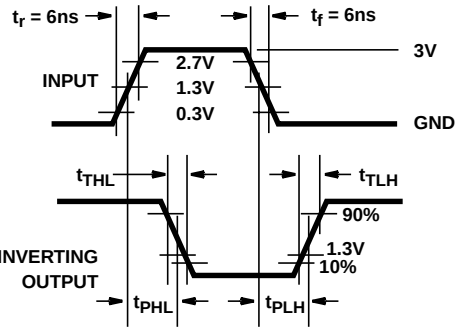


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

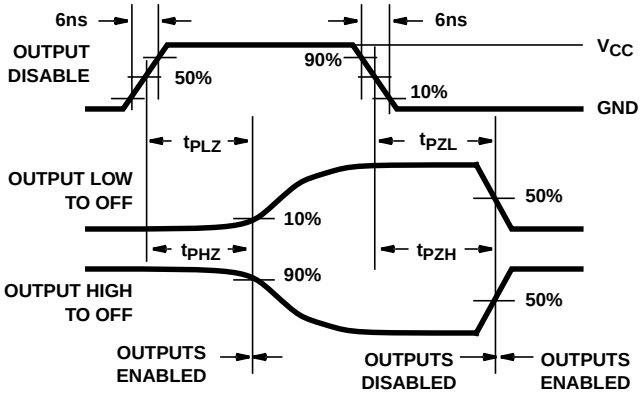


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

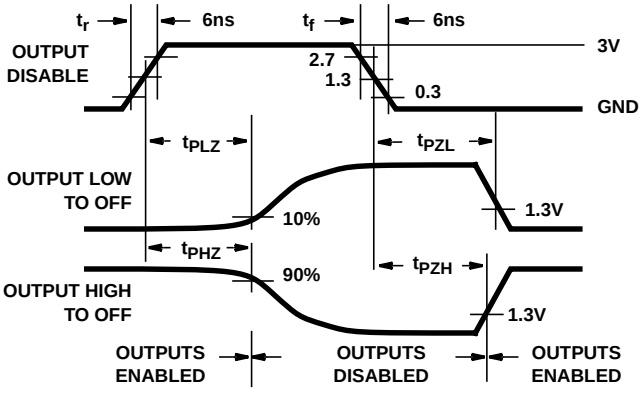
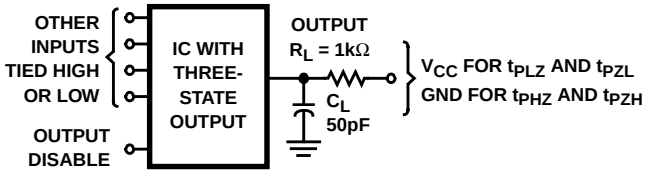


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM

Test Circuits and Waveforms (Continued)



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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