# Liquid Crystal Displays Standard Character Modules Application Notes

\*\*\*\*\* FEATURES OF OUR LCD MODULES \*\*\*\*\*\*

\*\*\*\*\* FEHIURES OF OUR LOD HODOLES AND 1.COMPACT AND LIGHT WEIGHT 2.HIGH CONTRAST AND WIDE WIEWING ANGLE 3.LOW POWER CONSUMPTION AND LOW VOLTAGE

# Seiko Insitunenis Embl



1.15

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## Dot Matrix Liquid Crystal Display Module

Character Type

#### **FEATURES**

- Slim, light-weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interface
- Available EL and LED backlight type
- Available in wide temperature type

The table below shows a quick reference guide of the character LCD modules. You can see the standard specifications and other optical specifications on the reference page of each model shown in the table below.

		-	-		1.9.			
Character Format (character x line)		16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2	
Model			M1641	M1632	L1642	L1652	L1614	L2012
<b>Reflective</b>			M16410AS	M16320AS	L164200J000S	L165200J200S	L161400J000S	L201200J000S
EL backlight			M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
LED backligh	t		M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
Reflective (w	ide temp)		M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
LED backligh	t (wide ten	np)	M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
Character for	nt		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor			
Module	Reflective	9	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
size	EL backlig	ght	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
(HxVxT) mm	LED back	light	80,0 x 36,0 x 15,8	80,0 x 30,0 x 15,8	80,0 x 36,0 x 15,8	122,0 x 44,0 x 15,8	87,0 x 60,0 x 15,8	116,0 x 37,0 x 15,8
View ing area	a (HxV) mr	n	64,5 x 13,8	62,0 x 16,0	64,5 x 13,8	99,0 x 24,0	61,8 x 25,2	83,0 x 18,6
Character siz	ze (HxV) n	nm	3,07 x 5,73	2,78 x 4,27	2,95 x 3,80	4,84 x 8,06	2,95 x 4,15	3,20 x 4,85
Dot size (Hx\	/) mm		0,55 x 0,75	0,50 x 0,55	0,50 x 0,55	0,92 x 1,10	0,55 x 0,55	0,60 x 0,65
Pow er supply	y voltage (	VDD-VSS)	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
Current cons	umption	IDD	1,5	2,0	1,6	2,0	2,7	2,0
(mA,typ)		ILC	0,2	0,2	0,3	0,4	1,1	0,4
Driving methe	od (duty)		1/16	1/16	1/16	1/16	1/16	1/16
			KS0066	KS0066	KS0066	KS0066	KS0066	KS0066
Built-in LSI			or equivalent	MSM5839	MSM5839	MSM5839	KS0063	KS0063
				or equivalent	or equivalent	or equivalent	or equivalent	or equivalent
Operating		normal temp.	0 to + 50	0 to + 50	0 to + 50			
temperature	( °C)	w ide temp.	- 20 to + 70	- 20 to + 70	- 20 to + 70			
Storage		normal temp.	- 20 to + 60	- 20 to + 60	- 20 to + 60			
temperature	( °C)	w ide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80			
Weight	Reflective	9	25	25	25	50	50	40
(g, typ.)	EL backlig	ght	30	30	30	55	55	45
	LED back	light	35	40	35	65	65	60
	Model		5S	5S	5S	5C	5A	5A
Inverters	Pow er su	ipply (V)	+ 5.0	+ 5,0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
for EL	current co	onsumption (mA	10	10	10	35	45	45
	Forw ard	current						
LED	consumpt	tion (mA)	100	112	100	240	200	154
backlight	Forw ard	input voltage						
	(V,typ.)		+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1
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## Dot Matrix Liquid Crystal Display Module

Character Type

## **FEATURES**

- Slim, light-weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interface
- Available EL and LED backlight type
- Available in wide temperature type

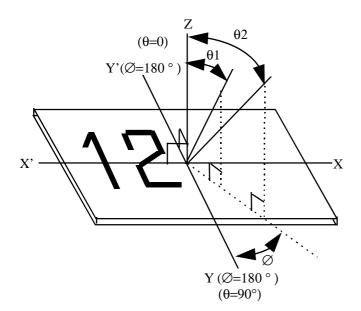
The table below shows a quick reference guide of the character LCD modules. You can see the standard specifications and other optical specifications on the reference page of each model shown in the table below.

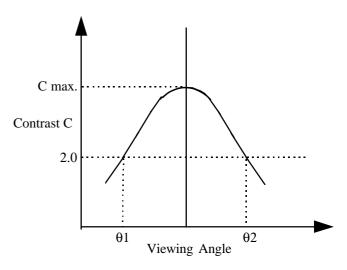
Character Fo	ormat (chara	cter x line)	20 x 2	20 x 4	24 x 2	40 x 2	40 x 4
Model			L2022	L2014	L2432	L4042	M4024
Reflective			-	L201400J000S	L243200J000S	L404200J000S	M40240AS
EL backlight			-	L201421J000S	L243221J000S	L404221J000S	M40249DWS
LED backlight	t		-	L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS
Reflective (w	ide temp)		L202200P000S	L201400L000S	L243200L000S	L404200L000S	M40240CS
LED backligh	t (w ide temp	o)	L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS
Character for	nt		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module	Reflective		180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
size	EL backligh	ıt	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
(HxVxT) mm	LED backlig	ght	180,0 x 40,0 x 14,8	98,0 x 60,0 x 15,8	118,0 x 36,0 x 15,8	182,0 x 33,5 x 16,3	190,0 x 54,0 x 16,3
View ing area	a (HxV) mm		149,0 x 23,0	76,0 x 25,2	94,5 x 17,8	154,4 x 15,8	147,0 x 29,5
Character siz	ze (HxV) mm	ı	6,00 x 9,66	2,95 x 4,15	3,20 x 4,85	3,20 x 4,85	2,78 x 4,27
Dot size (Hx\	/) mm		1,12 x 1,12	0,55 x 0,55	0,60 x 0,65	0,60 x 0,65	0,50 x 0,55
Pow er supply	y voltage (V	DD-VSS)	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
Current cons	umption	IDD	4,2	2,9	2,5	3,0	8,0
(mA,typ)		ILC	2,6	1,2	0,5	1,0	3,0
Driving metho	od (duty)		1/16	1/16	1/16	1/16	1/16
			KS0066	KS0066	KS0066	KS0066	KS0066
Built-in LSI			KS0063	MSM5839	KS0063	KS0063	MSM5839
			or equivalent	or equivalent	or equivalent	or equivalent	or equivalent
Operating		normal temp.	-	0 to + 50	0 to + 50	0 to + 50	0 to + 50
temperature	( °C)	w ide temp.	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
Storage		normal temp.	-	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
temperature	( °C)	w ide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight	Reflective		80	55	40	70	90
(g, typ.)	EL backligh	it	-	60	45	75	105
	LED backlig	ght	110	70	60	95	140
	Model		-	5A	5A	5C	5D
Inverters	Pow er sup	ply (V)	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
for EL	current con	sumption (mA)	-	45	45	25	80
	Forw ard cu	urrent					
LED	consumptio	on (mA)	320	240	150	260	480
backlight	Forw ard in	put voltage					
	(V,typ.)		+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1
Page			27	29	32	35	38

## **Definition of Optical Characteristics Term**

**Angles**  $\emptyset$  and  $\theta$ 

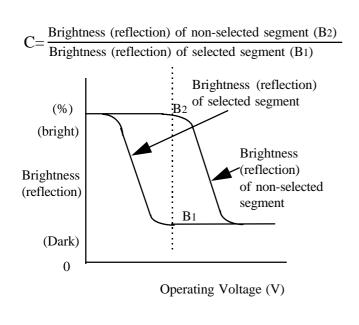
**Viewing Angle**  $\theta_1$  and  $\theta_2$ 

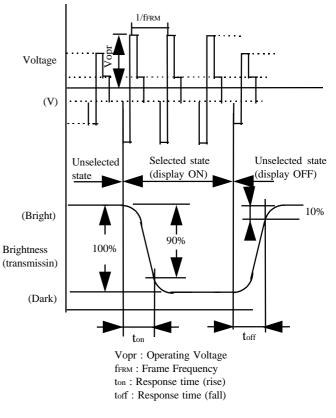




#### Contrast C







- **16** Characters x 1 line
- **5 x 7 Dot Matrix + Cursor**
- 1/16 Duty
- **5V single Power Supply**
- Available in EL and LED Backlight type

## ■ Absolute Maximum Ratings

V <sub>SS</sub> =0V, Ta=2						a=25°C
lte	em	Symbol	Conditions	Min.	Max.	Unit
Po	ow er supply	V <sub>DD</sub>		-0.3	6.0	V
vo	oltage	VLC		-0.3	V <sub>DD</sub>	V
In	put voltage	Vin		-0.3	V <sub>DD</sub> +0.3	V
0	perating temp	perature				
	Normal	Topr		0	+50	٥C
	Wide	Topr		-20	+70	٥C
St	torage tempe	rature				
	Normal	Tstg		-20	+60	٥C
	Wide	Tstg		-30	+80	٥C
S	torage		< 48 hrs	+20	+85	%RH
hι	umidity		<1000 hrs	+20	+65	%RH

## Mechanical Characteristics

Item		Specifications	Unit
Module size (H x \	/)	80.0 x 36.0	mm
Thickness Reflective/EL		11.3	mm
	LED	15.8	mm
View ing area (H x	V)	64.5 x 13.8	mm
Character size wit	h cursor (H x V)	3.07 x 6.56	mm
Mounting hole dist	ance (H x V)	75.0 x 31.0	mm
	Reflective	25	g
Weight	EL backlight	30	g
	LED backlight	35	g

## **Electrical Characteristics**

		$V_{DD}=5V\pm 5\%$	, V <sub>SS</sub> =	:0V, T	a=0 ~	50ºC
ltem	Symbol	Conditions	Min.	Тур.	Max.	Unit
Pow er supply	V <sub>DD</sub>		4.75	5.00	5.25	V
voltage	$V_{DD}\text{-}V_{LC}$		3.0	-	6.3	V
Input High	V IH1		2.2	-	Vdd	V
voltage Low	V <sub>IL1</sub>		0	-	0.6	V
Output High	V OH1	-юн=0.205mA	2.4	-	-	V
voltage Low	V <sub>LH1</sub>	-lol=1.2mA	1	-	0.4	V
Current consur	mption *					
Normal Temp	lod	Ta=25⁰C	-	1.3	2.0	mA
type	ILC	V <sub>LC</sub> =0.25V	-	0.2	0.6	mA
Wide Temp.	DD	Ta=25⁰C	-	1.6	2.5	mA
type	LC	V <sub>LC</sub> =-0.6V	-	0.3	1.0	mA

\* test pattern : check board pattern

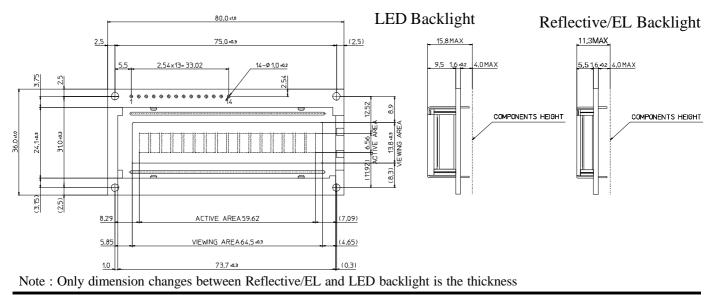
#### ■ Pin Function

No.	Name	Function
1	VSS	GND
2	VDD	Pow er supply voltage +5V
3	VLC	Liquid crystal driving voltage
4	RS	L : Instruction code input
		H: Data input
5	R/W	L : Data w rite from MPU to LCM
		H : Data read from LCM to MPU
6	E	Enable
7	DB0	Data bus line
8	DB1	Data bus line
9	DB2	Data bus line
10	DB3	Data bus line
11	DB4	Data bus line
12	DB5	Data bus line
13	DB6	Data bus line
14	DB7	Data bus line

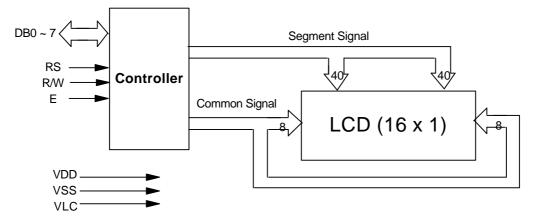
H: Horizontal, V: Vertical

## Dimensions

M1641~(1x16) Unit: mm. General tolerance  $\pm 0,5~\text{mm}$ 



## ■ Circuit Block diagram



#### ■ Recommended Operating Voltage

The recommended value (Vopr) for an ambient temperature

is as follow s. Vopr=VDD - VL							
Temperat	ure (ºC)	-20	0	+25	+50	+70	
Vopr (V)	Normal	-	5.00	4.75	4.50	-	
	Wide	6.20	5.90	5.60	5.40	5.20	

## ■ Optical Characteristics

#### 1. Normal Temperature Range Type

			Ta=2	1ºC, \	/opr=	4.75V
ltem	Symbol	Conditions	Min.	Тур.	Max.	Unit
View ing	<b>q</b> 1	C ≥2	-	1	-15	
angle	<b>q</b> 2	$F = 0^{\circ}$	55	-	-	deg.
	<b>q</b> 2- <b>q</b> 1		70	-	-	
Contrast	С	$q = +25^{\circ}, F = 0^{\circ}$	-	5	-	-
	ton (rise)	<b>q</b> =0°	-	150	200	msec
Response	toff (fall)	F =0 °	1	200	220	msec
time	ton (rise)	$q = 0^{\circ}, F = 0^{\circ}$	-	750	800	msec
	toff (fall)	Ta = 0°C, Vopr=5.0V	-	600	700	msec

Measuring equipment : Canon illuminater LC-4SR

#### 2.Wide Temperature Range Type

Ta=21°C, 1/16 Duty, Vopr=V <sub>DD</sub> - V <sub>L</sub>						
ltem	Symbol	Conditions	Min.	Тур.	Max.	Unit
View ing	<b>q</b> 1	C≥2	-	-	-15	
angle	<b>q</b> 2	$F = 0^{\circ}$	55	-	-	deg.
	<b>q</b> 2- <b>q</b> 1		70	-	-	
Contrast	С	$q = +20^{\circ}, F = 0^{\circ}$	-	5	-	-
		Vop=5,6v				
	ton (rise)	$q = 0^{\circ}, F = 0^{\circ}$	-	150	200	msec
Response	toff (fall)	Ta = 21ºC, Vopr=5.6V	1	200	220	msec
time	ton (rise)	$q = 0^{\circ}, F = 0^{\circ}$	1	750	800	msec
	toff (fall)	Ta = 0⁰C, Vopr=5.9V	-	600	700	msec

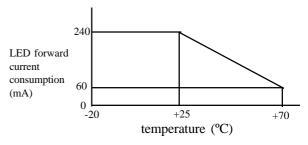
Measuring equipment : Canon illuminater LC-4SR

## LED Backlight

#### 1. Absolute Maximum Ratings

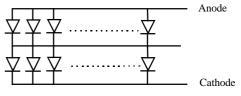
1. Absolute Maxin			a=25⁰C
Item	Symbol	Specifications	Unit
LED forw ard current	ŀF	240	mA
consumption *			
LED reverse voltage	Vr	8	V
Allow able loss	PD	1.05	W
Operating temperature	Topr	-20 ~ +70	٥C
Storage Temperature	Tstg	-40 ~ +80	٥C

\* LED forward current consumption and operating temperature characteristics are as follows.



#### 2. Electrical Characteristics

2. EICCIIC		Ta	=25ºC			
Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
LED forw ard	Vf	IF=120mA	3.8	4.1	4.4	V
input voltage						
LED reverse	lr	Vr=8V	-	-	0.16	mA
current						
Peak Emitting w	Peak Emitting w avelength			570	-	nm
Spectral half-w	IF=120mA*	-	30	-	nm	
Brightness	L	IF=120mA*	120	150	-	cd/m²



total number of LED chips  $=2 \times 8 = 16 \text{ pcs}$ 

## ■ EL Backlight

#### **1.Absolute Maximum Ratings**

Item	Symbol	Standard	Unit
Operating	Vopr	AC 150V, 1KHz	V
voltage		Sinew ave	
Operating	Topr	0 ~ +50	٥C
temperature			
Storage	Tstg	-20 ~ + 60	٥C
temperature			
Storage		0 ~ 10 % RH (60 ℃)	
humidity		0 ~ 30 % RH (40 °C)	

#### 2. Brightness, Current, Life Characteristics

Item	Conditions	Specifications	Unit
Brightness	100V, 400Hz	40 min.	cd/m²
	Sinew ave		
Current	100V, 400Hz	1.5 max.	mA
	Sinew ave		
Life	100V, 400Hz, Sinew ave	3,000	
	25ºC,50%RH		hrs
	Using 5S Inverter	6,000	
	25ºC,50%RH		

#### 3. Suitable Inverter 5S

# **3.1 Electrical Characteristics** (When combined with EL lamp)

			Ť	a=25⁰C
Item	Symbol	Conditions	Specifications	Unit
Oscillating	f <sub>INV</sub>	V <sub>IN</sub> =5VDC	550 typ.	Hz
frequency				
Output voltage	Vоит	VIN=5VDC	100 typ.	V
Output current	ЮUT	VIN=5VDC	1.5 typ.	mA
Input current	Vin		10	Vrms
Voltage	lin	VIN=5VDC	5 typ	VDC

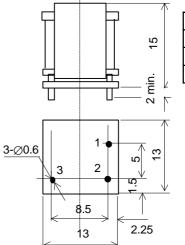
#### **3.2** Tolerance (Inverter only)

Item	Specifications	Unit
Input voltage	3.0 to 6.0	V
Load range	25 to 40	cm²

#### **3.3 Maximum Ratings (Inverter only)**

Item	Specifications	Unit
Input voltage	7.0	V
Load range	50	cm²
Operating temperature	-10 to +60	٥C
Storage temperature	-20 to +70	٥C

#### 3.4 Inverter Dimensions (unit : mm)



4		
	Pin No.	Function
	1	Input : 5V DC
	2	Common : GND
	3	Output



Typ. Max.

5.25

6.3

Vdd

0.6

-

0.4

3.0

1.0

3.0

1.0

5.00

-

-

-

-

-

1.8

0.4

2.0

0.5

Unit

V

V

V

V

V

V

mΑ

mΑ

mΑ

mΑ

V<sub>DD</sub>=5V± 5%, V<sub>SS</sub>=0V, Ta=0 ~ 50°C

Min.

4.75

3.0

2.2

0

2.4

-

-

\_

-

-

Pow er supply voltage +5V

L : Instruction code input

Liquid crystal driving voltage

L : Data w rite from MPU to LCM

H : Data read from LCM to MPU

Conditions

-юн=0.205mA

-IOL=1.2mA

Ta=25°C

VLC=0.25V

Ta=25⁰C

V<sub>LC</sub>=-0.6V

Function

H: Data input

Data bus line

Anode (+) for LED backlight

Cathode (-) for LED backlight

Enable

GND

- 16 Characters x 2 line
- 5 x 7 Dot Matrix + Cursor
- 1/16 Duty
- **5V single Power Supply**
- Available in EL and LED **Backlight type**

## ■ Absolute Maximum Ratings

V <sub>SS</sub> =0V, 1a=25 <sup>o</sup>						1=25°C
lte	em	Symbol	Conditions	Min.	Max.	Unit
P	ow er supply	Vdd		-0.3	6.0	V
vo	oltage	VLC		-0.3	V <sub>DD</sub>	V
In	put voltage	Vin		-0.3	V <sub>DD</sub> +0.3	V
Operating temperature		perature				
	Normal	Topr		0	+50	٥C
	Wide	Topr		-20	+70	٥C
S	torage tempe	rature				
	Normal	Tstg		-20	+60	٥C
	Wide	Tstg		-30	+80	٥C
S	torage		< 48 hrs	+20	+85	%RH
hι	umidity		<1000 hrs	+20	+65	%RH

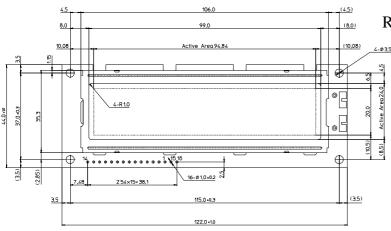
## Mechanical Characteristics

Item		Specifications	Unit
Module size (H x V	')	122.0 x 44.0	mm
Thickness Reflective/EL		11.3	mm
	LED		mm
View ing area (H x	ew ing area (H x V)		mm
Character size wit	h cursor (H x V)	sor(HxV) 4.84x9.66 mi	
Mounting hole dista	ance (H x V)	115.0 x 37.0	mm
	Reflective	50	g
Weight	EL backlight	55	g
	LED backlight	65	g

H : Horizontal, V : Vertical

## Dimensions

L1652 (2x16) Unit: mm, General tolerance  $\pm 0.5$  mm



#### Reflective/EL Backlight

Electrical Characteristics

Symbol

VDD

VDD - VLC

VIH1

VIL1

Vон1

VLH1

ЬD

LC

ldd

LС

test pattern : check board pattern

Name

VSS VDD

VLC

RS

R/W

Е

DB0

DB1

DB2

DB3

DB4

DB5

DB6

DB7

А

Κ

ltem

voltage

type Wide Temp.

type

No.

1

2

3

4

5

6

7

8

9

10

11

12

13

14

(15)

(16)

Input

Pow er supply

voltage Low

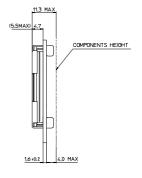
Output High

voltage Low

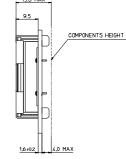
High

Current consumption \* Normal Temp

■ Pin Function

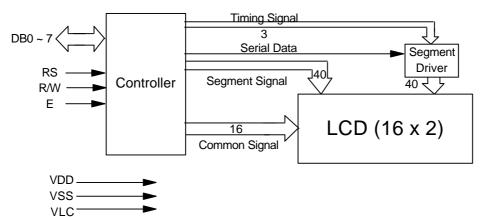


#### LED Backlight



Note : Only dimension changes between Reflective/EL and LED backlight is thickness.

## ■ Circuit Block diagram



## ■ Recommended Operating Voltage

The recommended value (Vopr) for an ambient temperature

is as follows. Vopr=VDD - VLC						/dd - Vlc
Temperat	ture (°C) -20 0 +25 +50 +70				+70	
Vopr (V)	Normal	-	5.00	4.75	4.50	-
	Wide	6.20	5.90	5.60	5.40	5.20

## Optical Characteristics

#### 1. Normal Temperature Range Type

	Ta=21°C, 1/16 Duty, Vopr=4.75					4.75V
ltem	Symbol	Conditions	Min.	Тур.	Max.	Unit
View ing	<b>q</b> 1	$C \ge 2$	-	-	-15	
angle	<b>q</b> 2	F = 90 °	55	1	-	deg.
	<b>q</b> 2- <b>q</b> 1		70	1	-	
Contrast	С	<b>q</b> =+5°, <b>F</b> = 90°	-	5	-	-
	ton (rise)	<b>q</b> =0°	-	150	200	msec
Response	toff (fall)	F =0 °	1	200	220	msec
time	ton (rise)	$q = 0^{\circ}, F = 0^{\circ}$	-	750	800	msec
	toff (fall)	Ta = 0°C, Vopr=5.0V	-	600	700	msec

Measuring equipment : Canon illuminater LC-4SR

#### 2.Wide Temperature Range Type

Ta=21°C, 1/16 Duty, Vopr=V <sub>DD</sub> - V <sub>LC</sub>					
Symbol	Conditions Min. Typ. Max. U				
<b>q</b> 1	C≥2	-	-	-15	
<b>q</b> 2	$F = 90^{\circ}$	55	1	-	deg.
<b>q</b> 2- <b>q</b> 1	Vop=5,6v	70	-	-	
С	<b>q</b> =+20°, <b>F</b> = 90°	-	5	-	-
	Vop=5,6v				
ton (rise)	$q = 0^{\circ}, F = 90^{\circ}$	-	150	200	msec
toff (fall)	Ta = 21⁰C, Vopr=5.6V	-	200	220	msec
ton (rise)	$q = 0^{\circ}, F = 90^{\circ}$	-	750	800	msec
toff (fall)	Ta = 0°C, Vopr=5.9V	-	600	700	msec
1	q         1           q         2	$q$ 1 $C \ge 2$ $q$ 2 $F$ = 90 ° $q$ 2 $F$ = 90 ° $q$ 2 $F$ = 90 ° $q$ 2 $Q$ = +20°, $F$ = 90 ° $C$ $q$ =+20°, $F$ = 90 °           ton (rise) $q$ = 0°, $F$ = 90 °           ton (rise) $q$ = 0°, $F$ = 90 °           ton (rise) $q$ = 0°, $F$ = 90 °           toff (fall)         Ta = 21°C, Vopr=5.6V           ton (rise) $q$ = 0°, $F$ = 90 °           toff (fall)         Ta = 0°C, Vopr=5.9V	$q$ 1 $C \ge 2$ - $q$ 2 $F$ = 90 °         55 $q$ 2 q 1         Vop=5,6v         70 $C$ $q$ =+20°, $F$ = 90 °         -           vop=5,6v         70         -           ton (rise) $q$ =0°, $F$ = 90 °         -           ton (rise) $q$ =0°, $F$ = 90 °         -           ton (rise) $q$ =0°, $F$ = 90 °         -           ton (rise) $q$ =0°, $F$ = 90 °         -           ton (rise) $q$ =0°, $F$ = 90 °         -           ton (rise) $q$ =0°, $F$ = 90 °         -           ton (rise) $T$ = 0°C, Vopr=5.9V         -	q 1 $C \ge 2$ -         -           q 2         F = 90°         55         -           q 2         F = 90°         55         -           q 2 - q 1         Vop=5,6v         70         -           C         q =+20°, F = 90°         -         5           Vop=5,6v         -         -         5           ton (rise)         q = 0°, F = 90°         -         150           toff (fall)         Ta = 21°C, Vopr=5.6V         -         200           ton (rise)         q = 0°, F = 90°         -         750	q 1 $C \ge 2$ -         -         -15           q 2 $F = 90^{\circ}$ 55         -         -           q 2 · q 1         Vop=5,6v         70         -         -           C $q = +20^{\circ}, F = 90^{\circ}$ -         5         -           Vop=5,6v         -         -         5         -         -           ton (rise) $q = 0^{\circ}, F = 90^{\circ}$ -         150         200           ton (rise) $q = 0^{\circ}, F = 90^{\circ}$ -         200         220           ton (rise) $q = 0^{\circ}, F = 90^{\circ}$ -         750         800           toff (fall)         Ta = 0^{\circ}C, Vopr=5.9V         -         600         700

Measuring equipment : Canon illuminater LC-4SR

## LED Backlight

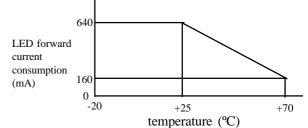
#### 1. Absolute Maximum Ratings

Ta=25⁰C

000

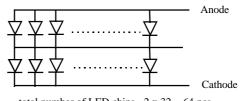
Item	Symbol	Specifications	Unit		
LED forw ard current	urrent l⊧ 640		mA		
consumption *					
LED reverse voltage	Vr	8	V		
Allow able loss	Po	2.8	W		
Operating Temperature	Topr	- 20 ~ +70	٥C		
Storage Temperature	Tstg	- 40 ~ + 80	٥C		

\* LED forward current consumption and operating temperature characteristics are as follows.



#### 2. Electrical Characteristics

					la	=25°C
Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
LED forw ard	Vf	IF=320mA	3.8	4.1	4.4	V
input voltage						
LED reverse	lr	Vr=8V	-	-	0.2	mA
current						
Peak emitting	IR	IF=320mA*	-	570	-	nm
w avelength						
Spectral	DI	IF=320mA*	-	30	-	nm
half-w idth						
Brightness	L	IF=320mA*	150	170	-	cd/m²



total number of LED chips  $=2 \times 32 = 64 \text{ pcs}$ 

## ■ EL Backlight

#### **1.Absolute Maximum Ratings**

Item	Symbol	Standard	Unit
Operating	Vopr	AC 150V, 1KHz	V
voltage		Sinew ave	
Operating	Topr	- 10 ~ +50	٥C
temperature			
Storage	Tstg	-20 ~ + 60	٥C
temperature			
Storage		0 ~ 10 % RH (60 ℃)	
humidity		0 ~ 30 % RH (40 ℃)	

#### 2. Brightness, Current, Life Characteristics

Item	Conditions	Specifications	Unit
Brightness	100V, 400Hz	40 min.	cd/m²
	Sinew ave	50 typ.	
Current	100V, 400Hz	3.0 typ.	mA
	Sinew ave	4.5 max	
Life	100V, 400Hz, Sinew ave	1,500	
	25ºC,50%RH		hrs
	Using 5C Inverter	3,500	
	25ºC,50%RH		

#### 3. Suitable Inverter 5C

#### 3.1 Electrical Characteristics (When combined with EL lamp)

			1	a-25 C
Item	Symbol	Conditions	Specifications	Unit
Oscillating	finv	VIN=5VDC	490 typ.	Hz
frequency				
Output voltage	Vоит	VIN=5VDC	92 typ.	V
Output current	ЮUT	VIN=5VDC	3.0 typ.	mA
Input current	Vin		5	Vrms
voltage	lin	VIN=5VDC	35 typ	mA

To-250C

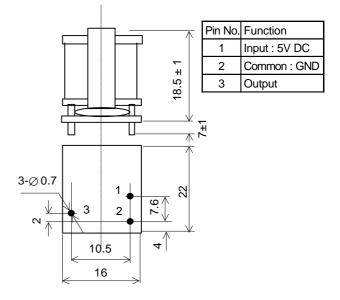
#### **3.2** Tolerance (Inverter only)

Item	Specifications	Unit
Input voltage	3.0 to 6.0	V
Load range	25 to 40	cm²

#### **3.3 Maximum Ratings (Inverter only)**

Item	Specifications	Unit
Input voltage	7.0	V
Load range	50	cm²
Operating temperature	-10 to +60	٥C
Storage temperature	-20 to +70	٥C

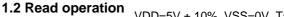
#### **3.4 Inverter Dimensions (unit : mm)**



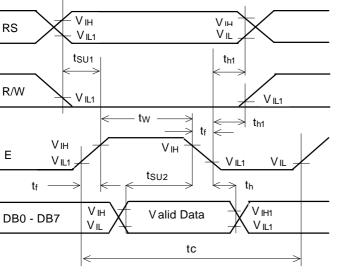
## **1. Timing Characteristics**

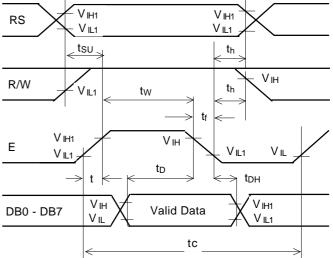
# **1.1 Write operation**

	VDD=5V	/ ± 10%. VS	5S=0V, Ta=	:25°C
Item	Symbol	Min.	Max.	Unit
Enabel cycle time	tc	500	-	ns
Enable rise time	tr	-	25	ns
Enable fall time	tf	-	25	ns
Enable pulse width	tw	220	-	ns
Setup time R/W, RS	ts∪1	40	-	ns
Hold time R/S, RS	th1	10	-	ns
Data setup time	ts∪2	60	-	ns
Data hold time	th2	10	-	ns



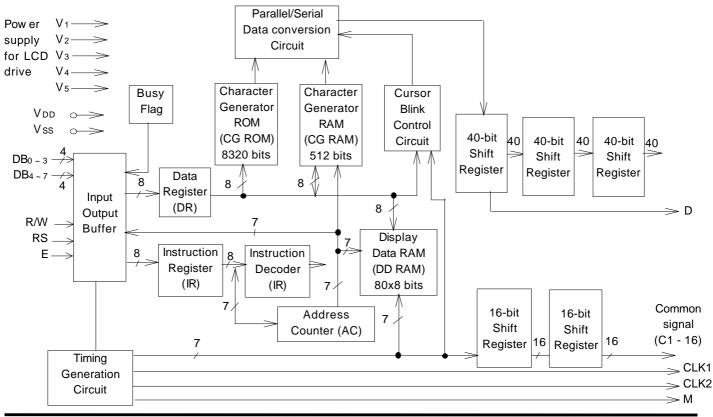
	VDD=5	/ ± 10%. VS	SS=0V, Ia=	25°C
ltem	Symbol	Min.	Max.	Unit
Enabel cycle time	tc	500	-	ns
Enable rise time	tr	-	25	ns
Enable fall time	tf	-	25	ns
Enable pulse width	tw	220	-	ns
Setup time R/W, RS	ts∪	40	-	ns
Hold time R/S, RS	th	10	-	ns
Data delay time	tD	-	120	ns
Data hold time	tDH	10	-	ns





## 2. Basic Operation

#### 2.1 Block Diagram of Controller KS0066



#### 2.2 Registers

The controller (KS0066) has to kinds of eight-bit registers ; the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown below table 1. The IR stores instruction codes such as Display Clear and Cursor Home, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but can not be read to the MPU. The DR temporarily stores data to be written into DD RAM or CG RAM, or data read from D RAM or CG RAM. For data write, the data written into the DR from the MPU is automatically written into DD RAM or CG RAM by internal operation. For data read, when the data address is written into the IR, the specified data is read out to the DR by internal operation. Then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

RS	R/W	Operation
0	0	IR selection, IR write. Internal operation : Display Clear, Cursor Home, etc
0	1	Busy flag (DB7) and address counter (DB0 to DB6) read
1	0	DR selection, DR w rite. Internal operation : DR to DD RAM or to CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

#### 2.3 Busy Flag (BF)

The busy flag indicates whether the module is ready to accept the next instruction. As shown in table, the signal is output to DB<sub>7</sub>, if RS=0 and R/W=1. If the busy flag is 0, the next instruction can be written. Therefore, the busy flag status needs to be checked before executing an instruction. To execute an instruction without checking the flag status, wait for more than the execution time of prior instruction. For the execution time of each instruction, see section 3 "Instruction Outline".

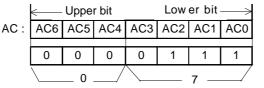
#### 2.4 Address Counter (AC)

The address counter specifies an address when data is written into DD RAM or CG RAM and when the data stored in DD RAM or CG RAM is read out. If an address Set instruction (for DD RAM orCG RAM) is written into IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB<sub>0</sub> to DB<sub>6</sub> if RS=0 and R/W=1 as shown in table 1.

#### 2.5 Display Data RAM (DD RAM)

DD RAM has a capacity of up to 80 x 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM that are not used for display can be used as general data RAM. A DD RAM address to be set in the AC is expressed in hexadecimal form as follows. Example : DD RAM address "07"

The correspondence between the DD RAM address and the display digits of the LCD panel is described in the followings.



#### 2.6 Address Location

The DD RAM address and the display digit of the LCD panel correspond as follows for LCD modules driven by 1/16duty and one controller can display maximum 80 characters.

	1	2	3	 15	16	17	18	19	20	 38	39	40	Display digit
Line 1	00	01	02	 0E	0F	10	11	12	13	 25	26	27	DD RAM
Line 2	40	41	42	 4E	4F	50	51	52	53	 65	66	67	address (HEX)

When the display digits are less than 40, the display begins at the head positions of the two lines. In this case, first line end address and the second line start address are not consecutive.

#### 2.6.1 M1641

 1
 2
 3
 4
 5
 6
 7
 8
 9
 10
 11
 12
 13
 14
 15
 16
 Display digit

 Line 1
 00
 01
 02
 03
 04
 05
 06
 07
 40
 41
 42
 43
 44
 45
 46
 47
 DD RAM address (HEX)

Note : This is initialised as a 2 line display because of no LCD driver. Character No.9 must be addressed as first position of 2nd line, which is 40 (HEX).

#### 2.6.2 M1632, L1642, L1652

2.0.2 MI1032, L	2.0.2 MITO52, ET042, ET052																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	address (HEX)
2.6.3 L1614																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	DD RAM
Line 3	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	address (HEX)
Line 4	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	

## **Operation Instruction**

Consequently, the end address of line 1 and the start address of line 3 are consecutive. Also, the end address of line 2 and the start address of line 4 are consecutive. The DD RAM address 00H to 27H are displayed in line 1 and line 3 and 40H to 67H in line 2 and line 4 by executing Display Shift.

#### 2.6.4 L2012, L2022

,	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	DD RAM
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	address (HEX)
2.6.5 L2014														-							
-	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	DD RAM
Line 3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	address (HEX)
Line 4	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	
	Line 2 2 <b>014</b> Line 1 Line 2 Line 3	Line 2 40 2014 1 Line 1 00 Line 2 40 Line 3 14	Line 1 00 01 Line 2 40 41 2014 1 2 Line 1 00 01 Line 2 40 41 Line 3 14 15	Line 1 00 01 02 Line 2 40 41 42 2014 Line 1 00 01 02 Line 2 40 41 42 Line 2 40 41 42 Line 3 14 15 16	Line 1 $\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Line 1 00 01 02 03 04 Line 2 40 41 42 43 44 2014 1 2 3 4 5 Line 1 00 01 02 03 04 Line 2 40 41 42 43 44 Line 3 14 15 16 17 18	Line 1 $\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Line 1 00 01 02 03 04 05 06 Line 2 40 41 42 43 44 45 46 2014 1 2 3 4 5 6 7 Line 1 00 01 02 03 04 05 06 Line 2 40 41 42 43 44 45 46 Line 3 14 15 16 17 18 19 1A	Line 1 00 01 02 03 04 05 06 07 Line 2 40 41 42 43 44 45 46 47 2014 1 2 3 4 5 6 7 8 Line 1 00 01 02 03 04 05 06 07 Line 2 40 41 42 43 44 45 46 47 Line 3 14 15 16 17 18 19 1A 1B	Line 1 00 01 02 03 04 05 06 07 08 Line 2 40 41 42 43 44 45 46 47 48 2014 1 2 3 4 5 6 7 8 9 Line 1 00 01 02 03 04 05 06 07 08 Line 2 40 41 42 43 44 45 46 47 48 Line 3 14 15 16 17 18 19 1A 1B 1C	Line 1 00 01 02 03 04 05 06 07 08 09 Line 2 40 41 42 43 44 45 46 47 48 49 2014 1 2 3 4 5 6 7 8 9 10 Line 1 00 01 02 03 04 05 06 07 08 09 Line 2 40 41 42 43 44 45 46 47 48 49 Line 3 14 15 16 17 18 19 1A 1B 1C 1D	Line 1 00 01 02 03 04 05 06 07 08 09 0A Line 2 40 41 42 43 44 45 46 47 48 49 4A 2014 1 2 3 4 5 6 7 8 9 10 11 Line 1 00 01 02 03 04 05 06 07 08 09 0A Line 2 40 41 42 43 44 45 46 47 48 49 4A Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 2014 1 2 3 4 5 6 7 8 9 10 11 12 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 2014 1 2 3 4 5 6 7 8 9 10 11 12 13 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 2014 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 2014 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 2014 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 2014 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 2014 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 2014 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26	Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 2014 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 Line 1 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 Line 2 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 Line 3 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27

Consequently, the end address of line 1 and the start address of line 3 are consecutive. Also, the end address of line 2 and the start address of line 4 are consecutive. The DD RAM address 00H to 27H are displayed in line 1 and line 3 and 40H to 67H in line 2 and line 4 by executing Display Shift

#### 2.6.6 L2432

Line 1       00       01       02       03       04       05       06       07       08       09       0A       0B       0C       0D       0E       0F       10       11       12       13       14       15       16       17       DD RAM         Line 2       40       41       42       43       44       45       46       47       48       49       4A       4B       4C       4D       4E       4F       50       51       52       53       54       55       57       address (HEX)         26.3       L4042       1       42       43       44       45       65       51       52       53       54       55       57       address (HEX)         26.3       L4042       1       42			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Display digit
2.6.3 L4042       1       2       3       3       15       16       17       18       19       20       38       39       40       Display digit         Line 1       00       01       02       0E       0F       10       11       12       13       25       26       27       DD RAM         Line 2       40       41       42       4E       4F       50       51       52       53       65       66       67       address (HEX)         2.6.4 M4024       1       2       3       15       16       17       18       19       20       38       39       40       Display digit         Line 1       00       01       02       0E       0F       10       11       12       13       25       26       27       DD RAM         Line 1       00       01       02       0E       0F       10       11       12       13       25       26       27       DD RAM         Line 2       40       41       42       4E       4F       50       51       52       53       65       66       67       DD RAM         Line 3 <t< td=""><td></td><td>Line 1</td><td>00</td><td>01</td><td>02</td><td>03</td><td>04</td><td>05</td><td>06</td><td>07</td><td>08</td><td>09</td><td>0A</td><td>0B</td><td>0C</td><td>0D</td><td>0E</td><td>0F</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>DD RAM</td></t<>		Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	DD RAM
1       2       3		Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	address (HEX)
Line 1 00 01 02 0E 0F 10 11 12 13 25 26 27 DD RAM Line 2 40 41 42 4E 4F 50 51 52 53 65 66 67 address (HEX) 2.6.4 M4024 1 2 3 0E 0F 10 11 12 13 38 39 40 Display digit Line 1 00 01 02 0E 0F 10 11 12 13 25 26 27 Line 2 40 41 42 4E 4F 50 51 52 53 65 66 67 DD RAM Line 3 00 01 02 0E 0F 10 11 12 13 25 26 27 address (HEX)	2.6.3	L4042																					Diam		-1: -: i t		•
Line 2 40 41 42 4E 4F 50 51 52 53 65 66 67 address (HEX) 2.6.4 M4024 1 2 3 15 16 17 18 19 20 38 39 40 Display digit Line 1 00 01 02 0E 0F 10 11 12 13 25 26 27 Line 2 40 41 42 4E 4F 50 51 52 53 65 66 67 DD RAM Line 3 00 01 02 0E 0F 10 11 12 13 25 26 27 address (HEX)			1	2	3				15	16	17	18	19	20					-								
2.6.4 M4024       1       2       3		Line 1	00	01	02				0E	0F	10	11	12	13						25	26	27	DD	RAN	1		
1       2       3        15       16       17       18       19       20        38       39       40       Display digit         Line 1       00       01       02        0E       0F       10       11       12       13        25       26       27         Line 2       40       41       42        4E       4F       50       51       52       53        65       66       67       DD RAM         Line 3       00       01       02        0E       0F       10       11       12       13        25       26       27         Line 3       00       01       02        0E       0F       10       11       12       13        25       26       27       address (HEX)		Line 2	40	41	42				4E	4F	50	51	52	53					-	65	66	67	add	ress	s (HE	EX)	
Line 1       00       01       02        0E       0F       10       11       12       13        25       26       27         Line 2       40       41       42        4E       4F       50       51       52       53        65       66       67       DD RAM         Line 3       00       01       02        0E       0F       10       11       12       13        25       26       27         Line 3       00       01       02        0E       0F       10       11       12       13        25       26       27	2.6.4	M4024																									
Line 2       40       41       42       4E       4F       50       51       52       53       65       66       67       DD RAM         Line 3       00       01       02       0E       0F       10       11       12       13       25       26       27       address (HEX)			1	2	3				15	16	17	18	19	20					-	38	39	40	Disp	olay	digit		
Line 3 00 01 02 0E 0F 10 11 12 13 25 26 27 address (HEX)		Line 1	00	01	02				0E	0F	10	11	12	13					-	25	26	27					
		Line 2	40	41	42				4E	4F	50	51	52	53						65	66	67	DD	RAN	1		
Line 4 40 41 42 4E 4F 50 51 52 53 65 66 67		Line 3	00	01	02				0E	0F	10	11	12	13						25	26	27	add	ress	s (HE	EX)	
		Line 4	40	41	42				4E	4F	50	51	52	53					-	65	66	67					

M4024 has two LCD controllers. Since the capacity for each is 80 characters (40 characters x 2 lines), M4024 can display 160 characters (40 characters x 4 lines) by using two LCD controllers. Line 1 and 2 are activated by E1. Line 3 and 4 are activated by E2. All the four lines cannot be shifted at the same time. Instructions must be written using E1 and E2 to distinguish the upper two lines from the lower two lines.

#### 2.7 Character Generator ROM (CG ROM)

CG ROM generates 5x7 dot-matrix character patterns from eight-bit character codes. In LCD modules of 5x7 dot-matrix character pattern, CG generates 192 types of 5x7 characters. Table 2 shows the correspondence between the CG ROM character codes and character patterns of 5x7 dot-matrix.

#### 2.8 Character Generator RAM (CG RAM)

CG RAM is used to create character patterns freely by program. Eight types of 5x7 dot-matrix character patterns can be written into a CG RAM. Table 3 shows the character patterns created from CG RAM addresses and CG RAM data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

#### 2.9 Cursor/Blink Control Circuit

The circuit generates the cursor or blink. When the address counter (AC) selects the address of DD RAM, the cursor or the blink appears in the digit corresponding to the address. When the address counter is 08H, a cursor or blink position is in the 9th digit in line 1 as shown below.

The cursor or blink also appears when the character generator RAM (CG RAM) is selected by the address counter. In this case, the cursor or blink position has no meaning.

		AC	6 AC	C <sub>5</sub> A	C4 /	AC3	AC <sub>2</sub>	AC	1 AC	C <sub>0</sub>							
	AC	0	C	)	0	1	0	0	(	)							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	address (HEX)

# **Operation Instruction**

Table 2 Correspondence between character codes and character pattern (5x7 dot -matrix)

\_\_\_\_

									nara				401	maa	<u> </u>
Upper 4 bits Low er 4 bits	0000	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)														
XXXX0001	(2)														
XXXX0010	(3)			::: :::											
XXXX0011	(4)														
XXXX0100	(5)														
XXXX0101	(6)														
XXXX0110	(7)														
XXXX0111	(8)														
XXXX1000	(1)														
XXXX1001	(2)														
XXXX1010	(3)														
XXXX1011	(4)														
XXXX1100	(5)														
XXXX1101	(6)														
XXXX1110	(7)														
XXXX1111	(8)														

Table 3 Relation between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM) (5x7 dot-matrix)

		Chai (DD						(	CG R	AM /	٩ddr	ess						racte S RA				
7	6	5	4	3	2	1	0	5	4	3	2	1	0		7	6	5	4	3	2	1	0
←	Upp	er bi	t	L	.ow e	er bit	$t \rightarrow$	+ ۱	Jppe	r bit	Lo	wer	$\rightarrow$	*	←	Upp	ber b	it	L	ow e	er bit	$\rightarrow$
											0	0	0		*	*	*	1	1	1	1	0
											0	0	1			$\wedge$		1	0	0	0	1
											0	1	0					1	0	0	0	1
0	0	0	0	*	0	0	0	0	0	0	0	1	1					1	1	1	1	0
											1	0	0					1	0	1	0	0
											1	0	1					1	0	0	1	0
											1	1	0			V		1	0	0	0	1
											1	1	1		*	*	*	0	0	0	0	0
											0	0	0		*	*	*	1	0	0	0	1
											0	0	1			$\wedge$		0	1	0	1	0
											0	1	0					1	1	1	1	1
											0	1	1					0	0	1	0	0
0	0	0	0	*	0	0	1	0	0	1	1	0	0					1	1	1	1	1
											1	0	1					0	0	1	0	0
											1	1	0			V		0	0	1	0	0
											1	1	1		*	*	*	0	0	0	0	0
											0	0	0		*	*	*					
											0	0	1			$\uparrow$						
								 <u> </u>			0	1	0									
0	0	0	0	*	1	1	1	1	1					I								
											1	0	1		Γ	T						
											1	1	0			$\downarrow$						
											1	1	1		*	*	*					

Example of character pattern (R) and (¥)

\* : don't care bit

Notes : - In CG RAM data, "1" corresponds to Selection and "0" to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond to each other (three bits, eight bytes).

- CG RAM address bits 0 to 2 specify a line position for a character pattern, Line 8 of a character pattern is the cursor position where the logical OR of the cursor and CG RAM data is displayed. Set the data of line 8 to "0" to display the cursor. If the data is changed to "1", bit 1 lights, regardless of the cursor.

- The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

- When regarding a character pattern from CG RAM, set to "0" all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00H and 08H select the same character.

## **Operation Instruction**

## 3. Instruction Outline

When MPU controls LCD controller on the LCD module, MPU directly controls only two registers of the controllers; the Instruction Register (IR) and the Data Register (DR). Prior to internal operation start, the controller temporarily stores control information in these registers, so as to interface with various types of MPUs or peripheral control ICs which operate at different speeds from speed of controller internal operation.

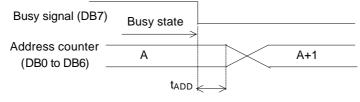
Table 4 shows the instructions and their execution time.

While the controller is executing an instruction and internal operation is in progress, the controller will accept and execute no instruction other than the Busy Flag/Address Read instruction.

Since the busy flag is set to "1" while an instruction is being executed, check the busy flag status and make sure it is "0" before sending an instruction from the MPU to the controller.

To send instructions without checking the busy flag, make sure that the interval between two instructions is much longer than the execution time of the prior instruction.

After the execution of writing/reading data instruction to/from CG/DD RAM, RAM address counter is automatically incremented or decrement by one. This increment/decrement / is executed after the busy flag is set to "0". The time from the fall edge of busy flag to the end of address counter renewal (tADD) is as shown below.

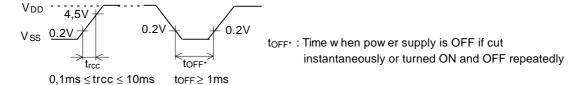


tADD depends on the clock oscillation frequency (fosc) t<sub>ADD</sub> = 1.5 (s)

## 4. Initialization

#### 4.1 Automatic Initialisation

The system is automatically initialised at power-on if the following power supply conditions are satisfied.



In automatic initialisation, the following instructions are executed.

- \* Display Clear
- \* Function Set
  - DL = 1 : Interface data length : Eight bits
- N = 0, F = 0: 1/8 duty, character font : 5 x 7 dot-matrix
- Display ON/OFF control
- D = 0: Display OFF
- C = 0 : Cursor OFF
- B = 0 : Blink OFF
- Entry Mode Set
- I/D = 1 : Increment
- S = 0: No display shift

Since some conditions set by initialisation may not be suitable for the LCD module, execute further Function Set instruction. The busy flag (BF) is kept busy until initialisation ends. The busy state remains for 20ms after VDD reaches to 4.5V.

If the power supply conditions are not satisfied and automatic initialisation is not executed. Execute initialisation using instruction according to section 4.2, "Initialisation by Instruction".

#### 4.2 Initialisation by Instruction

If automatic initialisation is not executed because the power supply conditions are not satisfied, use interface data length of eight bits or four bits instructions shown in table 4 and table 5 to implement initialisation.

Since it is unknown whether the interface data length is set to eight bits or four bits at power on, execute Function Set twice to set the interface data length to eight bits and then set the required interface data length by executing further Function Set instruction.

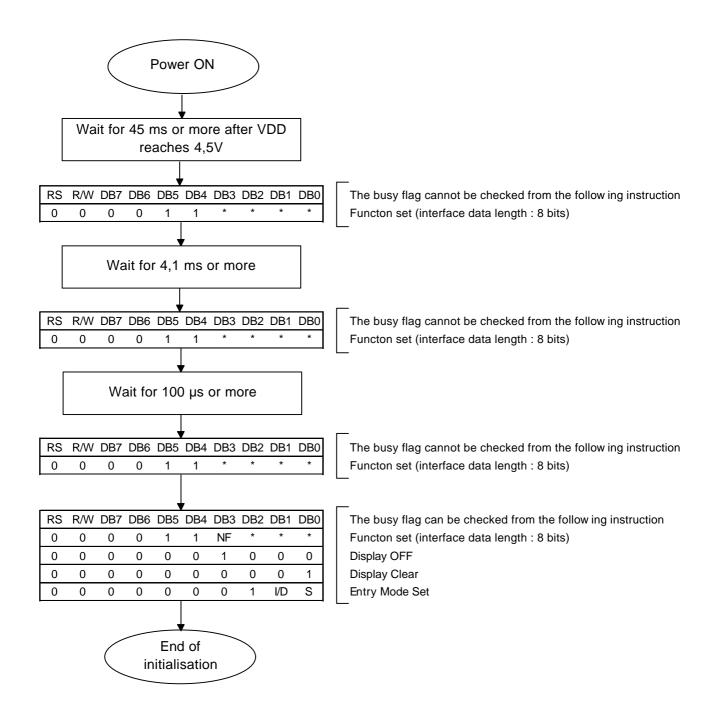
fosc

#### Table 4 List of Instruction

Instruction					Cod	е					Function	Execution
Instruction	RS	R/W	DB7	$DB_6$	DB <sub>5</sub>	DB4	DB <sub>3</sub>	DB <sub>2</sub>	DB <sub>1</sub>	DB <sub>0</sub>	Function	time **
(1) Display Clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1,64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position, shifted display returns to home position and DD RAM contents do not change	1,64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and w hether display w ill be shifted w hen data is w ritten or read	40 µm
(4) Display ON/OFF Control	0	0	0	0	0	0	1	D	с	в	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µm
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40 µm
(6) Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), the duty (N), and character fonts (F)	40 µm
(7) CG RAM Address Set	0	0	0	1		<u></u>	Acg	1	<u></u>	<u></u>	Sets CG RAM address to start transmitting or receiving CG RAM data	40 µm
(8) DD RAM Address Set	0	0	1				A <sub>DD</sub>				Sets DD RAM address to start transmitting or receiving DD RAM data	40 µm
(9) BF/Address Read	0	1	BF				AC				Reads BF indicating module in internal operation and AC contents (use for both CG RAM and DD RAM)	0 µm
(10) Data Write to CG RAM or DD RAM	0	1		<u> </u>		Wi	rite D	ata			Writes data into DD RAM or CG RAM	40 μm t <sub>ADD</sub> =6μm
(11) Data Read from CG RAM or DD RAM	1	1				Re	ad D				Reads data from DD RAM or CG RAM	40 μm tadd=6μm
* : Don't care bit A <sub>CG</sub> : CG RAM addres A <sub>DD</sub> : DD RAM address				ncrem Decrei				1 : Bli 0 : Bli			N = 1 : 1/16 duty N = 0 : 1/8 duty or 1/11 duty	
AC : Address counter					y shift play s				-	ay sh or mo	ift $F = 1 : 5 x 10$ dot matrixvement $F = 0 : 5 x 7$ dot matrix	
				splay splay	ON OFF			= 1 : = 0 :			BF = 1 : Internal operation in BF = 0 : Instruction can be a	
				ursor ursor				= 1 : 8 = 0 : 4				

\*\* Execution time in the above Table indicated the maximum value w hen fosc is 250KHz. It changes w hen fosc changes. When fosc = 270 KHz : 40  $\mu$ s x 250 / 270 = 37  $\mu$ s

#### Table 5. Interface Data Length : Eight bits



## **5. Instruction Detail**

#### 2.5.1 Display Clear

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Display CLEAR clears all display and returns cursor to home position (address 0). Space code 20H is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC, if it was shifted, the display returns to the original position. The cursor or blink go to the left end on line 1, except M4024. In M4024, if the cursor or blink is on line 3 or line 4, it returns to the left end of line 3. After execution of the Display Clear instruction, I/D = 1 (increment) of Entry Mode is set.

#### 2.5.2 Cursor Home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	*

CURSOR Home returns cursor to home position (address 0). DD RAM address 0 is set to the AC. The display returns to the original position if it was shifted. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left end, except M4024. In M4024, if the cursor or blink on line 3 or line 4, it returns to the left end of line 3.

#### 2.5.3 Entry Mode Set

		R/W								
Code	0	0	0	0	0	0	0	1	I/D	S

ENTRY Mode Set sets the direction of cursor movement and determines whether display is shifted.

I/D :The DD RAM address is incremented or decremnted by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S: If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not changed only the display moves, There is no display shift for reading form DD RAM.

When S = 1 and I/D = 1, the display shifts one digit to the left after data write to DD RAM.

When S = 1 and I/D = 0, the display shifts one digit to the right after data write to DD RAM.

If S = 0, the display does not shift.

#### 2.5.4 Display ON/OFF Control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
-											ı.

Code	0	0	0	0	0	0	1	D	С	В	
											•

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the character on the cursor position start blinking Cursor ON/OFF and blinking is done at the digit indicated by the DD RAM address specified by the AC

- D: When D = 1, the display is turned ON
  - When D = 0, the display is turned OFF

If D = 0 is used, display data remains in DD RAM. Therefore the data can be displayed again by setting D = 1.

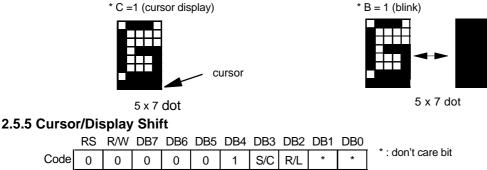
- C: When C = 1, the cursor is displayed
  - When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the character fonts.

B: When B = 1, the character at the cursor position starts blinking.

When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds when fosc is 250KHz. The cursor and blinking can be set at the same time.



Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents. The cursor position and the AC contents match. This instruction is useful for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data, In a 2-line display, the cursor is shifted from digit 40 (DD RAM address 27) of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time Display shift moves the display of each line only horizontally. Therefore, the display pattern of line 2 is not shifted to line 1 and display pattern of line 1 is not shifted to line 2.

Note : M1641 operates internally as 8 characters x 2 line display, L1614 as 32 characters x 2 line-display, L2014 as 40 characters x 2 line-display and M4024 as two 40 characters x 2 line-display. See section 2.6 Address Location.

## **Operating Instruction**

R/L	Operation
0	The cursor position is shifted to the left (the AC is decremented by one)
1	The cursor position is shifted to the right (the AC is incremented by one)
0	The entire display is shifted to the left with the cursor
1	The entire display is shifted to the right with the cursor
	0 1 0

#### 2.5.6 Function Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	Ν	F	*	*

\* : don't care bit

Function Set sets the interface data length, the number of display lines and the character font.

DL : Interface data length

When DL = 1, the data length is set at eight bits (DB7 to DB0)

When DL = 0, the data length is set at four bits (DB7 to DB4). In 4-bit interface, the upper four bits are transferred first, then the lower four bits follow.

N : When N = 1, the duty is set to 1/16

When N = 0, the duty is set to 1/8 or 1/11

F : Character font

When F = 1, the character font is set to 5 x10 dot matrix

When F = 0, the character font is set to 5 x 7 dot matrix.

If N is set to 1, F becomes " Don't care bit"

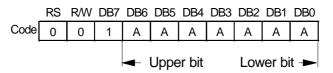
Ν	F	Number of display line	Character font	Duty	LCD module		
0	0	1	5 x 7	1/8	-		
0	1	1	5 x 10	1/11	-		
1	*	2	5 x 7	1/16	M1641, M1632, L1642, L1652, L1614, L2012		
					L2022, L2014, L2432, L4042, M4024		

Function Set instruction must be executed prior to all other instructions except Busy Flag/Address Read. If another instruction is executed first, no interface data length is effective.

#### 2.5.7 CG RAM Address Set



CG RAM addresses expressed as binary AAAAAA are set to the AC. The data written from or read to the MPU is for the CG RAM. **2.5.8 DD RAM Address Set** 



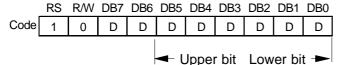
DD RAM address expressed as binary AAAAAA are set to the AC. Then data written from or read to the MPU is for the DD RAM. When N = 0 (one-line display) the addresses are 00H to 4HH. When N=1 (two-line display : M1632, L1642, L1652, L2012, L2022, L2432, L4042), the addresses used for display in line 1 (AAAAAA) are 00H to 27H and those for line 2 (AAAAAA) are 40H to 67H. As for M1641, L1614, L2014 and M4024, see section 2.6 Address Location.

#### 2.5.9 Busy Flag/Address Read



The BF signal is read out, indicating whether the module is working internally because of the previous instruction. When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0. When BF = 0, the next instruction can be accepted, Therefore, make sure that BF = 0 before writing the next instruction. The AC values binary AAAAAA are read out at the same time as the busy flag read. The AC addresses are used for both CG RAM and DD RAM, and the Address Set before the execution of this instruction determines whether the address is for CF RAM or DD RAM.

#### 2.5.10 Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. CG RAM Address Set or DD RAM Address Set before this instruction selects either RAM. After the write operation, the address is incremented or decremented automatically according to Entry Mode Set. Entry Mode Set also determines whether display shifts or not after the write operation.

#### 2.5.11 Data Read from CG RAM or DD RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D	D	D	D	D	D	D	D
				ŀ	Upper bit Lower bit -					

Binary eight-bit data DDDDDDDD is read from CG RAM or from DD RAM. CG RAM Address Set or the DD RAM Address Set before this instruction selects either RAM. CG RAM Address Set or the DD RAM Address Set must be executed immediately before this instruction. If no Address Set instruction is executed before a read instruction, the first read data is invalid. Data is normally read from the second time, if read instructions are executed consecutively. For DD RAM, if Cursor Shift instruction is executed just before reading DD RAM< there is no need to execute an Address set instruction because the Cursor Shift instruction does this.

After a read operation, the address is automatically incremented or decremented by one according to Entry Mode Set, but the display isn't shifted regardless of Entry Mode set.

Note : The AC is automatically incremented or deremented by one according to Entry Mode Set after Data Write to CG RAM or DD RAM instruction is executed. If a read instruction is executed immediately after this instruction, RAM data specified by the AC is not read out. Correct data is read out under the following conditions.

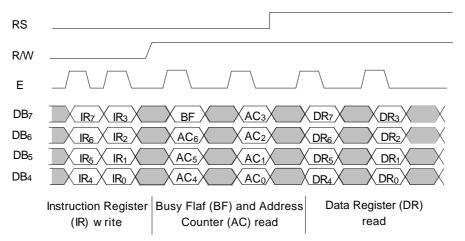
- \* An Address Set instruction is executed immediately before a read instruction
- \* For DD RAM. the Cursor Shift instruction is executed immediately before a read instruction
- \* The second, or later, instruction is executed in consecutive execution of read instructions

## 6. Interfacing to MPU

LCD modules containing controller can interface to both 4-bit and 8-bit MPU

#### 6.1 Interface in 4-bit operation

When interface data is 4 bits long, data is transferred using only four buses; DB4 to DB0. DB0 to DB3 are not used. Data transfer between the controller and the MPU ends when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB4 to DB7 when interface data is 8 bits long) are transferred first, then lower order 4 bits (content of DB0 to DB3 when interface data is 8 bits long) are transferred first, then lower order 4 bits (content of DB0 to DB3 when interface data is 8 bits long) are transferred. Check the busy flag after 4-bit data has been transferred twice. Then the busy flag and address counter data are read out by two transfers.



#### 6.2 Interface in 8-bit operation

When interface data is 8 bits long, data is transferred using the 8 data buses of DBo to DB7.

