Automatic Gain Control (AGC) circuits

Theory and design

by

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Introduction

In the early years of radio circuits, fading (defined as slow variations in the amplitude of the received signals) required continuing adjustments in the receiver's gain in order to maintain a relative constant output signal. Such situation led to the design of circuits, which primary ideal function was to maintain a constant signal level at the output, regardless of the signal's variations at the input of the system. Originally, those circuits were described as automatic volume control circuits, a few years later they were generalized under the name of Automatic Gain Control (AGC) circuits [1,2].

With the huge development of communication systems during the second half of the XX century, the need for selectivity and good control of the output signal's level became a fundamental issue in the design of any communication system. Nowadays, AGC circuits can be found in any device or system where wide amplitude variations in the output signal could lead to a lost of information or to an unacceptable performance of the system.

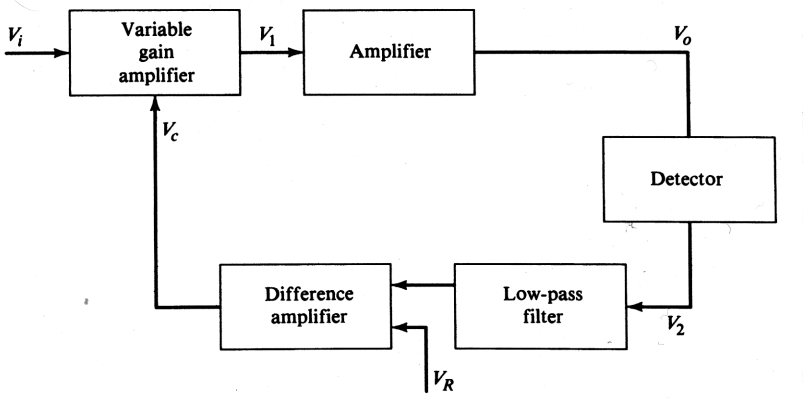
The main objective of this paper is to provide the hypothetical reader with a deep insight of the theory and design of AGC circuits ranging from audio to RF applications. We will begin studying the control theory involved behind the simple and primary idea of an AGC system. After that, with the theory as our guide, we will study and describe the characteristics and performance of the most popular AGC system components. Finally, a few practical AGC circuits will be presented and analyzed. At each section, emphasis will be made on those parts of the circuit that could be potentially implemented in an integrated circuit form.

A list of references will be presented at the end of this paper for the eventual reader who could be interested in learning or reading more about this subject.

Theory of the Automatic Gain Control system [1,2,9]

Many attempts have been made to fully describe an AGC system in terms of control system theory, from pseudo linear approximations to multivariable systems. Each model has its advantages and disadvantages, first order models are easy to analyze and understand but sometimes the final results show a high degree of inaccuracy when they are compared with practical results. On the other hand, non-linear and multivariable systems show a relative high degree of accuracy but the theory and physical implementation of the system can become really tedious.

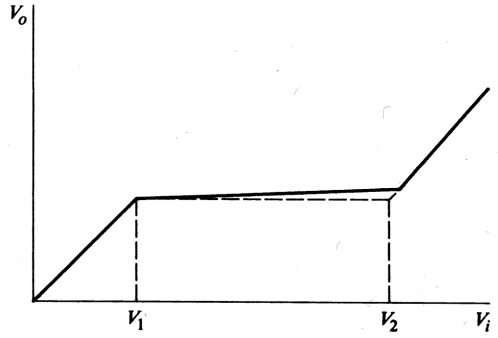
From a practical point of view, the most general description of an AGC system is presented in figure 1. The input signal is amplified by a variable gain amplifier (VGA), whose gain is controlled by an external signal V_C. The output from the VGA can be further amplified by a second stage to generate and adequate level of V_O. Some the output signal's parameters, such as amplitude, carrier frequency, index of modulation or frequency, are sensed by the detector; any undesired component is filtered out and the remaining signal is compared with a reference signal. The result of the comparison is used to generate the control voltage (V_C) and adjust the gain of the VGA.



AGC block diagram [1]
Figure 1

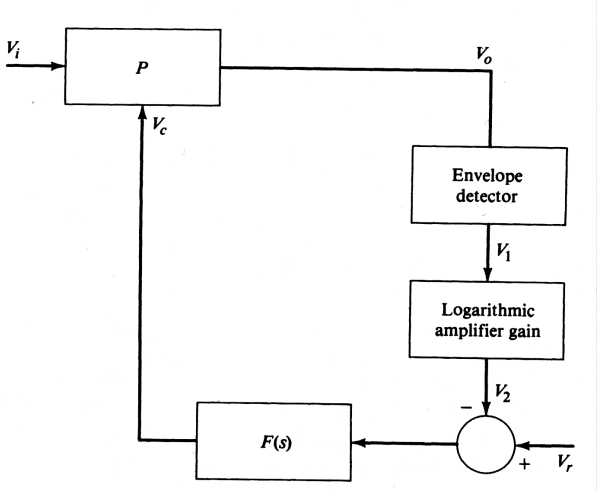
Since an AGC is essentially a negative feedback system, the system can be described in terms of its transfer function. The idealized transfer function for an AGC system is illustrated in figure 2. For low input signals the AGC is disabled and the output is a linear function of the input, when the output reaches a threshold value (V1) the AGC becomes operative and maintains a constant output level until it reaches a second threshold value (V2). At this point, the AGC becomes inoperative again; this is usually done in order to prevent stability problems at high levels of gain.

Many of the parameters of the AGC loop depend on the type of modulation used inside the system. If any kind of amplitude modulation (AM) is present, the AGC should not respond to any change in amplitude modulation or distortion will occur. Thus the bandwidth of the AGC must be limited to a value lower than the lowest modulating frequency. For systems where frequency or pulse modulation is used, the system requirements are not that stringent.



AGC's ideal transfer function [1]
Figure 2

As mentioned before, an AGC system is considered a nonlinear systems and it is very hard to find solutions for the nonlinear equation that arise during the analysis. Nevertheless, there are two models that describe the system's behaviour with a good degree of accuracy and are relatively easy to implement when the small signal transfer equations of the main blocks are known (which is usually the case).



Decibel-based AGC system [1]
Figure 3

Although there is no name for the first model, it could be described as the decibel-based linear model. The block diagram for this model is show in figure 3, in this model the variable gain amplifier (VGA) P has the following transfer function.

$$P = K_1 e^{+aV_C}$$

$$V_O = V_i K_1 e^{+aV_C}$$

Where V_O and V_i are the output and input signal, K_1 is a constant and *a* is a constant factor of the VGA. Following the signal path we find that the logarithmic amplifier gain is:

$$V_2 = \ln V_1 = \ln K_2 V_O$$

Where K_2 represents the gain of the envelope detector. Assuming that the output of the envelop detector is always positive (otherwise the logarithmic function becomes complex which translates in a non working circuit), the output of the logarithmic amplifier is a real number an the control voltage becomes:

$$V_C = F(s)(V_R - V_2) = F(s)(V_R - \ln K_2 V_O)$$

F(s) represents the filter transfer function. Knowing that the VGA shows an exponential transfer function we can apply the logarithm function at both sides of the equation.

$$\ln V_O = aV_C + \ln V_i K_1$$

Thus, the control voltage can be expressed as:

$$aV_C = \ln V_O - \ln V_i K_1$$

Using the expression for V_C that we found before

$$\ln V_O[1 + aF(s)] = \ln V_i + aF(s)V_R + \ln K_1 - aF(s)V_R \ln K_2$$

Since we are only interested in the output-input relationship, let K_1 and K_2 be equal to one. Thus, the above equation becomes:

$$\ln V_O[1 + aF(s)] = \ln V_i + aF(s)V_R$$

If V_O and V_i are expressed in decibels, we can use the following equivalence

$$\ln V_O = 2.3 \log V_O$$

Then,

$$\ln V_O = \frac{2.3}{20} V_{OdB} = 0.115\, V_{OdB} \text{ dB}$$

Finally, the equation that relates input and output (both in dB) can be rewritten as

$$V_{OdB} = \frac{V_{idB}}{1 + aF(s)} + \frac{8.7aF(s)V_R}{1 + aF(s)}$$

This type of AGC system shows a linear relationship as long as input and output quantities are expressed in decibels. From the last expression it is easy to see that the behaviour of the system is determined by the *a* factor of the VGA and the filter F(s). F(s) is usually a low pass filter, since the bandwidth of the loop must be limited to avoid stability problems and to ensure that the AGC does not respond to any amplitude modulation that could be present in the input signal.

An important parameter in any control system is the steady-state error that is defined as[5]:

$$e_{ss} = \lim_{t\to\infty} e(t) = \lim_{s\to 0} sE(s)$$

where E(s) is the error signal in the feedback path. Applying the definition given above to the AGC system we find that the position error constant is given by:

$$e_{ss} = \frac{1}{1 + aF(0)}$$

where F(0) is the DC gain of the F(s) block and a is the constant factor of the exponential law Variable Gain Amplifier (VGA). Thus, in order to maintain the steady state error as small as possible the DC gain of the F(s) block (usually a low pass filter) must be as large as possible.

The simplest F(s) block that can be used in the system is a first order low pass filter whose transfer function is defined as follows:

$$F(s) = \frac{K}{\frac{s}{B} + 1}$$

where K is the DC gain of the filter and B is the bandwidth. Using this expression in the equation of the steady state error we find that:

$$e_{ss} = \frac{1}{1 + aK}$$

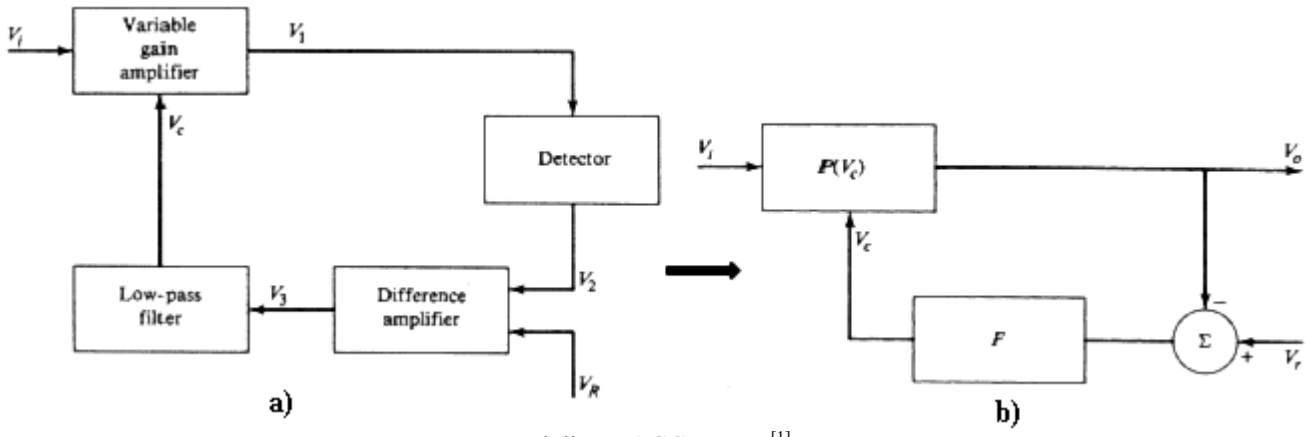
And the total DC output of the AGC system is given by:

$$V_{ODC} = \frac{V_{IDC}}{1 + aK} + \frac{8.7aKV_R}{1 + aK}$$

It can be seen that if the gain loop K is much greater than 1, the output is almost equal to $8.7V_R$ and the steady state change in the input is greatly reduced. AGC systems that include a reference voltage inside the control loop are referred as delayed AGC.

The second model of an AGC system does not contain a logarithmic amplifier within the loop but still contains a exponential type VGA. Despite the fact that the system's complexity increases, it is still possible to find small signal models for small changes from a particular operating point [1].

The block diagram shown in figure 4a can represent such system. It is important to notice that the VGA and the detector are the only nonlinear parts of the system. Assuming unity gain for the detector and the difference amplifier, the system can be reduced to the block diagram shown in figure 4b.



Pseudolinear AGC system [1]
Figure 4

Here, Vo and Vi are input and output signal respectively, F is the combined transfer function of the filter and difference amplifier. The output voltage Vo equal PVi, where P represents the gain of the VGA and it is a function of the control voltage Vc. Following the signal path, we can see that the control voltage is given by:

$$V_C = (V_r - V_O)F$$

Since we are interested in the change in the output voltage due to a change in the input voltage we can take the derivative of Vo with respect to Vi, therefore:

$$\frac{dV_O}{dV_i} = \frac{d}{dV_i}(PV_i) = P + V_i \frac{dP}{dV_i}$$

The last derivative on the right side of the equation can be further developed applying the chain rule and using the equation for the control voltage, thus:

$$\frac{dP}{dV_i} = \frac{dP}{dV_C}\frac{dV_C}{dV_i} = \frac{dP}{dV_C}\frac{dV_C}{dV_O}\frac{dV_O}{dV_i} = \frac{dP}{dV_C}(-F)\frac{dV_O}{dV_i}$$

Therefore, the expression for $\frac{dVo}{dVi}$ an be rewritten as:

$$\frac{dV_O}{dV_i}\left(1 + FV_i\frac{dP}{dV_C}\right) = P$$

Alternatively

$$\frac{dV_O / V_O}{dV_i / V_i} = \left(1 + FV_i\frac{dP}{dV_C}\right)^{-1}$$

It is clear that the loop gain is a function of the input signal, which translates into a relative degree of non-linearity and complicates the analysis of the transient response of the system, since the pole location is also dependant on the input signal. Nevertheless, it is possible to numerically evaluate the characteristic parameters of the loop if the $P(V_C)$ function is know and a set of initial conditions is taken as an starting point.

All the AGC systems considered here provide a continuous sampling of the output signal and a continuous adjustment of the VGA. There are a few applications where the output signal is sampled at specific intervals of time and gain is adjusted only at those intervals. Those systems are known as pulse-type AGC systems and its analysis is usually performed using sampled data techniques.

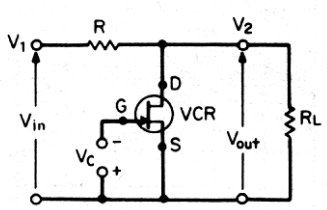
Components of an AGC system

There are many component and circuit configurations that can be used as a variable gain amplifier (VGA), which is the main component of an AGC system. The main factors that must be taken in consideration while selecting a suitable circuit are: frequency response, available control voltage, desired control range of the VGA, and settling time and finally, system configuration.

The following circuits can be used form the low to the radio frequency range assuming that they are implemented using the proper technology and considering important practical issues such as bypassing, ground planes, impedance matching, parasitics, and component selection.

a) Low frequency circuits

For low frequency circuits the most common configuration consists of an operational amplifier and a voltage controlled attenuator. The basic voltage controlled attenuator consists of a fixed resistor connected in series with a field effect transistor (usually a JFET) working in the triode region. Such configuration is shown in figure 5.



Basic voltage controlled attenuator [3]
Figure 5

It can be shown that the output voltage is given by:

$$V_{out} = V_{in} \frac{R_L (1 + g_{ds} R_L)^{-1}}{R + R_L (1 + g_{ds} R_L)^{-1}}$$

As V_{gs} approaches $V_{gs(off)}$, g_{ds} approaches to zero an there is no attenuation of the input signal. If the value of R_L is much higher that $r_{ds(on)}$ and R the above equation simplifies to:

$$V_{out} = V_{in} \frac{1}{1 + R g_{ds}}$$

The output transconductance is given by:

$$g_{ds} = g_{dso} \frac{V_{GS(OFF)} - V_{GS}}{V_{GS(OFF)}}$$

Where:

$$g_{dso} = \frac{2 I_{DSS}}{|V_{GS(OFF)}|}$$

Combining both equations:

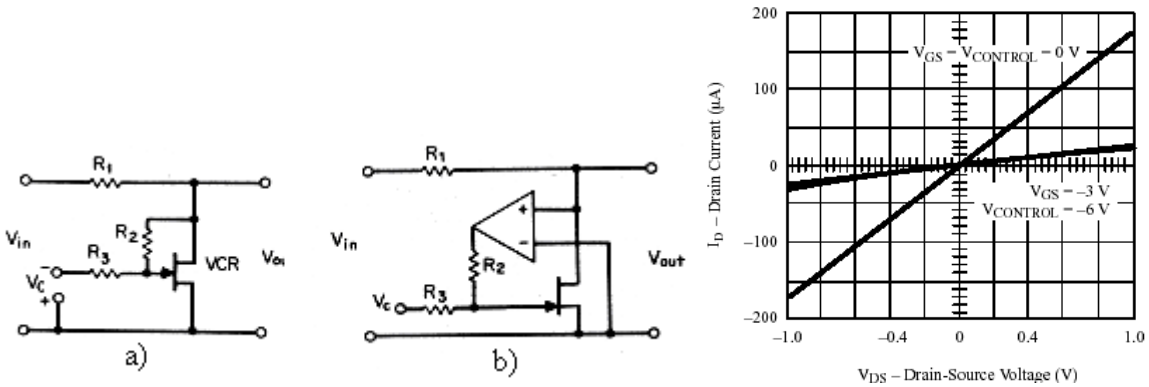
$$V_{out} = \frac{V_{in}}{1 + Rg_{dso}\left[\left(V_{GS(OFF)} - V_{GS}\right)/V_{GS(OFF)}\right]}$$

The above circuit has two serious drawbacks, high harmonic distortion and limited signal handling capability. Both problems can be solved by feeding back one half of drain- source voltage to the gate, such modification simplifies the output transconductance equation to:

$$g_{ds} = g_{dso}\left(1 - \frac{V_C}{2V_{GS(OFF)}}\right)$$

which is a linear function of Vc.

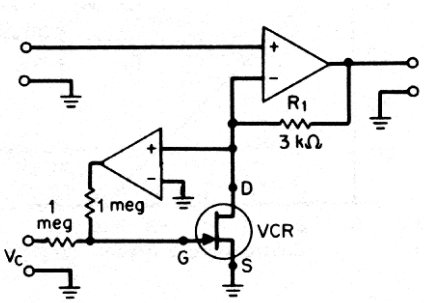
To avoid loading the output the value of the feedback resistors must be higher than R1, and if isolation from the control voltage to the output is desired a follower must be connecter between the feedback network and the output.



a)Voltage controller attenuator with feedback b)With feedback and isolation[3]
c)Linearization due to feedback network
Figure 6

The following circuits illustrate the use of a voltage-controlled attenuator inside the feedback loop of an operational amplifier. For the first circuit (Figure 7), the overall gain of the stage is given by:

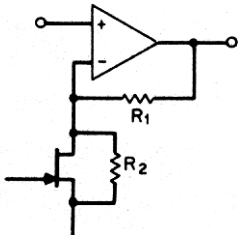
$$A = 1 + R_1\, g_{dso}\left(1 - \frac{V_C}{2V_{GS(OFF)}}\right)$$



Variable gain operational amplifier [3]
Figure 7

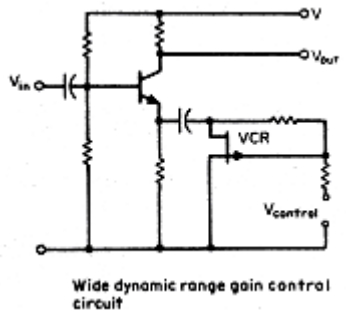
If a minimum gain greater than 1 is required (Figure 8), a second resistor can be place in parallel with the JFET. This arrangement introduces an extra factor of R_2/R_1 in the above equation, thus:

$$A = 1 + \frac{R_2}{R_1} + R_1\, g_{dso}\left(1 - \frac{V_C}{2V_{GS(OFF)}}\right)$$



Variable gain operational amplifier with $A_{min} > 1$ [3]
Figure 8

Finally, in order to block any DC component that could be present in the input signal and keep the FET working in deep triode region, a capacitor must be placed in series with the FET attenuator. The value of the capacitor will depend on the required cut off frequency and the equivalent impedance seen from the connection point. See figure 9.



Voltage controller attenuator [3]
with DC blocking capacitor
Figure 9

When using FET as a component of a voltage attenuators it is important to keep in mind the following issues:

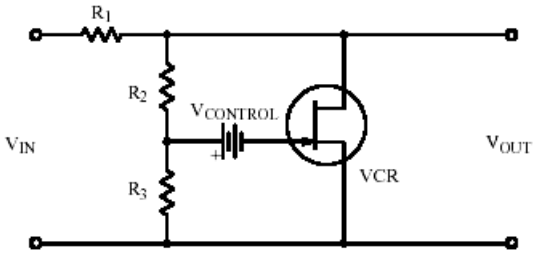
a) The FET in triode region behaves as a resistor only for small voltage values of V_{DS}.

b) The output transconductance (g_{ds}) is approximately a linear function of V_{GS}.

c) The linearity of g_{ds} decreases as V_{GS} approaches $V_{GS(OFF)}$.

d) Feeding back one half of V_{DS} to the gate of the FET improves linearity and dynamic range.

Finally, if a differential control voltage is available the FET attenuator can be implemented as follows.



FET attenuator with differential Vc [3]
Figure 10

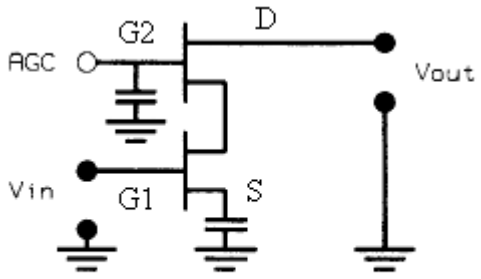
The control voltage of this circuit only needs to be one half of that of the conventional attenuator to achieve the same value of $g_{ds,}$ but the improvement in linearity an dynamic range are preserved.

b) High frequency circuits

Most of the above circuits can be used of to a few hundreds of megahertz, depending on the component selection, grounding, bypassing, impedance matching and physical layout of the circuit.

Nowadays, with the high performance requirements of modern systems and devices it is advisable to study the most common techniques that are typically implemented in integrated circuit (IC) form.

The first device that can be found in integrated and discrete form is the Dual Gate MOSFET or DG-MOSFET. This device can be modeled as two MOSFET in cascode configuration with the input signal applied to the first gate (G1), and a second control signal applied to the second gate (G2). This second signal controls the gain of the overall stage and it is usually referred as the AGC signal.

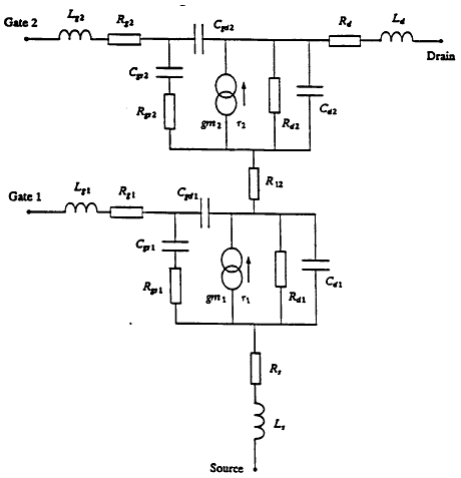


A.) Conventional dual gate configuration.

Figure 11[6,7]

The useful frequency range and electrical characteristics of the DGMOSFET is highly dependant on the technology used during the fabrication of the device. Until now the best devices have been fabricated using HEMT (High Electron Mobility Transistor) technology for gigahertz range and conventional MOS technology for lower frequency applications.

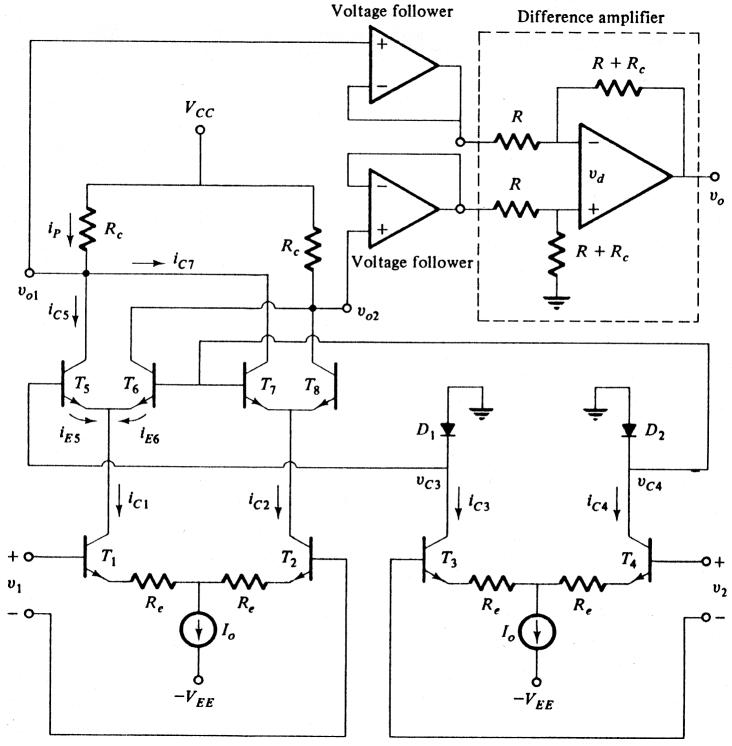
Although DGMOSFET shows good high frequency performance, it is not widely used due to the lack of accurate models and a poor understanding of its characteristics. Nevertheless, a large amount of research has been already done and now it is possible to find some SPICE models for commercial devices (Siliconix and Philips) moreover, an experimental model for gigahertz applications was developed and optimized by C. Licqurish, M. J. Howes and C. M. Snowden at the University of Leeds using S parameters[7].



DGMOSFET equivalent model[7]
Figure 12

The second topology that is commonly found in high frequency circuit is the Gilbert cell or analog multiplier [8,9,4]. Although it was primarily designed to be used as a mixer, it has been included as a fundamental part of variable gain amplifiers such as the CLCXXX series of National Semiconductor [11].

A complete diagram of a four quadrant multiplier circuit is shown in figure 13. The collector



Four quadrant analog multiplier[9]
Figure 13

currents of T1 and T4 can be shown to be:

$$i_{C1} = \frac{I_O}{2} + \frac{v_1}{2(R_e + h_{ib})} \qquad i_{C2} = \frac{I_O}{2} - \frac{v_1}{2(R_e + h_{ib})}$$

$$i_{C1} = \frac{I_O}{2} - \frac{v_2}{2(R_e + h_{ib})} \qquad i_{C1} = \frac{I_O}{2} + \frac{v_2}{2(R_e + h_{ib})}$$

Also, applying KCL

$$i_{C1} = i_{E5} + i_{E6}$$
$$i_{C2} = i_{E7} + i_{E8}$$

Using the exponential relationship for the emitter current of T5 and T6 and dividing

$$\frac{i_{E5}}{i_{E6}} = e^{\frac{(V_{BE5} - V_{BE6})}{V_T}}$$

Combining the last two equations:

$$i_{E5} = \frac{i_{C1}}{1 + e^{-\frac{(V_{BE5} - V_{BE6})}{V_T}}}$$

Applying KVL at the collector loop of T3 and T4

$$V_{BE5} - V_{BE6} = V_{C3} - V_{C4}$$

Thus, i_{E5} can be rewritten as:

$$i_{E5} = \frac{i_{C1}}{1 + e^{-\frac{(V_{C3} - V_{C4})}{V_T}}}$$

Similarly for i_{E7}

$$i_{E7} = \frac{i_{C1}}{1 + e^{-\frac{(V_{C4} - V_{C3})}{V_T}}}$$

The current i_P is the sum of i_{C5} and i_{C7}, that can be assume to be equal to the sum of i_{E5} and i_{E7}. Thus

$$i_P = \frac{i_{C1} + i_{C2} e^{-\frac{V_{C3} - V_{C4}}{V_T}}}{1 + e^{-\frac{V_{C3} - V_{C4}}{V_T}}}$$

The currents i_{C3} and i_{C4} generate a voltage across D1 and D2. which are equal to the collector voltage of T3 and T4 and obey the exponential law:

$$i_{C3} = I_S e^{-\frac{v_{C3}}{V_T}} \quad i_{C3} = I_S e^{-\frac{v_{C4}}{V_T}}$$

Dividing:

$$\frac{i_{C3}}{i_{C4}} = e^{-\frac{V_{C3}-V_{C4}}{V_T}}$$

Using the above expression in the equation for I_P

$$i_P = \frac{i_{C1}i_{C4} + i_{C2}i_{C3}}{i_{C4} + i_{C3}}$$

Finally, writing the last equation in terms of v_1, v_2 and I_O

$$i_P = \frac{I_O^2/2 + v_1 v_2/[2(R_e + h_{ib})^2]}{I_O}$$

Then v_{O1} and v_{O2} are given by:

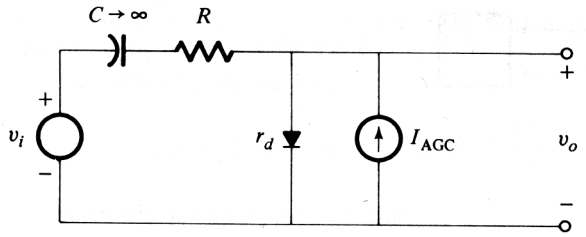
$$v_{O1} = V_{CC} - \frac{I_O R_C}{2} - \frac{R_C}{2I_O(R_e + h_{ib})^2} v_1 v_2$$

$$v_{O2} = V_{CC} - \frac{I_O R_C}{2} + \frac{R_C}{2I_O(R_e + h_{ib})^2} v_1 v_2$$

Thus, the output of the differential amplifier is given by:

$$v_o = \frac{R_C}{I_O(R_e + h_{ib})} v_1 v_2$$

It is clear that one of the inputs can be use as the AGC voltage while the main signal is injected on the other input. Modern IC multiplier can exhibit a wide bandwidth and a high degree of accuracy, nevertheless, for non-critical applications it is possible to achieve accuracies of 1% using discrete components. An excellent Gilbert cell in integrated circuit form with a bandwidth product of 10 GHz is available from Intersil Corporation, part number HFA3101[10].



Basic diode attenuator[9]
Figure 14

Finally, the equivalent of the JFET attenuator at high frequencies is usually implemented with a diode whose bias point is varied according to a control voltage V_c or a control current I_c. Figure 14 describes this technique, the circuit operates as follows: the current I_{AGC} can not flow into the resistor due to the DC blocking capacitor C but it can flow into the diode, biasing it into the forward region. Assuming that the amplitude of v_i is small such that the diode is kept forward biased. The small signal diode resistance r_d and R form a voltage divider, thus the output voltage is given by:

$$v_O = \frac{r_d}{r_d + R} v_{in}$$

The small signal resistance of a PN junction diode is approximately given by:

$$r_d \approx \frac{V_T}{I_{AGC}}$$

If we substitute this expression into the voltage divider equation and assumed that the value of R is much higher than r_d, the following expression is found:

$$v_O \approx \frac{V_T}{R I_{AGC}} v_{in}$$

If the bias current I_{AGC} is proportional to the envelope value of v_{in}, $I_{AGC}=KV_{env}(t)$, then the output voltage v_o can become constant despite of the variations in v_{in}.

For radio frequency application general purpose diodes are not useful and they are replaced by PIN diodes. A PIN diode is a silicon semiconductor consisting of a layer of intrinsic material contained between two layers of highly doped p and n type silicon. When the diode is forward biased, a finite amount of charge is injected into the intrinsic layer. This finite amount of charge, consisting of electron and holes, has a finite lifetime (τ) before recombination occurs. The density of charge within the intrinsic layer determines the conductance of the diode, whereas the lifetime determines the low frequency limit of the device for useful applications [12.13].

PIN diodes behave as a normal diode for low frequency values, but if the frequency is increased well above certain level, determined by $f_C = 1/2\pi\tau$, the diode becomes a pure linear resistor whose value can be controlled by a DC o low frequency signal. For frequencies at least ten times f_c the intrinsic resistance of the diode can be modelled by the following equation[12,13].

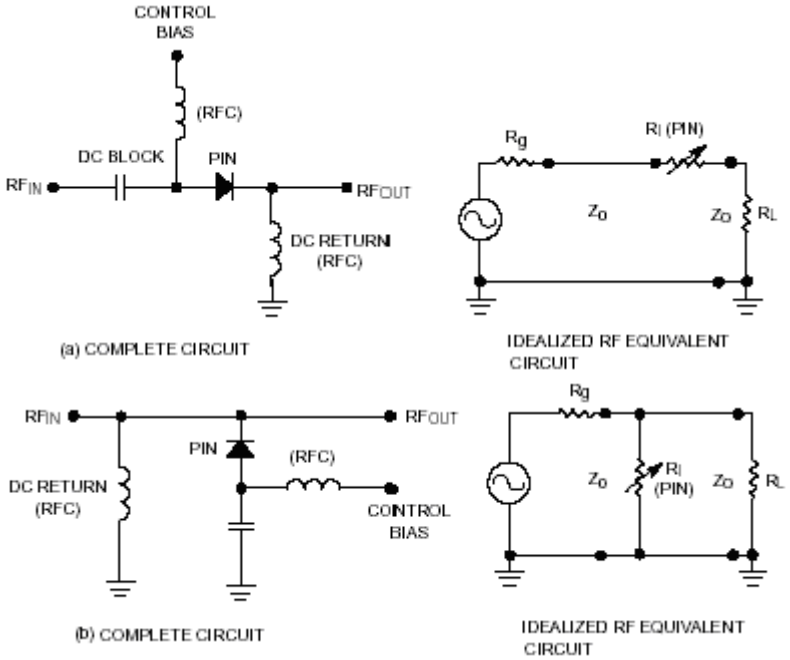
$$R_I = \frac{K}{I_{DC}^X}$$

Where K and x are constants that depend strongly on the fabrication process and are often calculated empirically.

This interesting property of the PIN diode allows the design of switches, attenuators, modulators and detectors. Figure 15 shows the two basic configurations for RF attenuators using PIN diodes. The attenuation for each configuration assuming, that the diode us purely resistive is given by [12,13]:

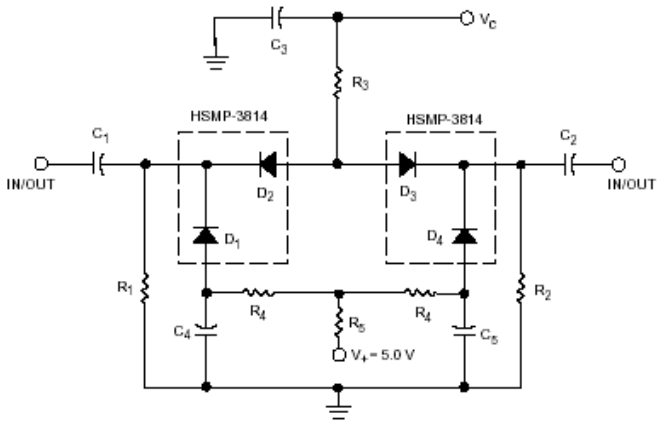
$$\alpha_{(series)} = 20 \log\left(1 + \frac{R_I}{2Z_o}\right)$$

$$\alpha_{(shunt)} = 20 \log\left(1 + \frac{Z_o}{2R_I}\right)$$



PIN diode attenuator a) Series b) Parallel
Figure 15[12,13]

A practical PIN attenuator developed by Agilent Technologies is show in figure 16. It shows a good performance from 300KHz to 3GHz[12,13,6].



Practical PIN diode attenuator [12.13,6]
Figure 16

R1 and R2 provide the DC return path, while R4 and R3 provide the appropriate impedance matching for the PIN diodes.

The last component of an AGC system is the logarithmic amplifier, though it is only included in high performance AGC system it is important to study its basic characteristics and configurations.

As pointed before, an ideal diode shows the following transfer equation:

$$I_D = I_S(e^{\frac{V_D}{nV_T}} - 1)$$

where:

I_S= reverse saturation current

n= constant between 1 and 2 for silicon diodes

$V_T = \frac{kT}{q}$ =thermal voltage.

k= Boltzman constant

restricting the operation voltage in such way that the exponential term is greater than 1 and n≈1, the equation can be approximated as:

$$I_D \approx I_S e^{\frac{V_D}{V_T}}$$

If the diode is part of the feedback loop of an operational amplifier just as shown in figure 17, then, the current I_D can be written as:

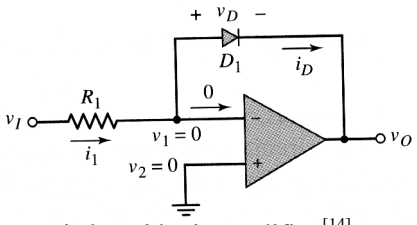
$$i_D = \frac{V_{in}}{R}$$

Thus,

$$i_D = \frac{V_{in}}{R} = I_S e^{\frac{V_O}{V_T}}$$

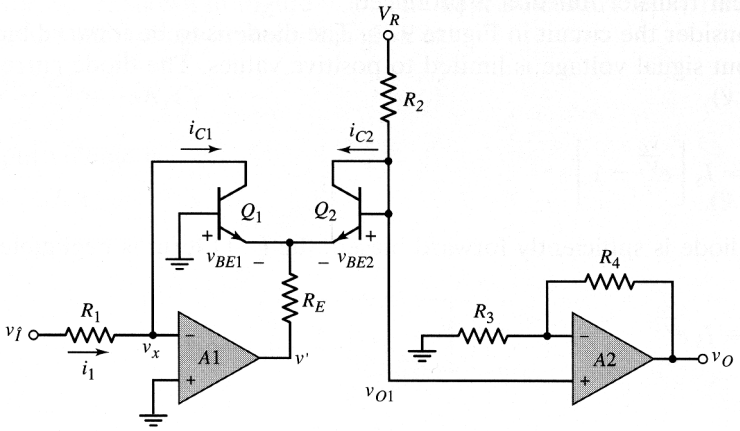
Taking the natural logarithm on both sides and solving for V_O

$$V_O = -V_T \ln\left(\frac{V_{in}}{I_S R}\right)$$



Basic logarithmic amplifier [14]
Figure 17

This equation shows that the output voltage is proportional to the logarithm of the input voltage. The main drawback of this circuit is the high temperature dependence it shows due to the inclusion of I_S in the transfer function. Is can be cancelled by placing a matched diode (or diode connected transistor) as shown in figure 18.



Logarithmic amplifier with I_S cancellation [14]
Figure 18

Assuming that both transistors are matched and operating in active region, which constrains V_{in} to be a positive value, the analysis of the circuit proceeds as follows.

From the exponential relationship of a bipolar transistor $I_C = I_S e^{\frac{V_{BE}}{V_T}}$ and applying KVL around the base-emitter junctions of Q1 and Q2, we obtain the following:

$$v_{O1} = v_{BE1} - v_{BE2}$$

and

$$v_{O1} = V_T[(\ln i_{C2} - \ln I_S) - (\ln i_{C1} - \ln I_S)] = -V_T \ln\left(\frac{i_{C1}}{i_{C2}}\right)$$

The collector current of Q1 is given by

$$I_{C1} = \frac{V_{in}}{R_1}$$

Ignoring the base current of Q2 and assuming that $V_R >> v_{BE2}-v_{BE1}$, the collector current i_2 is approximately given by:

$$I_{C2} \approx \frac{V_R}{R_2}$$

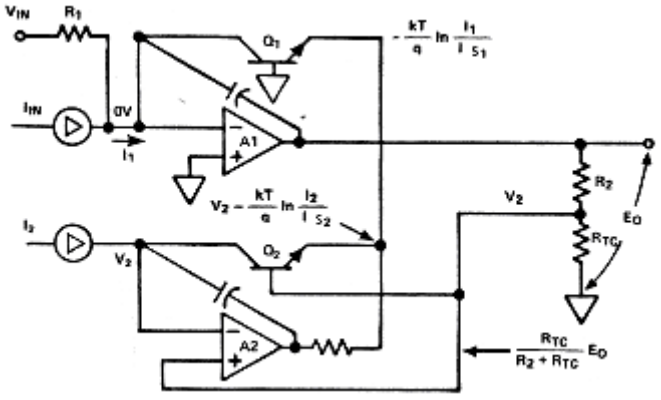
Then v_{O1} can be expressed as:

$$v_{O1} = -V_T \ln\left(\frac{v_{in}}{R_1}\frac{R_2}{V_R}\right)$$

Finally v_O is simply v_{O1} multiplied by the gain of the second amplifier

$$v_O = -V_T\left(1+\frac{R_4}{R_3}\right)\ln\left(\frac{v_{in}}{R_1}\frac{R_2}{V_R}\right)$$

This expression does not include I_S, thus it shows lower temperature dependence than the basic circuit. The final step is to minimize the effect of the thermal voltage in the transfer equation of the log amplifier.



Temperature compensated log amplifier [4]
Figure 19

The circuit in figure 19 show a temperature compensated log amplifier. The analysis of the circuit proceeds as follows, I_1 is the input current and I_2 is either a second input or a reference current. The emitter base voltage of Q1 is:

$$v_{BE1} = -V_T \ln\left(\frac{I_1}{I_{S1}}\right)$$

Similarly, the base emitter voltage of Q2 (ignoring the base current) is:

$$v_{BE2} = -V_T \ln\left(\frac{I_2}{I_{S2}}\right)$$

Since both emitters are at the same voltage, we can write:

$$V_2 - V_T \ln\left(\frac{I_2}{I_{S2}}\right) = -V_T \ln\left(\frac{I_1}{I_{S1}}\right)$$

The output voltage and V_2 are linked through the voltage divider form by R_2 an R_{TC}, then:

$$E_0 = \left(1 + \frac{R_2}{R_{TC}}\right) V_2 = -\left(1 + \frac{R_2}{R_{TC}}\right) V_T \ln\left(\frac{I_1}{I_2}\right)$$

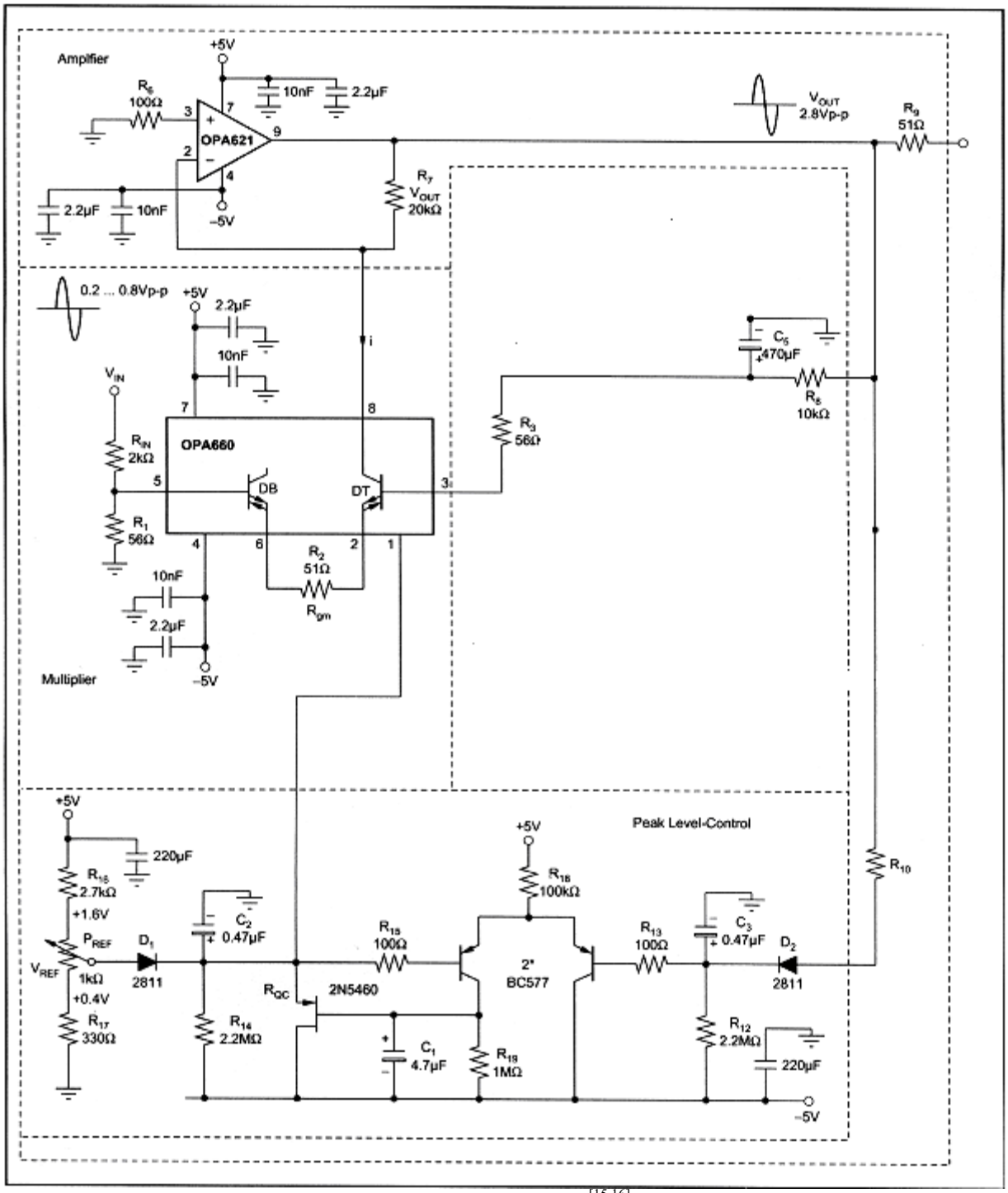
The temperature variations due to V_T can be cancelled if the temperature coefficient of the voltage divider is the complement of that of V_T (approximately 0.085 mV/°C).

Complete AGC system

Finally, a practical AGC system is shown in figure 20. This circuit is included in the demo board of the OPA660 [15,16] of Burr Brown (now part of Texas Instruments). The OPA660 is a high

bandwidth, high slew rate Operational Transconductance Amplifier whose transconductance can be varied by means of a resistor connected to pin 1.

In this circuit, the input signal is attenuated by the resistive divider at the input of the OPA660 and converted into a current I_{OUT}. The output current is converted back into a voltage by the second amplifier OPA621. The peak value of the output voltage is checked against the reference voltage V_{REF} by the discrete differential amplifier. The error voltage is multiplied by the gain of the discrete differential amplifier, applied to the gate of the JFET 2N5460 and filtered by the RC network (R_{19} and C_1). The output transconductance of the JFET adjusts the quiescent current at pin 1, thus, changing the transconductance of the OPA660 and modifying the total gain of the circuit. The process continues until the system reaches the steady state.



Complete AGC system [15,16]
Figure 20

Conclusions:

AGC systems are part of any wireless communication system where a constant output signal is desired. The complexity of the AGC system is determined by the requirements of the communication system, therefore the analysis, design and implementation can become quite difficult. Nonetheless, the two basic models showed in this work provide enough tools to calculate and characterize the basic parameters of the system and translate them into working circuits. The inclusion of some additional circuits, such as a logarithmic amplifier, provides a way of linearizing the system.

At low and medium frequencies, FET's working in the linear region combined with a resistive feedback network provide the best method for implementing a variable gain amplifier, while keeping distortion at a minimum and providing a wide dynamic range. At higher frequencies IC-MOSFET, DGMOSFET, Gilbert cells, OTA and PIN diodes provide a better performance and the advantage that they can be implemented in integrated circuit technology.

For both cases a careful selection of components, bypassing, printed circuit layout, impedance matching, temperature effects and IC layout can play a very critical role in the performance of the circuit.

AGC systems and circuits will continue to evolve as long as wireless technology becomes faster, smaller and more complex. New devices, circuits and techniques must be studied, developed and implemented.

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