Almost all low-power RF transmitter ICs have an on-chip power amplifier stage where the output pin is either an open collector or open drain. The RF power amplifier stage of all Melexis transmitters is setup with a bipolar transistor that provides an open collector. The collector output must be supplied with a DC voltage to bias the transistor stage. This is usually done through an inductor. The inductor can be either tuned to the operating frequency by means of a parallel capacitor, or the inductor is set to a large value that doesn't affect the output impedance - known as an RF choke -.

RF designers used to work with S-parameters, that sometimes have a problem with this approach of undefined output impedances. In some cases, where they are provided, the S-parameters are not the ones of the output device but the complex conjugate values the device should see to deliver maximum output power. The S-parameters of the device itself are not very useful because the output stage equivalent circuit is essentially a large resistance in parallel with a small capacitance and little parasitic inductance of the pins. Let's assume a capacitance of about 2.5pF and a resistance of 10kΩ. Trying to match this impedance to the load - which is usually at 50 to 400Ω - would give very little output because the device would be saturated.

A more useful approach to design the output matching network is to consider the output capacitance, the supply voltage, the saturation voltage of the output stage and the required power output. To avoid saturation of the output stage (which would increase the level of the harmonics), the saturation voltage of the Melexis TH720xx transmitters can be assumed to be 1.2V. While for the TH7122x transceivers a saturation voltage of 0.7V is applicable. The saturation voltage is fairly independent of the supply voltage.

The peak output voltage swing is limited by the supply voltage V_{cc} minus the saturation voltage V_{sat}. It can be 1.8V for the transmitters and 2.3V for the transceivers, if they run from a 3V supply.

The optimum load resistance can be calculated as:

$$R_L = \frac{(Vcc - Vsat)^2}{2 \times Po}$$

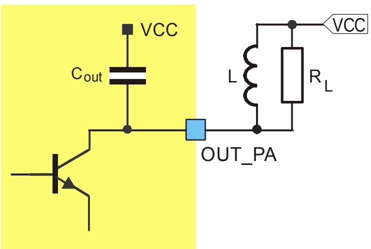
***Example**: If we assume a required RF power of P_O = 6.3mW (or 8dBm), taken from a TH720xx transmitter at 3V supply and with V_{sat} = 1.2V, then the optimum load resistance would be R_L = 256Ω. A slightly smaller load resistance might be chosen to ensure the output stage does not saturate at supply voltage drops.*

The output capacitance C_{out} of the transistor is typically at 2 - 3pF. It can be considered in two ways:

1. For simple resonant frequency tuning together with the inductor and an external tank capacitor (in this case the inductor could be formed by a loop antenna for example).
2. To be included as a capacitor of the output matching network.

It is usually required to adjust the matching network for best results and to compensate for board layout parasitics.

Power amplifier output stage



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