Transistor Amplifiers

Purpose

The aim of this experiment is to develop a bipolar transistor amplifier with a voltage gain of minus 25. The amplifier must accept input signals from a source impedance of 1 k and provide an undistorted output amplitude of 5 V when driving a 560 load. The bandwidth should extend from below 100 Hz to above 1 MHz.

Introduction

An electrical signal can be amplified by using a device which allows a small current or voltage to control the flow of a much larger current from a dc power source. Transistors are the basic device providing control of this kind. There are two general types of transistors, bipolar and field-effect. Very roughly, the difference between these two types is that for bipolar devices an input current controls the large current flow through the device, while for field-effect transistors an input voltage provides the control. In this experiment we will build a two-stage amplifier using two bipolar transistors.

In most practical applications it is better to use an op-amp as a source of gain rather than to build an amplifier from discrete transistors. A good understanding of transistor fundamentals is nevertheless essential. Because op-amps are built from transistors, a detailed understanding of op-amp behavior, particularly input and output characteristics, must be based on an understanding of transistors. We will learn in Experiments #9 and #10 about logic devices, which are the basic elements of computers and other digital devices. These integrated circuits are also made from transistors, and so the behavior of logic devices depends upon the behavior of transistors. In addition to the importance of transistors as components of op-amps, logic circuits, and an enormous variety of other integrated circuits, single transistors are still important in many applications. For experiments they are especially useful as interface devices between integrated circuits and sensors, indicators, and other devices used to communicate with the outside world.

The three terminals of a bipolar transistor are called the emitter, base, and collector (Figure 7.1). A small current into the base controls a large current flow from the collector to the emitter. The current at the base is typically one hundredth of the collector-emitter current. Moreover, the large current flow is almost independent of the voltage across the transistor from collector to emitter. This makes it possible to obtain a large amplification of voltage by taking the output voltage from a resistor in series with the collector. We will begin by constructing a common emitter amplifier, which operates on this principle.

A major fault of a single-stage common emitter amplifier is its high output impedance. This can be cured by adding an <u>emitter follower</u> as a second stage. In this circuit the control signal is again applied at the base, but the output is taken from the emitter. The emitter voltage precisely follows the base voltage but more current is available from the emitter. The common emitter stage and the emitter follower stage are by far the most common transistor circuit configurations.
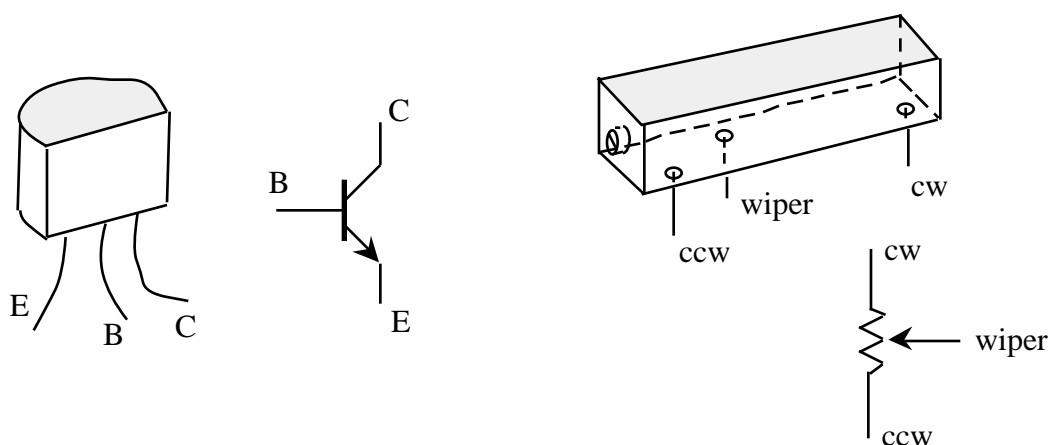

Figure 7.1   Pin-out of 2N3904 and 1 k trimpot

Readings

D&H Chapter 8.1 through 8.6 on bipolar transistors.

Horowitz and Hill, Chapter 2 also may be helpful, especially 2.01–2.03, 2.05, the first page of 2.06, 2.07, 2.09–2.12, and the part of 2.13 on page 84 and 85. Table 2.1 and Figure 2.78 give summaries of the specifications of some real devices.

Theory

CURRENT AMPLIFIER MODEL OF BIPOLAR TRANSISTOR

From the simplest point of view a bipolar transistor is a current amplifier. The current flowing from collector to emitter is equal to the base current multiplied by a factor. An NPN transistor operates with the collector voltage at least a few tenths of a volt above the emitter voltage, and with a current flowing *into* the base. The base-emitter junction then acts like a forward-biased diode with an 0.6 V drop: $V_B \approx V_E + 0.6V$. Under these conditions, the collector current is proportional to the base current: $I_C = h_{FE} I_B$. The constant of proportionality is called h_{FE} because it is one of the "h-parameters," a set of numbers that give a complete description of the small-signal properties of a transistor (see Bugg Section 17.4). It is important to keep in mind that h_{FE} is not really a constant. It depends on collector current (see H&H Fig. 2.78), and it varies by 50% or more from device to

device. If you want to know the emitter current rather than the collector current you can find it by current conservation: $I_E = I_B + I_C = (1/h_{FE} + 1) I_C$. The difference between I_C and I_E is almost never important since h_{FE} is normally in the range $100 - 1000$. Another way to say this is that the base current is very small compared to the collector and emitter currents.
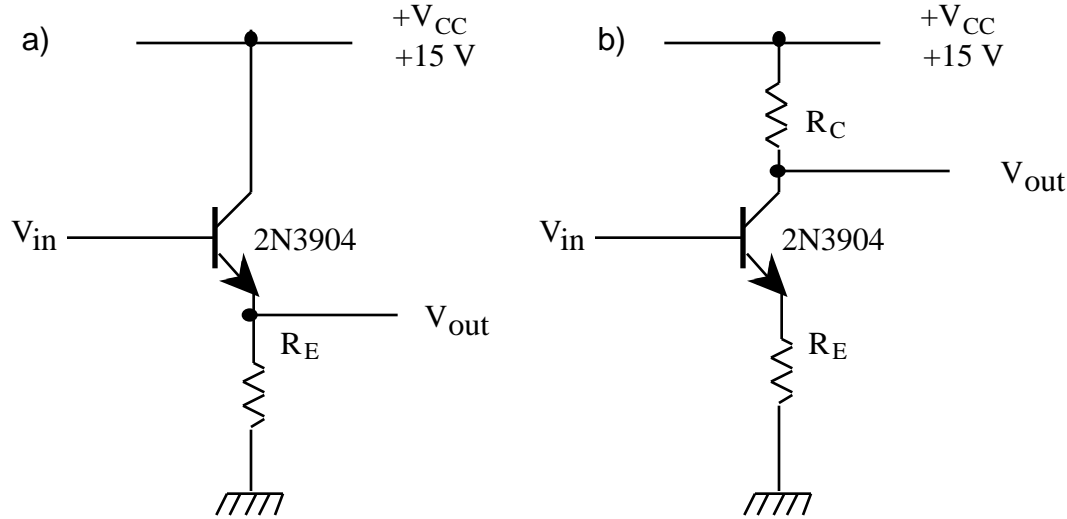

Figure 7.2   a)   Emitter follower stage   b) Common Emitter Stage

Figure 7.2 shows the two main transistor-based circuits we will consider. In the emitter-follower stage the output (emitter) voltage is simply related to the input (base) voltage by a diode drop of about .6 eV. An ac signal of 1 volt amplitude on the input will therefore give an AC signal of 1 volt on the output, i.e. the output just "follows" the input. As we will see later, the advantage of this circuit is as a buffer due to a relatively high input and low output impedance.

In the common emitter stage of figure 7.2b, a 1 volt ac signal at the input will again cause a 1 volt ac signal at the emitter. This will cause an ac current of $1\text{volt}/R_E$ from the emitter to ground, and hence also through R_c. V_{out} is therefore $15 - R_c(1\text{volt}/R_E)$ and we see that there is an ac voltage gain of $-R_c/R_E$.

Although we are only looking to amplify the AC signal, it is nonetheless very important to set up proper dc bias conditions or quiescent points. The first step is to fix the dc voltage of the base with a voltage divider (R_1 and R_2 in Figure 7.3). The emitter voltage will then be 0.6 V less than the base voltage. With the emitter voltage known, the current flowing from the emitter is determined by the emitter resistor: $I_E = V_E/R_E$. For an emitter follower, the collector is usually tied to the positive supply voltage V_{CC}. The only difference between biasing the emitter follower and biasing the common emitter circuit is that the common emitter circuit always has a collector resistor. The collector resistor does not change the base or emitter voltage, but the drop across the collector resistor does determine the collector voltage: $V_C = V_{CC} - I_C R_C$.
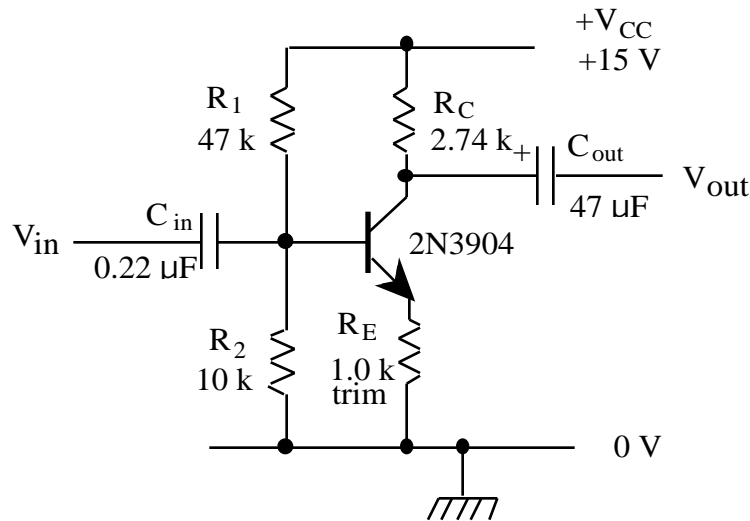
Figure 7.3   Biased Common Emitter Amplifier

There are three subtleties to keep in mind when biasing common-emitter or emitter-follower circuits. First of all, the base bias voltage must be fixed by a low enough impedance so that changes in the base current do not alter the base voltage. This is essential because the base current depends on h_{FE} and so is not a well determined quantity. If the base voltage is determined by a divider (as in Figure 7.3), the divider impedance will be low enough when:

$$R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} << h_{FE} R_E. \tag{1}$$

As we will see in a moment, this equation just says that the impedance seen looking into the divider (The Thevenin equivalent or $R_1 \| R_2$) should be much less that the impedance looking into the base. Another point to keep in mind is that when you fix the quiescent point by choosing the base divider ratio and the resistors R_E and R_C, you are also fixing the dc power dissipation in the transistor: $P = (V_C - V_E) I_E$. Be careful that you do not exceed the maximum allowed power dissipation P_{max}. Finally, the quiescent point determines the voltages at which the output will clip. For a common emitter stage the maximum output voltage will be close to the positive supply voltage V_{CC}. The minimum output voltage occurs when the transistor saturates, which happens when the collector voltage is no longer at least a few tenths of a volt above the emitter voltage. We usually try to design common emitter stages for symmetrical clipping, which means that the output can swing equal amounts above and below the quiescent point.

The voltage gain of the emitter follower stage is very close to unity. The common emitter stage, in contrast, can have a large voltage gain:

$$A = -\frac{R_C}{R_E}. \tag{2}$$

If we are interested in the ac gain, then R_C and R_E stand for the ac impedances attached to the collector and emitter, which may be different from the dc resistances. In our circuit we use C_E to bypass part of the emitter resistor at the signal frequency.

INPUT AND OUTPUT IMPEDANCES

The input impedance is the same for both emitter followers and common emitter stages. The input impedance looking into the base is

$$r_{in} = (h_{FE} + 1)R. \tag{3}$$

In this expression R is whatever impedance is connected to the emitter. For a common emitter, R would usually just be the emitter resistor, but for an emitter follower R might be the emitter resistor in parallel with the input impedance of the next stage. If you want the input impedance of the whole stage, rather than just that looking into the base, you will have to consider r_{in} in parallel with the base bias resistors.

The output impedance of a common emitter stage is just equal to the collector resistor.

The output impedance looking into the emitter of an emitter follower is given by

$$r_{out} = \frac{R}{h_{FE} + 1}. \tag{4}$$

Now R stands for whatever impedance is connected to the base. For our two-stage amplifier shown in Figure 7.5, the emitter-follower base is connected to the collector of a common emitter stage, and so R is the output impedance of that stage, which is equal to R_C.

EBERS-MOLL MODEL OF BIPOLAR TRANSISTOR

A slightly more detailed picture of the bipolar transistor is required to understand what happens when the emitter resistor is very small. Instead of using the current amplifier model, one can take the view that the collector current I_C is controlled by the base-emitter voltage V_{BE}. The dependence of I_C on V_{BE} is definitely not linear, rather it is a very rapid exponential function. The formula relating I_C and V_{BE} is called the Ebers-Moll equation, and it is discussed in H&H Section 2.10.

For our purposes, the Ebers-Moll model only modifies our current amplifier model in one important way. For small variations about the quiescent point, the transistor now acts as if it has a

small internal resistor r_e in series with the emitter

$$r_e = 25 \; \frac{1 \; mA}{I_C} \; .$$

The magnitude of the intrinsic emitter resistance r_e dependes on the collector current I_C.

The presence of the intrinsic emitter resistance r_e modifies the above Equations (1) – (4). In Equations (1) and (2) we should substitute $R_E \rightarrow R_E + r_e$, and for Equation (3) we need to substitute $R \rightarrow R + r_e$. Equation (4) is modified to read

$$r_{out} = \frac{R}{h_{FE} + 1} + r_e . \tag{4'}$$

The most important of these results is the modified Equation (2)

$$A = -\frac{R_C}{R_E + r_e} . \tag{2'}$$

which shows that the common emitter gain does not go to infinity when the external emitter resistor goes to zero. Instead the gain goes to the finite value $A = -R_C / r_e$.

Problems

1. Calculate the quiescent voltages V_B, V_E, and V_C, and the currents I_E and I_C for the common emitter circuit in Figure 7.4. How much power is dissipated in the transistor itself? Is the power safely below P_{max}? (See Appendix for 2N3904 Data Sheet.)

2. Find the ac voltage gain of the circuit in Figure 7.4 for 10 kHz sine waves with the emitter bypass capacitor C_E removed. Estimate the maximum amplitude of the output before clipping occurs. (The maximum output voltage is limited by the positive supply voltage, and the minimum is determined by the requirement that the collector voltage must be at least a few tenths of a volt above the emitter voltage.)

3. The emitter bypass capacitor can provide an AC ground path for the emitter, increasing the gain of the amplifier at high frequency. Considering the effects of the intrinsic emitter resistance r_e, what is the maximum possible AC voltage gain of the amplifier in Figure 7.4? Will this gain likely be realized for 10 kHz sine waves? Why or why not?

4. What setting of the emitter trimpot is needed to give the required gain of –25? For the single stage in Figure 7.4, what are the input and output impedances r_{in} and r_{out} at 10 kHz

and a gain of –25? (Note that r_{in} is the impedance looking into the base in parallel with the base divider impedance.) Calculate the fraction of the original amplitude obtained when a 560 load is connected to the output via a coupling capacitor.

5.   Calculate the output impedance for the emitter follower circuit shown in Figure 7.5. What fraction of the original output amplitude do you expect to obtain when you attach the 560 load to the emitter follower output?
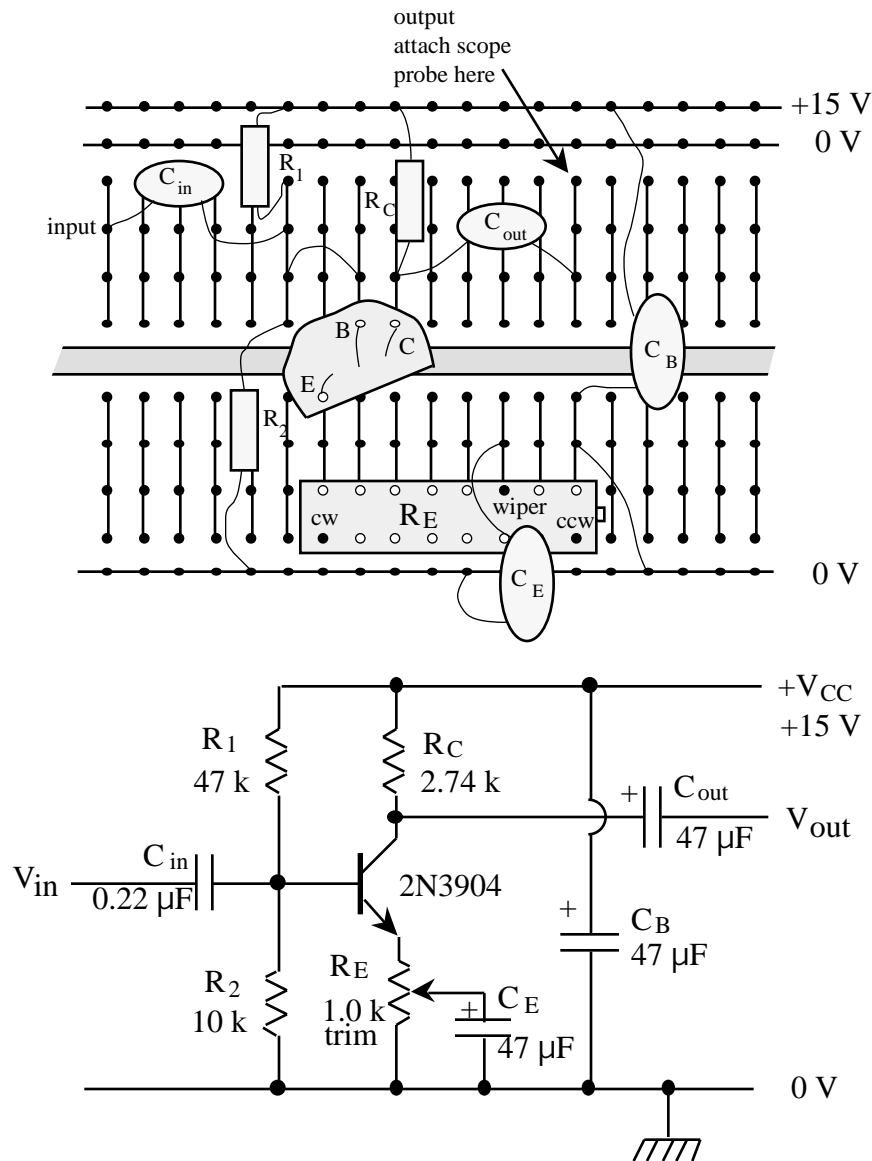

Figure 7.4   Common Emitter Stage Layout and Schematic

New Apparatus and Methods

A drawing to help you identify the leads of the 2N3904 transistor and the trimpot is shown in Figure 7.1. The 2N3904 is an NPN device, as indicated by its symbol with an outward pointing arrow. The arrow for a PNP device points in. To keep the convention straight, remember Not Pointing iN for NPN. Your trimpot may not look exactly like the one shown, but it will have the three leads wiper, cw, and ccw. The wiper moves toward the cw lead when the screw is turned clockwise.

The transistor amplifier uses dc power at +15 V only. Use just the positive section of the dc power supply. Disconnect the negative line from your circuit board.

In Figure 7.4 we show the first amplifier stage and a suggested circuit board layout. Your circuit will be easier to understand if you try to keep the physical layout looking like the schematic diagram. Use the wiring color code given in Experiment #4.

Use the oscilloscope 10x probe to observe the amplifier outputs. This minimizes capacitive loading and reduces the risk of spontaneous oscillations.

Outline of the Experiment

1   Verify that the 2N3904 is an NPN transistor using the digital multimeter. Is the 2N3906 a PNP or an NPN transistor?

2.   Construct a common emitter transistor bias circuit. Confirm that the quiescent voltages are correct. Add coupling capacitors to the circuit to make an ac amplifier, and measure the ac voltage gain for 10 kHz sine waves. Verify that the gain has the expected value, and confirm that the output amplitude can reach 5 V before the extremes of the sine waves are clipped.

3.   Make a variable gain amplifier by bypassing part of the emitter resistance with a capacitor. Find the maximum possible voltage gain and compare with your prediction.

4.   Adjust the gain to the required value of –25. Find the effect on the output amplitude of placing a source impedance of 1 k   in series with the signal source. Also observe what happens when you place a 560   load between the output and ground.

5.   Now build an emitter follower stage as an impedance buffer between the amplifier and the

load. Verify that the emitter follower alone has unit voltage gain. What happens now when you connect the load to the emitter follower output?

6.   Test the performance of the complete circuit under the specified conditions: 1 k source impedance and 560 load. First reset the overall gain to –25 if it has changed. Check that the 5 V undistorted output amplitude is still available. Measure the gain versus frequency from 1 Hz to 10 Mhz.

Detailed Procedure

POLARITY CHECK

Determine the polarities of the emitter-base and base-collector diode junctions of a 2N3904 using the diode tester on your digital multimeter. Now check the polarities for a 2N3906. Is it an NPN or a PNP transistor? The pin-out for a 2N3906 is the same as for a 2N3904.

COMMON EMITTER AMPLIFIER: QUIESCENT STATE

The first step is to construct the bias network and check that the correct dc levels (quiescent voltages) are established. Assemble the common emitter stage as shown in Figure 7.4, but without the input and output coupling capacitors or the emitter capacitor (without C_{in}, C_{out}, and C_E). The wiper contact on the emitter resistor R_E should not be connected to anything yet. Measure the resistors before putting them in the circuit, and if they differ from the values used in your calculations, recalculate the quiescent voltages. Before turning on the power, disconnect the power supply from the circuit board for a moment and check that it is set to +15 V. Then turn on the power, and check the dc levels V_B (at the transistor base), V_E (at the emitter) and V_C (at the collector).

The quiescent levels should agree with your calculations to within 10%. If they do not, there is something wrong that must be corrected before you can go on.

COMMON EMITTER AMPLIFIER: FIXED GAIN

Convert the previous circuit to an ac amplifier by adding the coupling capacitors C_{in} and C_{out}. Be sure to observe the polarity of polarized capacitors. The capacitors will transmit ac signals but block dc signals. This allows you to connect signals without disturbing the quiescent conditions.

When you switch on the power, you may see high frequency spontaneous oscillations. These must be suppressed before you can proceed.

Assemble a test set-up to observe the input and output of the amplifier with 10 kHz sine waves, using the 10x scope probe for the output. You may need to add a 220 k resistor to ground after C_{out} to keep the dc level at the scope input near ground. Vary the input amplitude to find the output amplitude at which clipping begins. Can you get a 5 V undistorted output amplitude (10 V p-p)?

Measure the gain of the amplifier for 10 kHz sine waves at an amplitude about half the clipping level. While you are at the bench, compare the measured gain with that predicted from the measured values of components:

$$A = -\frac{R_c}{R_E + r_e}.$$

If they differ by more than 5% find the cause and correct the problem before you go ahead.

COMMON EMITTER AMPLIFIER–VARIABLE GAIN

Connect the wiper of the 1.0 k trimpot R_E through the bypass capacitor C_E to ground. Verify that the quiescent point has not changed significantly.

Observe the change in gain as you traverse the full range of the trimpot using 10 kHz sine waves. Start with the contact at ground (bottom of diagram) and move it up until C_E bypasses all of R_E. When approaching maximum gain turn down the input amplitude (a long way) so that the output signals are still well shaped sine waves. If the output is distorted the amplifier is not in its linear regime, and our formulas for the ac gain are not correct.

Compare the measured maximum gain with the value predicted in the homework for several output amplitudes going down by factors of two. Do theory and experiment tend to converge as V_{out} tends to zero?

COMMON EMITTER AMPLIFIER: INPUT AND OUTPUT IMPEDANCE

Set the amplifier gain to –25 for 10 kHz sine waves. What trimpot setting gives a gain of –25?. (To see where the trimpot is set, remove it from the circuit and measure the resistance from cw to wiper or from ccw to wiper.)

Simulate the required source impedance by inserting a 1 k resistor in series with the input. What fraction of the original output amplitude do you see? Is this as expected? Remove the 1 k resistor before the next test so that you test only one thing at a time.

Connect a 560   load from the output to ground. What fraction of the original output do you now see? Is this as expected?

EMITTER FOLLOWER OUTPUT STAGE

In the emitter follower circuit, the input signal is applied to the base of the transistor, but the output is taken from the emitter. The emitter follower has unit gain, *i.e.* the emitter "follows" the base voltage. The input impedance is high and the output impedance is low.

Ordinarily the quiescent base voltage is determined by a bias circuit. In the present case the collector voltage V_C of the previous circuit already has a value suitable for biasing the follower, so a direct dc connection can be made between the two circuits.

Assemble the emitter follower circuit shown in Figure 7.5. Do not connect the 560   load to the output yet.

Carry out appropriate dc diagnostic tests. This time we expect the collector to be at +15 V, the base to be at the collector voltage of the first stage, and the emitter to be about 0.6 V below the collector. Correct any problems before moving on.

Confirm that the voltage gain of the emitter follower is unity. Drive the complete system with the function generator. Observe the ac amplitudes at the input of the emitter follower and at the output. Measure the ac gain of the emitter follower stage. (Again you may need to add a 220 k   resistor to ground after C_{out} to keep the dc level at the scope input near ground.) You may want to put the scope on ac coupling when you probe points with large dc offsets.

Attach a 560   load from the output to ground. What fraction of the unloaded output do you now see? Compare with your calculations.
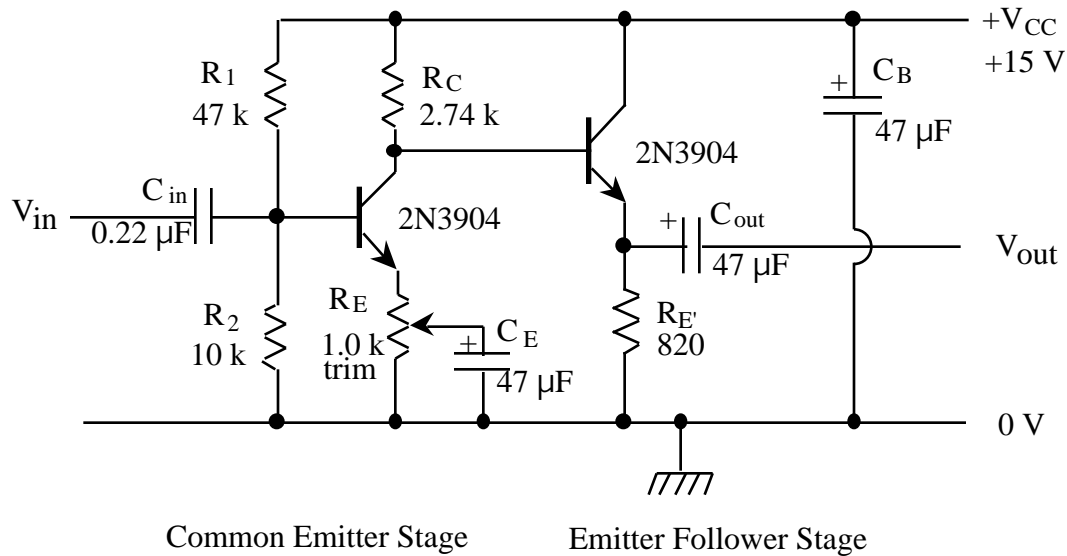
Figure 7.5   Complete Two-stage Amplifier Circuit

FINAL TESTS

Reset the gain to –25 with the 1 k   source resistor and the 560   output load in place. Check the linearity of the amplifier for 10 kHz sine waves by measuring the output amplitude at several input amplitudes, extending up into the clipped regime. Graph V_{out} versus V_{in}. The slope should equal the gain in the linear region of the graph.

Set the amplitude to be about one half the clipped value, and then determine the upper and lower cut-off frequencies f_+ and f_- by varying the frequency of the sine waves.   Can you understand the origin of these frequency cutoffs?

Appendix

Data sheet for the 2N3904. (See also Horowitz and Hill, Table 2.1)

The 2N3904 is an NPN silicon bipolar junction transistor.

ABSOLUTE MAXIMUM RATINGS

V_{CE} 40 V   (collector to emitter voltage)

V_{EB} 6 V   (emitter to base voltage)

I_C 200 mA   (collector current)

P_{max} 300 mW   (power dissipation)

TYPICAL CHARACTERISTICS

h_{FE} 200   (current gain. See H&H Figure 2.78 for typical dependence on I_C.)

f_T 300 MHz   (frequency where internal capacitances cause gain to be

                                 reduced to unity)

C_{EB} 10 pF   (internal emitter-base capacitance)

C_{BC} 3 pF   (internal base-collector capacitance)