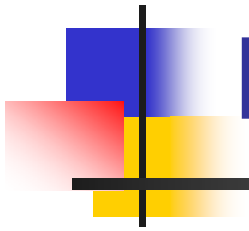


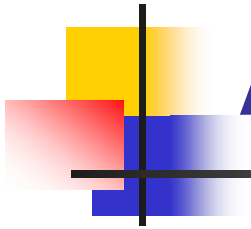
Lecture 5

CSE 140L

Instructor: C.K. Cheng

Oct. 26, 2005

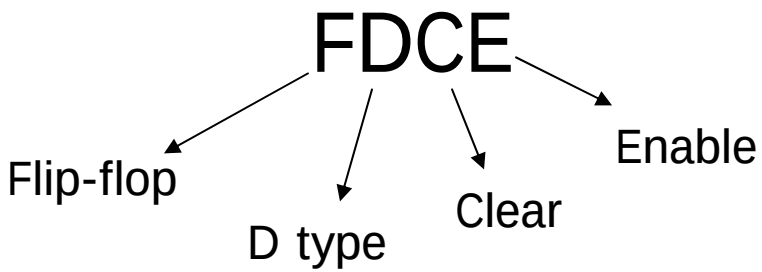
Courtesy of Jianhua Liu



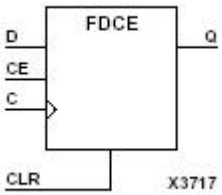
Agenda

- D flip-flops in Xilinx
- Introduction to Lab 2 assignment
  - Shifter register
  - Asynchronous counter
  - Synchronous counter
  - Gray Counter
  - Pseudo random sequencer
- A complete example of 4-bit binary counter design

FDCE



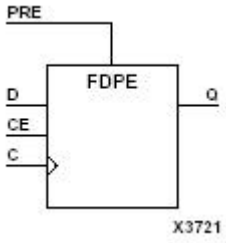
So it's a D flip-flop with Clear and Enable signals, and Clear has priority over Enable.



Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

FDPE

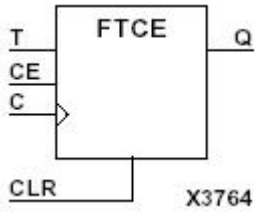
- D flip-flop with Preset and Enable



Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	↑	0
0	1	1	↑	1

FTCE

- T flip-flop with Clear and Enable



Inputs				Outputs
CLR	CE	T	C	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	0	X	No Chg
0	1	1	↑	Toggle

Shift Register

- What's that for?

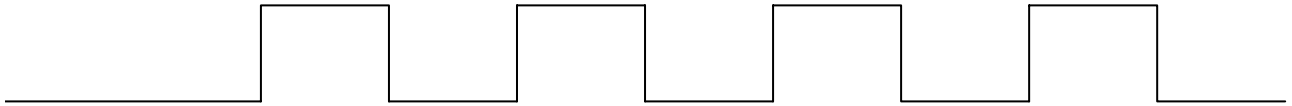
1

1	1	0	1

1	1	0	1

8:03pm

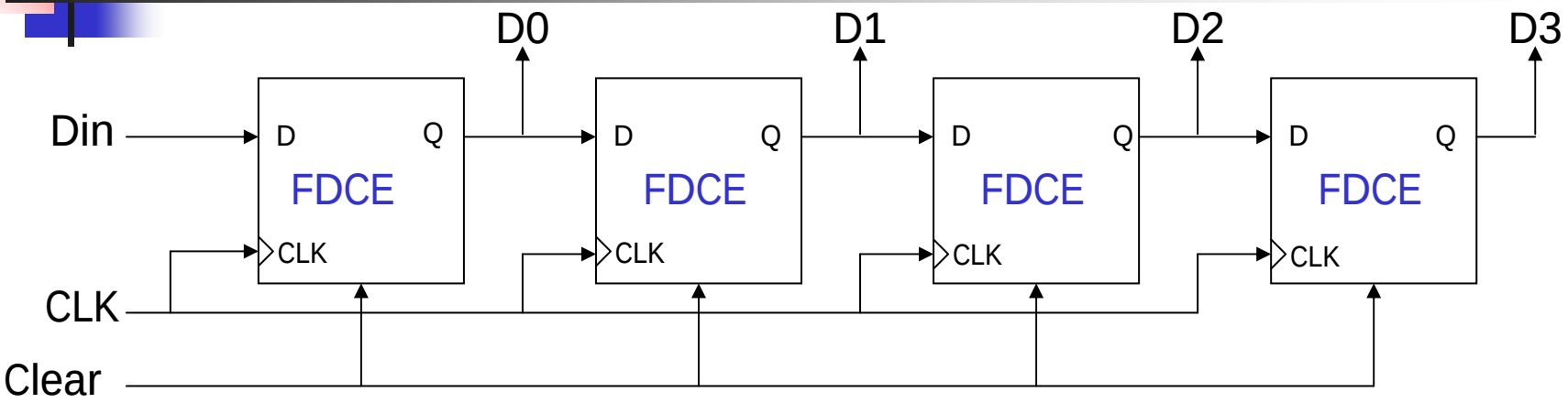
Shift Register



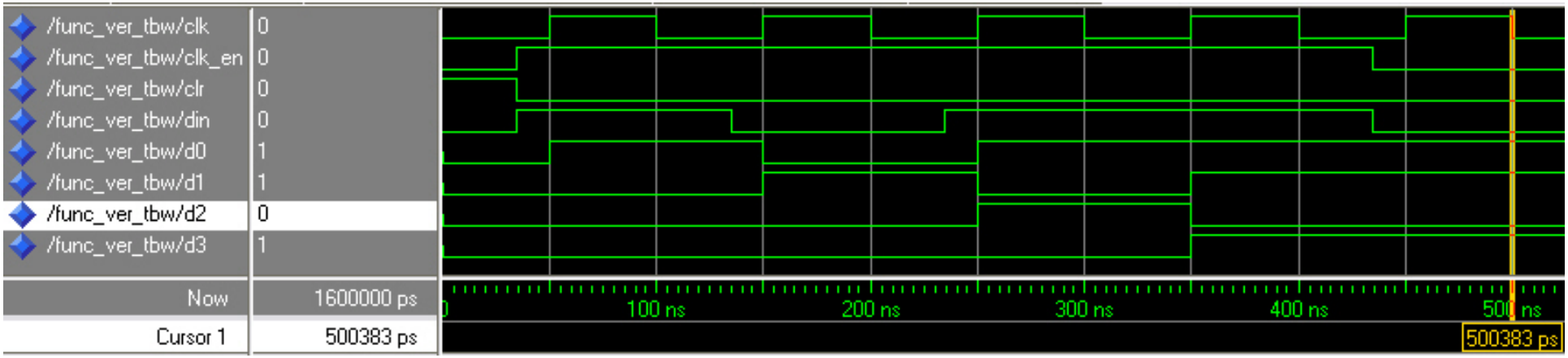
	8:00pm	8:01pm	8:02pm	8:03pm
Din	1	0	1	1
D0	0	1	0	1	1
D1	0	0	1	0	1
D2	0	0	0	1	0
D3	0	0	0	0	1

We want

Shift Register

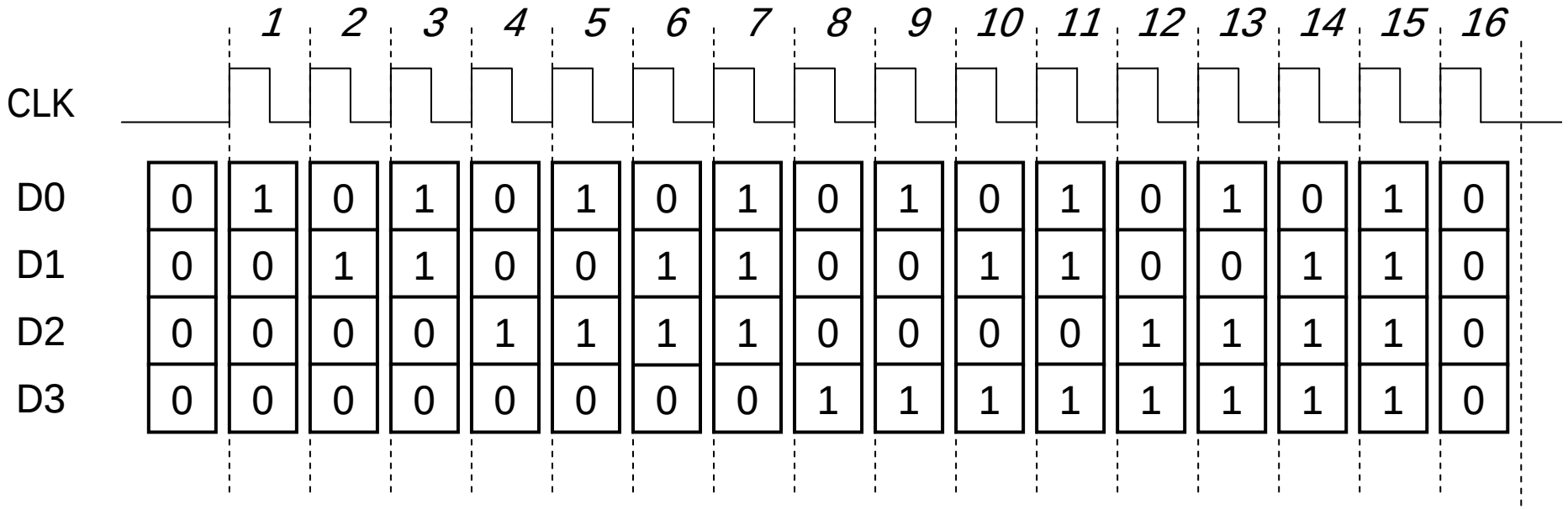


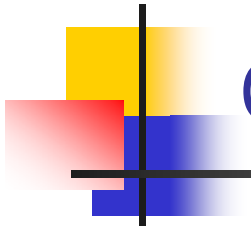
Verification



Counters

- A counter counts the number of clock cycles



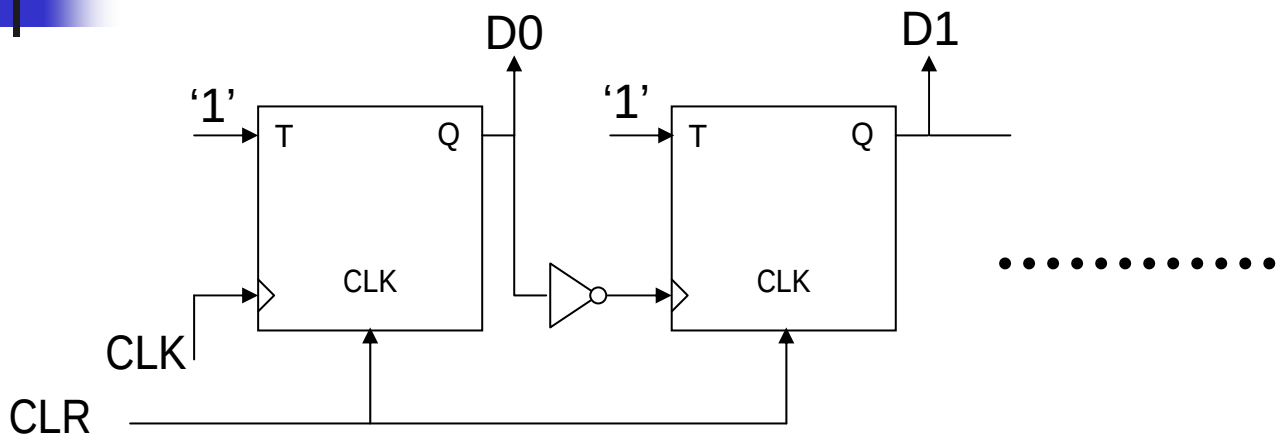


Counter Styles

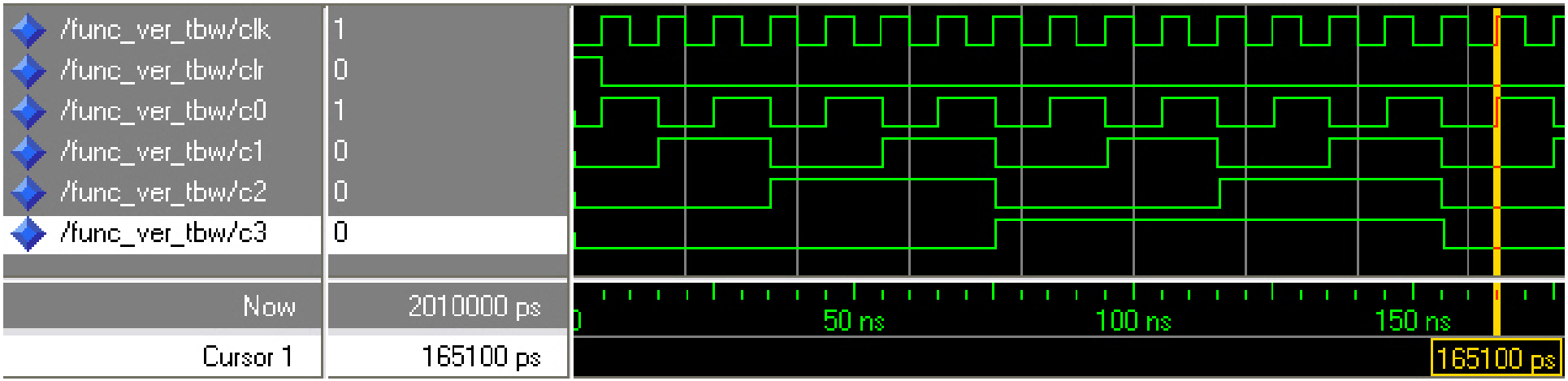
- Synchronous counter
  - All flip-flops are governed by a universal global clock signal
- Asynchronous counter
  - No universal global clock signal;
  - Less area
    - You have more flexibility in designing FSMs
  - Less power
    - Eliminates simultaneous D flip-flop switching during clock transitions
  - High speed
    - In terms of throughput
  - But …hard to design and error prone
    - Complicate protocol for inter-module communication
    - Timing!

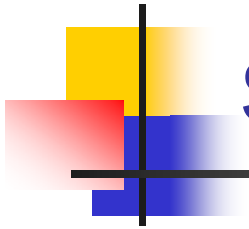
Asynchronous Counter

Design



Verification



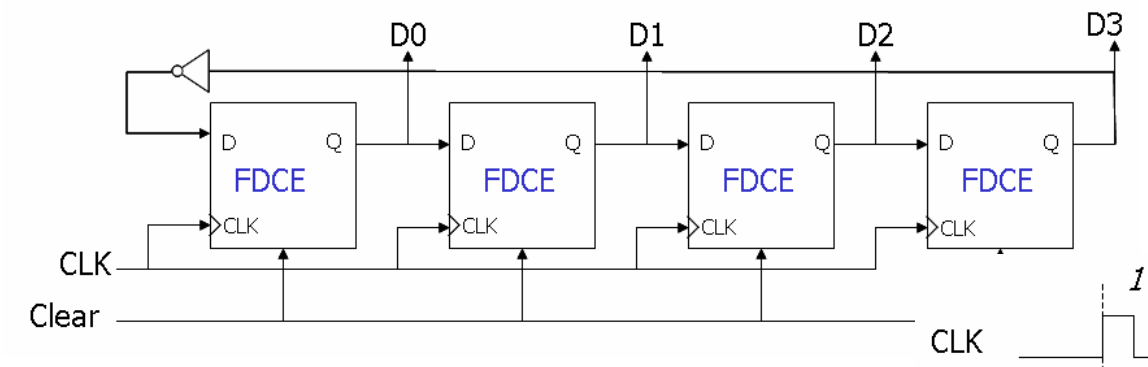


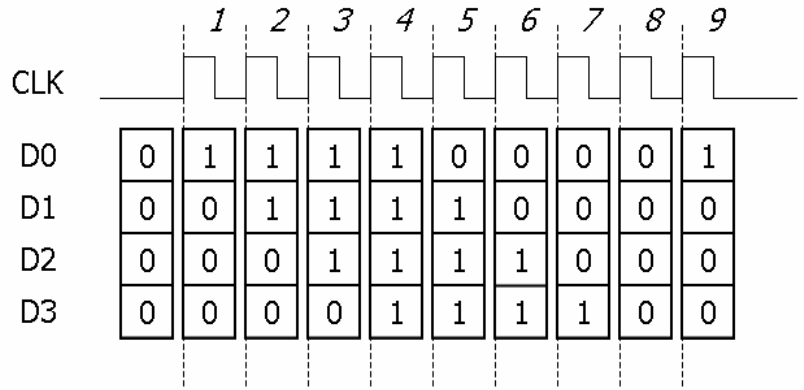
Synchronous counter

- Binary counter
  - We’ll see a design example of this
- Johnson counter
- Gray counter

Johnson Counter

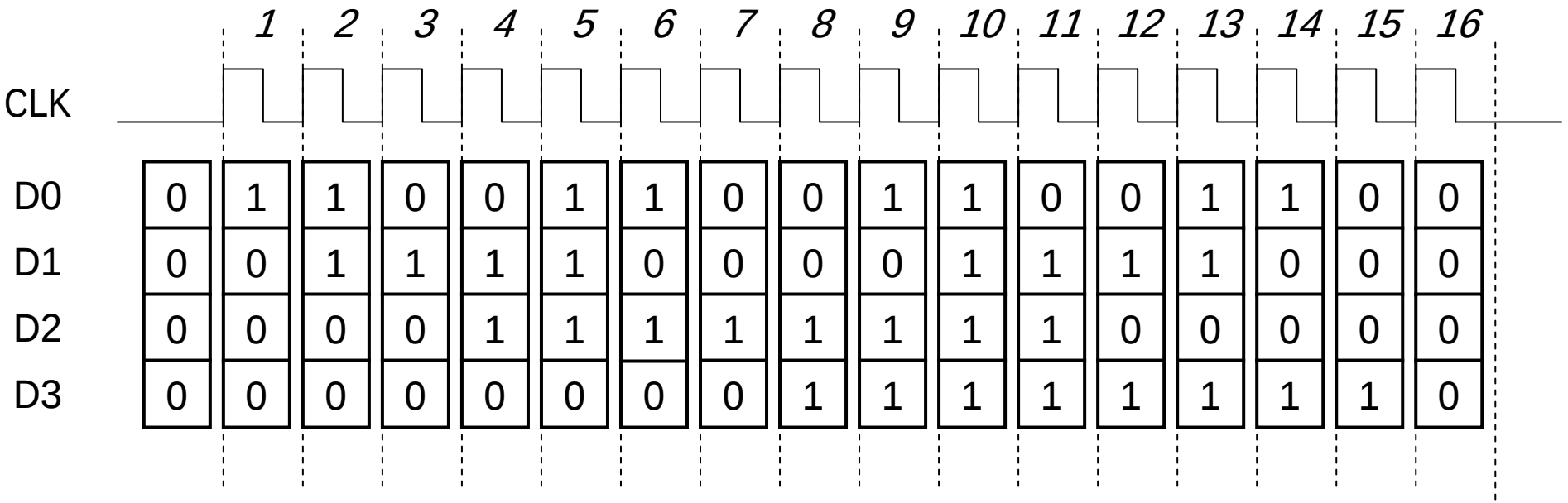
- Last output inverted and feed back to the first input.
- also called Mobius counter because it resembles the famous Mobius band.

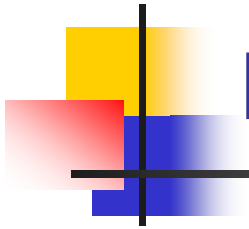




Gray Counter

- Every two neighboring states differ only in one bit
- Good for reducing hazards in the circuit

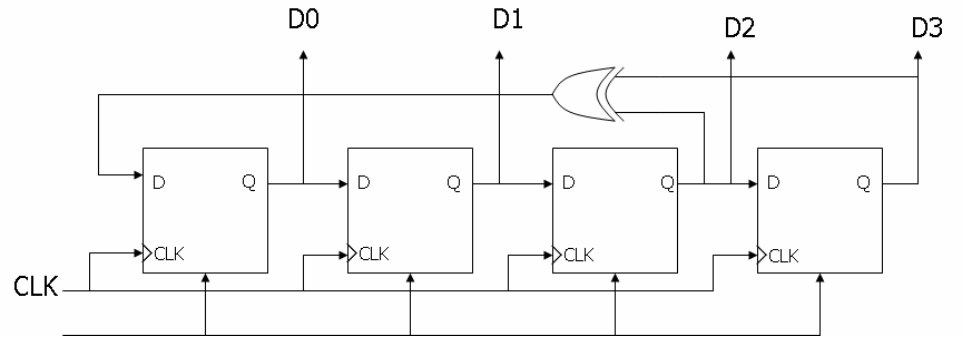




Pseudo Random Sequencer

- A pseudo random sequencer generates a sequence of pseudo random bits.
- Pseudo means it’s not complete random, it’s actually a cyclic bit sequence with a large period.
- Usually implemented using Linear Feedback shifter Register (LFSR).

Random Sequencer



- The length of the cycle depends on
  - The feedback network
  - The initial state

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CLK																
D0	1	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1	0
D1	1	1	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1
D2	1	1	1	0	0	0	1	0	0	1	1	0	1	0	1	1	1
D3	1	1	1	1	0	0	0	1	0	0	1	1	0	1	0	1	1
	15	14	12	8	1	2	4	9	3	6	13	10	5	11	7	15	14