AN823

Analog Design in a Digital World Using Mixed Signal Controllers

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INTRODUCTION

The purpose of this Application Note is to familiarize engineers with PIC16C78X design considerations, specifically:

- Potential noise problems in mixed signal design
- Features and performance of the new analog/digital peripherals
- Some common applications for the PIC16C78X

The PIC16C781 and PIC16C782 are the first devices in a new line of mixed analog/digital microcontrollers from Microchip. These microcontrollers are a marriage of our traditional microcontroller architecture with new mixed signal peripherals that change many of the old conventions of embedded microcontroller design. Not only do the new peripherals open up new applications for the microcontroller, they bring new design concerns that might be unfamiliar to traditional microcontroller designers. This Application Note will highlight some of the common problems associated with mixed signal design and offer techniques for overcoming these problems. It will also cover the features and performance of the new peripherals. Finally, this Application Note covers some of the common applications that take advantage of the PIC16C78X's unique peripherals.

NOISE AND MIXED SIGNAL DESIGN

The first area to cover concerning mixed signal design is identifying and controlling potential noise sources. Traditionally, microcontroller designs have enjoyed relative immunity to noise concerns, due to their high noise margins (typically measured in tenths of volts). However, the addition of analog blocks designed to handle low level signals change some of the design priorities. Noise levels in the millivolt and microvolt range can now have a significant impact on the performance of the system. Therefore, it is important that the designer acquires new tools and techniques for controlling, and where possible, eliminating noise.

IDENTIFYING NOISE SOURCES

Identifying potential noise sources in a design is the first step in controlling or eliminating noise in a mixed signal design. Almost any active circuit in a design can generate noise; however, some circuits are more likely to become noise generators than others. The following is a short list of common sources of noise:

1. Oscillators: This one is an obvious source of periodic AC noise. However, designers should remember that oscillators also have output drivers which can generate fast rise time transients and ringing that is unrelated to the oscillator frequency.
2. High current/power drive circuits: Another source of fast rise time transients and ringing.
3. Amplifiers/Comparators: The amplifier can become unstable driving capacitive loads. Amplifiers and comparators can oscillate if their bypass capacitors are missing or inadequate.
4. Switching power supply circuits: These circuits can be significant sources of noise because they incorporate both oscillators and high drive currents.
5. Circuits with external connections: These circuits are subject to not only the noise sources inside the cabinet, but also all the external sources including ESD and RFI.
6. Fast rise time logic: Any logic device with a rise time of less than 5-10 nanoseconds is capable of generating noise in the 1 to 100 MHz range.

This list is by no means complete. There are other circuits and systems in any design which may be a potential source of noise. However, a good general rule of thumb is: ‘If it is high speed, high power, or is not bypassed correctly, it can generate noise.’

Once the noise sources have been identified, the next step is to determine if the noise source can be eliminated or must be minimized. Obviously, some noise sources (such as oscillators) cannot be removed and must be minimized. However, other unintentional or undesirable oscillators can often be removed. Sometimes small changes made at the beginning of a design can significantly reduce the probability of noise-related problems. For instance:

1. Verify that all bypass capacitors are present and adequate for their circuits.
2. Verify the load impedance and drive capability of all amplifiers.
3. Use local linear regulation from an intermediate voltage to significantly reduce the noise from a high power, central switching power supply.
4. Use slower devices in place of fast switching devices to reduce the amount of rise time transient related noise.
5. Limit the rise time of faster devices and physically separate the devices and their traces from sensitive inputs and circuitry.
6. Physically and electrically isolate low level analog circuitry from high power drivers to significantly lower the noise level in the analog circuitry.
7. Eliminate layout patterns which reinforce electrical and magnetic noise fields, such as sharp corners and loops.

For noise sources that cannot be eliminated, the only option is to isolate sensitive circuitry from the source of the noise. In extreme cases, isolation may require shielding and/or opto-isolation of common signals. However, in most cases, careful design and attention to how noise travels in a design are sufficient to limit noise to a manageable level. The following sections will examine the more common pathways used by noise to travel around a circuit.

ELECTRICAL NOISE PATHS

Electrical noise typically travels by one of two methods of transmission: conducted and radiated.

Conducted noise is defined as noise carried into the affected circuit by an existing electrical connection in the design. Typically this is a signal trace, ground trace, or power connection. Conducted noise can be:

- periodic AC noise, repeating AC waveforms
- transient, one-shot impulse noise
- DC offset and error voltages
- uncorrelated broadband noise from non-switching devices

Radiated noise, on the other hand, travels as:

- an electrical field
- a magnetic field
- an electromagnetic or RF wave

Radiated noise is always transient or periodic AC in nature, never DC. Radiated noise is also the more difficult noise source to identify and correct due to its more intangible path. The following sections cover the more common paths that noise follows around a design, plus a collection of tips for controlling the noise.

CONDUCTED NOISE

Conducted electrical noise is, on the other hand, noise which travels on the conductors within a design. The secret to controlling conducted noise is to identify the path from the source to the affected circuit and then either eliminate the source, the path, or both. While noise can travel on any conductor, the more common paths are typically the power and ground connections. Power and ground connect to every section of the design, making them prime targets for conducted noise. In addition, power and ground carry the supply current needs of the entire circuit, making them the source of some of the highest power noise as well. Careful attention to the layout of power and ground within a mixed signal design is an important step to eliminating many of the conducted noise problems.

A form of conducted noise unique to power and ground connections is noise generated by the interaction of the trace's impedance (resistance/inductance) and power supply currents flowing in the traces. Because both lines carry current between the power supply and every active device in the design, any inductance/resistance in the power and ground is particularly undesirable because the impedance will translate the variations in power supply currents directly into noise voltages. This means that a single power or ground trace will have a noise potential that is the composite of every current flowing in the trace. This kind of noise can be particularly troublesome because the currents in the ground traces can produce AC, DC, and transient noise.

The noise translates into noise on every signal generated or received by every circuit using the ground to various degrees. Therefore, minimizing resistance and inductance in the power supply (particularly in the ground trace) is an important design priority. The best method for minimizing impedance of a ground is to replace discrete ground traces with a ground plane (copper pour).

CONDUCTED NOISE: GROUNDS

Copper grounds translate AC and DC currents into electrical noise due in part to the finite resistance of the trace. Copper is a very good conductor, but it does have some resistance and that resistance will convert any current flow in the trace into a voltage. Furthermore, the current flow in a ground trace will produce a range of ground potentials along the length of the trace. So, when a high current drive output switches at one end of the trace, it is reasonable to expect that circuits that share the ground trace with the driver will experience a shift in the ground potential proportional to the change in current. Further, if multiple high current drives share a common ground, the shift in ground potential will be a composite of the current flows generating both positive and negative shifts as the different drivers switch on and off. The size of the voltage shift, from Ohm's law, is a function of the change in current and the impedance (resistance and inductance) of the ground path. Therefore, to minimize the effect of high supply currents, the design must have the minimum ground resistance between the drive and the power supply.

A copper conductor's resistance is proportional to the length of the conductor, multiplied by its resistivIty (ρ), divided by the cross sectional area (see Equation 1). From Equation 1 it can be seen that the minimum resistance occurs when the conductors length (L) is kept to a minimum and the area (A = width* thickness) of the conductor is at a maximum. Therefore, for minimum ground voltage shifts, the ground traces in a mixed signal design should be kept as short and wide as possible. Using thicker copper is also helpful in minimizing trace impedance, but is often impractical. The optimum solution is to take the ground width to its maximum by generating a ground plane.

EQUATION 1: RESISTANCE EQUATION

$$R = \frac{\rho * L}{A}$$

While copper grounds translate AC and transient currents into electrical noise due to the copper's resistance, a larger contribution is typically due to the inductance of the ground. Inductance-translated noise voltages are in response to much smaller AC and transient current flows in a design. The difference in noise and current is due to the interaction of the frequency of the noise current and the inductance of the ground. Higher frequency and faster rise time currents generate larger noise voltages than lower frequency, slower rise time currents. Unfortunately, each time a digital device changes state in the circuit, it generates a current impulse in the ground connection of the device. Due to the higher frequency operation of most digital devices, even a device running at a low frequency will still generate high frequency noise caused by the fast rise time of the logic. The best option open to the designer trying to limit high frequency noise is, therefore, to limit the inductance of the ground trace.

A ground trace behaves inductively because, like every other conductor, it creates a magnetic field in response to the current flow. The inductance of a trace is dependent upon:

- length of the conductor
- configuration (whether straight or coiled)
- presence of any ferrous materials in the field

To reduce inductance in a conductor:

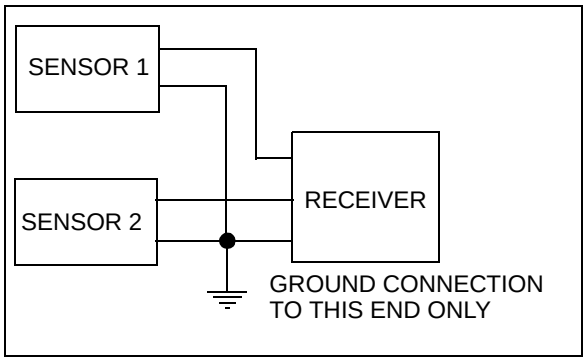
1. Keep trace lengths short, eliminating corners.
2. As much as is practical, keep traces straight, no loops.
3. Where possible, use non-ferrous materials like aluminum for cabinets and brackets.

Two circuits that share a common ground with identical noise voltages are immune to the Common mode ground noise because their ground references are shifting up and down together. If the ground trace between two circuits carries little or no current, and the trace has a minimum of resistance and inductance, then the ground potential of both circuits will be the same and any common noise present on the grounds will cancel out. This means that if sensitive circuits are grounded together on an isolated ground (separate from high current circuits). The ground carries only a minimal current flow in the trace between the circuits. Therefore, the sensitive circuits will not be significantly affected by the high current circuits, even if they ultimately share a common power source. The trick is to make sure that the current flows in the sensitive circuit grounds are as small as possible and the inductance and resistance of the ground is kept to an absolute minimum.

Sensor signals are especially susceptible to ground noise due to their low level outputs and their high output impedance. Low output levels from high impedance drivers have little power. Consequently, sensors seldom have the drive capability to overpower even lowest levels of introduced noise. The best solution is to prevent the introduction of noise in the first place. Prevention is best accomplished by:

1. Using a short/wide common ground (ground pour) between the sensor and it's ADC or amplifier.
2. Limiting the ground connection to the sensor and its receiver only. The only common ground connection to the rest of the circuit should be at the receiver, as shown in Figure 1.
3. Physically separating the sensor, its connections, and the input filter and receiver from all high power and fast rise time circuits.
4. Putting a low pass filter on all analog sensor inputs to the ADC.

FIGURE 1: SENSOR GROUNDS



To summarize, grounds are especially sensitive to noise due their function as the 0V reference in a circuit, and the presence of all the circuit ground currents. The best prevention for noise on the ground return is to:

- keep all ground traces short and wide (ground plane)
- isolate high current drives on separate ground returns
- put sensitive circuits and sensors on their own dedicated ground traces

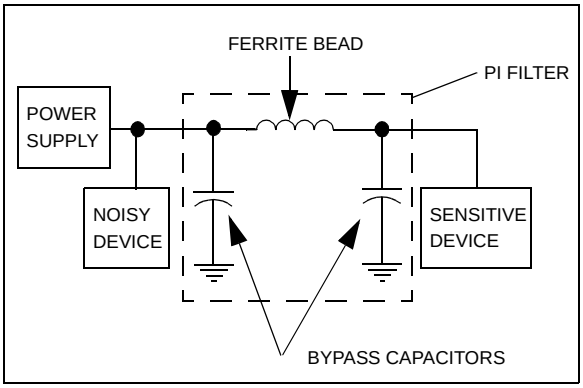
CONDUCTED NOISE: POWER SUPPLIES

The circuit power supply is another common path for electrical noise to travel through a mixed signal design. Power supply traces have the same level of connectivity in a circuit as the ground, and are also subject to the same effects of resistance and inductance, so it is no surprise that it also acts as a conduit for conducted noise. Therefore, all of the precautions outlined in the previous section apply equally well to power trace as they did with grounds. Fortunately, most analog devices are designed for relative immunity to power supply noise (the PSRR specification) so the effects of noise transmission via the power supply tend to have a smaller overall impact on circuit performance. But be careful, PSRR is no substitute for bypass capacitors. PSRR also drops off with frequency, so PSRR provides little or no protection from high frequency noise.

Power supply traces are also different in that they are not used as the 0V references in the circuit. In many cases (especially in ground referenced applications) variations in supply voltage from device to device do not cause as much of a problem in mixed signal designs as do variations in ground potential. This opens up some possibilities for filtering and isolation of noise that are not possible with ground systems. Specifically, it allows the use of power supply trace's parasitic inductance as part of a filtering system.

In fact, it can be beneficial to increase a power supply trace's inductance to further enhance the filtering characteristic. Typically, the inductance is increased through the use of Ferrite beads in series with a power connection to a device. By placing a Ferrite bead in series with a power supply connection, the cutoff frequency of the filter network is significantly lowered, cutting out more of the higher frequency noise. The combination of the Ferrite bead and the normal inductance of the trace provide the series inductance of the filter, and the bypass capacitors on the devices and capacitances in the power supply provide the capacitors to ground, creating the low pass filter in Figure 2.

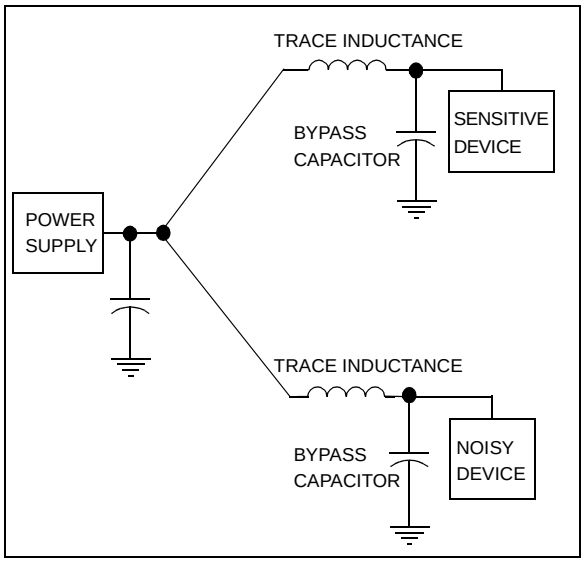
FIGURE 2: POWER SUPPLY PI FILTERING



The result is a network that resists varying currents flowing through the network, plus a low impedance AC short to ground on either side. The network provides a path for DC power while creating a barrier to AC and transient noise. An important note to remember is that Ferrite materials differ in their effectiveness for different frequencies. When selecting a Ferrite Bead, it is important to select a material designed for the noise frequency range.

While isolating noisy circuits through the use of inductor/capacitor “PI” filters is one of the most effective methods for controlling conducted noise on a power supply trace, a similar (less expensive, but less effective) effect can be achieved by simply separating power supply traces for different circuits. Separate power supply traces create a similar filter configuration by using the natural inductance of the power supply trace as the inductor of the PI network. Although inductance is a desired effect in this configuration, it must be remembered that long power traces will also increase the trace resistance. Separate power traces do, however, have the desirable effect of putting two in-line inductors and three capacitors to ground between noise and sensitive circuits, as shown in Figure 3.

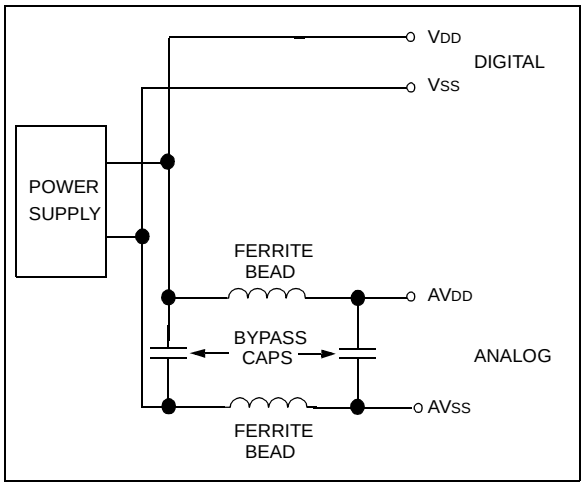
FIGURE 3: POWER TRACE FILTER



A natural extension of the separate supply method is to separate the power supplies of circuitry within a single device. The performance of the PIC16C78X analog peripherals is significantly improved due to the separation of the noisier digital supply from the analog supply within the chip. A simple method for controlling noise in a PIC16C78X mixed signal design is to maintain the separation of the power supplies outside of the device: one for slower low current analog functions, and the second for the faster medium current digital functions. Keep in mind that the AVSS and VSS connections, as well as the AVDD and VDD connections, must be kept within 0.3 volts of each other.

Figure 4 demonstrates an example split supply with with split power and ground.

FIGURE 4: SPLIT SUPPLIES



CONDUCTED NOISE: BYPASS CAPACITORS

A related issue to power supply and ground noise is the subject of bypass capacitor selection. The bypass capacitors not only provide an immediate local supply of energy for transient power supply demands, they also act as elements in the low pass filter network discussed in the previous section. Using a bypass capacitor that is too small, or ineffective at the noise frequency, will not only increase ripple voltage in power supply filtering, it can actually create oscillations by allowing a feedback path through the power supply. Therefore, it is important that the selection of bypass capacitors be based on the circuit requirements rather than simply using the traditional 0.1 µF ceramic.

Part of a bypass capacitors purpose is to provide for the short-term supply of current for powering active devices. In digital logic, the bypass capacitors supply the impulse switching currents required to charge/discharge the gate capacitance of the numerous MOSFET transistors on each clock transition. In high drive circuits, the bypass capacitors provides a similar function by supplying the initial current demands of the output until the current flow from the power supply stabilizes at the new load. In both applications, the primary requirement for the bypass capacitors are its capacitance/current capability. For logic and microcontrollers, the traditional 0.1 µF ceramic capacitor is sufficient due to its relatively high capacitance and the low Equivalent Series Resistance (ESR) typical of ceramic capacitors. For higher power drives such as switching power supplies and high current drivers, the requirements for bypass capacitors are much higher. Typically, the higher capacitance requirements dictate using electrolytic capacitors. However, standard electrolytic capacitors typically have too high an ESR rating to effectively transfer power at the current levels required by the circuit. As a result, specially designed low ESR capacitors have been developed to handle the higher charge and discharge current requirements.

Low power analog circuits also use the bypass capacitor for another purpose. The bypass capacitors act together with the trace inductance to form a filtering network which limits the transfer of noise between devices. For this function, a single large-value capacitor is often ineffective due to limits in the capacitors effective frequency range. In instances of broad band high frequency noise, often two or more capacitors in parallel are required to provide the necessary effective frequency range to filter out all of the high frequency noise components.

The upper frequency limit for a capacitor is expressed by its Self Resonant Frequency (SRF). SRF is defined as the frequency at which the parasitic inductances of the capacitor resonate with its capacitance, and is the upper limit of a capacitor's effective frequency range. Careful selection of a bypass capacitor should include research on the capacitors SRF and the likely frequencies of noise that will be present in the design.

Note:	Typically the trace inductance, in combination with the bypass capacitors, is sufficient for the filtering function. However, if additional filtering is needed for low frequency noise, it may be necessary to include an inline inductor, or Ferrite Bead, in the supply lead to lower the cut off frequency of the filter network.

The bypass capacitor requirements of different circuits are dependent upon the functions they will be performing and their tolerance to noise. Care must be taken to choose bypass capacitors which will be effective in the specific application.

The PSRR of the analog circuit, the frequency of adjacent noise sources, and output drive needs of the circuit should be considered in the selection of a bypass capacitor. In addition, not all capacitors are created equal. Using a low cost electrolytic capacitor in place of a low ESR capacitor may seem like a reasonable substitution. However, the losses due to the capacitor's higher ESR can result in abnormal heating of the capacitor leading to a rather dramatic failure. Ceramic capacitors also come in a variety of materials, each with its own strengths and weaknesses. X7R ceramic capacitors are less expensive and are available in many larger values. However, they also have a lower SRF which limits their effectiveness against high frequency noise. A 1000 pF NPO ceramic capacitor can actually be more effective against 50-100 MHz noise than a 0.1 µF X7R. Careful selection of a bypass capacitor up front in the design can save considerable time in identifying noise problems later on.

As with power supplies and ground traces, the trace length between a bypass capacitor and its device can have a significant effect on the bypass capacitor's performance. The bypass capacitor's function is to supply power and act as a filtering element to remove noise. Adding a resistive/inductance element between the device and its bypass capacitor reduces the capacitor's effectiveness by increasing the capacitor's parasitic inductance and resistance. The resulting increased losses during energy transfers between the capacitor and its device can significantly reduce the capacitor's effectiveness. Therefore, it is very important that all bypass capacitors must be mounted as close as possible to their devices. The traces connecting the capacitor to the device must be kept as short and as wide as possible to minimize any stray impedance that might interfere with the quick, low-loss transfer of energy between the capacitor and the device.

Unfortunately, the SRF for most capacitor types are not widely published. To help with this problem, Table 1 is included as a guideline with this Application Note that lists some of the typical SRFs for common types of capacitors.

TABLE 1: SRF FOR COMMON CAPACITORS*

Type	Capacitance	SRF
Tantalum (chip)	10 µf	600 kHz
Polyester (leaded)	1.0 µf	2 MHz
X7R Ceramic (chip)	0.1 µf	11 MHz
COG/NPO Ceramic (chip)	1000 pF	90 MHz
X7R Ceramic (leaded)	0.1 µf	7 MHz

* From page 88 of the "*Circuit Designers Companion*" by Tim Williams

RADIATED NOISE

Radiated noise is electrical noise which is coupled through:

- Electrical fields
- Magnetic fields
- Radio frequency energy

Due to its less tangible path, radiated noise can be one of the most intimidating noise problems to diagnose and correct. Often, the noise seems to magically appear out of thin air. However, once the designer understands the basic mechanisms of radiated noise, much of the mystery disappears and the methods for eliminating or controlling the noise problems become fairly simple. Typically, radiated noise travels via one or more of a few basic mechanisms:

- Electrostatic (capacitive) coupling
- Inductive (magnetic) coupling
- Electrostatic discharge (ESD)
- Radio Frequency interference (RFI)

The following sections include explanations of the various mechanisms and examples of the more common techniques for diagnosing the problem as well as remedies.

RADIATED NOISE: ELECTROSTATICLY COUPLED NOISE

Electrostatic or Capacitive coupling is electrical noise coupled from one conductor to another via an electric field between the conductors in the same manner as a capacitor transfers AC signals between its plates. Basically, electrostatic coupled noise travels via the unintended capacitors in a design. The two conductors involved can be two wires in a bundle, or two traces that pass each other on a PCB. Any two conductors will create some capacitance between them. Fortunately, capacitive coupling falls off quickly with the distance separating the conductors, and it is not very efficient for moderate-to-low rise time signals. Therefore, electrostatic coupled noise typically is limited to high frequency and fast rise time signals, and conductors in close proximity to each other. For designs suffering from capacitively coupled noise, the secret to controlling the noise is to reduce the capacitance to such a small value that the amount of noise coupled between the conductors is negligible.

In Capacitive coupling, the amount of noise coupled between two conductors is proportional to the frequency of the noise and the parasitic capacitance formed by the two conductors. Therefore, a good test for capacitively coupled noise is to monitor the noise level of the affected circuit and see if changing the capacitance between the affected circuit and surrounding circuits causes a shift in the noise level. To change the coupling capacitance, try moving the suspect conductors passing near the affected circuit. If the conductor spacing can not be easily changed, try introducing a non-ferrous material into close proximity with the affected area. Human tissue, in the form of a finger tip is usually effective. If the noise is affected by moving the conductor, or poking around with a finger, then the mechanism is probably capacitive.

Note:	Remember to exercise caution around high power and voltage circuitry to prevent electrical shock.

Assuming that the frequency of the noise cannot be reduced, the only method available to the designer is to reduce the amount of coupling capacitance. Given that the two conductors form the two plates of a capacitor, with the capacitance proportional to the area of overlap divided by the distance between the conductors. The two best methods for reducing the capacitively coupled noise are:

1. Minimize the overlapping area of the two conductors. Basically, this means that conductors carrying noisy signals should overlap other conductors as little as possible.

   Recommendations:

   -Isolate noisy wires in separate wire bundles.

   -Cross noisy signals at right angles.

2. Maximize the distance between the conductors.

   Recommendations:

   -Physically by separating the conductors.

   -Electrically by separating the conductors with another grounded conductor. The grounded shield conductor can be the shield on a cable or simply a ground trace between the two conductors.

Note:	A narrow shield conductor or shielding trace will be less effective if it has a high inductance or resistance between the area it is shielding and it's connection to ground. The inductance and resistance will allow the shield to be pulled capacitively by the noisy conductor. The resulting electrical noise coupled to the shield will then couple capacitively from the shield to the conductor that is being shielded. Therefore, shields must have short and wide connections to ground to be effective.

RADIATED NOISE: INDUCTIVELY COUPLED NOISE

Magnetic or Inductive coupling is electrical noise coupled from one conductor to another via a magnetic field. At its simplest, a transformer is just two coils of wire wound around a common bobbin. Power transformers increase the power coupling by inserting a ferrous material, but even an open-air core will couple energy from one winding to another. Inductively coupled noise makes use of this same mechanism to couple noise from one conductor to another. The conductors can be:

- individual wires bundled together in a harness
- close traces on a board
- wires routed through the same ferrous metal structure

Fortunately, inductive coupling is not very efficient at high frequencies due to the inductive nature of coils in general. Therefore, it is usually easy to distinguish from capacitively coupled noise on the basis of frequency. Low to mid frequency noise is typically inductively coupled, and high frequency is typically capacitively coupled. Some typical sources of magnetically coupled noise are:

- Fluorescent light ballasts
- Power transformers
- Motors
- CRT monitors

The basis of magnetic coupling is two conductors: one carrying a changing current, and the other unbiased. As the current changes in the first winding, it builds and collapses its magnetic field. When the lines of the changing magnetic field cut through the second conductor, a current is induced in that conductor. The magnitude of the current is dependent on three factors:

1. The strength of the magnetic field at the second conductor
2. The number of loops in the second conductor that pass through the field
3. The presence of a ferrous material

Inductively coupled noise operates in the same manner: noise currents in the noisy wire produce a changing magnetic field which induces a noise current in the second conductor, coupling the noise.

Determining if inductive coupling is causing noise on a conductor is handled in much the same way as capacitive coupling. The noise level in the affected conductor is monitored, and the physical relationship to other conductors and magnetic components in the design is changed. If the noise is suspected to be coupling from a 60 Hz magnetic source (i.e., a transformer, or ballast), try viewing the noise with the scope line-triggered. If the noise becomes a stable wave form, the noise is synchronized to the power line and the suspicion has been confirmed. If the noise is not line related, and the conductor can not be moved for proximity testing, try monitoring the noise with one channel of an oscilloscope and sniff for the possible noise sources with a second channel using a loop of wire attached to the probe. Inverting and adding the second channel to the first will then cancel out the common signals. If the noise being sniffed is causing the noise in the affected conductor, the noise level should drop when the sniffer probe is near the source of the noise.

Note:	If the noise level is not reduced, try adding the two channels without inverting the second channel. The polarity of the signal from the pickup loop may already be inverted depending on the orientation of the loop.

The solution to minimizing magnetic coupling is simply to minimize the magnetic field strength impingeing on the second conductor. Several options are available to accomplish this:

1. Route high current noisy conductors in their own separate bundle, away from sensitive wiring.
2. Route sensitive wiring away from magnetic noise sources, (i.e., motors, fluorescent lamp ballasts, solenoids, and transformers).
3. Avoid using ferrous metal brackets for holding sensitive cabling, especially if the brackets are also in contact with sources of varying magnetic fields.
4. If rerouting of the wiring or circuitry is not an option, magnetic shielding (Mu Metal) can be used to create magnetic shielding to protect sensitive wiring and circuitry. While this method is effective, it may not be cost effective.
5. Use a transformer with a minimal external field, such as a toroidal transformer.

RADIATED NOIESE: ESD

Electrostatic discharge, or ESD, is one of the most destructive forms of radiated noise. ESD is literally the sudden transfer of a static charge from one body to another, either through an ionized air path or by direct contact. The voltages involved can be as low as 3-5 volts, or as high as 25,000-30,000 volts. While the human body can feel discharges of 5,000 volts or more, electronic circuitry can be damaged by a discharge of as little as 10 volts. Even if the discharge does not immediately result in the failure of the system, latent damage can produce a ‘Walking Wounded’ effect, allowing a circuit to continue to work until a minor stress causes a complete failure. ESD can also produce less drastic effects:

- corrupted memory
- glitches in peripherals
- unwanted program jumps

Unfortunately, the only way to test a design’s immunity to ESD is to subject the device to static shock and then test for any loss of function or performance.

Fortunately, there are a couple of precautions that can be taken in a design to protect against the potential damage of ESD. The first method is to provide alternate grounding paths that will channel the discharge energy into harmless ground paths. ESD always chooses the easiest path to ground, so channeling the energy is simply a matter of providing an easier path to discharge. Typically, this channel is in the form of a heavy braid or grounded chrome feature, near any exposed or vulnerable connections (buttons, displays, or connectors). The second method is to provide a resistive load into which the energy can be dissipated, such as:

- Spark arresters
- Transorbs
- MOVs
- Series resistors

During the discharge event, the resistive load absorbs the energy of the discharge and dissipates it as heat. Under normal operation, the protection device is dormant, presenting a load only when the high voltages of a discharge are present.

RADIATED NOISE: RFI

Radio Frequency Interference, or RFI, is noise generated by one circuit which interferes with the operation of another circuit. For the purpose of this Application Note, we will concentrate on how to deal with the susceptibility of a circuit to RFI. Suitable texts covering the elimination of RFI generated by a design are readily available and can provide a much more in-depth coverage of the subject.

A circuit may be said to be susceptible to RFI if its operation or performance is changed in the presence of a radio frequency signal. Circuits that exhibit susceptibility to RFI are typically sensitive to only a certain range of frequencies and not the entire electromagnetic spectrum. Determining the frequency ranges to which a circuit is sensitive is the first step in correcting RFI susceptibility.

Testing for RFI susceptibility is typically performed in an 'anechoic' chamber. An 'anechoic' chamber is a sealed room lined with RF absorbent Ferrite tiles. Once the device is placed in the room, the device is subjected to RF energy swept in both frequency and power level, and the device is monitored for abnormal behavior. If any abnormality occurs, the frequency and the severity of the behavior is noted for analysis following the test.

Note:	The chamber has two purposes, 1: ensure that the RF energies bombarding the device are only those being generated for the test, and 2: the absorbent tiles limit reflections which could cause peaks and nulls in the RF field, skewing the test results.

Once the RFI susceptible frequencies have been identified, correcting the problem becomes a fairly straightforward matter:

1. Determine the portion of the circuit susceptible to the RFI energy.
2. Identify the correlation between the RFI frequency and the affected elements in the circuit. Some of the ways a circuit can be susceptible are the following:
   - The length of a wire or trace is near a multiple of ¼ the RFI wavelength, creating a resonant frequency antenna.
   - One or more of the dimensions of the enclose is an exact multiple of ¼ the RFI wavelength creating a resonant cavity.
   - A parasitic inductance and capacitance within the circuit form a resonate circuit at the RFI frequency.
   - A transistor or IC amplifier within the circuit has gain at the RFI frequency.
   - An unshielded optical detector within the circuit is susceptible to the RFI frequency.
3. Once the correlation is identified:
   - Shield the susceptible circuit elements.
   - De-tune the resonating elements to a frequency at which the circuit is immune or has no gain.
   - Decrease the Q of the resonating elements by introducing a loss resistor into the resonate circuit.
   - Prevent the entry of the RFI by adding shielding and/or filtering on the external connections.

Selective shielding of sensitive components with a conductive cover can significantly reduce a circuits susceptibility to RFI. Photo etched brass shields are inexpensive, wave solderable, and can be ordered to custom specifications for a small NRE charge. Plastic connectors can be ordered with built-in shielding. Often, components with a particular sensitivity are available with the option of a built-in shielding as well. Some plastics can even be cast with a carbon content that renders the plastic semi-conductive.

Another method for combating RFI involves the filtering of the all long run conductors using Ferrite beads. Ferrite materials are effective over different ranges of frequencies, depending on the mixture of the material. A designer can use this aspect of a beads performance to increase the impedance of the line over a range of frequencies. In addition, a shorted secondary can be added to 'short out' the noise over the effective frequency range of the material. Finally, Ferrite beads can be used in conjunction with the input and output parasitic capacitances of IC's to form low-pass LC filters which filter out the RFI.

A third method for controlling RFI involves introducing losses in the resonant circuit susceptible to RFI. This can be accomplished by:

- inserting low to medium value resistance in series with long traces
- terminating long traces in a series RC
- adding blocks of resistive foam in cavities susceptible to RFI

These methods provide a resistive loss which dissipates the RF energy before it can build to disruptive levels.

An often overlooked method for improving RFI immunity in a design is to reduce the amount of RF energy generated within the cabinet by other unintentional radiators in the design. Often, RFI will mix with other frequencies already present in a design, producing beat frequencies that can cause interference and hide the source of the problem. RFI can be generated by impedance mismatches between a high speed driver and its receiver, or by fast rise time drivers. The following options can remove the heterodyning frequency and alleviate the RFI susceptibility:

- Limiting the rise time of high speed outputs within the circuit to reduce the amount of RFI generated within the design.
- Matching source and load impedances on high speed signals to also reduce the amount of RFI radiated by the trace carrying the signal.

DESIGN GUIDE LINES

Design guidelines for noise reduction in mixed signal designs.

- Keep all Power and Ground traces short and wide to limit resistance and inductance of the leads.
- Use separate Power and Ground traces for sections of the design which use high power drives and low level signals. Also separate analog and digital functions.
- Connect all analog, digital, and power supply ground traces at only one location, as close to the power supply as possible.
- It is better to suppress or eliminate noise at its source, rather than rely on filtering to remove noise from sensitive circuits.
- Separate fast rise time signals from low level sensitive signals.
- Use bypass capacitors with a self-resonate frequency that is much greater than the highest noise frequency.
- Never rely on PSRR for noise rejection. Always use bypass capacitors.
- To cover a broad noise frequency spectrum, use multiple bypass capacitors in parallel.
- Keep leads between ICs and bypass capacitors short and wide.
- To prevent coupling between traces, do not cross traces or run for long length in parallel.
- Separate wiring with high current and power signals from wiring with low level signals.
- Keep wiring and sensitive circuitry away from high current/power magnetic components.
- Keep sensitive low level signal traces short and use Ferrite beads to limit susceptibility to RFI.
- Include ESD suppression circuitry on all inputs and outputs which will be externally accessible.
- Provide low resistance ground paths near all external controls and display.
- For high sensitivity circuits, use EMI/RFI shields to protect the circuit from stray noise.
- To prevent radiation from fast rise time signals, always terminate fast RT signals into their characteristic impedance.

PERIPHERAL PERFORMANCE SPECIFICATIONS

This section explores the performance of the new analog and digital peripherals, identifies key features, and presents general design guidelines for the PIC16C78X. Information concerning the exact address and bit configuration for each peripheral has been omitted here for clarity. For exact specifications, and the specific configuration for each peripheral, the designer is referred to the PIC16C781/782 Data Sheet. For a more complete explanation of the specifications, the designer is referred to the following Application Notes. All notes are available from Microchip's web page at www.microchip.com:

1. AN682 Using Single Supply Operational Amplifiers in Embedded Systems
2. AN685 Single Supply Temperature Sensing with Thermocouples
3. AN688 Layout Tips for 12-bit ADC Applications
4. AN693 Understanding ADC Performance Specifications
5. AN699 Anti-Aliasing, Analog Filters for Data Acquisition Systems
6. AN700 Implementing an ADC Using a Member of the PIC16C6XX Family of Microcontrollers
7. AN722 Operational Amplifier Topologies and DC Specifications
8. AN723 Operational Amplifier AC Specifications and Applications

It is recommended that the designer read and understand these documents before continuing with the following sections. The documents provide explanations and background information important to the understanding the concepts discussed.

OPERATIONAL AMPLIFIER

One of the most versatile analog peripherals in the PIC16C78X is the Operational Amplifier module (OPA). The inverting and non-inverting pins are available on RA0 and RA1, with the amplifier output on RB3. Together, the three terminals comprise all the standard connections for an operational amplifier (op amp).

In addition to the three terminals of the device, additional controls, available through the module's peripheral registers, allow the designer to:

- minimize the input offset voltage
- control the amplifier Gain Bandwidth Product
- configure the amplifier as a voltage comparator

The following sections contain an overview of the amplifier's performance specifications and control options.

COMMON MODE VOLTAGE

The first parameters to be discussed concerning the performance of the operational amplifier are the input Common mode voltage range and the output voltage swing. Common mode voltage is defined as the range of input voltages that the op amp can accept at its inputs and still comply with its performance specifications. For the op amp in the PIC16C78X, the Common mode voltage is 0V to V_{DD}-1.4V. For a 5V_{DC} system, this would make the range 0V to 3.6V. While the range is somewhat restricted, it is important to note that both the input and output Common mode voltages include V_{SS} (ground). Including ground in the Common mode range is particularly important for compatibility with ground referenced sensors.

Like the Input Common Mode Voltage specification, the Output Voltage Swing specification determines the minimum and maximum output voltages that can be driven by the op amp. However, there are two important notes concerning this specification:

1. The output swing is affected by load, therefore the Output Voltage Swing is always specified driving a specified load. Sourcing or sinking higher currents will reduce the output swing, and lower currents will increase the swing.
2. The linearity of the amplifier is not guaranteed to the full Output Voltage Swing. Full Power Bandwidth should be used for determination of the maximum linear output swing for a given frequency signal.

The Common mode range also limits the input and output range of the op amp to positive voltages only. While most amplifier configurations assume a differential supply, modifications for single-ended supplies are not difficult and a number of reference texts are available which cover the required design techniques. More information concerning amplifier design from a single supply is available in the section covering sensor amplifier applications of the operational amplifier in Application Note AN682.

GAIN BANDWIDTH PRODUCT

The next operational amplifier performance specification to be discussed is the Gain Bandwidth Product, or GBWP. All Voltage mode op amps are designed with a low pass filter function integrated into their design to stabilize their operation in feedback amplifier configurations. The low pass generally has a corner frequency between 0.1 and 200 Hz, and rolls off the gain of the op amp at a rate of 20 dB per decade of frequency. GBWP is defined as the frequency at which the internal low pass function decreases the open loop gain of the amplifier to unity.

In design, the effect of GBWP is the loss of feedback gain with frequency, resulting in a gradual increase in the DC error of the output as the frequency of a signal increases.

The op amp in the PIC16C78X family of microcontrollers has the option of two GBWP settings: 30 kHz (typ) or 3 MHz (typ). The reason for two GBWP settings is related to current consumption; the 30 kHz setting draws less current than the standard 3 MHz setting. The 30 kHz setting is typically used in applications that have a need for low power consumption at the expense of speed. For example, slow speed sensors like temperature, humidity, or ion chambers in smoke detectors operating from battery power could use the 30 kHz setting. The 3 MHz GBWP setting is more common and is typically the choice for faster filter and control applications.

SLEW RATE AND FULL POWER BANDWIDTH

Another important performance parameter is Slew Rate, and its alternate representation, Full Power Bandwidth (FPBW). Slew rate is defined as the maximum output voltage change over a specific time, typically measured in V/µs. FPBW is another form of slew rate defined as the maximum frequency the output can be driven over its full output range without distortion. FPBW and slew rate are related by Equation 2:

EQUATION 2: FULL POWER BAND BANDWIDTH AND SLEW RATE EQUATION

$$FPBW = \frac{Slew\ Rate}{2\pi(V_{OMAX})^*}$$

$^*V_{OMAX}$ = *Maximum output voltage swing without significant distortion*

In design, Slew Rate represents the limiting factor in an amplifier's ability to track pulse and step function inputs. FPBW translates slew rate into terms of frequency to define the ability of the amplifier to faithfully reproduce the incoming sine wave over the output voltage range. Both GBWP and FPBW are important parameters to consider in the design of amplifier circuits that are expected to operate near the high frequency limit of the operational amplifier.

Due to the GBWP setting control of the amplifier's gain, the GBWP setting will also affect Slew Rate and FPBW of the amplifier. Operating the amplifier with a GBWP of 30 kHz will result in a corresponding reduction in the Slew Rate and FPBW of the amplifier. To determine the effect upon the Slew Rate and FPBW due to the GBWP setting, the designer is referred to the Specifications section of the Data Sheet for graphs outlining the affect of GBWP setting on Slew Rate and FPBW.

Note:	At lower frequencies, FPBW is limited by the output swing of the amplifier. At higher frequencies, FPBW is dictated by the amplifier slew rate (see Equation 2).

INPUT OFFSET VOLTAGE

Input offset voltage is defined as a DC offset error between the amplifier inputs. Typically, input offset error is due to minor differences in the transistor pair at the inputs to the amplifier. In older discrete op amps, a pin was made available for connecting a trim resistor for offset voltage adjustment. Newer microcontroller applications handle the problem by mathematically calibrating out the offset. The drawback to manual adjustment is both the added cost of the manual operation/ calibration as well as the dependence of input offset voltage upon ambient temperature. Additional calibration time/cost of a single fixed adjustment calibration is of limited value.

The PIC16C78X has improved upon this process by making input offset voltage adjustment an automatic calibration function under control of the software. Upon demand by the software, the automatic calibration module will switch the op amp from its external connections to an internal test circuit. The module then calibrates the amplifier for minimum offset voltage while being driven by a Common mode voltage reference. The calibration module offers the option of performing the calibration with either a fixed 1.2V Common mode voltage, or with a programmable voltage supplied by the DAC. In addition, the microcontroller can monitor the ambient temperature using an external thermistor and, whenever a change in temperature is sufficiently large, recalibrate to minimize the offset voltage change with temperature.

The calibration process is initiated by setting the CAL bit in the CALCON register. If the process completes normally, the CAL bit will be cleared to indicate a successful calibration. If a problem occurs with calibration and it does not complete normally, the CALERR bit will set to indicate the error.

Note:	Designers must remember that the performance of the op amp is only warranted while the input Common mode voltages are observed. Attempting to calibrate the op amp module outside the specified Common mode voltage may result in calibration failure.

INPUT BIAS CURRENT / LEAKAGE CURRENT

The final parameter to discuss is the op amp's low leakage inputs, or as the specification is labeled in the DC Characteristics chart, Input Bias Current. Much of the confusion that exists over this specification is due to the misleading naming convention applied to these inputs, so a short explanation of the specifications and their meaning is in order. In discrete bipolar op amps, Input Bias Current did indeed specify the current flow required to bias the input transistors of the amplifier. In discrete CMOS op amps, however, Input Bias Current no longer specified a bias current since the input MOSFET transistors do not have a gate bias current. Instead, the specification was re-used to specify the leakage currents associated with ESD and offset voltage trim circuitry tied to the input pins. In the PIC16C78X op amp, the specification was widened to include the leakage currents of the other functions multiplexed onto the pin as well. In all three cases, Input Bias current specifies the current flow at the op amp inputs. The difference lies in the reason for the current flow. That is why the PIC16C78X Data Sheet will refer to the specification as both Input Bias Current, and Input Leakage Current. When discussing the performance of the op amp, Input Bias Current is used as standard terminology for op amps. When discussing the behavior of the pin in general, Leakage current is used for common terminology with other pin specifications. In either case, the current flow specified for the amplifier inputs has been minimized as much as possible in the design of the op amp.

In design, it is important to remember that, while the value of the current is small, (typically <50 nano-Amps), it can affect the performance of an amplifier that has mismatched large input impedances. An amplifier with an effective input impedance of 100K ohm on one port and zero (0) ohms on the other can suffer over 5 mV of offset due to the voltage generated in the input/feedback resistors in response to the input bias current. Large input impedances can also increase the noise voltage of the amplifier. If a large input resistance necessitates the use of large-valued resistors, the effects of input bias current can be minimized by insuring that the Thevenin input impedance presented to both the inverting and non-inverting inputs is equal. Driving the inputs with equal impedances generates offset voltages that are approximately equal and opposite, resulting in a cancellation at the output of the amplifier.

COMPARATOR MODE

One of the useful features of the op amp module is its ability to operate as a voltage comparator. Setting the CMPEN bit in the OPACON register converts the operation amplifier into a voltage comparator. While the comparator will not have a 4:1 multiplexer on its input nor a multiplexed reference, all three terminals of the comparator are available for use, just like the other two comparators in the PIC16C78X. Also, due to the output being multiplexed with port bit RB3, interrupt-on-change can be configured using the PORTB Interrupt-on-Change feature. In addition to interrupt, the other controls for the operational amplifier are also available. GBWP will change the response time of the comparator, similar to the speed control for comparators C1 and C2. The input offset calibration module is also available to trim the input offset of the comparator, just as it trims the offset voltage in the operational Amplifier mode.

One advantage to the Op Amp/Comparator is the ability to trim the comparator's input offset voltage. To trim the comparator's input offset voltage, the module must first be set into Amplifier mode for the calibration. Once calibration is complete, the module can be set back into Comparator mode and the comparator will retain the input offset trim. In fact, performing a calibration on the operation amplifier/comparator will yield a comparator with better input offset performance than the existing voltage comparators C1 and C2.

OPERATIONAL AMPLIFIER TIPS

- Keep all Common mode input voltage between V_{SS} and V_{DD}-1.4V.
- Program all I/O pins corresponding to operation amplifier terminals for analog operation using the ANSEL register. Bits 0,1,7 = 1.
- Use 30 kHz GBWP setting for minimal power supply current draw.
- For tight control of the input offset voltage, use an external Thermistor to measure ambient temperature. When the temperature shift is sufficient to move the input offset voltage out of the needed tolerance, recalibrate input offset voltage to minimize it's drift with temperature.
- Balancing the effective input impedance present at the inverting and non-inverting inputs can further minimize offset and noise voltages at the op amp output.
- To minimize input offset errors in Comparator mode, calibrate input offset voltage in operational Amplifier mode then switch to Comparator mode.
- To generate an interrupt using the Comparator mode of the operational amplifier, configure RB3 as a digital input and enable Interrupt-on-Change.

VOLTAGE COMPARATORS (C1 and C2)

The dual Voltage Comparator module is similar to the voltage Comparators available in other Microchip microcontrollers. However, the module's response time has been improved and the following new features have been added:

- Two response time options, normal and slow
- Both comparators have the option of external outputs
- Both comparators have output polarity control
- Both comparators have independent Interrupt-on-Change
- Comparator C2 has the option to synchronize it's output to the Timer1 clock
- Both comparator outputs are mirrored to a common register for simultaneous reading
- Each comparator incorporates an independent 4-to-1 input multiplexers

COMMON MODE VOLTAGE

Similar to the operation amplifier, the voltage comparator input Common mode voltage range is limited to the range (V_{SS}-0.7V) to (V_{DD}-1.4). As with the op amp, the operational specifications for the voltage comparators are only warranted for Common mode voltages within the specified voltage range. To monitor voltage greater than V_{DD}-1.4, the signal must be scaled by a voltage divider to shift the input voltage within the Common mode voltage limits (See Figure 5).

In this example, V_{IN} is scaled by the resistor divider R1, R2. The ratio of R1 and R2 is chosen to generate a voltage within the Common mode range when V_{IN} is at its maximum voltage.

For zero crossing detection, the VSS-0.7V limit is sufficiently negative for inputs clamped to VSS by an external diode. To scale large negative voltages into the Common mode range of the comparator, connecting a resistor divider to VDD instead of VSS can provide a positive offset to the signal, scaling and shifting the input into the Common mode voltage range of the comparator (See Figure 6).

FIGURE 5: VOLTAGE ABOVE VDD -1.4V

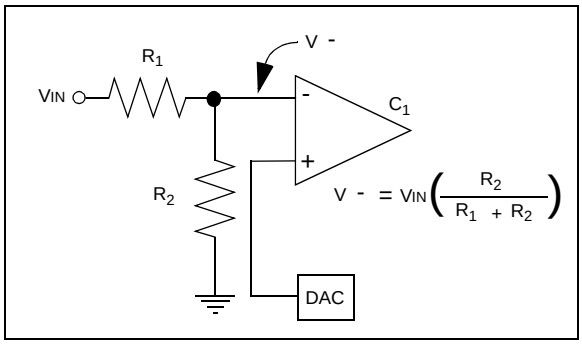
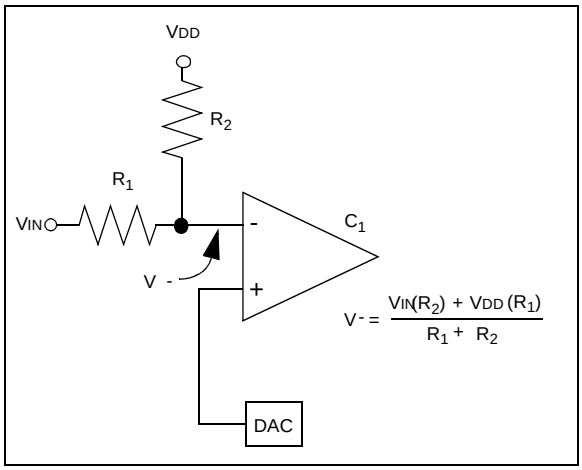


FIGURE 6: VOLTAGE BELOW VSS -0.7V



RESPONSE TIME

Similar to the GBWP option in the operational amplifier, two response time speed options are available for the voltage comparators. The normal speed option configures the comparators for the fastest response time of 75 nano-seconds typical. For lower current consumption, selecting the slow speed option configures the comparators for a response time of 5 micro-seconds typical.

COMPARATOR OUTPUTS

A new feature of the voltage comparator module is the ability to independently bring the comparator outputs to external pins. Port pins RB6 and RB7 can be configured individually as outputs for comparators C1 and C2, respectively. Both RB6 and RB7 have the capability to source and sink when configured as comparator outputs, as well as drive the full current capability of 25 mA typical.

Access to the comparator outputs allows the comparators to drive external circuitry, as well as provide feedback to their own inputs for designs using hysteresis, such as:

- Schmitt triggers
- Oscillators
- PWM generators

The comparator outputs are not synchronized to the system clock, although comparator C2 has the option to synchronize to the clock input to Timer1.

OUTPUT POLARITY

An additional feature of the voltage comparator is the ability to control the comparator output polarity. Control is via the separate configuration registers for each comparator. This feature is important for applications using the comparator output option and applications using the comparator as analog feedback for the PSMC.

An example application requiring flexibility in output polarity and comparators is a ‘window comparator.’ Both comparators share a common input, but use different reference voltages. A window comparator determines when a signal voltage is within a specified voltage range. It is convenient to be able to invert the polarity of one comparator such that the output state indicates a voltage within the window, and is common to both comparators. Control of the comparators output polarity allows the designer to specify a common logic sense for inside and outside indication.

When the comparators are used with the PSMC, the internal comparator output is used as a trigger to terminate or skip pulse outputs from the PSMC. In designs using a current Control mode topology, the control of output polarity is important because the comparator must be able to terminate the PSMC pulse correctly for either a high side or low side current sense. If the current sensor feedback voltage is positive-going, polarity is not a problem, because the sensor voltage will start out below the reference and rise with increasing current. Once the output exceeds the reference, the comparator output will go low, and the pulse will terminate. However, if the system uses a high side current sense, the feedback voltage may be negative-going, in which case, the sense voltage will start out above the reference and the output will have to be inverted. Having control of the output polarity alleviates this problem by allowing the designer to determine the state of the output.

TIMER1 CLOCK SYNCHRONIZATION

The new voltage comparator feature, unique to comparator C2, is the ability to synchronize the output of the comparator to the Timer1 clock. The output of comparator C2 is common to the same pin as the Timer1 gate enable input. The synchronization feature is designed to allow C2 to act as a control for the Timer1 gate input without creating a race condition on the clock input. Timer1 is configured to always clock on the rising edge of its clock signal. Synchronizing the output of C2 to the falling edge of the clock ensures the gate signal will always be stable prior to the active transition of the clock if C2 is used to generate the gate signal.

COMPARATOR TIPS

- To clear an Interrupt-on-Change generated by the comparator outputs, it is necessary to read the comparator output from the comparator configuration registers CM1CON0 or CM2CON0. Although both outputs are mirrored in CM2CON1, reading the CM2CON1 register will not clear the Interrupt-on-Change mismatch latch, which will regenerate the interrupt as soon as GIE is set.
- The bypass capacitor on the analog and digital V_{DD} should be a 0.1 µF ceramic capacitor. If either capacitor is missing or ineffective, the comparator output may oscillate when the comparator inputs are within 10 mV of each other due to feedback through the power supply.
- An internal connection between the DAC and the comparator allows the designer to create a programmable threshold comparator without an external connection to either reference. In addition, the DAC reference can be programmed for the VREF1 input, allowing the software to scale an external reference input to the comparators.
- The output bits present in the CM1CON0, CM2CON0, and CM2CON1 registers are synchronized to the internal microcontroller clock. The external outputs of the voltage comparators are asynchronous to the microcontroller clock.

VOLTAGE REFERENCE (VR)

Another useful module in the PIC16C78X microcontroller is the on-board voltage reference. The VR module provides a stable 3.072V reference voltage, and most of the analog modules within the PIC16C78X microcontroller have the option to use the VR module as their internal voltage reference. In addition, the VR module has the option to provide an output for external circuitry on pin RB0.

BANDGAP REFERENCE

The internal reference standard for the VR module is a stable bandgap reference circuit, which is enabled whenever the VR module, Brown-out Reset (BOR) circuit, or Programmable Low Voltage Detect (PLVD) module is selected. In all three cases, the bandgap reference will remain active so long as the module using the reference is enabled.

During the initial stabilization time following startup, the Bandgap reference may not be compliant with its specifications for accuracy and drift. To assist with the control of circuits that may use the reference, a stability flag BGST in the LVDCON register is provided to indicate when the reference has stabilized to within its specified performance level. Systems that rely on the stability of the reference voltage should monitor this flag and delay any critical measurements until after the flag is set, indicating the Bandgap reference has stabilized.

The electrical parameters that are important for any design utilizing the internal reference are:

- Bandgap startup time
- Temperature coefficient
- Load regulation
- Supply regulation

Bandgap startup time is defined as the warm-up time delay between enabling the Bandgap reference and the time when the reference has stabilized to within its specified accuracy. Temperature coefficient specifies the output voltage drift of the reference with changes in the ambient temperature. Load regulation specifies the output voltage shift in response to changes in the load present on the RB0 pin. And finally, supply regulation specifies output voltage shift with changes in the supply voltage.

BANDGAP STARTUP TIME

The time required for the Bandgap reference to stabilize is specified in the Data Sheet to be no more than 30 µs. However, determining the start of the stabilization time can be ambiguous due to the number of modules that can enable the VR module. The BOR, PLVD and VR modules can all enable the reference and, to complicate the issue, the BOR circuit is enabled through the configuration fuses (not software) so the module may already be enabled when the device comes out of RESET. To assist in determining the stability of the reference, a BGST flag has been included in the PLVD configuration register. This bit will be cleared until the Bandgap has stabilized, after which the bit will be set indicating that the reference has been enabled and has stabilized. It is recommended that any time the VR module is enabled, all peripherals refrain from using the VR module as a reference until the BGST bit is set.

OUTPUT VOLTAGE TEMPERATURE COEFFICIENT

The Output Voltage Temperature Coefficient is not specified for the Bandgap reference directly. Instead, the temperature coefficient is specified for the bandgap/VR module combination. This parameter is specified in parts per million per degree Centigrade (ppm/C). To determine the actual voltage change with temperature, Equation 3 can be used.

EQUATION 3: VOLTAGE CHANGE WITH TEMPERATURE

$$\Delta V_{OUT} = \frac{(\text{TEMP COEFF}) * (\Delta T) * (3.072V)}{10^6}$$

LOAD REGULATION

Load regulation is defined as the change in output voltage per milli-amp of current sourced by the VR module output. In practice, this means that the output voltage of the VR module will sag with load current. Typically the parameter is specified as milli-volts/milli-amp. To determine the specific output voltage for a specific load resistance on RB0, use equation 4:

EQUATION 4: LOAD RESISTANCE EQUATION

$$V_{OUT}[mV] = \frac{Load\ Reg * (3.072V)(1000)}{R_{LOAD}\ (OHMS)}$$

From Equation 4, it can be seen that the lower the load resistance on the RB0/VR pin, the greater the shift in the reference voltage output. Therefore, for high current loads, it is recommended that the RB0/VR output be buffered to prevent inaccuracies in the output voltage.

SUPPLY REGULATION

Supply regulation specifies the change in output voltage with changes in the microcontroller supply voltage. This parameter is specified in milli-volts/volt, so changes in power supply voltage on the order of volts will only have milli-volts of effect on the reference output. Typically, this value is 1 mV/V giving an output shift of less than 0.1% over the entire power supply range of the part (2.7V to 5.5V). For applications using 8-bit ADCs and DACs, this is less than ¼ of 1 LSb.

VOLTAGE REFERENCE TIPS

- The minimum resistive load that should be connected to the VR output without violating the load and current specifications of the module is 680 ohms.
- Using a resistive divider between the VR output and V_{SS} is a simple, inexpensive method for generating a virtual ground for single ended op amp circuits.
- When using a resistive divider to generate a virtual ground, the parallel combination of the resistor values should equal the Thevenin equivalent of the input and feedback resistances in the amplifier circuit.
- The internal and external VR module outputs that are isolated by a buffer amplifier internal to the part, so using the reference internally does not affect the output load regulation of the module.

DIGITAL-TO-ANALOG CONVERTER

A new peripheral in the PIC16C78X microcontrollers is the 8-bit Digital-to-Analog converter, or DAC. The DAC is a Voltage mode converter capable of a rail-to-rail output. Specifications for the DAC include parameters describing:

- Linearity
- Output drive capability
- Response to external signals input into the module's reference input

Configuration options include an external output on the RB1/V_{DAC} pin and reference voltage selection. For more information concerning programming of the DAC, please refer to the chapter covering the DAC in the PIC16C78X Data Sheet (DS41171). Available at www.microchip.com.

SLEW RATE AND SETTLING TIME

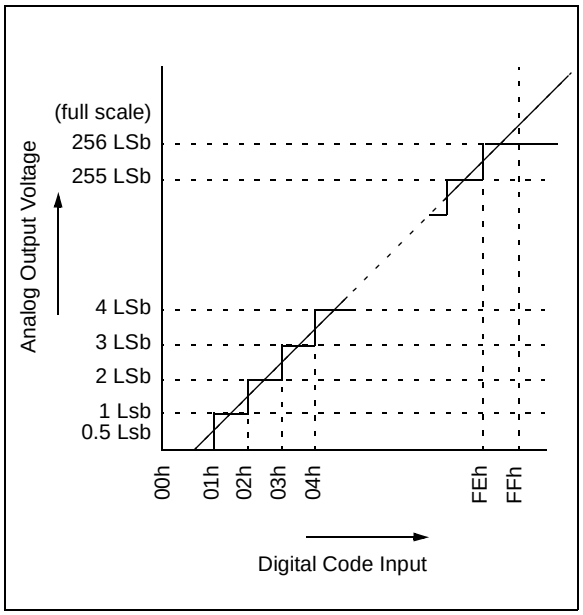
Two of the important parameters for the DAC are its output Slew Rate and settling time. Because the DAC can utilize an external voltage reference through the $V_{REF}1$ input, it has applications in scaling external signals for conversion in the ADC or level sensing using the voltage comparators. As a result, the ability of the DAC to accurately track an external signal is important to the overall accuracy of the ADC or comparator circuitry. Slew Rate specifies how fast the output can change voltage in response to a reference change, or a change in the DAC binary value, and is similar to the op amp slew rate specification. Settling time specifies the time for an output to settle the within ½ LSb of its final value. Together, they specify how long it takes the DAC output to transition from one voltage to another in response to a change.

ACCURACY/LINEARITY

The accuracy/error specified for the DAC module includes:

1. Integral non-linearity error (INL)
2. Differential non-linearity error (DNL)
3. Gain error
4. Offset error
5. Monotonicity

FIGURE 7: DAC TRANSFER FUNCTION



OFFSET ERROR measures the first actual output voltage transition of a code versus the first ideal transition of a code. Offset error is typically caused by offsets in the DAC output amplifier and results in a shift of the entire transfer function. Offset error can be calibrated out of the system by introducing an offset in a subsequent analog stage. Additional gain error can be introduced into a system through the interaction of the output drive capability, so the designer should be careful not to violate the output loading specifications of the DAC.

GAIN ERROR measures the maximum deviation of the last actual output voltage transition versus the last ideal transition, adjusted for offset error. This error appears as a change in slope for the transfer function. The difference between the gain error specification and the older full scale error is that full scale error did not take offset error into account. Gain error can also be calibrated out of the system by adjusting the reference voltage.

Linearity errors refer to the uniformity of the voltage change with a code change. They are a function of the R-2R resistor matching and cannot be calibrated out of the system by external adjustments.

INTEGRAL NON-LINEARITY ERROR is a measure of the actual voltage output versus the ideal voltage output, adjusted for gain error and is the worst case error for all codes.

DIFFERENTIAL NON-LINEARITY ERROR measures the maximum actual voltage step versus the ideal voltage step. As with Integral non-linearity, it is a function of the resistor matching and cannot be calibrated out of the system by external adjustments.

DAC TIPS

- If a sensor signal is input to the VREF1 input, the DAC is configured for the VREF1 as reference, and the ADC is configured to use the DAC as an input, the DAC can be used to scale the sensor output signal prior to conversion by the ADC.
- As a diagnostic for the ADC, configure the ADC and DAC to use the internal VR reference, configure the ADC for input from the DAC, and perform ADC conversions for incremental DAC values. If the ADC is operating correctly, the values should be within 1-2 counts over the 8-bit range.
- When using the DAC for scaling of an external voltage via VREF1, the resistive ladder allows scaling of input voltage down to VSS. Offset error will still apply, as it is due to the buffer amplifier and not the resistive network.

ANALOG-TO-DIGITAL CONVERTER

A standard peripheral in the Microchip microcontroller family is the 8-bit Analog-to-Digital converter, or ADC. The ADC in the PIC16C78X microcontroller is a standard 8-bit ADC with:

- 10 input multiplexer
- 4 input reference multiplexer
- 4 clock options

INPUT SELECTOR

The ADC input selector gives the ADC the option of 8 external inputs and 2 internal inputs. The 8 external inputs are available via the 8 analog I/O pins AN<7:0>. In most cases, the ADC inputs and other analog functions coexist independently on the analog I/O, allowing the ADC to perform conversions on the inputs and outputs of other analog functions. However, care must be taken due the capacitive loading of the ADC input. The op amp is particularly sensitive to conversions performed on its inverting and non-inverting inputs, due to potential instabilities caused by the increased capacitance.

The two additional internal inputs are connected to the DAC and VR signals internally for both diagnostic and compound functions. The internal connection of these two signals allows an internal verification of the ADC performance as a simple diagnostic. Using the DAC, the ADC can completely verify its operation by performing successive conversions on the DAC output as the DAC is stepped from 00h to FFh, validating all codes without requiring an external connection. Using the internal DAC input, a compound function can also be created using the DAC as a voltage scaling input for the ADC. This configuration allows the software to scale a sensor input for the greatest possible conversion resolution.

ANALOG I/O SELECTION

An important point to remember is that any pin used as an analog input should be configured for analog use via the ANSEL register. When analog voltages are present on the input to a digital input buffer, both the N and P channel devices in the buffer are driven into their linear region, causing partial conduction in both devices. When both devices conduct, an additional supply current is passed from V_{DD} to V_{SS}, increasing the current draw of the device. Therefore, it is recommended that any pin with a linear voltage present be configured for analog operation by setting (=1) the corresponding bit in the ANSEL register.

REFERENCE SELECTOR

The four reference voltage options available with ADC include the:

- Internal VR voltage reference
- AV_{DD} power supply voltage
- DAC output voltage
- External reference input $V_{REF}1$

The internal VR voltage reference supplies a cost effective, Bandgap stabilized, 3.072 voltage reference. AV_{DD} as a reference give the ADC it's maximum possible input range. The output of the DAC allows the designer to scale the ADC reference for the maximum resolution for each individual input. And finally, to allow for custom reference voltage, the ADC has the option to use an external reference input on $V_{REF}1$.

CLOCK OPTIONS

The ADC module has the option of 4 separate clocking options: three divided from the microcontroller clock, and one from an internal RC oscillator. The clock options allow the generation of the following conversion times, as shown in Table 2.

TABLE 2: CONVERSION TIME VS. MICROCONTROLLER CLOCK

Clock Option		Microcontroller Clock Frequency			
Option	**ADCS1: ADCS0**	**20 MHz**	**INTRC (4 MHz)**	**455 kHz**	**INTRC (37 kHz)**
$2T_{OSC}$	00	950 ns**(2)**	4.75 µs**(2)**	41.8 µs	514 ms**(3)**
$8T_{OSC}$	01	3.80 µs**(2)**	19 µs	167 µs	2.05 ms**(3)**
$32T_{OSC}$	10	15.2 µs	76 µs	668 µs**(3)**	8.22 ms**(3)**
RC	11	19 - 57 µs**(1,4)**	19 - 57 µs**(1,4)**	19 - 57 µs**(1,4)**	19 - 57 µs**(1,4)**

Legend: Shaded blocks are outside recommended range

1: The RC source has a typical conversion time of 38 µs.

2: These values violate the minimum required Tad time.

3: For faster conversion times, the selection of another clock source is recommended.

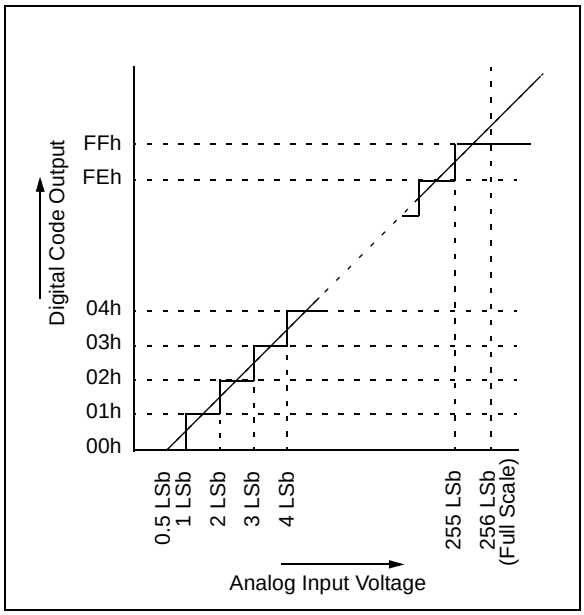
4: When device frequency is greater than 1 MHz, the RC ADC conversion clock source is recommended for SLEEP operation only.

ADC ACCURACY AND LINEARITY

The absolute accuracy (absolute error) specified for the ADC includes the sum of all contributions for:

- Offset error
- Gain error
- Quantization error
- Integral non-linearity error
- Differential non-linearity error
- Monotonicity

FIGURE 8: ADC TRANSFER FUNCTION



The **absolute error** is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the ADC is specified as < ± 1 LSb for ADCREF = VDD (over the device's specified operating range) (see Figure 8). However, the accuracy of the ADC degrades as VDD diverges from ADCREF.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. **Quantization error** is typically ± ½ LSb and is inherent in the analog-to-digital conversion process. The only way to reduce quantization error is to use an ADC with a greater resolution.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function and is due to offset error in the amplifiers of the ADC. Offset error can be calibrated out of a system through the induction of offsets in the preceding analog functions. Additional offset errors can be introduced into the system through the interaction of the input leakage current and source impedance at the analog input, so care should be taken in the design of the input circuitry.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in the slope of the transfer function. The difference between gain error and full scale error is that full scale error does not take offset error into account. Gain error can usually be calibrated out in software.

Linearity error refers to the uniformity of the code changes. The problem with linearity errors is the inability to calibrate them out of a system. **Integral Non-Linearity error** is a measure of the actual code transition versus the ideal code transition, adjusted by the gain error for each code. **Differential Non-Linearity** measures the maximum actual code width versus the ideal code width. This measure is not adjusted.

If the linearity errors are very large, the ADC may become **Non-Monotonic**. This occurs when the digital values for one or more input voltages are less than the value for the next lower input voltage step.

ACQUISITION TIME AND CONVERSION SPEED

For the ADC module to meet its specified accuracy, the internal Sample-and-Hold capacitor (CHOLD) must be allowed to charge to within ½ LSb of the voltage present on the input channel (see Analog Input Model in Figure 8). The analog source resistance (RS) and the internal sampling switch resistance (RSS) will directly affect the time required to charge CHOLD. In addition, RSS will vary over the power supply voltage range (AVDD), and RS will affect the input offset voltage at the analog input (due to pin leakage current). Therefore:

1. The maximum recommended impedance for any analog sources is 10 kOhms.
2. Following any change in the analog input channel selection, a minimum acquisition delay must be observed before another conversion can begin.

To calculate the minimum acquisition time, Equation 5 may be used. This equation calculates the acquisition time to within ½ LSb error, assuming an 8-bit conversion (512 steps for the PIC16C781/782 ADC). The ½ LSb error is the maximum error allowed for the ADC to meet its specified accuracy (see Example 1).

EQUATION 5: ADC MINIMUM CHARGING TIME

$$V_{HOLD} = (ADC_{REF} - (ADC_{REF}/512)) \cdot (1 - e^{-T_{CAP}/C_{HOLD}(R_{IC} + R_{SS} + R_S)})$$

Given: $V_{HOLD} = (ADC_{REF}/512)$, *for 1/2LSb resolution*

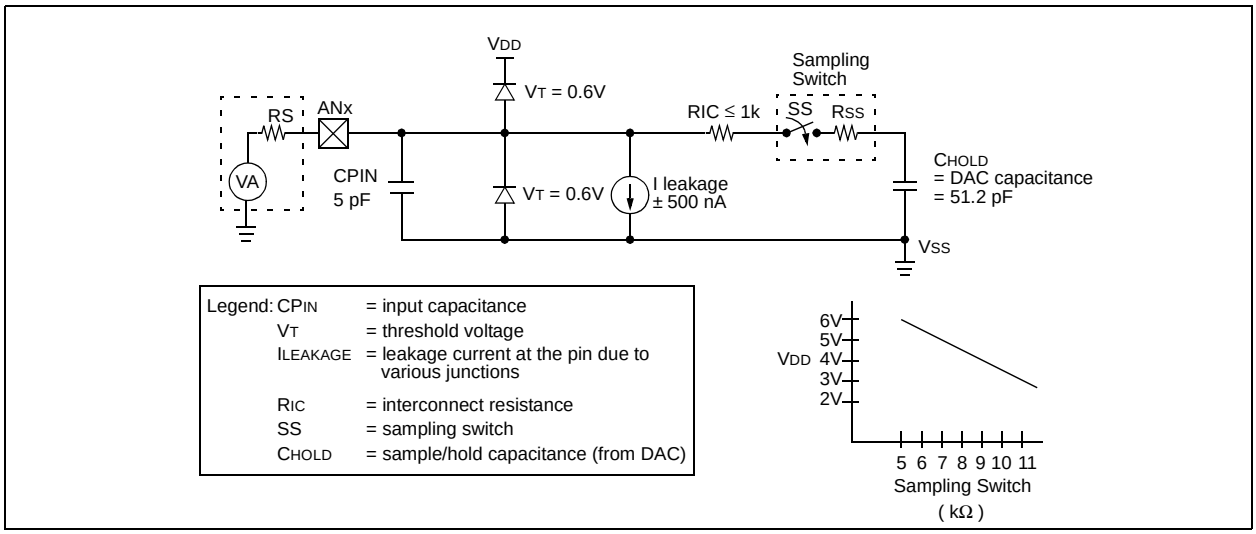
The above equation reduces to:

$$T_{CAP} = -(51.2\ pF)(1\ k\Omega + R_{SS} + R_S)\ Ln(1/511)$$

EXAMPLE 1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

TACQ = Amplifier Setting Time +
Holding Capacitor Charging Time +
Temperature Coefficient
TTACQ = 5 µs + TCAP + [(Temp - 25 °C)(0.05 µs/ °C)]
TCAP = -CHOLD (RIC + RSS + RS) In(1/511)
-51.2 pF (1 kΩ + 7kΩ + 10kΩ) In(0.0020)
-51.2 pF (18 kΩ) In(0.0020)
-0.921 µs (-6.2364)
5.747 µs
TACQ = 5 µs + 5.747 µs + [(50 °C -25 °C)(0.05µs/ °C)]
10.747 µs + 1.25 µs
11.997 µs

FIGURE 9: ANALOG INPUT MODEL



Example 1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions:

- CHOLD = 51.2 pF
- RS = 10 kΩ
- 1/2 LSb error
- VDD = 5V-> RSS = 7 kΩ

Note 1: The reference voltage (ADCREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10kΩ. This is required to meet the pin leakage specification.

ADC TIPS

- Care must be taken when using the AN6 pin in ADC conversions due to its close proximity to the OSC1 pin if the external oscillator is enabled.
- For current and noise reduction, the ADC can be configured to operate while the microcontroller is in SLEEP mode. The clock source for the ADC must be the ADC RC oscillator, because the microcontroller clock will be stopped during SLEEP.
- Acquisition time is affected by the impedance of the source driving the ADC input. Designers should review the previous section to insure sufficient acquisition time following the selection of a new analog channel.
- The ADC input uses a capacitive sample and hold on it's input channel as part of the conversion process. Care must be taken not to initiate a conversion on either the inverting or non-inverting channel of the op amp, as the added capacitance can cause instability in the feedback of the amplifier.

PROGRAMMABLE SWITCH MODE CONTROLLER

A new mixed signal peripheral in the PIC16C78X is the Programmable Switch Mode controller or PSMC. The primary purpose of the PSMC is to control the drive of external power systems using Pulse mode control. It can operate as either a Pulse Skipping Modulation or Pulse Width Modulation control. Its mixed signal nature is due to its ability to regulate the presence and/or width of the pulses in response to analog feedback via the comparator module.

There are several advantages to Pulse mode control:

1. Pulse mode control systems are very linear. The linearity of a Pulse mode system is dictated by the accuracy of the pulse timing rather than individual drive transistor linearity.
2. Pulse mode control systems are more power efficient. The power drive circuitry of Pulse mode systems operate in the saturation region of the transistors resulting in the absolute minimum power dissipation for the devices. The minimal loss in Pulse mode driver makes the Pulse mode control system one of the most efficient power control and transfer system topologies. Linear systems, on the other hand, operate their drivers in the linear region of the transistors, resulting in a much higher power dissipation and, as a result, a much lower efficiency.
3. Pulse mode power control systems can generate output voltages greater than, less than, and with the same or opposite polarity relative to their supply. Linear power control systems can only generate output voltages less than (and the same polarity as) their supply.

With the higher efficiency of Pulse mode controls and their reliance on timing rather than linear operation, the PSMC is an obvious control peripheral choice for any microcontroller-based power system.

PULSE MODE

The PSMC can generate either a Pulse Width Modulated (PWM) or Pulse Skip Modulated (PSM) output. Pulse Width Modulation varies the width of the output pulse based on analog feedback from the comparators. Pulse Skip Modulation controls the presence or absence of fixed width pulses based on feedback from the comparators (See Figure 10 and 12).

PWM

To configure the PSMC for PWM mode, three values must be set:

1. Pulse frequency
2. Minimum duty cycle
3. Maximum duty cycle

The pulse frequency is a function of the microcontrollers clock frequency and the prescaler selection in the PSMC. Equation 6 is used to determine the pulse frequency.

EQUATION 6: PULSE FREQUENCY EQUATION

$$F_{PULSE} = \frac{Fosc}{16 * prescaler}$$

Equation 6 can also be reversed to give microcontroller frequencies options for a desired pulse frequency using Equation 7:

EQUATION 7: DESIRED PULSE FREQUENCY

$$F_{OSC} = F_{PULSE} * 16 * PS$$

F_{OSC} is calculated for PS = 1, 2, 4, and 8

Using the prescaler and various oscillator frequencies for the microcontroller, pulse frequencies as low as 289 Hz can be generated using the internal 37 kHz oscillator, or as high as 1.25 MHz can be generated from a 20 MHz crystal.

The minimum and maximum duty cycle settings are application-specific and cannot be determined by a universal equation. The designer is therefore referred to the appropriate reference documentation for the type of design and topology to be used. The PSMC is capable of the following minimum and maximum duty cycle settings shown in Tables 2 and 3.

TABLE 2: MINIMUM DUTY CYCLE

Minimum Duty Cycle	MINDC<1:0>
0.0%	00
12.5%	01
25.0%	10
37.5%	11

TABLE 3: MAXIMUM DUTY CYCLE

Maximum Duty Cycle	MAXDC<1:0>
50.00%	00
62.5%	01
75.0%	10
93.75%	11

PULSE SKIP MODE (PSM)

To configure the PSMC for PWM mode, two values must be set:

1. Pulse frequency
2. Duty cycle

The pulse frequency is a function of the microcontrollers clock frequency and the prescaler selection in the PSMC. The equations outlined in the previous sections are the same for both PSM and PWM operation.

The duty cycle setting is a function of the drive topology, and as in the previous section, cannot be determined by a universal equation. The appropriate reference documentation for the type of design and topology are listed at the end of this Application Note. The PSMC is capable of the following fixed duty cycle settings shown in Table 4:

TABLE 4: FIXED DUTY CYCLE SETTINGS

Fixed Duty Cycle	DC<1:0>
12.50%	00
37.50%	01
62.50%	10
93.75%	11

SINGLE/DUAL FEEDBACK

To support a wide variety of topologies, the PSMC has the option to use either single or dual feedback from the comparator module. In single channel feedback, only comparator C1 is used as an input by the PSMC. The logic sense of the feed back is negative true, (i.e., if the output of the comparator goes low, then PSMC pulses are either terminated or skipped, depending upon the modulation used). In dual channel feedback, comparators C1 and C2 are used as sources of feedback by the PSMC. The logic sense for dual channel feedback is negative true OR, (i.e., if the output of comparator C1 OR C2 goes low, then PSMC pulses are either terminated or skipped, depending upon the modulation used).

SINGLE/DUAL OUTPUT

The PSMC also has the option of a Single or a Dual (alternating) output. In single Output mode, the PSMC generates pulses at the rated specified by the microcontroller oscillator and the prescaler selection on the PSMC1A output only. In the Single mode, pin RB7 is also available as a general purpose I/O.

In dual Output mode, pulses are generated alternately: first on pin RB7, then on RB6, then again on RB7 and so on. Each output produces pulses at ½ the calculated rate, with the combination of RB6 and RB7 generating the full frequency of pulse (see Figures 10, 11, and 12).

FIGURE 10: PSMC MODULE IN SINGLE OUTPUT PWM MODE

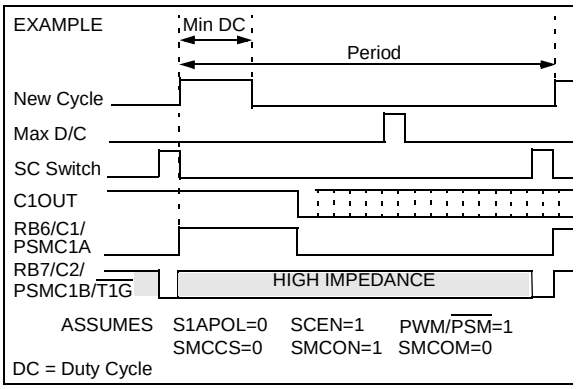


FIGURE 11: PSMC MODULE IN DUAL ALTERNATING OUTPUT PWM MODE

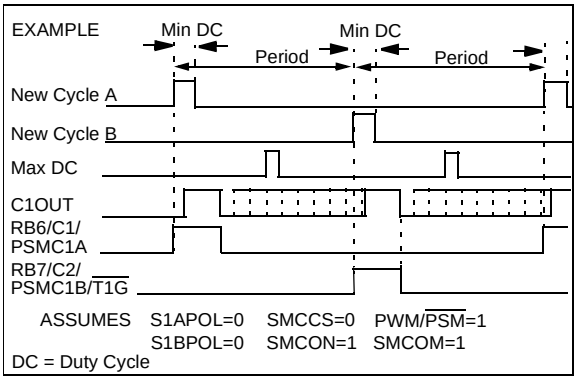
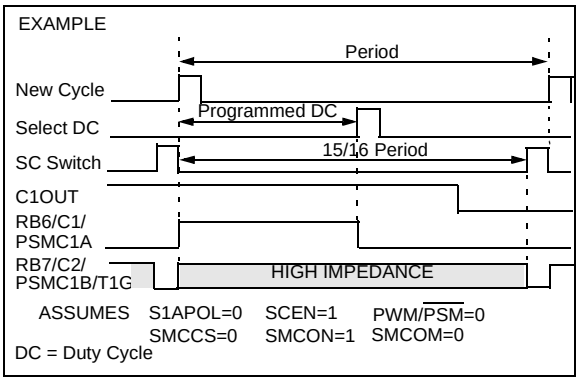


FIGURE 12: PSMC MODULE IN SINGLE OUTPUT PSM MODE

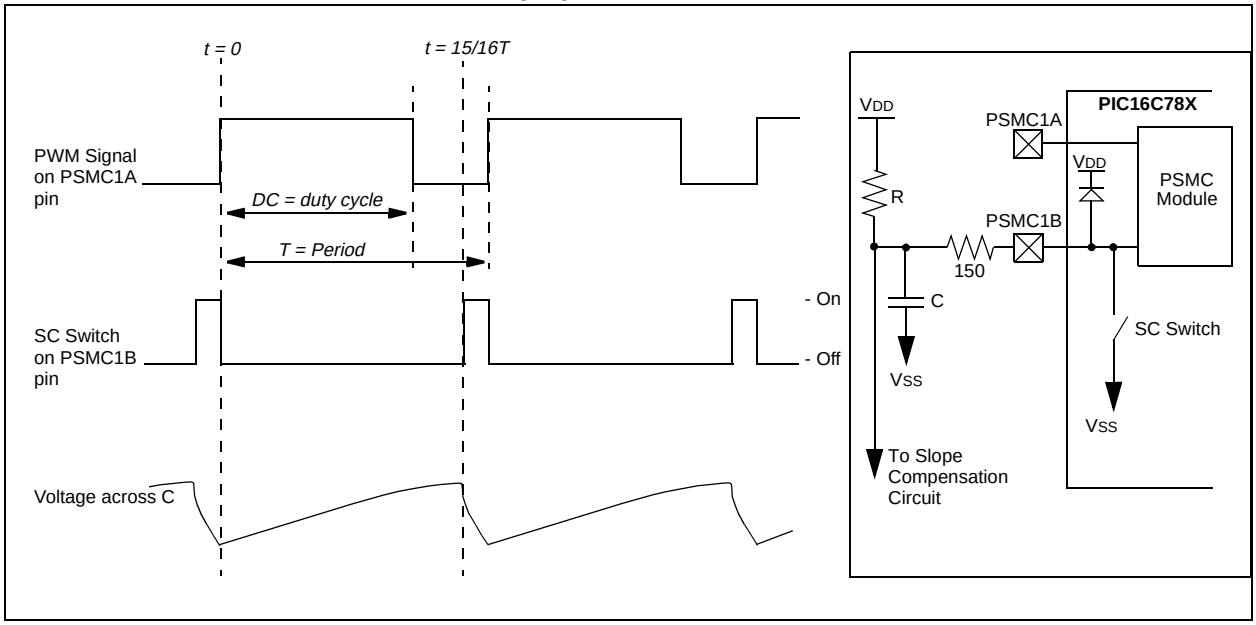


An additional output feature of the PSMC is the ability to control the polarity of each output individually. Whether operating in single or dual Output modes, the polarity of each output can be configured as either positive active or negative active. This feature alleviates the need for combination inverting and non-inverting MOSFET drivers. With individual polarity control, the software can configure the drive appropriately for either drive sense, or even opposite drive sense for each output. In fact, in some cases the output drive of RB6 and RB7 may be sufficient for direct drive of MOSFET transistors, in which case the ability to configure output polarity is a necessity.

SLOPE COMPENSATION OUTPUT

A final feature of the PSMC is the optional slope compensation output. The slope compensation output is an open drain drive which pulls the output low for the last 1/16th of every cycle. Its purpose is to generate a pseudo-ramp wave form which is used for slope compensation (see Figure 13).

FIGURE 13: SLOPE COMPENSATION (SC) SWITCH OPERATION



Slope compensation is a feature in switching power supplies which helps maintain stability when the output duty cycle exceeds 50%. When a switching power supply exceeds 50% duty cycle, it becomes susceptible to impulse noise from its supply side power source. The impulse noise can cause an exponentially increasing oscillation in the control loop that eventually leads to catastrophic failure. Slope compensation prevents this occurrence by generating a ramp function that is combined with the feedback, resulting in a reduction in the feedback level. The reduced feedback acts as a damper on the oscillation, quieting the response and restoring stability. For more information concerning how to implement slope compensation, please refer to the power supply design reference at the end of this Application Note.

The ramp waveform generated by the slope compensation output has another use. In Voltage mode power supplies, a ramp waveform is compared to a feedback error voltage. When the ramp voltage exceeds the error voltage, the output pulse is terminated and the inductor discharges into the output capacitor. For this mode to work, a ramp function is required that is synchronized to the pulse generator. The required ramp can be generated by the slope compensation output.

PSMC TIPS

- Whenever the PSMC is enabled in dual Output mode, the first pulse is always generated on the RB7 pin, then the RB6 pin.
- An important point to remember is that the TRISB register must be configured for RB6 and RB7 to be outputs if they are to operate as the pulse outputs of the PSMC. If bits 6 and 7 of TRISB are set, the pins will be configured as inputs and no pulse will be generated.
- If the PSMC is disabled, the outputs on RB6 and RB7 will return to the configuration of the next highest priority (comparator or digital output). Designers are cautioned to read Chapter 3 of the Data Sheet carefully concerning precedence of control for I/O port pins.
- During RESET, the outputs of the PSMC will be configured as inputs. It is important that any driver designs using RB6 and/or RB7 must default to an inactive state during RESET to prevent damage to the driver circuitry.
- One method of gating the pulse output of the PSMC in PWM mode is to program a minimum duty cycle of 0% and enable dual channel input, but enable only comparator C1. The polarity control of C2 will now operate as a software control, gating the output pulses on and off based on the state of the polarity bit.
- To improve the linearity of the ramp function generated by the slope compensation output, replace the pull-up resistor with a constant current source (See the Applications section concerning Op Amp designs).

ENHANCED TIMER 1

A modified original peripheral in the PIC16C78X is the enhanced Timer1 module. Timer1 operates in much the same way as it does in other microcontrollers, but with a few differences:

1. Timer1 does not have a separate oscillator. Instead, it can be configured to use the microcontrollers LP oscillator.

Note:	To use the LP oscillator, the microcontroller must be using the INTRC Oscillator mode, without CLKOUT

2. The Timer1 clock input has been moved to RA6 and is only available with Oscillator modes that do not use this pin (EC mode, INTRC w/o CLKOUT, or RC w/o CLKOUT).
3. A clock gate input has been added to pin RB7 which enables/disabled the clock input to the counter, following the prescaler. When the gating function is enabled, and the T1G is high, the counter is stopped. When the input is pulled low, the counter resumes counting.

TIMER1 OSCILLATOR

To minimize the number of functions multiplexed onto the microcontroller I/O pins, the normal Timer1 oscillator circuit has been replaced with a connection to the LP microcontroller oscillator. The LP oscillator has the same frequency capability as the original Timer1 oscillator, and like the Timer1 oscillator, the LP oscillator will continue to operate while the microcontroller is in SLEEP mode. In fact, when the LP oscillator is enabled via the Timer1 OSCEN bit, the oscillator will continue to run even if the timer itself is disabled. So oscillator startup time is not a factor in the timer accuracy.

Note:	When the LP Oscillator mode is enabled as a clock for the microcontroller, the oscillator halts oscillation during SLEEP mode.

TIMER1 CLOCK INPUT

The Timer1 external clock input has been multiplexed with the microcontroller I/O pin RA6. Among other functions, RA6 is also multiplexed with the microcontroller OSC2 and CLKOUT functions. Therefore, the T1CKI function is only available when the microcontroller is operating in one of three Oscillator modes:

- EC - external clock input
- INTRC w/o CLKOUT
- RC w/o CLKOUT

With the exception of the limit on availability, the T1CKI input is identical to the standard T1CKI input and is capable of operating to the full speed of the timer.

Note:	Operating the T1CKI input at speeds greater than the clock frequency of the microcontroller is not recommended due to timer synchronization problems. Please refer to the PIC16C78X Data Sheet for more information concerning this limitation.

TIMER1 GATE ENABLE

Timer1 has been enhanced with a new optional clock enable feature $\overline{T1G}$. $\overline{T1G}$ is an active low input, which when enabled, allows an external signal to gate the clock input to Timer1. The gate is located just before the Timer1 prescaler clock input. An active low on the input enables the prescaler and counter to increment on the rise edge of each clock. A high level input disables the Timer1 count and holds the prescaler/counter at their current values.

TIMER1 TIPS

- For proper operation, the $\overline{T1G}$ should be synchronized to the falling edge of the Timer1 clock.
- The $\overline{T1G}$ input can be used to measure the PSMC PWM output in switching power supply applications. The pulse width is proportional to the current supplied to the switching power supply output.

APPLICATIONS

The final section of this Application Note deals with applications for the individual/multiple peripherals by function. The purpose of this section is to provide the designer with possible application examples, not an in-depth tutorial in the design of a particular application. Further, the designs have been simplified to the minimum configuration to demonstrate the application. Where possible, references for further information are provided for supplemental design information.

SWITCHING POWER CONVERSION

The first potential area for applications of the PIC16C78X microcontroller is Switch mode power supplies. Switch mode power supplies or 'Switchers' are based on the concept of transferring energy in a switched inductive or capacitive element. The Switcher cycle begins by charging the transfer element, typically an inductor, with current. Next, the transfer element is switched to the load where the current charge flows into an output hold capacitor. The load then draws current from the output capacitor during the next charging cycle. The feedback loop is closed when the output voltage is compared against a reference, and the amount of charge in the next cycle is adjusted to compensate for any difference between the desired and actual output voltage.

Before diving into an explanation of the various switching power supply topologies, three basic concepts should be covered:

1. Voltage mode versus current mode control
2. Continuous versus discontinuous current operation
3. Proportional versus hysteresis feedback

All three concepts are common to almost all Switcher topologies, and a short explanation of each is useful in the discussion of the various switcher topologies.

VOLTAGE MODE

In Voltage mode control, a ramp waveform is used in combination with a feedback error signal to generate a PWM pulse. The PWM pulse is synchronized to the ramp waveform and goes active with the start of the ramp. The pulse stays active until the ramp voltage exceeds the feedback error signal, terminating the output pulse. The result is a pulse width proportional to the magnitude of the error signal voltage.

Figure 14 shows a block diagram of how a Voltage mode, proportional feedback controller can be implemented with the PSMC. The Slope Compensation output has an RC network attached to generate a pseudo ramp waveform at the input to the voltage comparator. The other input to the comparator is driven by an error amplifier which supplies an error voltage proportional to the difference between the desired voltage and the actual output voltage. At the start of the cycle, the PSMC initiates an output pulse. The ramping voltage from the slope compensation network continues until it exceeds the error voltage from the difference amplifier. When the ramp exceeds the error voltage, the PSMC ends the pulse and waits for the last 1/16th of the cycle. During the 1/16th of the cycle, the PSMC grounds the slope compensation output, which zeros the ramp for the next cycle and the pulse sequence starts over.

FIGURE 14: VOLTAGE MODE PROPORTIONAL FEEDBACK (PWM MODE ONLY)

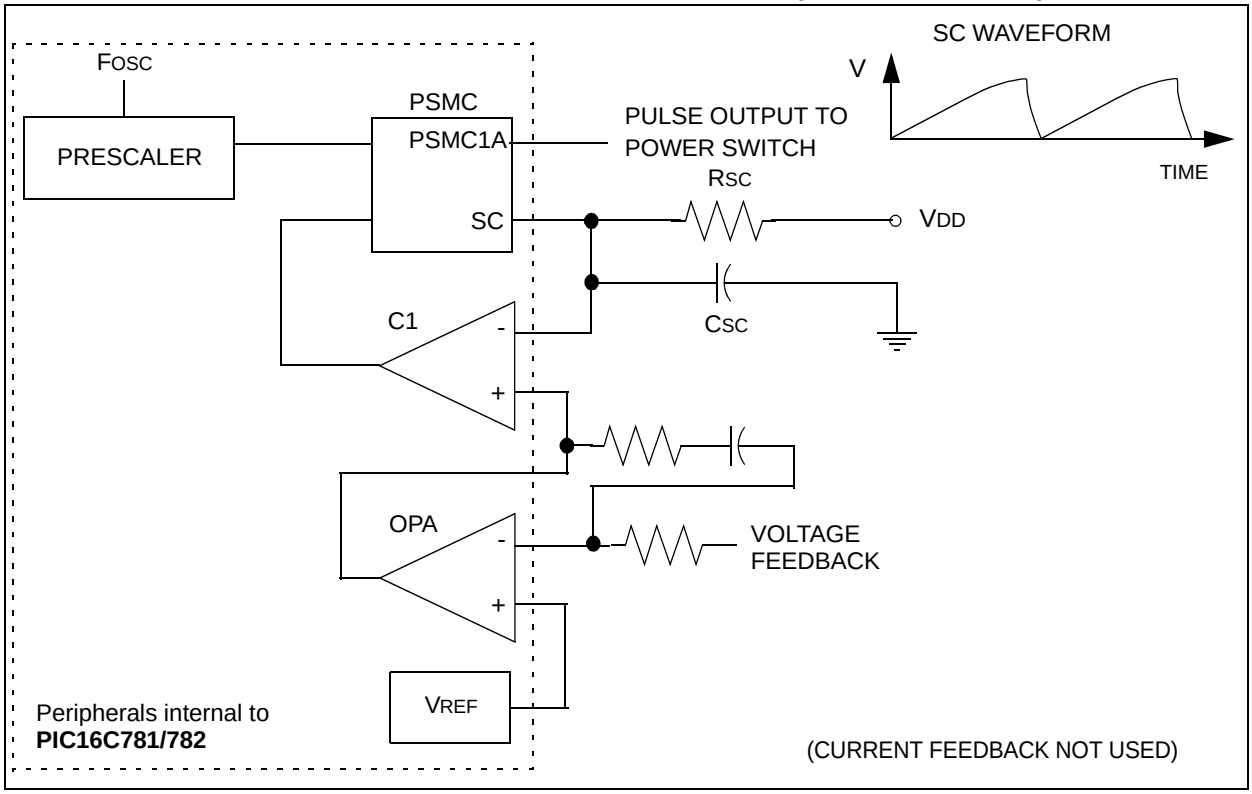


FIGURE 15: VOLTAGE MODE HYSTERESIS FEEDBACK (PSM MODE ONLY)

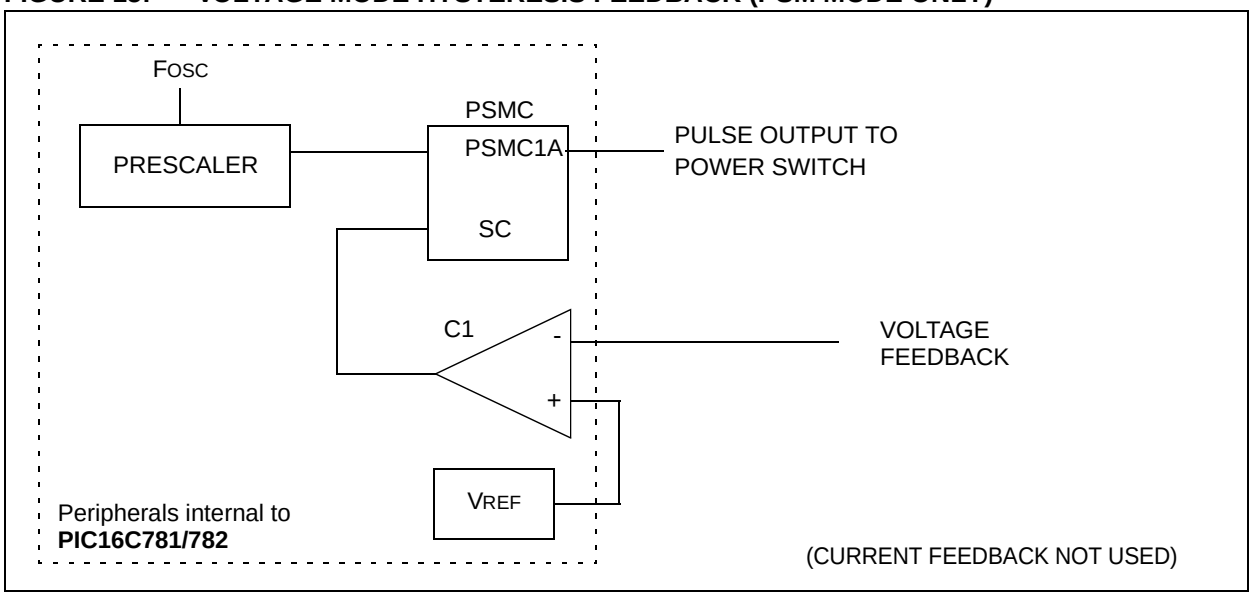


Figure 15 shows a block diagram of how a Voltage mode, hysteresis feedback controller can be implemented with the PSMC. The PSMC is set up to generate a fixed pulse output at the start of each cycle. Just prior to the initiation of the pulse, the PSMC tests the comparator feedback to determine if a pulse is required. If the feedback voltage is greater than the reference, no pulse is generated. If, however, the feedback voltage is lower than the reference, the PSMC generates the fixed pulse width until the feedback voltage is back above the reference.

Due to the simplicity of Voltage mode operation, topologies using Voltage mode control typically have fewer components and are somewhat easier to design. However, one of the main draw backs to Voltage mode is that it does not monitor the current flow in the inductor, which can result in a 'ratcheting up' of the magnetic

field in the inductor until the core saturates. When an inductor core saturates, its inductance drops, charge current significantly increases and the result is usually the spectacular failure of the MOSFET switching transistors.

CURRENT MODE

In Current mode control, a second inner control loop generates the PWM pulse width based on the error voltage and the current flow in the MOSFET/inductor. At the start of the cycle, a pulse is asserted by the PSMC. The current in the MOSFET/inductor is monitored, resulting in a ramp voltage proportional to the instantaneous current flowing in the pair. When the ramp voltage exceeds the error signal, the PSMC terminates the pulse. When the MOSFET turns off, the current flow in the inductor finds an alternate path through the diode, resulting in the charging of the output capacitor.

Figure 16 shows the block diagram of how a Current mode, proportional feedback control can be implemented using the PSMC. The voltage comparator and the PSMC form the inner current control loop. The PSMC initiates the pulse and the feedback voltage from the current flow monitor feeds back through the voltage comparator. When the current (voltage) exceeds the error voltage from the difference amplifier, the PSMC terminates the pulse and the PSMC waits for the start of the next pulse

FIGURE 16: CURRENT MODE PROPORTIONAL FEEDBACK (PWM MODE ONLY)

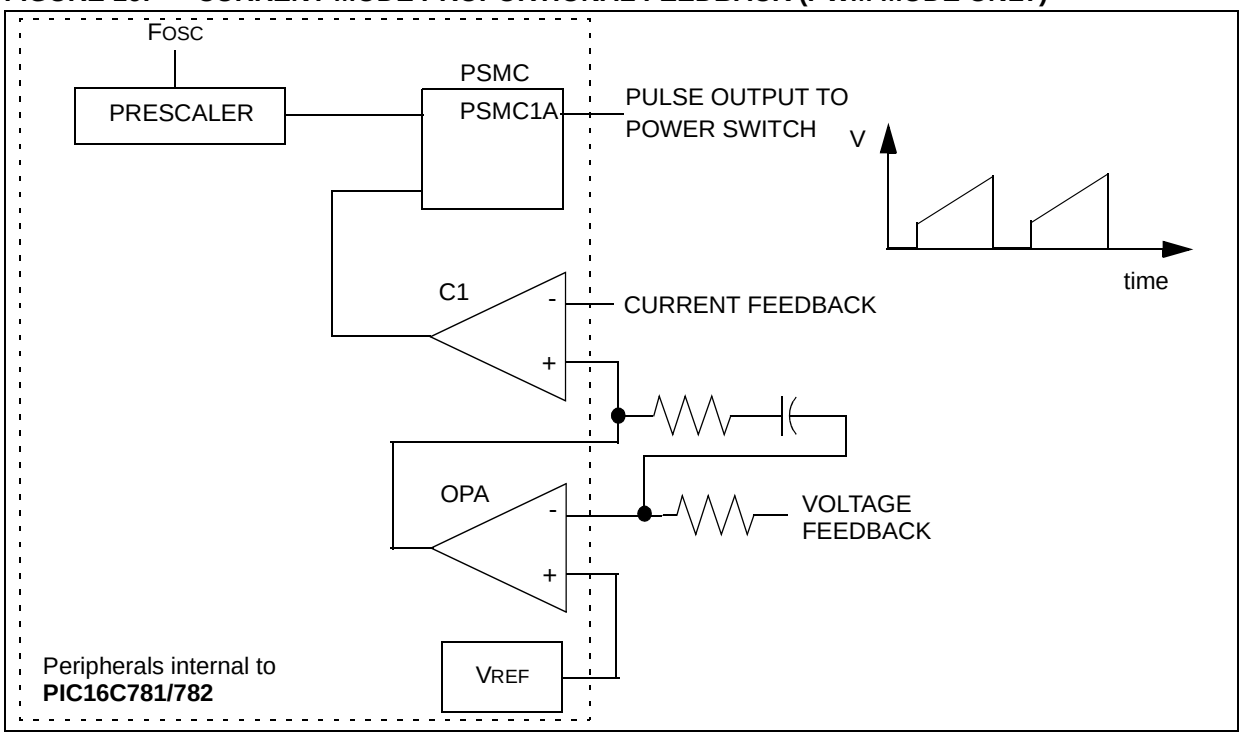
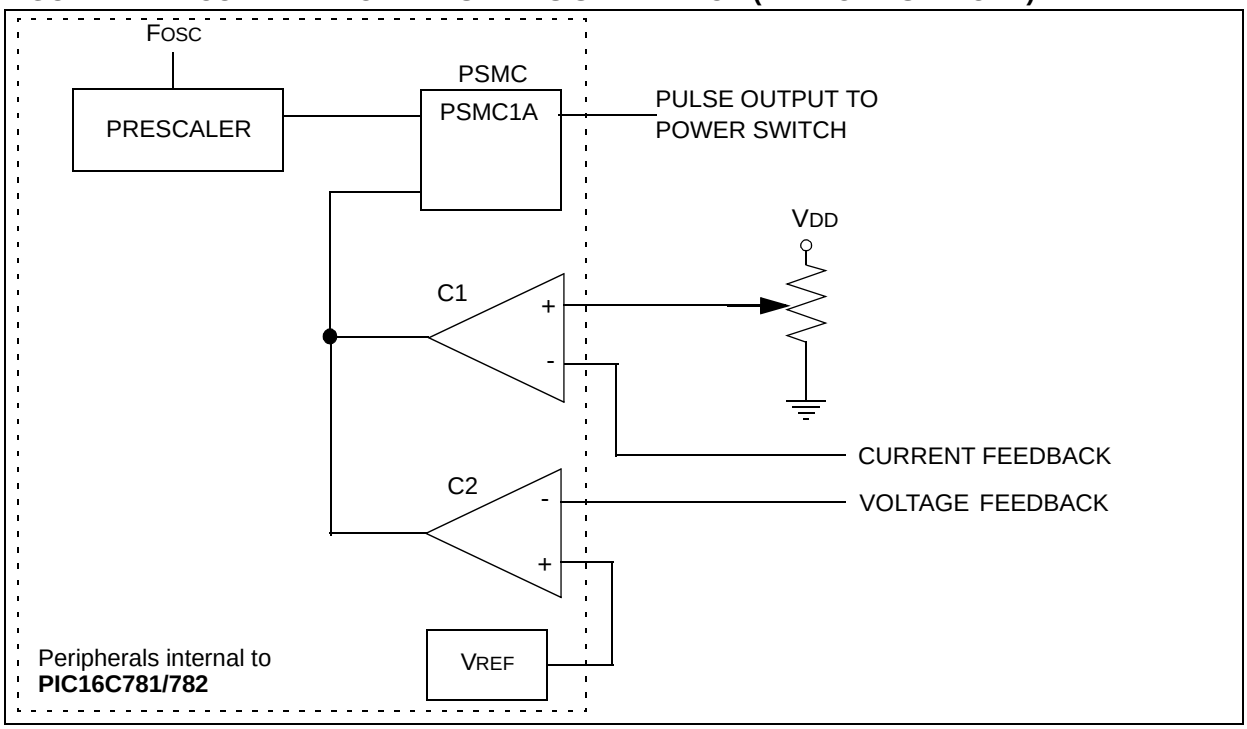


Figure 17 shows the block diagram of how a Current mode, hysteresis feedback control can be implemented using the PSMC. The voltage comparator C1 and the PSMC form the inner current control loop. If the output voltage is less than the reference, voltage comparator C2 is held high and the PSMC is enabled to initiate a pulse. Once the pulse is initiated, the feedback voltage from the current flow monitor feeds back through the voltage comparator. When the current (voltage) exceeds the voltage from the max current set point, the PSMC terminates the pulse and the PSMC waits for the start of the next pulse. If the output voltage is greater than the reference, voltage comparator C2 is held low and the PSMC is prevented from initiating the pulses.

FIGURE 17: CURRENT MODE HYSTERESIS FEEDBACK (PWM OR PSM MODE)



The main advantage to Current mode is that the ramp voltage generated from the current feedback includes any residual magnetic field (current flow) in the inductor. If any energy is left over from the previous cycle, the feedback voltage will start out at a higher level, resulting in a shortening of the charge pulse. As a result, the inductor cannot be charged beyond the level requested by the error signal, so the inductor cannot ratchet up to saturation.

Another advantage to Current mode control is that, with the inductor controlled by a loop, it is reduced to a simple current source in the feedback analysis of the system. Stability is now easier, since the feedback path has lost the phase shift from the inductor. The result is a system with greater phase margin and a simpler feedback filter.

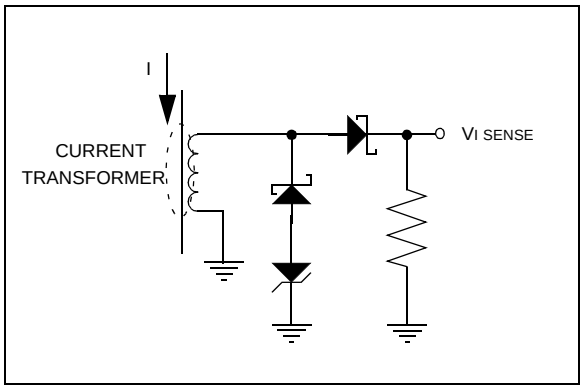
The main drawback to the current control system is that it is more complex, requiring a current monitor system in series with the inductor and the MOSFET switch. There are two typical methods for monitoring current:

- Resistive shunt
- Current transformer

The resistive shunt is a simpler, easier system to implement, but it does result in the loss of some of the transfer power as heat and the feedback voltage is typically low (100-500 millivolts). In addition, some topologies may put the shunt on the high side, making the translation of the voltage down within the Common mode voltage range of the comparator more difficult. Current transformers, on the other hand, do not have the heat problem of resistive shunts. They do not require an amplifier since the secondary winding can be wound to any ratio relative to the primary that is required, and they are isolated from the primary, so they can be ground-referenced without a problem. The only problem with current transformers is the need to include a clamp circuit to prevent ratcheting up of the core material to saturation.

Typically, the clamp circuit is composed of a fast switching diode in series with a Zener diode. During the discharge phase of the cycle, the energy stored in the current transformer is routed to the Zener diode by the fast switching diode (see Figure 18). Because the charge and discharge energies must be equal, discharging the current transformer's field into the Zener shortens the discharge time by the ratio of the sense voltage divided by the Zener voltage.

FIGURE 18: CLAMP CIRCUIT



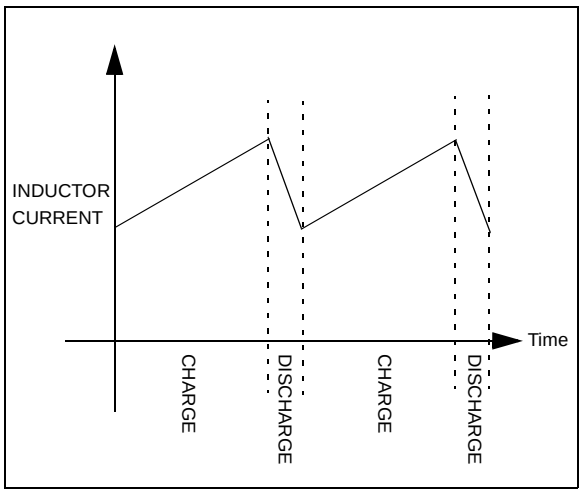
CONTINUOUS VS. DISCONTINUOUS CURRENT

Continuous versus discontinuous current operation specifies the behavior of the current flow in the inductor during the charge/discharge cycle of energy transfer. In Continuous mode, the current in the inductor does not go to zero at the end of the discharge cycle. In Discontinuous mode the current does go to zero. While this may sound like a small point, it does have ramifications on circuit design and performance (See Figure 19).

The performance of a continuous Current mode switcher is often superior to that of a Discontinuous mode circuit. Due to a continuous current flow in the inductor, a greater percentage of the load current is supplied by the inductor during the discharge phase of the cycle. Remember, if the inductor is not being charged, it is discharging into the output capacitors and the load. As a result, output filter capacitors will have to supply the load for a smaller percentage of the cycle, reducing their ripple current requirements. In addition, due to the longer discharge cycle, the peak inductor currents in continuous Current mode are lower, reducing the requirements on the inductor. The net result is that a Continuous mode supply has:

- Better output voltage regulation with load
- Lower output voltage ripple
- Smaller peak inductor currents

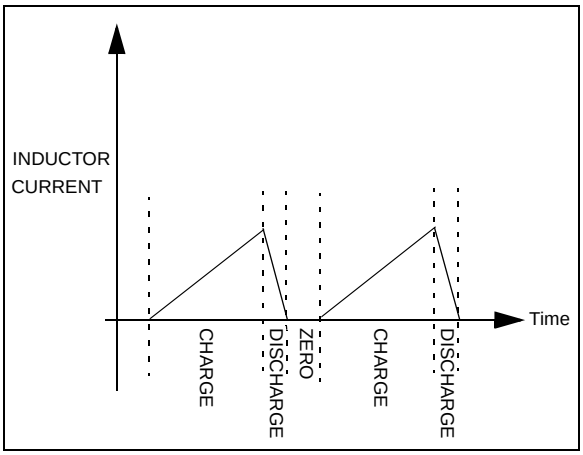
FIGURE 19: CONTINUOUS MODE



However, Continuous mode does have certain disadvantages. Continuous mode designs can handle only a specified range of load currents, and the minimum load current must be greater than zero. The minimum load is typically dictated by the minimum duty cycle the power supply controller can generate, since that dictates the minimum inductor charge current. When the current falls below the minimum current, the switcher goes discontinuous, the dynamic performance suffers and may become unstable. Continuous mode systems must also use proportional feedback to maintain continuous current operation, which is more complex and potentially unstable.

In discontinuous Current mode designs, the inductor current falls to zero at or before the end of the transfer cycle (See Figure 20). Discontinuous Current mode designs do not have a problem with zero current loads. By definition, they can operate with no current flowing in the inductor. It is just a matter of skipping charge pulses until the output voltage drops low enough to require another pulse. Many new battery-based switching systems use this capability to extend battery life by allowing a larger variation in the output voltage. The system charges the output capacitor, then goes to a minimum current SLEEP mode until the capacitor has discharged to a minimum operating voltage (at which point the controller wakes up and recharges the capacitor).

FIGURE 20: DISCONTINUOUS MODE



Another advantage to Discontinuous mode is the ease with which the loop can be stabilized. For basic stability, the only loop filter requirement is a simple low pass filter. Continuous mode controls typically require a more complex Proportional Integrator/Differentiator (PID) filter to maintain loop stability, due to the tighter control requirements to maintain continuous current flow.

The main drawback to Discontinuous mode, however, is that some cost/performance must be sacrificed. Because a greater percentage of load current must be stored for part of the cycle in the output capacitors, capacitors must have lower ESR ratings and larger capacitor values to minimize output sag under heavy loads. Also, because the peak current in the inductor is higher, the resulting output voltage ripple will be higher in discontinuous Current mode.

In the topology paragraphs to follow, six switching power supply configurations will be explored. For clarity and simplicity, it is assumed they are operating in discontinuous Current mode. The first four (Boost, Buck, Invert and Fly back) use an inductor as the transfer element. The last two (a Doubler and Inverter) use a capacitor as the transfer element.

PROPORTIONAL FEEDBACK

Figures 14 and 16 show typical proportional feedback systems using an op amp. The op amp is used to generate an error voltage based on the voltage difference between the actual output voltage and the reference voltage. The error signal is typically positive and proportional to the output voltage minus the reference. The error signal is used as a reference for the feedback comparator. Comparing the error signal and the ramp/current feedback allows the PSMC to generate the appropriate pulse widths required to make up any difference between the actual and desired output voltage. Using proportional feedback, ripple and noise performance are superior to hysteresis feedback with the only drawback being the requirement of an op amp to generate the error voltage and provide any needed feedback compensation required to maintain stability.

HYSTERESIS FEEDBACK

Figures 15 and 17 show typical Hysteresis feedback systems using a voltage comparator to gate the charge pulses generated by the PSMC. Feedback is achieved by comparing the output voltage to a fixed reference voltage. When the output voltage is greater than the reference, new charging pulses are disabled. However, when the output voltage falls below the reference, charging pulses are enabled and continue until the output capacitor is once again charged to a voltage greater than the reference. Hysteresis feedback is much simpler than proportional feed back, but overshoot and output regulation performance are poor due to the fixed charge pulse size.

SWITCHING POWER SUPPLY TOPOLOGIES

In the following paragraphs, six of the common switching power supply topologies will be examined:

- Boost
- Buck
- Invert
- Flyback
- Capacitive doubler
- Capacitive inverter

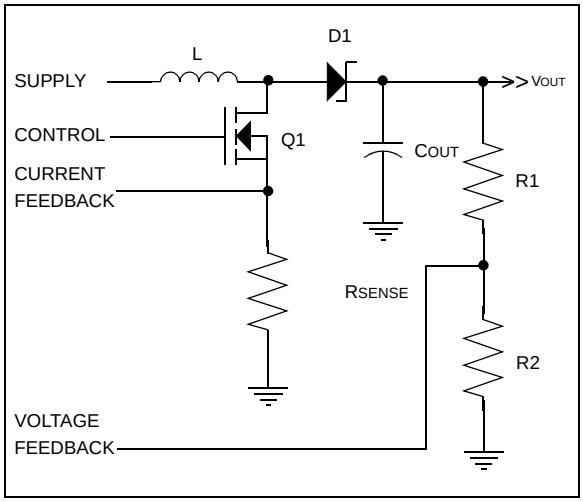
Each topology has its strengths and limitations based on how the energy is transferred from the source to the load. The purpose of these descriptions are to provide the designer with an overview of possible topologies, giving the designer a basic understanding of the operation of some of the more common switching power supply designs. For a more in-depth discussion of the design and operation of switching power supplies, the designer is referred to one of the numerous texts covering the subject of switching power supply design.

BOOST TOPOLOGY

Figure 21 shows a typical Boost topology. The Boost relies on the inductive kick of the inductor to generate an output voltage greater than the supply voltage. The energy transfer is initiated by the controller turning on Q1. Current builds in the inductor L until the controller terminates the pulse. When the controller turns Q1 off, the current flow in L looks for another path, resulting in a positive voltage large enough to forward bias D1. The current flows through D1 charging COUT, increasing the output voltage. The output is then sampled for feedback. This configuration has the potential for two feedback paths:

1. Feedback from RSENSE provides current feedback for Current mode controllers
2. Voltage feedback from the output VOUT, generated by R1 and R2

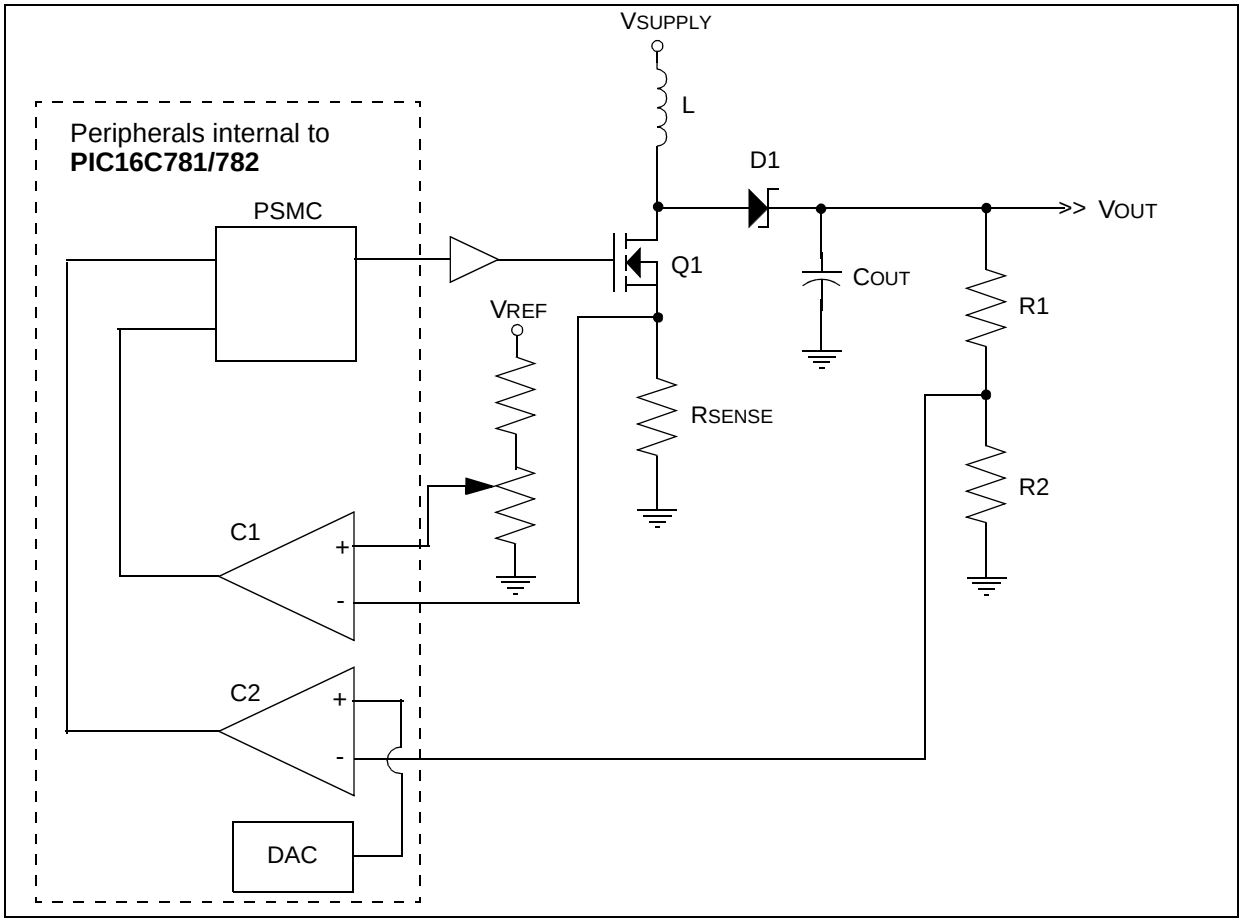
FIGURE 21: BOOST TOPOLOGY



BOOST CONFIGURATION, CURRENT MODE, PWM

Figure 22 shows an example of a boost configuration, Current mode, hysteresis feedback switching power supply using the PSMC. The PSMC generates the control for Q1, providing a PWM drive based on the current feedback from RSENSE. The output voltage feedback is connected to the second comparator for enabling and disabling the pulse generation based on the relative levels of the output voltage and the reference voltage supplied by the DAC. When the output voltage scaled by R1 and R2 is less than the DAC voltage, the PSMC generates current pulses using L and Q1, that in turn, charge COUT. When the scaled output voltage is equal or greater than the DAC voltage, current pulses are disabled and the output capacitor COUT provides current to the load. For this configuration to operate, the PSMC must be configured for PWM operation with a minimum duty cycle of 0%.

FIGURE 22: BOOST TOPOLOGY, CURRENT MODE, HYSTERESIS FEEDBACK



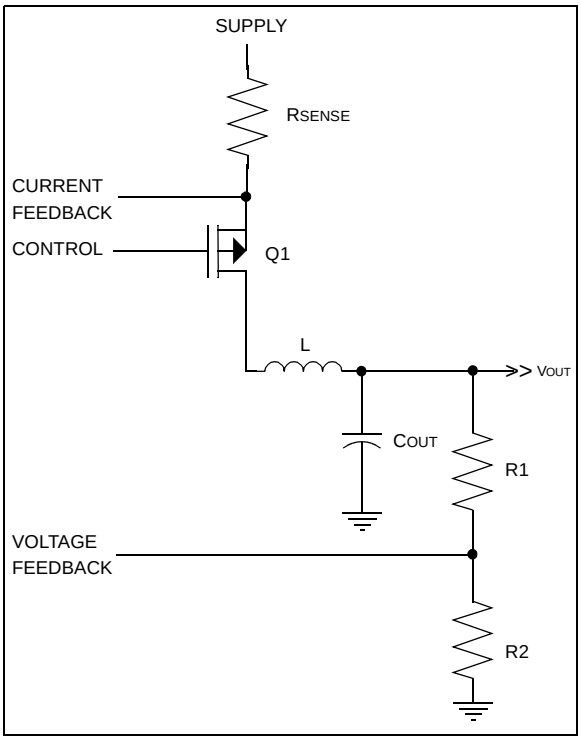
BUCK TOPOLOGY

Figure 23 shows a typical Buck topology. It relies on a duty cycle ratio to reduce the supply voltage to a lower output voltage. The energy transfer is initiated by the controller turning on Q1. Current begins to flow through the inductor into COUT. When the controller turns Q1 off, the current flow in L looks for another path, resulting in the forward bias of D1 as the MOSFET end of L goes to a negative voltage. This configuration has the same two potential feedback paths:

1. High side current sensing through RSENSE
2. Voltage feedback from the output VOUT, generated by R1 and R2

Note:	The high side current sense will require a difference amplifier to shift the current sense voltage comparator's Common mode voltage range.

FIGURE 23: BUCK TOPOLOGY



INVERTER TOPOLOGY

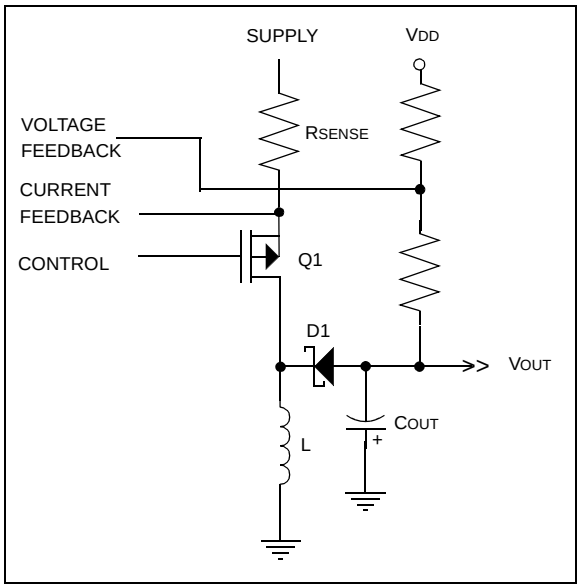
Figure 24 shows a typical inverter topology. The inverter relies on the inductive kick of the inductor to generate a negative output voltage. The energy transfer is initiated by the controller turning on Q1. The current builds in the inductor L until the controller terminates the pulse. When the controller turns Q1 off, the current flow in L looks for another path, resulting in a negative voltage which forward biases diode D1. The current flows out of COUT, charging it to a negative voltage. This configuration also has two potential feedback paths:

1. High side current sensing through RSENSE.
2. Feedback from the output VOUT, generated by R1 and R2.

Note 1: R2 is referenced from VDD, not VSS. This is done to generate a positive feedback voltage from the negative output voltage.

2: Due to the negative direction of charging for COUT, the polarity of either the comparator or the error amp must be reversed.

FIGURE 24: INVERTER TOPOLOGY

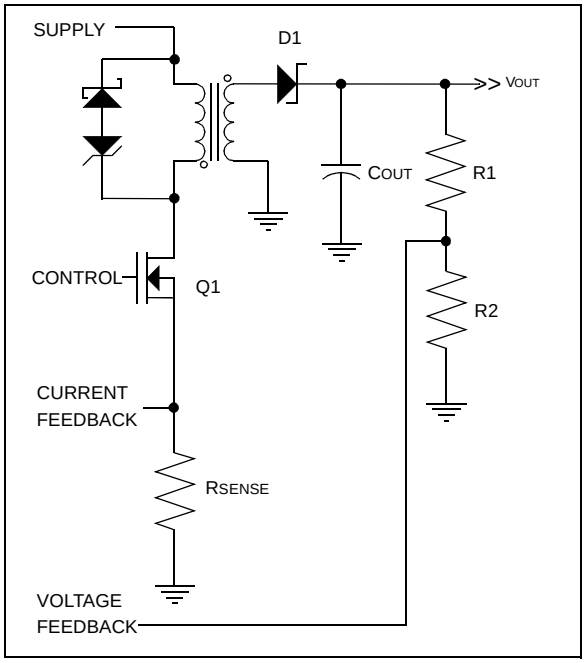


FLYBACK TOPOLOGY

Figure 25 shows a typical flyback topology. As with the boost topology, the flyback relies on the inductive kick of the inductor to generate an output voltage. The difference is that the flyback is designed to transfer the energy through the transformer to the secondary winding where the diode D1 is forward biased and the current charges COUT. Another difference with the flyback topology is that the output energy transfer is not ground referenced; therefore, the output voltage can be either greater than, less than, or negative relative to the supply voltage. As with the boost, this topology has two potential feedback paths:

1. The current sensed through RSENSE.
2. Output voltage feed back generated by R1 and R2.

FIGURE 25: FLYBACK TOPOLOGY



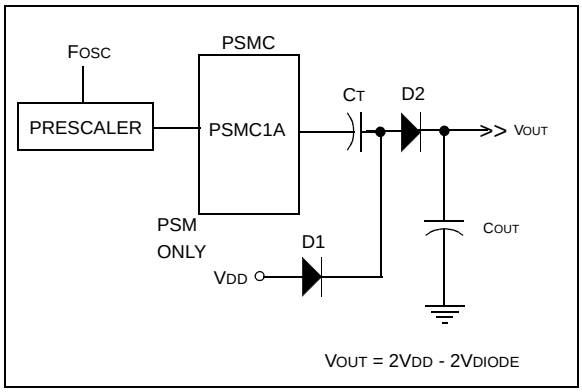
CAPACITIVE DOUBLER TOPOLOGY

Figure 26 shows a boost configuration switched capacitor power supply generating an output voltage double that of VDD. At the beginning of the cycle, the output of the PSMC is low, charging the transfer capacitor CT through D1. When the pulse is complete, the PSMC pulls its output high, raising the transfer capacitor to the VDD supply and turning off D1. The voltage between the positive terminal of CT and Vss is now nearly double the supply voltage. If the output voltage across COUT is less than double the supply voltage (minus a diode drop):

- diode D2 will forward bias
- the charge in CT and COUT will balance
- the output voltage across COUT increases

If the voltage across COUT is already near double the supply voltage, D2 remains unbiased, and the charge will remain in CT. This topology uses the PSMC as a fixed duty cycle pulse generator without any feedback. To force the PSMC to generate output pulses, it must be configured for a single feedback input. Voltage Comparator C1 must also be disabled with its output polarity inverted. This forces a logic high into the input of the PSMC, causing it to continuously generate pulses for the doubler.

FIGURE 26: SWITCHED CAPACITOR DOUBLER



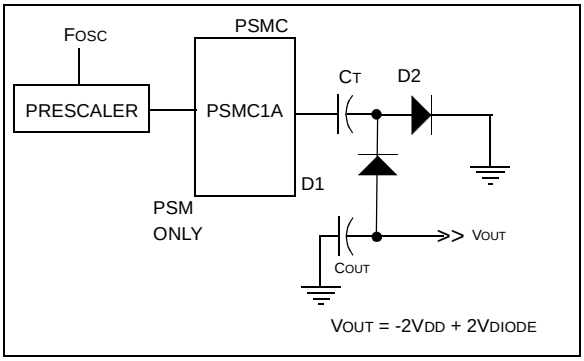
INVERTED CAPACITIVE DOUBLER

Figure 27 shows an inverting configuration of the switched capacitor power supply. This topology generates a negative output voltage equal and opposite to VDD. The PSMC charges the transfer capacitor CT when its output is high. Diode D1 is forward biased and the capacitor is charged to nearly the supply voltage. When the pulse is complete, the PSMC pulls its output low, pushing the transfer capacitor to ground and turning off D1. The voltage present at the negative terminal of CT is now the negative of the supply voltage. If the output voltage across COUT is less than the voltage across CT (minus a diode drop):

- diode D2 will forward bias
- the charge in CT and COUT will balance
- the negative voltage across COUT increases

If the voltage across COUT is already nearly the negative of the supply voltage, D2 will remain unbiased and the charge will remain in CT. This topology uses the PSMC as a fixed duty cycle pulse generator without any feedback. To force the PSMC to generate output pulses, it must be configured for a single feedback input and inverted output sense. Voltage comparator C1 must also be disabled with its output polarity inverted. This will force a logic high into the feedback input of the PSMC, causing it to generate pulses for the inverter.

FIGURE 27: SWITCH CAPACITOR INVERTER



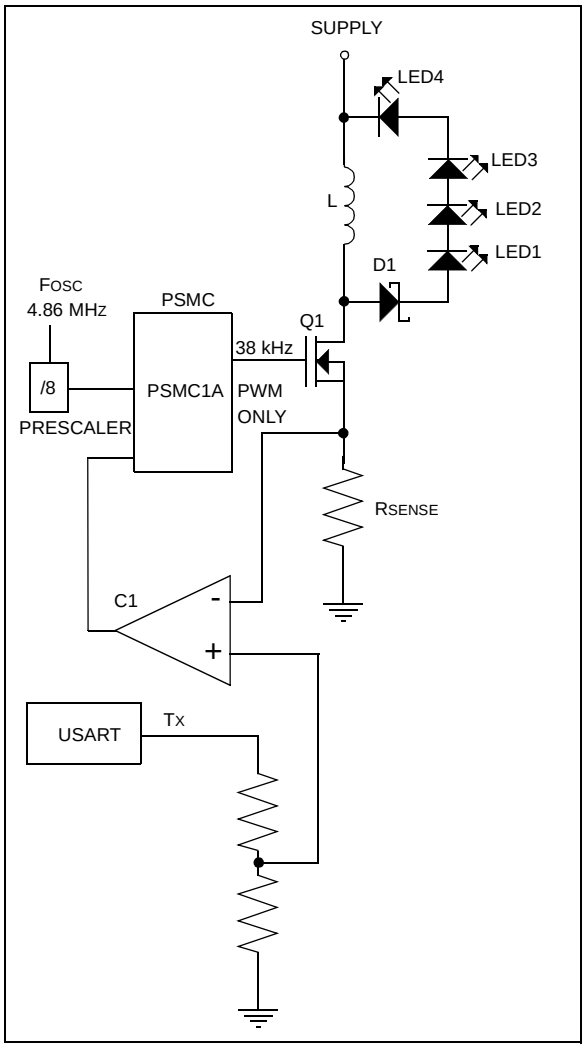
SWITCHED MODE POWER DRIVER APPLICATION

CONSTANT INTENSITY MODULATED IR LED DRIVER

Figure 28 shows an adaptation of the Boost configuration which drives a string of IR LEDs for optical data transmission. At the beginning of the cycle, the energy transfer is initiated by the PSMC turning on Q1. Current builds up in inductor L until the voltage feedback from the current sensor RSENSE exceeds the reference level from the DAC and the PSMC turns off Q1. The current flow in L1 must now find another conduction path, resulting in the forward bias of the freewheeling diode D1 and the IR LEDs. The energy in the inductor is then dissipated in the LEDs generating an IR light pulse. The PSMC then times out the pulse and restarts the charging pulse in the next cycle.

To achieve a standard pulse rate, the prescaler value and the microcontroller oscillator frequency are chosen such that the output pulse rate of the PSMC matches the desired pulse rate. Equation 8 can be used to calculate the possible microcontroller clock frequency options that will generate a desired pulse rate.

FIGURE 28: HI POWER IR LED DRIVER



EQUATION 8: CLOCK FREQUENCY/ PULSE RATE

$$F_{MICRO} = F_{PULSE} * 16 * PS$$

Where PS = 1, 2, 4, or 8 (pre-scaler value)

For example, to generate a pulse rate of 38 kHz, microcontroller clock frequencies of 608 kHz, 1.216 MHz, 2.432 MHz, and 4.864 MHz can be used.

Using this topology to drive the IR LED's has multiple advantages:

1. Because the current is transferred into the LEDs via the inductor, no power is lost in a linear current regulator for the LEDs.
2. Due to the Boost nature of the inductor, the accumulated forward voltage of the LED string can be greater than the supply voltage.
3. Using the DAC to control the current set point of the circuit means 38 kHz pulse rate can be AM modulated with a linear signal.
4. If comparator C2 is not used, the PSMC can be configured for dual comparator input and the polarity bit for C2 can be used to digitally key the output on/off.

FEEDBACK CONTROL

Another area for application of the PIC16C78X microcontroller is in feedback control systems.

Feedback systems control the output of some form of plant (motor, heater, etc.), by comparing the actual output against a reference and then adjusting its drive to compensate for any discrepancies. Using negative feedback, the system strives to push the plant such that the output is identical to the reference, much as the power systems in the previous section pushed the output voltage to match the internal voltage reference. Several factors affect the performance of feedback control systems. Typically, the most important factors are:

1. Loop gain: The feedback control must have sufficient gain to reduce any difference between the plants output and the reference to a minimal level without causing overshoot or instability problems.
2. Responsiveness: The system should respond quickly to changes in supply and load without falling into instability.
3. Settling Time: The system should smoothly adjust to changes in supply and load without overshoot and ringing.

STABILITY

Typically feedback controls incorporate one or more POLES and ZEROS in their response to:

- minimize errors
- smooth transitions
- maintain stability

Unfortunately, feedback control is unique in that variations in the plant, load, and supply all contribute to the dynamics of the system. Calculations concerning the frequency of the POLES and ZEROS in the feedback control are dependent upon the dynamics of the system, so it is not possible to provide a 'one size fits all solution' to feedback control. What can be done is to:

- supply an example
- point out a few of the pitfalls
- supply references for good texts which can prepare the designer for the necessary analysis and design required to maintain system stability

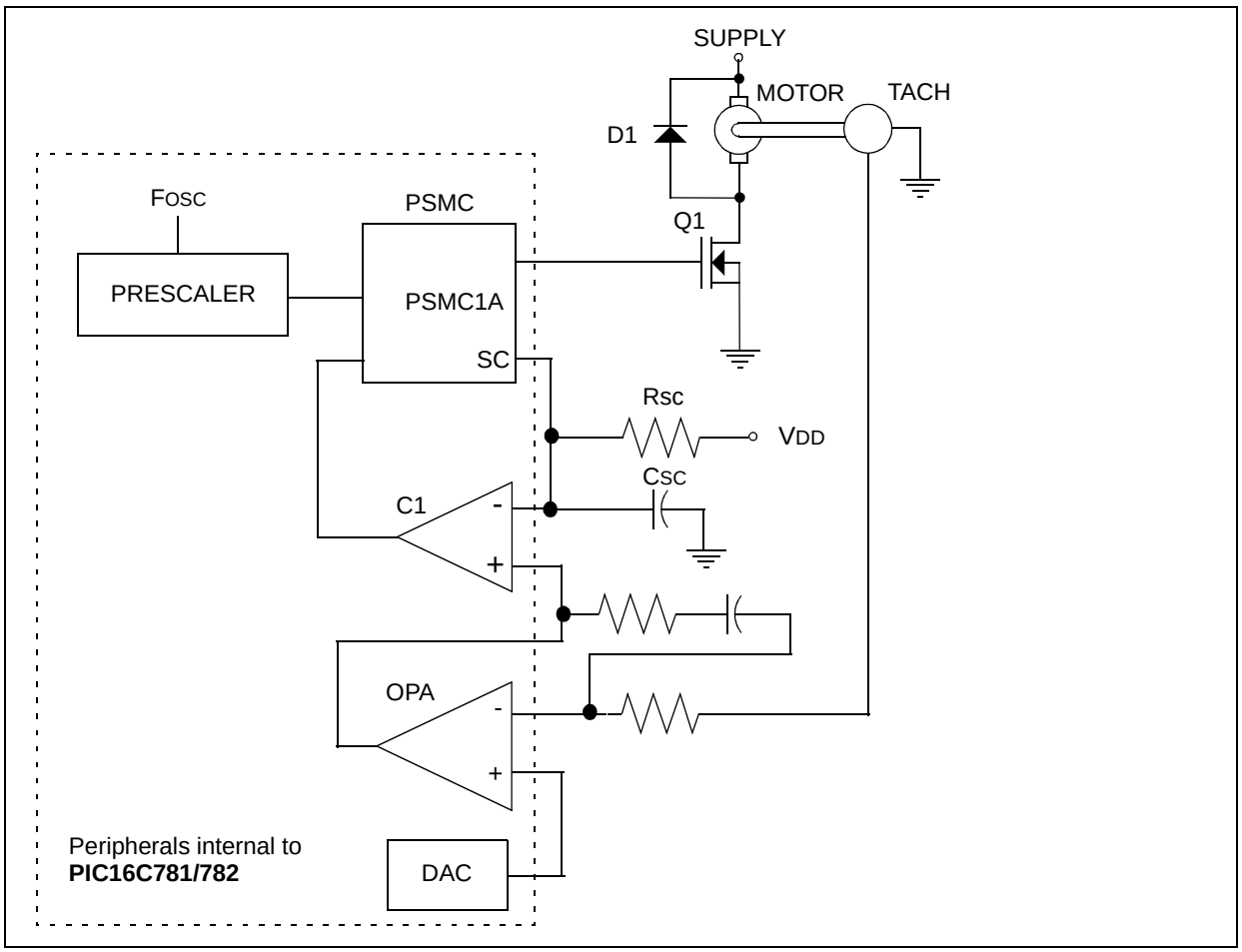
MOTOR SPEED CONTROL

Figure 29 shows an example of using the PIC16C78X as a feedback control for a motor speed control application. The combination of the PSMC, comparator, op amp, and DAC create a closed loop system for regulating the speed of the motor via PWM control of the power delivered to the motor. When the speed of the motor is less than the desired speed, the power delivered to the motor is increased and the motor speeds up. When the speed of the motor is greater than the desired speed, the power delivered is reduced and the motor coasts down.

The PSMC regulates the average power delivered to the motor through pulse width modulation, based on the speed feedback voltage from a tachometer. In the example, the PSMC uses its Slope Compensation output to generate a pseudo ramp waveform. At the start of the pulse cycle, the PSMC initiates a pulse and starts the ramp. As the ramp increases, the error voltage supplied by the op amp is compared with the ramp signal. While the ramp is less than the error signal, the output of the comparator remains high and the pulse continues. When the ramp is greater than the error signal, the comparator output goes low and the PSMC terminates the pulse.

The error signal which determines the duty cycle is generated by the op amp configured as a differential integrator. The integrator subtracts the feedback voltage generated by the tachometer from the reference voltage supplied by the DAC, and supplies the integrated difference to the PSMC comparator as a correction factor. As the motor nears the desired speed, the difference is reduced causing the PWM duty cycle to be reduced until the PWM output approaches zero. Once the motor is at the desired speed, the PSMC generates pulses as needed to overcome system losses and maintain the desired speed of the motor.

FIGURE 29: MOTOR SPEED CONTROL



In this system, an important facet of feedback control has been omitted for simplicity. Specifically, the phase/gain compensation network responsible for maintaining loop stability has been omitted. The compensation network is designed to provide frequency-dependent gain and phase correction for the feedback signals such that the total loop gain does not go through unity gain at a phase multiple of 360 degrees. If the loop does go to unity gain at 360 degrees, the system will oscillate at that frequency. The problem with designing feedback systems is determining what compensation is required for gain and phase to maintain stability without sacrificing response time. If too little energy is added to the system in response to a change in load, the system will be sluggish and slow to respond. If too much energy is added, the system can overshoot and ring. Striking the proper balance is not simple and is dependent upon how the system behaves in response to changes in power and load. Feedback controls must be analyzed and designed based on the complete system, including the load for the feedback, to provide stable, responsive, and smooth control.

Several techniques have been developed under the general topic of Control Theory for the analysis and modeling of feedback control systems. Root Locus, Bode Plots, and State space analysis are some of the more common, although State Space is generally accepted as the standard method in modern control theory. Unfortunately, covering even the basic concepts and techniques of control theory is beyond the scope of this document, so the designer is referred to one of the many good texts available on Control Theory.

SENSOR CONDITIONING

A third potential area for application of the PIC16C78X is in Sensor interface and conditioning. Sensor applications typically involve the conversion of some form of analog signal into a digital format for monitoring or control. Sensor applications may also involve the generation of signals, either as an excitation for the sensor, or as a carrier to be modulated by the sensor. Due to the breadth of sensors available and the variety of interfaces possible, this section will concentrate on the building blocks of sensors systems rather than complete interfaces. Examples of filters, amplifiers and converter topologies will be covered, in addition to ideas for a programmable attenuator, oscillator and PWM generator.

OPERATIONAL AMPLIFIER

Of all the analog peripherals in the PIC16C78X microcontroller, the op amp module is the most flexible. Simple resistive feedback networks can create a variety of amplifiers and converters.

Other resistor/capacitor combinations can create:

- integrators
- differentiators
- filters
- PID controllers

Its wide variety of applications make the op amp one of the most basic building blocks of sensor signal conditioning. The following sections explore some of the more common application blocks for the op amp module.

AMPLIFIER CONFIGURATIONS

The op amp module is primarily a general purpose amplifier. So it naturally follows that many of the building blocks possible with the op amp would also be amplifiers. Figures 30 through 34 show some of the common amplifier configurations using the op amp modules. Included in these figures are the design equations for choosing the gain-determining resistors.

Figure 30 shows a minimum component buffer amplifier. Feedback from the output to the inverting amplifier input drives the output to track the non-inverting input, forming a simple unity-gain amplifier. A common application for the buffer is the isolation of low drive sensor inputs, providing a high impedance load for the sensor, and a low impedance drive for any subsequent analog stages. Typically, the buffer is a good choice for isolating any signal which operates within the Common mode voltage of the amplifier. The frequency of the incoming signal should be checked against the GBWP and FPBW for the amplifier to insure the faithful reproduction of the signal.

FIGURE 30: BUFFER AMPLIFIER

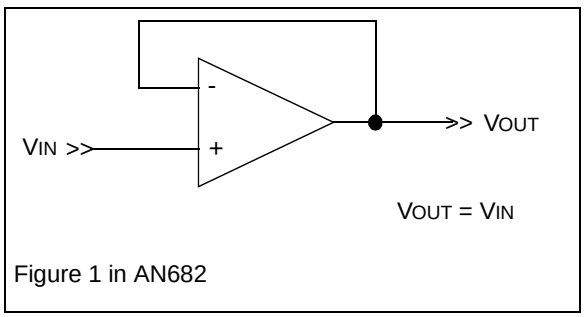


Figure 1 in AN682

Figure 31(A) shows the inverting amplifier configuration of the op amp. Resistors R1 and R2 create a feedback path around the amplifier that configure the gain for: VOUT/VIN = - R1/R2. The configuration is capable of either gain or attenuation based on the resistor choices in the feedback network. The configuration shown can accept negative inputs signals which will produce a positive output.

Figure 31(B) shows how to configure the amplifier for both negative and positive inputs, the ground reference connected to the non-inverting input is replaced with a virtual ground at some voltage above VSS and below VDD-1.4. When the amplifier is connected to the virtual ground, the design recognizes any input voltage below the virtual ground as a negative voltage and all outputs from the circuit are measured relative to the virtual ground.

FIGURE 31: INVERTING AMPLIFIER

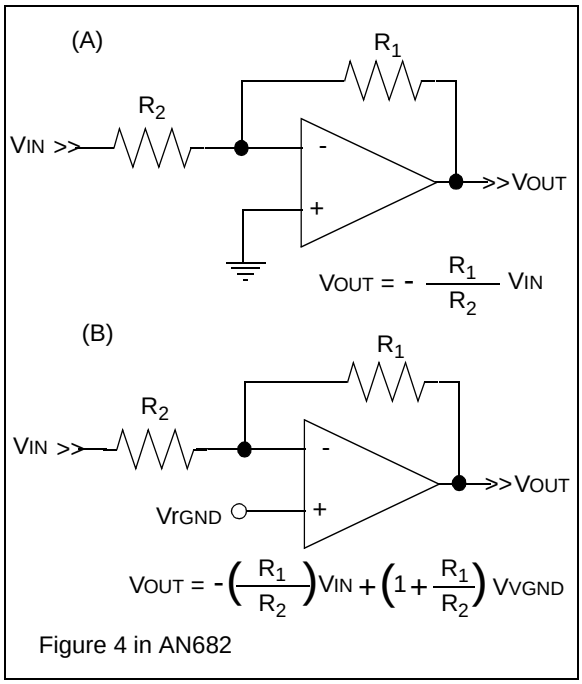


Figure 4 in AN682

Figure 32(A) shows the non-inverting amplifier configuration of the op amp. In this configuration, the gain of the circuit is 1 + (R1/R2). This configuration does not support negative input voltages, or gain settings below unity.

Figure 32(B) shows how to reconfigure the amplifier for bipolar operation, a virtual ground is substituted in place of the VSS connection to R2. In this configuration, any input voltage below the virtual ground is considered negative, and the output voltage is measured relative to the virtual ground.

FIGURE 32: NON-INVERTING AMPLIFIER

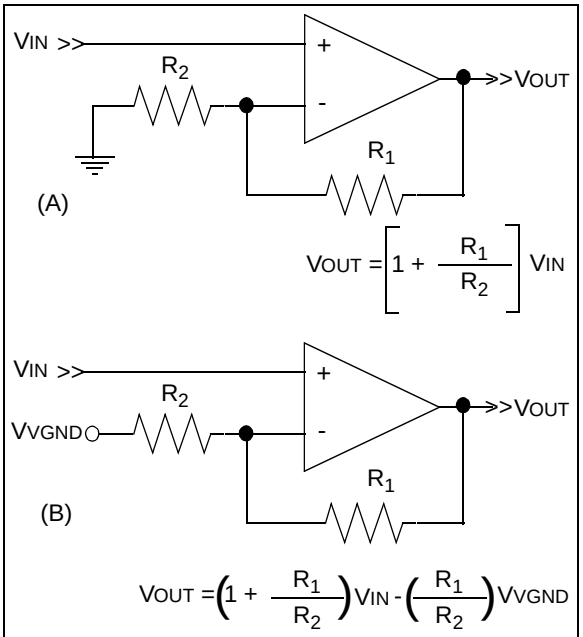


Figure 3 in AN682

Figure 33(A) combines the inverting and non-inverting configurations to create a difference amplifier. Matching the resistors in the inverting and non-inverting feedback paths creates a configuration which amplifies the input voltage difference by a gain equal to R1/R2. In the configuration shown:

- The circuit is limited to positive voltages
- V2 must be greater than V1
- The output is ground-referenced

Figure 33(B) demonstrates how to configure the amplifier for bipolar operation, the VSS ground connection to R1 is replaced with a virtual ground. The resulting circuit will treat all input voltage below the virtual ground as negative, and the output will be referenced to the virtual ground.

FIGURE 33: DIFFERENCE AMPLIFIER

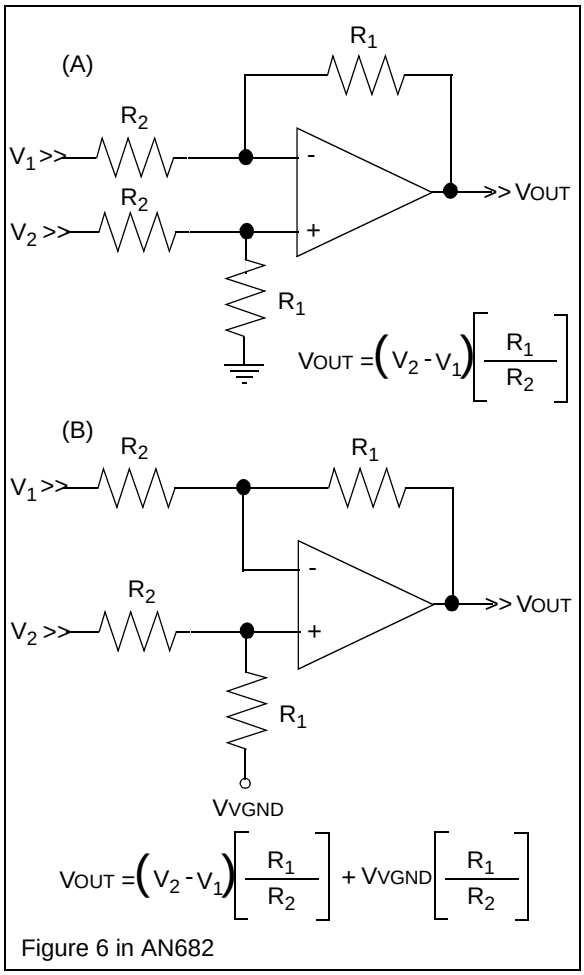
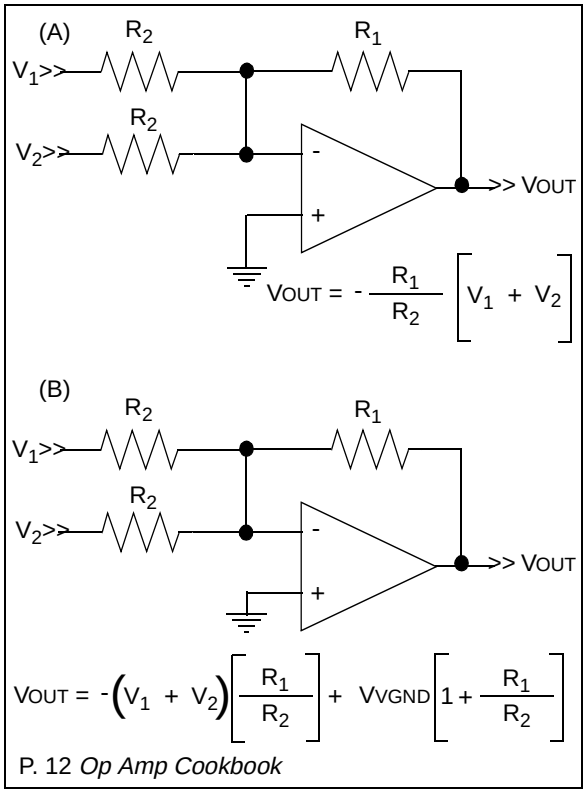


Figure 6 in AN682

Figure 34(A) is a variation on the inverting configuration, using two input paths to create an inverting summing amplifier with a gain equal to -(R1/R2). The configuration is capable of both controlled gain or attenuation, based on the resistor choices in the feedback network. In addition, the gain can be tailored for each input individually by varying R2. The configuration shown can accept negative inputs, or inputs with a net negative result (smaller positive voltage plus a larger negative voltage) resulting in a positive output.

Figure 34(B) shows how to configure the amplifier to operate on negative and positive inputs, the ground reference on the non-inverting input is replaced with a virtual ground at some voltage above VSS and below VDD-1.4. When the amplifier is connected to the virtual ground, the design recognizes any input voltage below the virtual ground as a negative voltage and all outputs from the circuit are measured relative to the virtual ground.

FIGURE 34: SUMMING AMPLIFIER



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CURRENT/VOLTAGE CONVERSION

The op amp module can also be used as the basis for converting voltages to currents and vice-versa.

Figure 35 shows two examples of how the op amp module can be used to convert a voltage input into a current output. Example A in Figure 35 is the simpler design, using the op amp to supply the output current. This configuration is good for current outputs of less than 2-4 milliamps and load resistance that can operate isolated from VSS and VDD. Figure 33(B) shows an alternative output capable of higher current output, and is not dependent upon an isolated load resistance. Further, Figure 35(B) can be modified to create a current source by replacing the NPN transistor with a PNP and moving RSENSE to VDD in place of VSS.

FIGURE 35: VOLTAGE TO CURRENT CONVERTER*

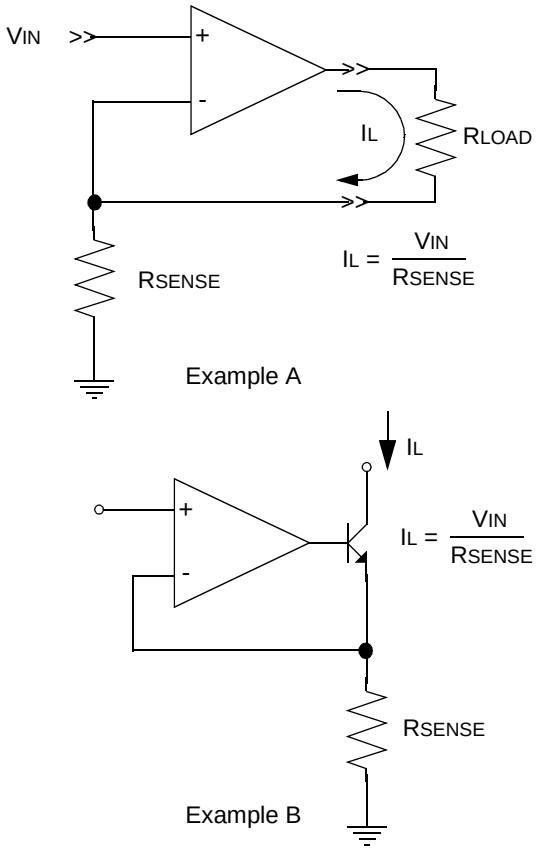

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Figure 36 shows the inverse conversion, a current to voltage converter. In this example, the reverse leakage current of the diode is amplified by the op amp to produce an output voltage proportional to the current. R1 in the feedback path establishes the relationship between the current flow and the output voltage. This example shows an op amp in combination with a photo diode to convert the light-dependent reverse leakage into a voltage for IR based receivers and visible light sensors.

FIGURE 36: CURRENT TO VOLTAGE CONVERTER

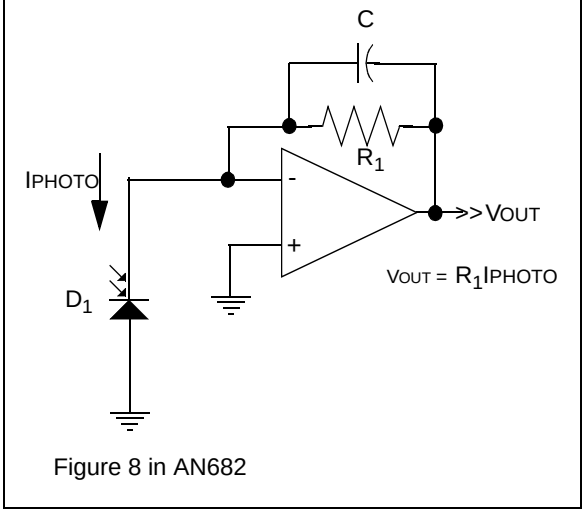

Figure 8 in AN682

MATH FUNCTIONS

Using frequency-dependent components expands the op amp's role from a simple amplifier to an analog math co-processor. Using certain combinations of resistors and capacitors, it is possible to create circuits capable of integration and differentiation.

Figure 37 shows a simple integrator based on the op amp, a resistor and a capacitor.

The output is the integral of the input multiplied by -1/(RC). To zero the integrator, two switches are shown for discharging the capacitor. The configuration shown can accept negative input voltages, generating a positive voltage output. To configure the circuit to accept both negative and positive input voltages, the V_{SS} connection to the non-inverting input must be replaced with a virtual ground reference between V_{SS} and V_{DD}-1.4V. The resulting circuit will treat all input voltage below the virtual ground as negative and the output will be measured in relation to the virtual ground reference.

FIGURE 37: INTEGRATOR

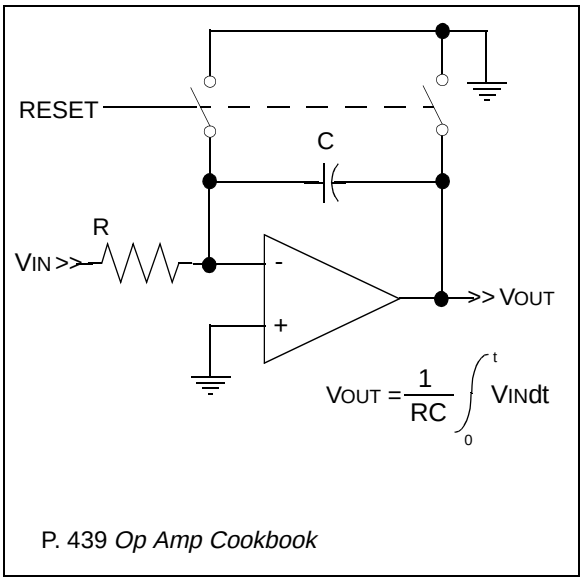

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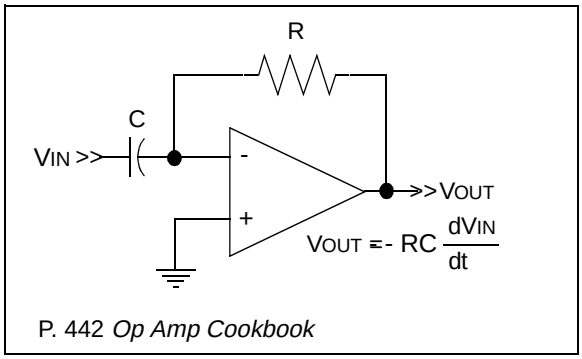
Figure 38 shows the complement to the integrator, a differentiator. The output for this circuit is the differential of the input with respect to time. The gain of the circuit is -RC multiplied by the differential of the input signal. The configuration shown can accept both positive and negative inputs, but can generate only positive output voltages.

FIGURE 38: DIFFERENTIATOR



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FILTERS

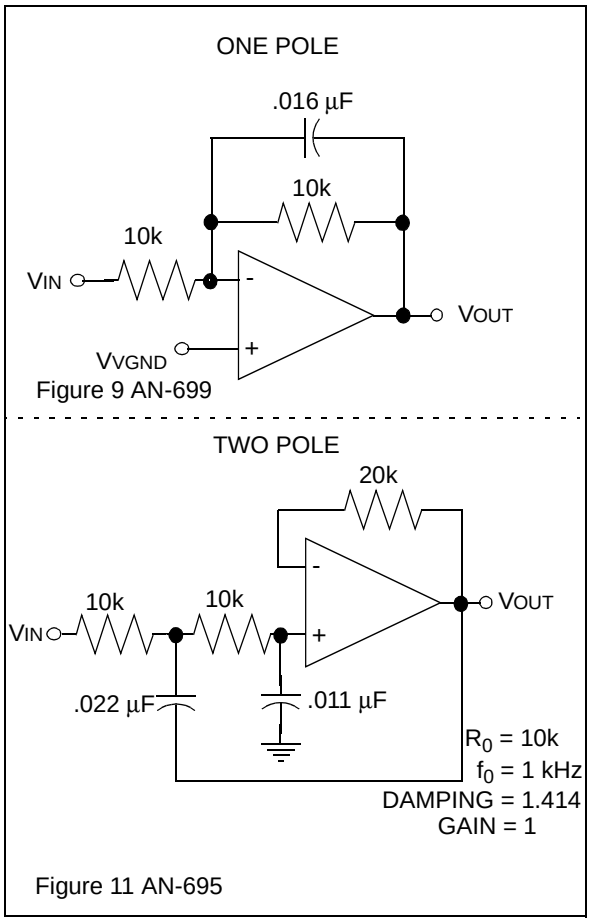
Simple variations on the op amp integrator and differentiator create frequency domain filters. The design methodology of filters and their derivation is a complex subject, well beyond the scope of this Application Note. However, Microchip Application Note AN699 examines filter design in greater depth. In addition, Microchip has made available a free CAD program 'FilterLab®' to assist in the development of op amp-based filters.

For simple filter applications, sample filters are shown in Figures 39-41 along with general descriptions of their performance. The last section dealing with filters discusses techniques for frequency and impedance scaling that allow the designer to modify general circuits for more specific applications. For more information, consult the "*Active Filter Cookbook*" by Don Lancaster (ISBN 0-7506-2986-X).

Figure 39 shows diagrams for a simple one pole and two pole low pass filter. The filters are designed for a 10 kOhm impedance, and a 1 kHz corner frequency. Both filters also exhibit a gain of 1 and are designed for a flat pass band. The roll off for the one pole filter is -6 Db/octave and -12 Db/octave for the two pole.

Note:	Low pass filters pass DC, so the input signals must be positive with respect to VSS to prevent clipping near ground.

FIGURE 39: LOW PASS FILTER



Two pole filters have one additional design parameter called 'damping.' 'Damping' is the tendency of the filter to oscillate at the corner frequency. High values of damping in the filter cause a peaking in the response and a sharp cutoff at the corner frequency. The filters presented here are designed for a damping of 1.414 which gives a flat pass-band with no peaking and a rounded roll-off at the corner frequency.

Figure 40 shows diagrams for a simple one pole and two pole high pass filter. As above, both filters are designed for a 10 kOhm impedance, and a 1 kHz corner frequency. Both filters also exhibit a gain of 1 and the two pole filters is designed for a damping of 1.414.

Note 1:	High pass filters do not pass DC, so the input signal can be bipolar; however, the outputs will only generate positive output voltages.
2:	To prevent clipping, the virtual grounds (VVGND) in the circuits must be tied to voltage sources between VSS and VDD-1.4V.

FIGURE 40: HIGH PASS FILTER*

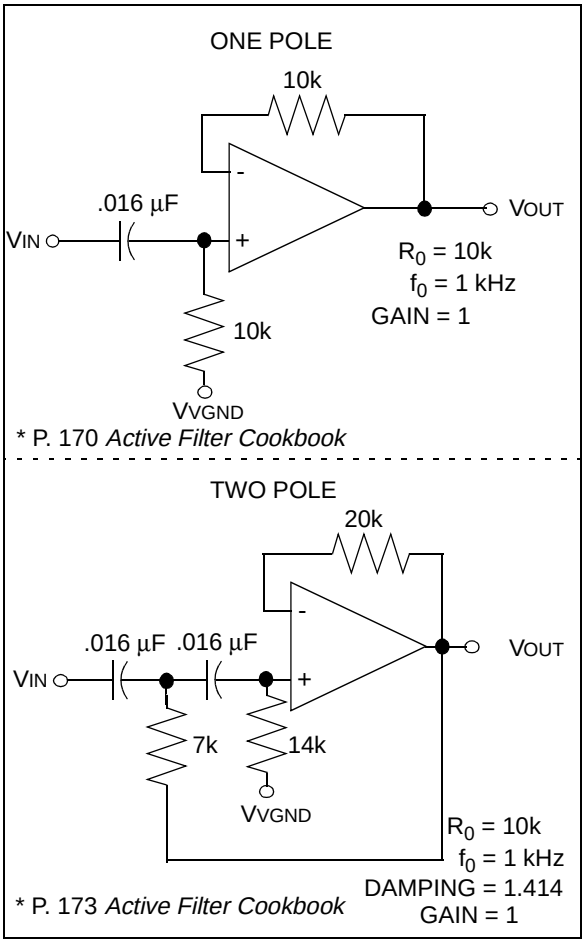
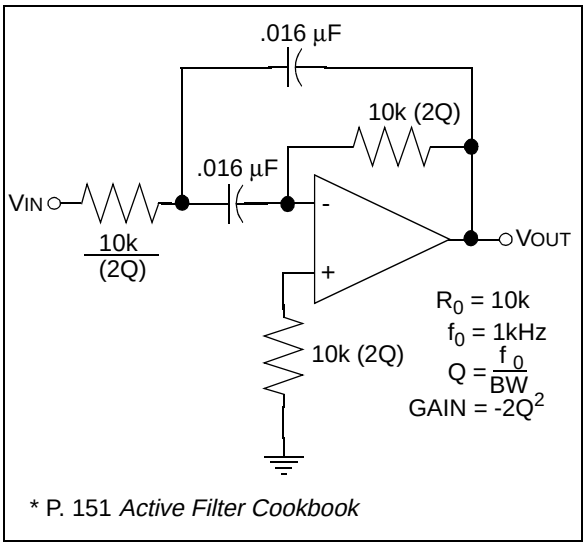


Figure 41 shows a diagram for a single pole band pass filter. The filter is designed for a 10 kOhm impedance, and a 1 kHz center frequency. The bandwidth of the filter is set by selecting an appropriate Q using the listed equation. The gain of the circuit is also dependent on Q squared, so the design should recognize that high values of Q (narrow bandwidth) can result in a significant circuit gain.

FIGURE 41: BANDPASS FILTER*



* P. 151 *Active Filter Cookbook*

FILTER IMPEDANCE/FREQUENCY SCALING

Once a basic filter design has been selected, the filter can then be scaled for impedance and frequency. Most filter designs are normalized to an impedance of 10 kOhm and a corner frequency of 1 kHz.

To change the impedance of the filter, first determine the scaling factor by dividing the new impedance by 10 kOhm, then multiply all the resistors in the circuit by the scaling factor and divide all the capacitors by the scaling factor. As an example, if the two-pole low pass in Figure 37 is to be scaled to 1 kOhm, the scaling factor is determined to be 1 kOhm/10 kOhm or 0.1. Next, the 10 kOhm resistors are multiplied by 0.1 resulting in 1 kOhm, and the capacitors are divided by 0.1, resulting in 0.22 µF and 0.11 µF.

To change the corner frequency of the filter, first determine the scaling factor by dividing the new frequency by 1 kHz, and then either: divide the input and feedback resistors by the scaling factor, or divide the input and feedback capacitors by the scaling factor. As an example, to scale the filter in Figure 32 from 1 kHz to 10 kHz, first determine the scaling factor, (i.e., 10 kHz/1 kHz or 10). Then replace either the two 10 kOhm resistors with 1 kOhm resistors, or change the capacitors from 0.022 µF and 0.011µF to 0.0022 µF and 0.0011 µF.

In both scaling operations, the ratio of the resistor in the input and feedback paths must not change or the damping of the filter will be affected. For a more in-depth explanation of scaling, refer to Chapter 3 of the "*Active Filter Cookbook*."

PID CONTROLLERS

Minor additions to the integrator described above creates a standard block for feedback controls systems, the Proportional Integrator Differentiator, or PID filter. A PID filter is designed to stabilize feedback control system by modifying the gain and phase of the closed loop system. The transfer function of the PID usually includes a POLE at zero frequency and a ZERO that can be adjusted to provide the necessary phase shift in the system.

The purpose of the zero frequency pole in the PID frequency response is two fold. First of all, it provides a 90 degree phase shift in the frequency response which helps improve the stability of the system. Particularly systems which exhibit a 360 degree phase shift without the PID filter. The second purpose for the zero frequency pole is to significantly increase the DC gain of the PID filter. The steady state error of the system is directly related to the DC gain of the loop. Therefore, increasing the DC gain of the PID filter decreases the steady state error of the loop.

Typically, a Bode Plot is constructed from the cascaded gain and phase of the loop elements plus the POLE from the PID. Next, a frequency for the ZERO is selected such that the phase shift from the ZERO pushes the phase of the network away from 360 at the unity gain frequency. Once a stable network is achieved, the loop is modeled and the final characteristics of the PID are adjusted for:

- desired natural frequency
- overshoot
- damping

This paragraph contains a fairly simplistic explanation of the design of feedback systems and PID controller performance selection. However, the actual design of feedback system is a fairly complex science and a full explanation is beyond the scope of this document. The designer is therefore referred to any of the commonly available texts on the subject of control theory for a more in-depth discussion of feedback system design.

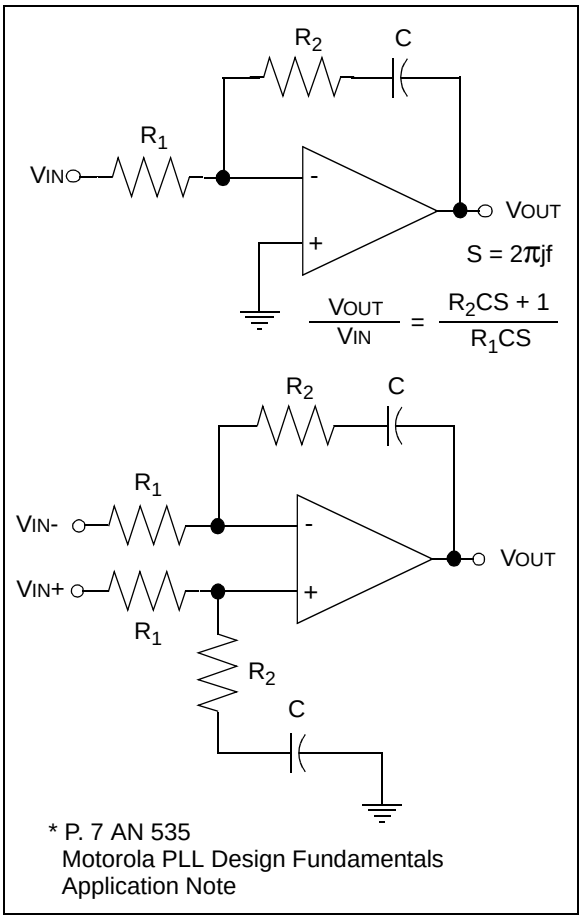
Examples of two PID circuits are shown in Figure 42. The first is an example of a single input PID with:

- a POLE at zero frequency
- gain of 1/(R1*C)
- a ZERO at R2*C

Note:	The frequency is expressed as S, the frequency in radians (2π) multiplied by j (the square root of -1).

The example shows a VSS referenced circuit which will operate with negative input voltages only. To configure the circuit for bipolar operation, the VSS connection of the non-inverting input must be replaced with a virtual ground between VSS and VDD-1.4. The second circuit is a PID combined with a difference amplifier. This circuit is particularly valuable, due to the common requirement of combining an error amplifier (subtracting the feedback from a reference) and the PID function into one op amp circuit.

FIGURE 42: PID, PROPORTIONAL INTEGRATOR/ DIFFERENTIATOR*



* P. 7 AN 535
Motorola PLL Design Fundamentals
Application Note

VOLTAGE COMPARATORS

The Voltage Comparators have multiple applications including:

- Level detection
- Schmitt triggers
- Pulse/PWM generation

The voltage comparators in the PIC16C78X have features for level detection including:

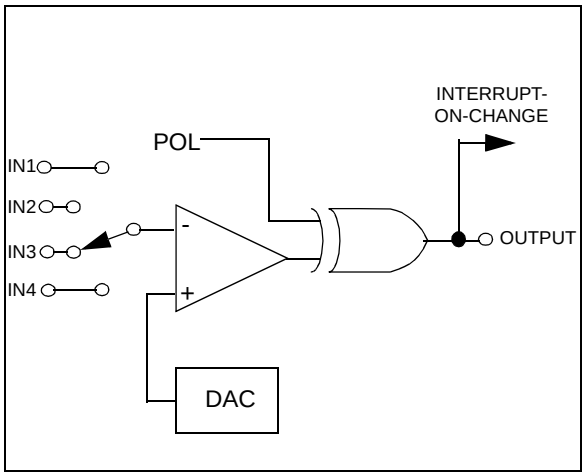
- Interrupt-on-Change
- 4-way input multiplexers
- Programmable output polarity
- External reference inputs
- Internal connections to the DAC for a programmable threshold

The ability to externally connect to the comparator outputs allows positive feedback for Schmitt trigger circuits. Adding an RC to a Schmitt trigger creates a multivibrator for pulse and ramp generation. Also, the combination of a ramp generator and a second comparator creates a voltage controlled PWM generator.

COMPARATOR CIRCUITS

Figure 43 shows a typical application of a voltage comparator in the PIC16C78X. The multiplexer switches the level sensor between 4 separate inputs. The DAC can provide a programmable threshold for each input or multiple levels for each. The output polarity control gives the designer the option of negative or positive true logic, and the interrupt-on-change capability allows the microcontroller to work on other functions or SLEEP until the limit is reached.

FIGURE 43: VOLTAGE COMPARATOR



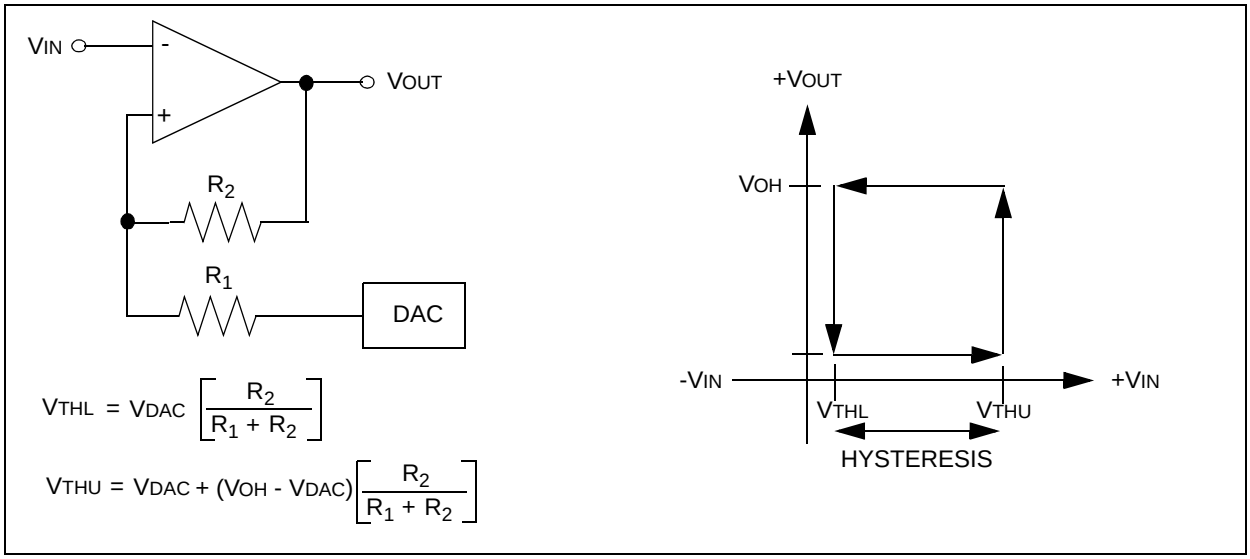
SCHMITT TRIGGERS

Figure 44 shows an example of a Schmitt trigger input using the external output capability of the voltage comparator module. The output of the comparator is fed back to the reference input through R2.The voltage reference is also fed to the comparator through a resistor R1. In this configuration, the trip threshold of the comparator is a function of the:

- DAC voltage
- Comparator output voltage
- Two resistors R1 and R2

When the output is high, the threshold is raised above the DAC voltage, and when the output is low, the threshold is lowered. As a result, when an input level trips the comparator, the comparator automatically pulls its threshold in the opposite direction to hold the state, generating a hysteresis to the threshold. From the equations, the thresholds will be symmetrical about V_{DAC} if V_{DAC} is centered at $V_{OH}/2$. As V_{DAC} is raised or lowered, the thresholds will shift toward V_{DD}. As V_{DAC} is lowered, the thresholds will shift toward V_{SS}.

FIGURE 44: SCHMITT TRIGGER



MULTIVIBRATORS

Figure 45 shows an example multivibrator oscillator. The circuit is based on the Schmitt trigger of the previous example with the addition of R_TC_T to the comparator input. When the oscillator starts:

- the output is high
- the threshold is pulled up to the high limit
- R_TC_T begins to charge

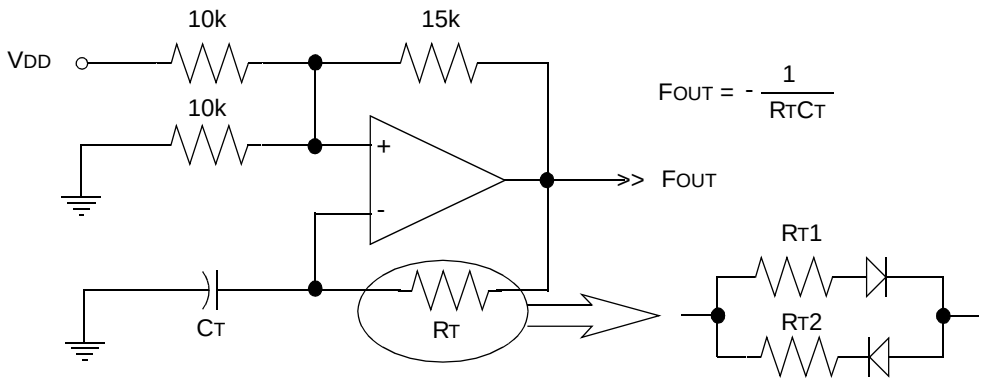
When the voltage across C_T exceeds the high threshold limit:

- the output goes low
- the threshold is pulled down to the low limit
- C_T begins to discharge

The pulse output of the circuit should be approximately 50% duty cycle and the frequency is a function of both the R_TC_T, and the hysteresis of the comparator. For the example, the hysteresis resistors have been selected to make the frequency equal to the reciprocal of the RC values. The output can be taken from the output of the comparator for a square wave, or from the inverting input if a triangle wave is needed.

If a duty cycle of other than 50% is desired, one modification that can be made to the circuit is to replace the R_T with two resistor diode networks, as shown in Figure 45. The duty cycle of the output can now be adjusted by varying the ratio of R1 to R2. For a ramp function, R1 can be replaced with a short and the waveform output taken from the inverting input of the comparator.

FIGURE 45: ASTABLE MULTIVIBRATOR*



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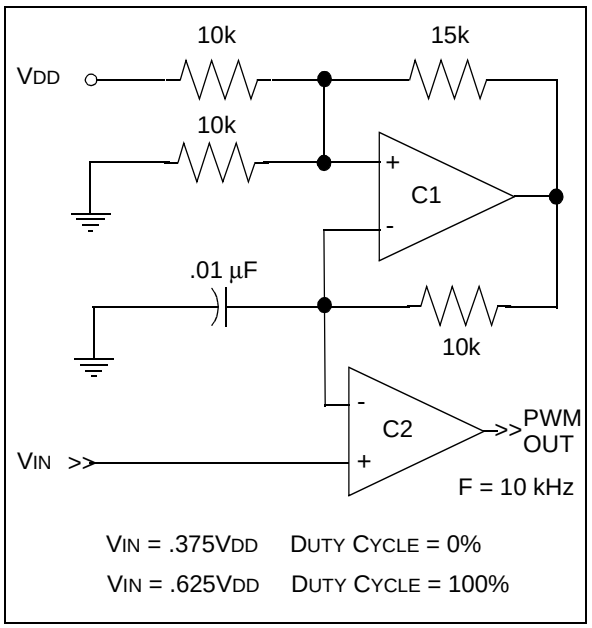
PULSE WIDTH MODULATION

Figure 46 uses the multivibrator example in the previous section to build a PWM generator. The pseudo-triangle wave form output of the multivibrator (C1) is connected to the input of the second comparator (C2) and the input voltage (V_{IN}) is connected to the reference input of C2. As the waveform ramps up, the output of C2 will remain high. When the waveform passes V_{IN} the output of comparator C2 will go low and stay low until the waveform once again falls below V_{IN}. The result is a PWM output (C2) with a duty cycle proportional to V_{IN}. There are two important factors to remember about this circuit:

1. V_{IN} must be between the two threshold voltages of the multivibrator to produce a pulse.
2. The square wave output of the multivibrator (C1) can not be used as a sync signal for the PWM output because both the start and end of the PWM pulses will move, relative to the output of C1, with changes in V_{IN}.

FIGURE 46: PULSE WIDTH MODULATION GENERATOR

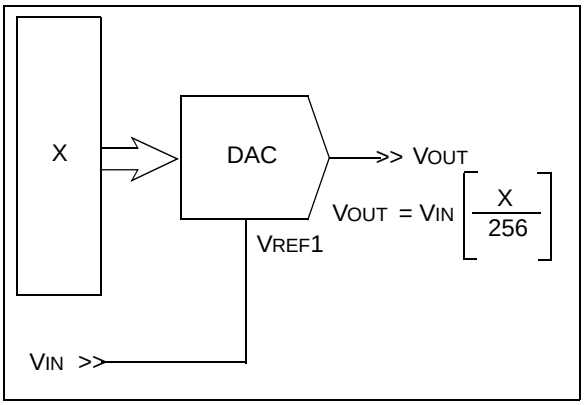


An improvement to this circuit would be to add the ramp waveform modification discussed in the previous section. The PWM signal would then have a fixed end time to its pulse and be synchronized to the square wave output of the multivibrator (C1).

DAC

The DAC provides a simple method for digitally scaling an analog signal. Figure 47 demonstrates using the DAC as a means of scaling an analog input. The voltage present on $V_{REF}1$ input is scaled via the DAC R-2R ladder to generate a scaled output voltage. Using the DAC to scale an output has applications in both matching the output voltages of two sensors, or scaling of the input for the maximum resolution from an ADC conversion. The only limitation on the DAC is that the incoming voltage must be positive and within the Common mode voltage range of the DAC (V_{SS} to V_{DD}). Further, the incoming frequency must be within the output bandwidth of the DAC output amplifier, typically 30 kHz.

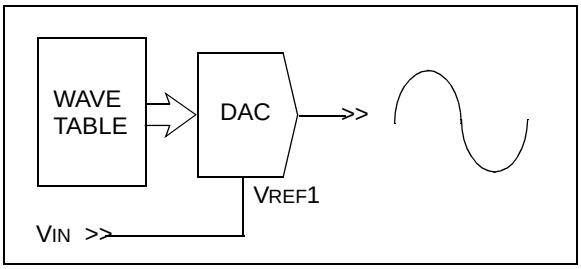
FIGURE 47: INPUT SCALING USING DAC



The DAC can also be used as an arbitrary waveform generator, as shown in Figure 48. In the example shown, the DAC is configured for an external output and then wave table data bytes are loaded into the DAC register at a controlled rate. The output of the DAC then reproduces the waveform based on the data and the update rate.

Note:	The maximum update rate is limited to 30 kHz.

FIGURE 48: ARBITRARY WAVEFORM GENERATOR



HIGH RESOLUTION ADC

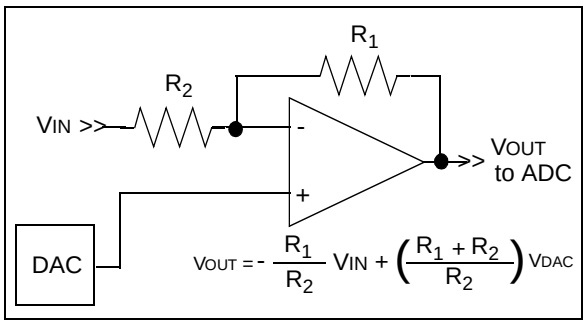
The last area of application for the analog peripherals in the PIC16C78X microcontroller to be covered by this Application Note is the creation of high resolution Analog-to-Digital converter configurations. System performance often requires a higher resolution ADC than the peripheral provided with the microcontroller. This section covers ADC topologies that allow the creation of high resolution ADC systems using the existing peripherals within the device. Topologies that will be explored are:

- a range extension system for the existing ADC
- a voltage to frequency ADC
- a dual slope ADC

EXTENDING THE EXISTING ADC RANGE

The first example expands the range of the existing ADC by creating a programmable offset input range for the ADC using the op amp and the DAC. Figure 49 shows a difference amplifier implemented with the op amp and the DAC. The unique feature of this circuit is that the gain for the non-inverting input is the reciprocal of the inverting input gain, resulting in an amplifier which subtracts a multiplied DAC signal from the unity gain incoming signal. In effect, the circuit shifts a segment of the larger input voltage range into a range the ADC can convert.

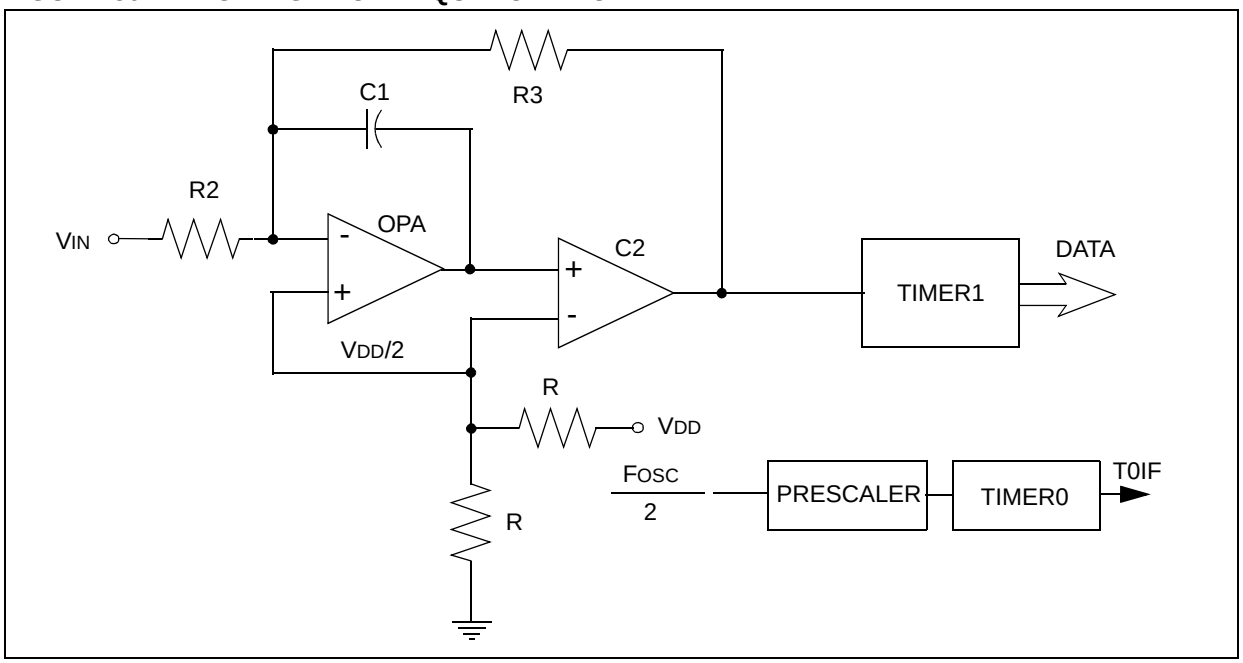
FIGURE 49: PROGRAMMABLE OFFSET CIRCUIT



Firmware can monitor the result of the conversion and adjust the output level of the DAC to maintain the incoming signal within the proper range of the ADC. If the input signal moves above or below the range of the window, the value presented to the input of the ADC will move to either the top rail or ground, depending on whether the input is above or below the window. An important limitation to remember concerning this system is that while the ADC gains range, it is at the cost of absolute accuracy.

The gain accuracy of the amplifier circuit and the accuracy of the DAC both play a factor in the final accuracy of the system. However, the errors in gain can be calibrated for both the DAC and the amplifier separately and removed from the final result with simple math.

FIGURE 50: VOLTAGE TO FREQUENCY ADC



VOLTAGE TO FREQUENCY ADC

Another configuration for a high resolution ADC is shown in Figure 50. The hi-resolution ADC uses Timer1, comparator C2, the op amp, and firmware to create a voltage to frequency ADC.The input voltage (0 - VDD/2) is fed into a differential integrator formed by R, C and the op amp. The input voltage causes the integrator output to fall at a rate proportional to the input voltage. When the integrator output falls below VDD/2, the output of the following comparator C2 will go high and the integrator output voltage rises quickly. When the integrator output passes above VDD/2, the comparator output goes low again and the cycle repeats. Once the system is stable, the output of the comparator is generating a frequency proportional to the input signal.

The conversion result is the frequency of the comparator output. The frequency is recovered by using The Timer0 and Timer1. Timer0 sets the period to be sampled, and Timer1 measures the number of cycles generated by the comparator output. To start the conversion:

- Timer0 and Timer1 are cleared
- Timer0 is configured to provide a fixed time delay

During the conversion, the Timer1 is incremented by each pulse from the C2 comparator. When Timer0 times out, the contents of Timer1 are then read. The conversion value is then the total count of Timer1, and the resolution of the conversion is determined by the maximum total count of Timer0. To start another conversion, Timer1 and Timer0 are set to zero and the software waits for the next Timer0 time-out. This converter can provide a resolution of up to 10 -12 bits, with careful selection of components.

Although this converter has good relative accuracy performance, the resistor VDD/2 division, op amp/Comparator input offset voltages, and slew rate variations limit it's absolute accuracy.

DUAL SLOPE ADC

The final example is that of a dual slope ADC using:

- DAC
- Comparator C2
- Op amp
- Internal voltage reference VR
- Timer1 (see Figure 51)

A dual slope ADC operates by charging a capacitor with the input voltage for a fixed time period, then discharging the capacitor at a fixed current and measuring the time to discharge. At the start of the conversion, the DAC is set to FFh and configured to use the external input VREF1. The fraction of 255/256th of the input voltage is passed through the DAC to the integrator formed by R, C, and the op amp. When the integrator has charged to VR/2, Timer1 is configured for fixed period time-out and started. While Timer1 is counting, the integrator is charging at a rate set by VIN. When Timer1 times out:

- the DAC is reconfigured for the VR reference input
- the Timer1 is cleared
- the Timer1 gate function is enabled

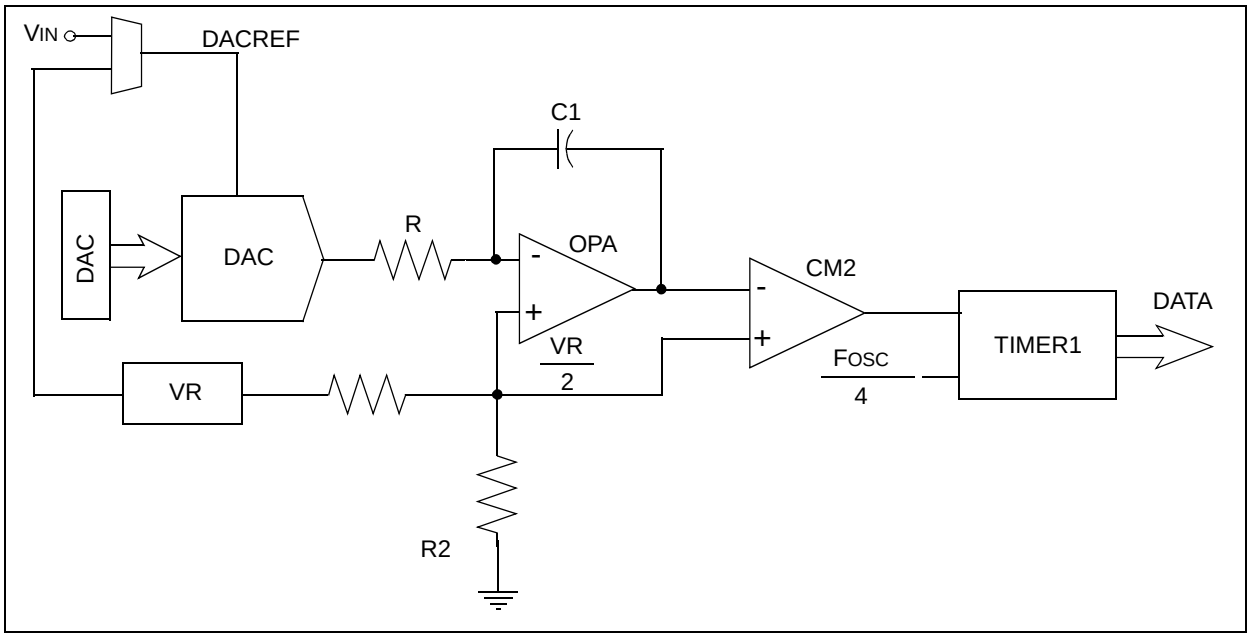
As the integrator slowly discharges in response to the higher input voltage, VR, Timer1 counts the time required for the integrator to discharge down to VR/2. When the integrator falls below VR/2, Timer1 stops counting and the value is read from the timer.

This converter can also provide a resolution of up to 10-12 bits, with careful selection of components. This converter also produces significantly less noise than the sigma-delta due to the limited number of output transitions (two). The dual slope ADC is limited in that the accuracy of the system is set by the losses in C1 and the accuracy of the DAC.

CONCLUSIONS

The PIC16C78X family of microcontrollers have been designed to be a bridge between the digital and analog world. The family of onboard digital and analog peripherals allows a level of digital control over analog systems not previously available in a single-chip solutions. The tight integration of analog and digital have created a microcontroller with the speed of an analog solution, and the flexibility of a digital microcontroller. Despite its flexibility and the wealth of peripherals, the family has been kept reasonable in size and cost without sacrificing performance. We believe the only limits in the applications of the PIC16C78X family of microcontroller are the limits of the imagination of the designers using it.

FIGURE 51: DUAL SLOPE ADC



REFERENCES

For more information concerning switching power supply design, please refer to Microchip's web page at www.microchip.com for additional Application Notes and Technical Briefs concerning:

- switching power supply design
- MOSFET driver selection
- example designs

To access the information concerning Power design, select the Application Note tab on the home page, then select 'Power Management.'

Another good technical reference for Switching power supply design is Abraham Pressman's book, '*Switching Power Supply Design*,' ISBN 0-07-052236-7.

Microchip Application Notes AN682, AN685, AN688 AN693, AN699, AN700, AN722, AN723.

The "*Op Amp Cook Book*" by Walter Jung is available from the Prentice-Hall publishing Company, ISBN 0-13-889601-1.

"*Amplifier Applications of Op Amps*" by Jerald Graeme is available from McGraw-Hill, ISBN 0-07-134642-2.

"*Switching Power Supply Design*, by Abraham Pressman, ISBN 0-07-052236-7.

"*Active Filter Cookbook*" by Don Lancaster, ISBN 0-7506-2986-X

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