AN949

Making Your Oscillator Work

Author: *Brett Duane*
Microchip Technology Inc.

INTRODUCTION

Many Microchip customers ask us for help when designing their oscillator circuits. Due to the great number of combinations of VDD and temperature ranges, crystal or resonator, loading capacitors, circuit layout and circuit board materials, it is not practical to provide a cookbook process that would work well for everyone or even for most users. However, there are measures that can be used to develop and test for good working oscillator circuits.

This application note breaks down the oscillator design process into the following three parts: specifying the operating conditions, selecting the components and testing oscillator performance. Other concerns are also discussed that may be helpful during layout and testing.

SPECIFICATIONS

First, you must decide on the following specifications:

- The temperature range over which the controller will be starting and operating.
- The range that VDD will vary across while the controller is starting and operating.
- Power requirements and operating frequency.

Once these have been decided, the circuit designer can begin testing to determine oscillator circuit components. Testing will require several of the target circuit boards populated only with the controller, oscillator circuits and a power source. These boards will be tested over the expected voltage and temperature ranges determined above. The required test equipment will be an ammeter (to read the controller IDD), voltmeter, thermometer and oscilloscope, with either a x100 probe or preferably with an FET probe.

Note:	The oscillator mode was not included as part of the specification. The mode selected will depend, in large part, on the timing element (crystal or resonator), frequency, VDD and temperature range.

Temperature

The product is expected to operate over some temperature range. Testing of oscillator operation will be conducted over the same or slightly larger range. The temperature affects transistor gain, capacitor values and the crystal/resonator frequency.

Voltage

As with temperature, the product will be expected to operate over some voltage range. Often, low-power products will be operating from batteries. Oscillator operation needs to be tested at slightly above the highest expected voltage down to slightly below the minimum voltage specified for the product. Other systems will have a regulated voltage source, but even these have some tolerance in the specified output voltage.

For example, the common 78L05 regulator will provide 100 mA at 5V, ±5% (5V, ±250 mV). In such a system, oscillator operation could be verified at 4.5V and 5.5V (slightly beyond the regulator output range). Be aware that the regulator output voltage may vary with temperature and this must also be considered.

Power Requirements and Operating Frequency

Something that many designers may not consider is that resonators require about three times the drive power than crystals. This has a direct impact on IDD and the maximum frequency at which the oscillator circuit can operate for a given VDD, temperature and oscillator mode.

At any VDD and temperature, the drive (power) required to make both crystals and resonators oscillate increases with frequency. At the same time, the oscillator power output decreases as frequency increases. As frequency increases, a resonator may fail to oscillate, while the crystal continues to operate quite well. Microchip PIC® microcontrollers can drive a crystal at 4.0 MHz in XT mode, but resonators often fail at lower frequencies under similar conditions. It is recommended that when resonators above approximately 3.5 MHz are being used, they be driven in the higher power HS mode, rather than XT mode. Testing should still be performed to determine the values of loading capacitors used.

Selection of a higher power oscillator mode will increase the controller IDD. Thus, the designer may be forced to consider using a crystal in place of a resonator based on frequency and current consumption.

CAPACITOR SELECTION

Initial testing determines the values of the loading capacitors to be used. One method consists of measuring the controller current while changing the loading capacitor values in the oscillator circuit (I_{DD} method). Another method breaks the oscillator circuit to measure oscillator loop phase shift (open-loop method). Both methods should be performed using the final circuit board that will be used in production.

Either of these testing methods is repeated on several copies of the same board, each with its own controller and crystal/resonator. Preferably, each of the controllers and crystals/resonators used for testing are obtained from as many different lots as possible. The capacitor values found for each board should be similar to all the other boards. The capacitor values are then averaged together, and the closest available standard capacitor values are used for further testing (start-up from Sleep test across temperature and V_{DD}). These capacitors should be mounted on the boards for the remainder of the oscillator testing.

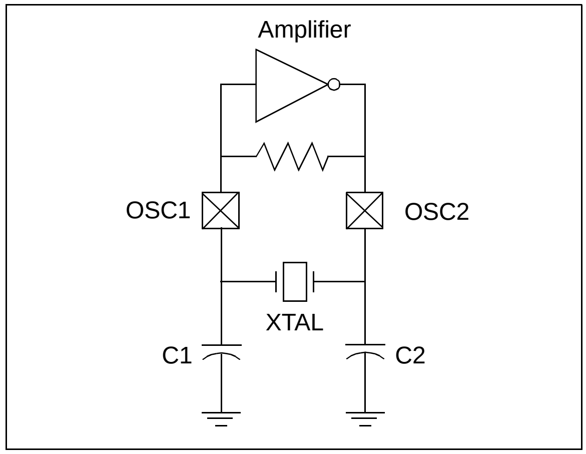
I_{DD} Method of Selecting Loading Capacitors

This method requires the controller port pins to be isolated or disconnected from the application circuits. The controller should be programmed to configure all pins so that they are outputs driving low, or configured as inputs externally pulled to V_{DD} or V_{SS}. No port pins should be allowed to float, as they can oscillate and draw additional I_{DD} current. The intent is to minimize I_{DD} by minimizing port pin currents.

While developing a new design, it is often easiest to mount the controller and oscillator circuit as the only devices on the circuit board. In this case, all port pins should be left unconnected (if possible) but configured as outputs and cleared. One pin could output a high pulse to indicate a proper start-up.

Testing, or calculation, determines an initial value for the loading capacitors, C1 and C2 (see Figure 1). At the nominal voltage and room temperature, a range of capacitor values is connected into the oscillator circuit. Both capacitors should have the same value. This testing seeks to find the capacitor values that result in the lowest I_{DD} for the selected oscillator mode. Once this pair has been found, oscillator start-up and performance are evaluated over the expected temperature and voltage ranges.

FIGURE 1: CLOSED OSCILLATOR LOOP



Open-Loop Method of Selecting Loading Capacitors

An alternative to selecting the loading capacitors based on the device I_{DD} is to use an open-loop method. This method breaks the closed-loop oscillator circuit at the inverter input (see Figure 2). A signal at the oscillator frequency is injected at the inverter input and is monitored by one channel of an oscilloscope. A second channel is connected to loading capacitor, C1, disconnected from the inverter input.

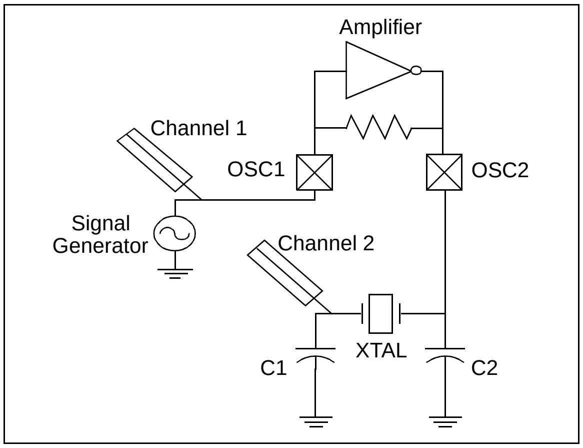
The value of C1 should be reduced by the capacitance of the scope probe for accurate measurements. If the probe has 10 pf of loading, and C2 is 33 pf, then C1 should be replaced with a 23 pf capacitor (or its closest standard value, 22 pf in this case).

The oscillator input signal is adjusted to match the crystal frequency at a level that prevents the amplifier from producing a distorted output. The exact frequency can be found by slowly sweeping the generator frequency while monitoring channel 2 for maximum amplitude. Often, the signal generator will need to have approximately 10 Hz (or less) resolution.

The values of the loading capacitors, C1 and C2, are then adjusted such that there is no phase shift between the two scope channels being monitored. The capacitors are adjusted in pairs, with C1 always less than C2 by the capacitance of the scope probe ($C1 = C2 - C_{PROBE}$). Increasing the capacitors will increase the phase shift, while reducing the capacitors will reduce the phase shift.

Using the phase shift as a guide, appropriate loading capacitors can be selected for the application circuit. Once the capacitor values that produce 0° (360°) phase shift are found, C1 will need to be increased by the scope probe capacitance; C2 may be used as is.

FIGURE 2: OPEN OSCILLATOR LOOP



TESTING/EVALUATION

Testing over temperature and voltage reveals if the oscillator circuit has problems. Each of the following are checked and possibly adjusted during testing:

- Starting
- Distortion/overdrive
- Circuit configuration
- Oscillator mode

If any changes to the oscillator circuit are made (during evaluation or required by manufacturing), testing should be repeated to verify that the changes are having the intended effects.

Starting

Testing is performed at the temperature and voltage extremes that the product will be expected to operate in. Using temperature and voltage as variables, four test points are checked. These are high temperature and high V_{DD}, high temperature and low V_{DD}, low temperature and high V_{DD} and low temperature and low V_{DD}. A fifth test point would be at a moderate temperature and V_{DD} (see Figure 3).

The test is to see if the oscillator will start from Sleep mode at each test point, and is the condition under which the oscillator has the greatest difficulty starting. After the initial power-up start, firmware places the controller in Sleep mode. An external interrupt can be used to wake the controller. When the interrupt is recognized, the controller will attempt to wake from Sleep and this starts the oscillator. Once the controller wakes, it can output a pulse to indicate a start. The time between the external interrupt and the output pulse could be used as a gauge to measure start-up time. This test is repeated at each test point (combination of temperature and voltage).

If the oscillator fails to start, the loading capacitors may need adjustment, a higher gain oscillator mode may need to be selected or a 1 to 2 MΩ resistor may be required between the OSC1 and OSC2 pins (see Figure 4, R2).

Distortion

The waveforms on the OSC1 and OSC2 oscillator pins are checked at the same 4 (or 5) combinations of V_{DD} and temperature. The waveform should be a smooth sinusoid. Distortion of the waveform consists of any kind of non-sinusoidal waveform and includes any clipping, straight edges (including sloping edges), spikes or sharp corners in the waveform. If distortion is present, the loading capacitors may require adjustment, a lower power oscillator mode may be needed or a resistor in series with the crystal may be required (see Figure 4, resistor R1) to reduce crystal drive.

Distortion indicates an overdriven crystal. While such oscillators start and operate quite nicely initially, there is a possibility that in time, the crystal may become damaged and cease to oscillate, or oscillate at some undesired frequency. Resonators can not be overdriven by Microchip's PIC microcontrollers.

Distortion is also a source of Electromagnetic Interference (EMI). If the oscillator waveform has large and frequent spikes, sharp corners or clipping, harmonics of the oscillator frequency are being generated and may be radiated into sensitive portions of the application. The designer should be aware that this may happen.

After each start-up test, the oscillator should run long enough to allow the waveforms on the oscillator pins to be examined at each temperature/V_{DD} combination. Use oscilloscope probes with the lowest possible loading effects. FET amplifier probes are preferred, but x100 probes may be used (set the oscilloscope coupling to AC; DC coupling presents additional loading on the oscillator and may cause it to stop). x10 probes often present great enough loading that waveforms displayed are often not truly representative of normal operation. With poorly optimized oscillators, oscillation may even be stopped when an x10 scope probe loads down the oscillator circuit.

FIGURE 3: TESTING OSCILLATOR START FROM SLEEP

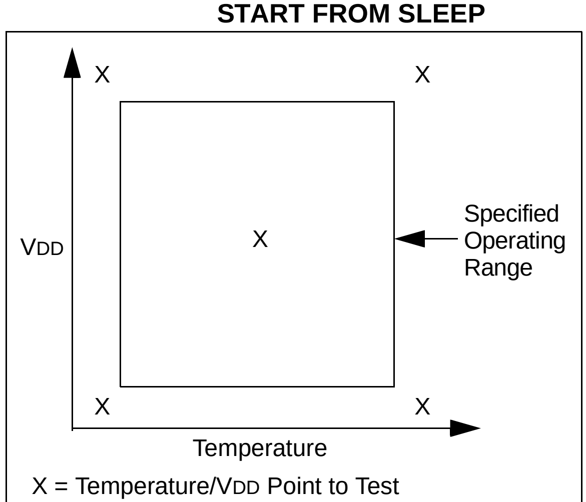
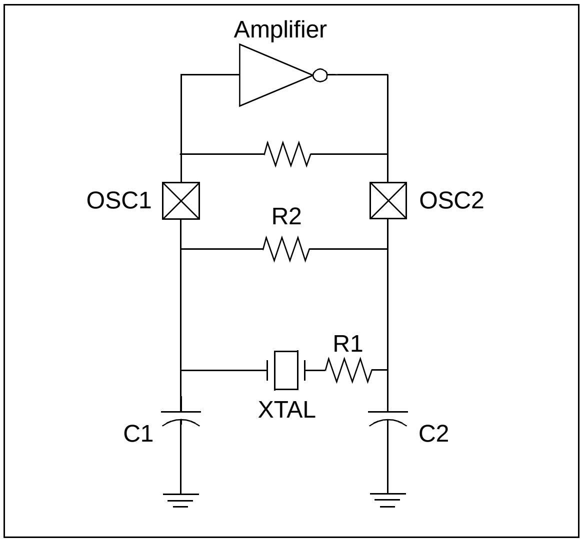


FIGURE 4: SERIES RESISTOR R1 REDUCES CRYSTAL DRIVE



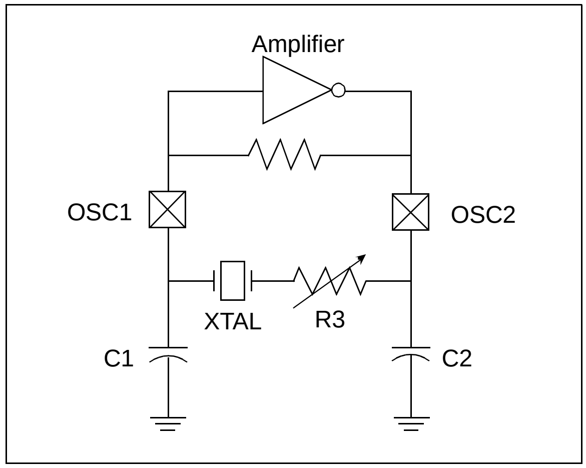
Negative Resistance Testing

Some customers perform additional testing based on a concept known as negative resistance. The general idea is that while the crystal or resonator adds resistance to the oscillator circuit, the oscillator amplifier (or inverter) provides gain in the form of negative resistance. When the total circuit resistance is 0 (zero) or negative, the oscillator will oscillate. When total circuit resistance becomes positive, the oscillator will fail. This test gives a measure of oscillator gain margin and the ability of the oscillator circuit to start.

Testing is performed at room temperature at a typical voltage. A variable resistance, R3, is inserted in series with the crystal and set to minimum resistance (see Figure 5). The oscillator is powered up and allowed to start.

R3 is slowly increased until the oscillator just fails. R3 is then removed from the circuit and measured. The resistance is then compared to the crystal Effective Series Resistance (ESR, as specified by the crystal/resonator manufacturer, not the crystal motional resistance). The measured value of R3 should be several times the crystal Effective Series Resistance in order to provide sufficient gain to start the oscillator under all conditions. Typically, most industrial applications seek a factor of 3, while automotive applications seek a factor of at least 5.

FIGURE 5: PLACEMENT OF RESISTOR FOR NEGATIVE RESISTANCE TESTING



CIRCUIT LAYOUT

The oscillator circuit connections should be as short as reasonably possible. This suggests that the oscillator circuit should be placed next to the controller and on the same surface. This also suggests that the loading capacitor grounds should be connected directly back to the controller. If possible, there should be no other connections or vias between the loading capacitors and the controller ground, except at the controller itself. The exception would be if a ground plane is present and the loading capacitors are connected to it.

SIGNAL LEVELS

Designers are often concerned that the oscillator waveforms do not meet the data sheet specifications. The specifications are intended to ensure that an externally provided clock signal can always clock the controller in place of a crystal oscillator circuit. Due to changes in V_{DD}, temperature and manufacturing variations, the actual oscillator thresholds for any particular controller often shift. However, the actual thresholds will always remain completely within the data sheet specifications. The oscillator waveform may exceed the data sheet specifications, but this should not be considered as an indication of a robust oscillator.

The actual oscillator thresholds will be somewhere within the specified thresholds' range (V_{IH} to V_{IL}) and will generally be a small portion of the clock input range. When used as an oscillator, the narrow range will shift and change size as voltage and temperature change between parts (even in the same lot). Feedback ensures that the oscillator output will be correctly biased between the actual input thresholds. The oscillator output amplitude will always exceed the actual input thresholds.

RESONATORS AND CRYSTALS

While this application note was written with crystals in mind, it applies equally well for resonators.

Resonators with internal loading capacitors are often used. Unfortunately, these capacitors are often larger than needed. During development and testing, use resonators without loading capacitors and external loading capacitors. Once final values are known, contact the resonator manufacturer for resonators with your loading capacitors. This is a common request, and the resonator manufacturer should have no problem meeting your specification. They may even have suitable parts in stock.

TUNING FORK CRYSTALS

This application note discusses oscillator circuits using resonators and “AT” cut crystals. Other crystal cuts may behave similarly.

One exception is tuning fork type crystals. The timing element is cut to form a tuning fork with the electrodes plated onto the legs of the fork. This type of crystal has very low drive requirements and correspondingly low maximum drive limits. Driving this type of crystal in HS or XT mode will likely destroy the crystal. Applying a DC bias to the crystal, even for a short time, is also likely to cause damage.

Many controllers offer a secondary oscillator for use with one of the internal timers, and is intended to provide an oscillator time base that operates even during Sleep. This oscillator shares its pins with some of the digital input/output pins. During controller initialization, it is important not to configure these pins as outputs as it would be possible to apply V_{DD} across the crystal and possibly damage it.

Other controllers also share the oscillator pins with In-Circuit Serial Programming™ (ICSP™) connections. These connections are used to program the controller after it has been mounted on the board. Typically, the signals on the programming circuits are near V_{DD} (5V) and may also damage the crystals. In such systems, one side of the crystal should be disconnected during programming or the crystal should somehow be isolated from the programming signals.

WRAPPING IT UP

This application note describes two different methods of selecting oscillator circuit components and two methods of evaluating the resulting oscillator performance. The test equipment required is typically found in reasonably equipped labs or can be easily obtained. The procedures are not complicated and do not require an in-depth understanding of oscillator design. Even though the procedures are quite simple, robust oscillators can be developed and the developer will gain confidence in his/her design.

CONCLUSION

Oscillator design requires knowing the operating conditions under which the oscillator will function, followed by testing to ensure that it will actually function as expected. The design phase involves component selection, sometimes guided by initial testing. The testing phase tests oscillator performance, either by testing actual operation under the previously specified conditions or by ensuring that there is sufficient gain margin to allow start-up and operation under all conditions. Several other factors, such as circuit board layout, signal levels and crystal and resonator concerns, are also discussed and may be helpful during the design phase.

FAQs

Question:

When I use an oscilloscope to probe the oscillator circuit, the oscillator stops. What's happening?

Answer:

There are two factors at work. The first is that the scope probe is adding capacitance to the existing loading capacitor. A second concern is that the probe is introducing high resistive loss into the oscillator circuit. Both changes can be enough to prevent the oscillator from working.

Oscillator circuits can be probed, but this requires care. A 100x probe reduces resistive and capacitive loading on the circuit being tested, compared with a 10x probe. Loading can be further reduced by switching the scope input coupling from DC to AC.

A better solution would be to use an FET amplifier probe. These probes apply the minimum resistive and capacitive loading to the circuits being tested.

Question:

I would like to use an In-Circuit Debugger (ICD) with this controller, but the connections to the controller are shared with a "tuning fork" style crystal. What should I do?

Answer:

ICDs make use of the ICSP (In-Circuit Serial Programming) connections to the controller to provide interactive debugging capability. The same concerns for ICSP apply to ICD operation. The crystal will need to be isolated or disconnected while the ICD is in use.

If the application requires the crystal, consider placing a socket on the board in place of the controller and programming the controller off-board.

Use an internal clock source instead of the crystal during development. Develop the timer code, but realize that the timer will be running at a different speed than expected.

Question:

I am trying to use a 4 MHz resonator with V_{DD} at 3V. The data sheet allows this, but the oscillator does not work. What am I doing wrong?

Answer:

You may be using the XT mode oscillator. When V_{DD} is raised, the oscillator may start working. Select the HS mode oscillator instead. This will allow the oscillator to work at a lower voltage, but will also draw additional current. Alternatively, change the resonator to a crystal, use XT mode as before and check the loading capacitor selection. When making such a change, retest the oscillator circuit to ensure that it will perform as expected.

Question:

I am using a 4 MHz crystal with V_{DD} at 5V and I am seeing a lot of distortion on the oscillator waveform. I have performed the testing described and I am otherwise satisfied with the oscillator performance. Should I be concerned? What can I do?

Answer:

If the application works with very low-power signals (radio or millivolt signals), the oscillator may interfere with normal operation. In such cases, a lower power oscillator mode may be required (switch from HS to XT mode). If the oscillator still shows distortion, drive to the crystal can be reduced by inserting a resister in series with the crystal (see Figure 3, use R1). A guard ring, ground plane or shielding around the oscillator circuit may also be helpful.

Generally, some distortion is acceptable, but be on the lookout for interference related problems.

Question:

I would like to tap into the oscillator circuit and use it as a frequency source elsewhere in my application. Is this possible?

Answer:

Yes, but this is not recommended. A higher gain oscillator mode may be required, while also controlling drive to the crystal using a series resister. The circuit tapping into the oscillator may also affect oscillator operation, so some form of isolation is suggested (consider an FET amplifier). Distortion in the oscillator waveform is more likely and may be coupled into the tapping circuit. Thoroughly test the resulting oscillator to be sure it performs as required.

This may be more trouble than it's worth. Consider alternatives if possible. One alternative would be to generate the clock elsewhere and couple it into the controller.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http:\\support.microchip.com
Web Address:
www.microchip.com

Atlanta
Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston
Westford, MA
Tel: 978-692-3848
Fax: 978-692-3821

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose
Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-750-3506
Fax: 86-591-750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Qingdao
Tel: 86-532-502-7355
Fax: 86-532-502-7205

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-2229-0061
Fax: 91-80-2229-0062

India - New Delhi
Tel: 91-11-5160-8632
Fax: 91-11-5160-8632

Japan - Kanagawa
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Taiwan - Hsinchu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

EUROPE

Austria - Weis
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Ballerup
Tel: 45-4420-9895
Fax: 45-4420-9910

France - Massy
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Ismaning
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

England - Berkshire
Tel: 44-118-921-5869
Fax: 44-118-921-5820

09/27/04