AN943

Practical PICmicro® Oscillator Analysis and Design

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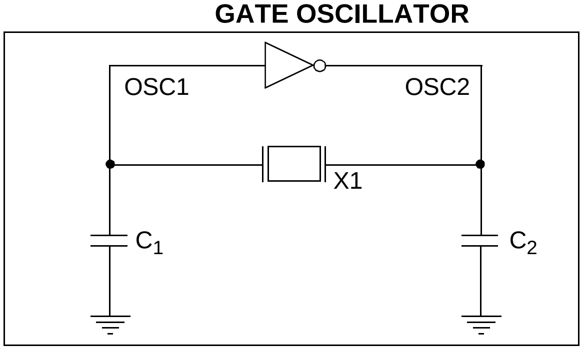
INTRODUCTION

There is a wealth of information written on the subject of designing and analyzing oscillator circuits. Sources range from academic and research papers to industry generated application guides. It is a daunting task for the embedded designer to work through all the available and sometimes conflicting information. All the designer is really interested in is a simple set of rules resulting in a reliable oscillator design that will work despite crystal aging, deviations between devices, temperature or voltage. The problem is the simple Crystal Pierce Gate Oscillator (Figure 1) has a "simplified" model (Figure 2) that is anything but simple. None of the values are fixed. Some vary with process, age, temperature and voltage. Some components have a nonlinear behavior with amplitude.

FIGURE 1: THE CRYSTAL PIERCE GATE OSCILLATOR



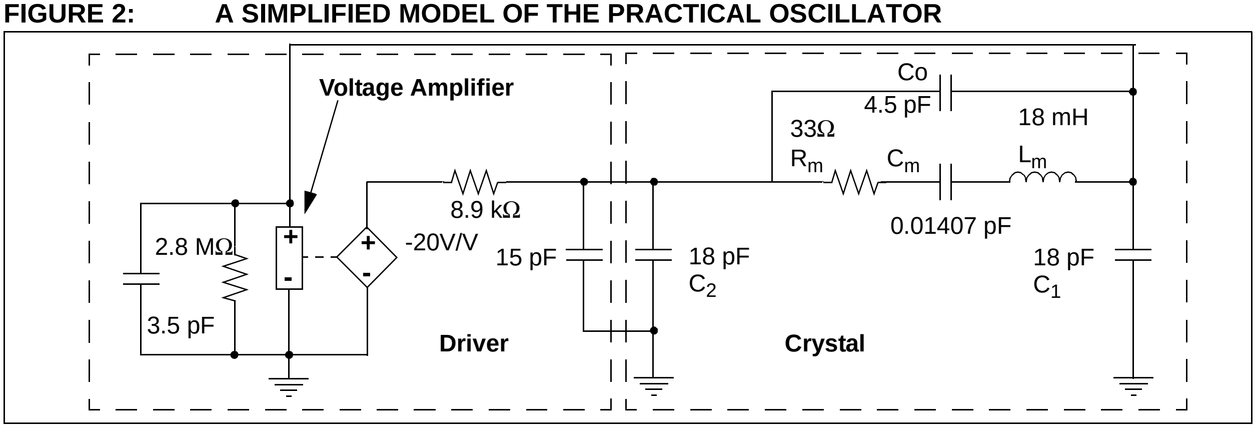
The purpose of this document is to explain the most critical aspects to designing and analyzing a reliable PICmicro MCU based oscillator.

Note:	Reading application notes AN826, *Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices* and AN849, *Basic PICmicro® Oscillator Design* prior to reading this application note is recommended. Concepts explained in the AN826 and AN849 are assumed to be prior knowledge.

The conditions for oscillation will be addressed in the first part of the document. The second part will look into the behavior of the crystal as part of a resonant tank and how the tank in turn, behaves when connected to the PICmicro device's driver to form an oscillator. The third part of the document discusses the typical gain headroom that an oscillator circuit needs to ensure reliable operation. The last section of the document introduces the reader to Negative Resistance Testing (NRT); a very simple yet reliable test that can evaluate an oscillator's performance.

Note:	The analysis in section two is done as a simulation study, but could also be done in the lab with the correct setup as described in **Section "Simulation Of The Oscillator's Open-Loop Response"**.

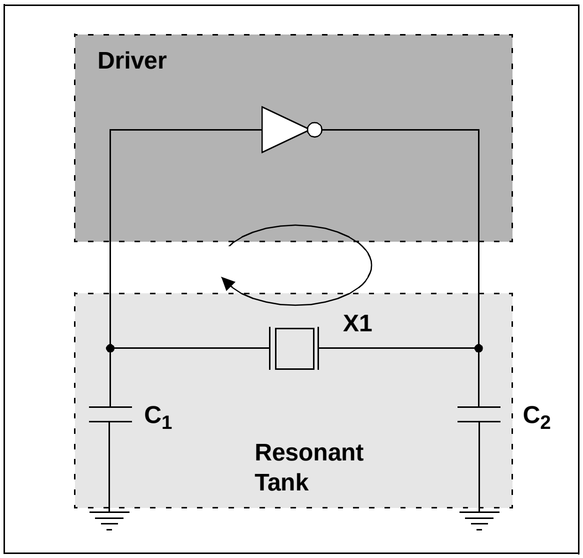
FIGURE 2: A SIMPLIFIED MODEL OF THE PRACTICAL OSCILLATOR



THE BARKHAUSEN CRITERIA

To achieve oscillation, the circuit must meet the Barkhausen criteria. The Barkhausen criteria states that the circuit must have a loop gain of unity or greater, and have a phase shift that is a multiple of 360°.

FIGURE 3: THE OSCILLATOR LOOP SHOWING TANK AND DRIVER PORTIONS



The driver portion of the oscillator circuit (Figure 3) is internal to the microprocessor. The external resonant tank consists of the crystal and the two load capacitors C_1 and C_2. The common reasoning is that the tank provides 180° of phase shift at the resonant frequency f_r with some signal attenuation. To meet the Barkhausen criteria, the driver must have sufficient voltage gain to ensure a total loop gain of unity or greater, and it must supply an additional 180° of phase shift. However, this common path of reasoning is not correct, especially at the higher frequencies in the megahertz ranges.

The reality of the design is that the driver provides power gain, not necessarily a voltage gain. At higher frequencies, the driver circuit has more than 180° of phase shift and can have a voltage gain less than unity when loaded. The passive resonant tank provides the missing voltage gain.

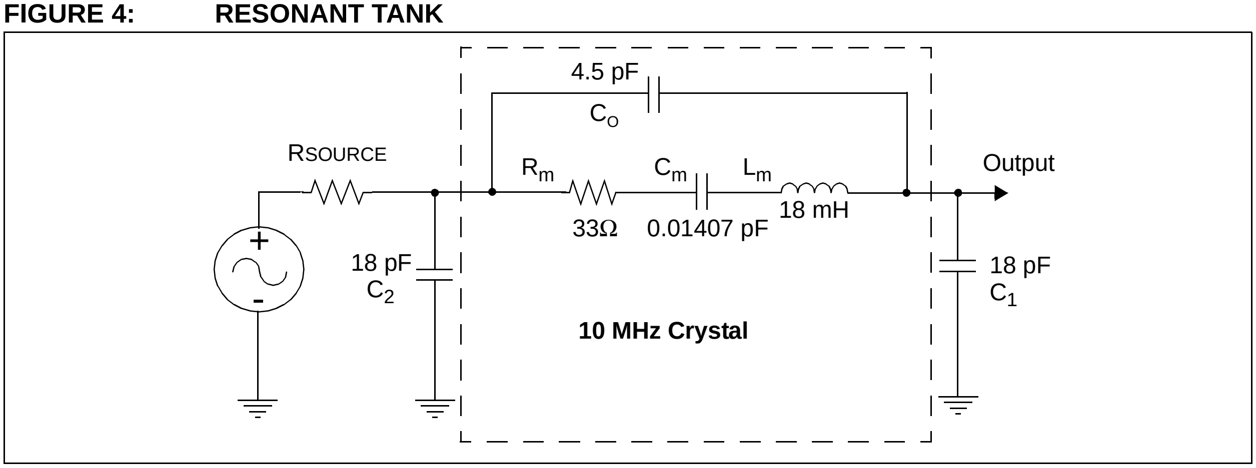
The rest of this document will use a generalized PICmicro MCU HS mode driver as an analysis example with a typical 10 MHz crystal. The load capacitors C_1 and C_2 are assumed to be equal to 18 pF.

Note:	These are general models and a specific device will vary greatly, but the same analysis techniques can be used.

THE PASSIVE RESONANT TANK

The resonant tank, shown in Figure 4, uses the equivalent of a 10 MHz crystal driven by a source voltage with an output impedance RSOURCE. The output is measured at C_1, which would be the input to the driver in a completed oscillator.

FIGURE 4: RESONANT TANK



The response of the passive resonant tank is shown in Figure 5, where RSOURCE is equal to 50Ω. It shows the crystal series resonant frequency, f_s, and anti-resonant frequency, f_a. It further shows the tank gain at 180° phase shift. At 180° of phase shift, the tank does attenuate the signal, but the passive gain increases as the frequency lowers towards f_s. It is important to point out that the maximum gain of the passive tank, at f_s, will reduce as the source impedance is increased. The reduction in gain is a result of lowering the Q or quality factor.

The maximum gain frequency will also move as the source resistance is increased, because C_2 is essentially shunted by a low-source impedance with little influence on the tank. The influence of the source impedance is shown in Figure 6 with the gray curve representing 50Ω and the black curve a 500Ω source impedance.

FIGURE 5: AC RESPONSE OF PASSIVE 10 MHz RESONANT TANK

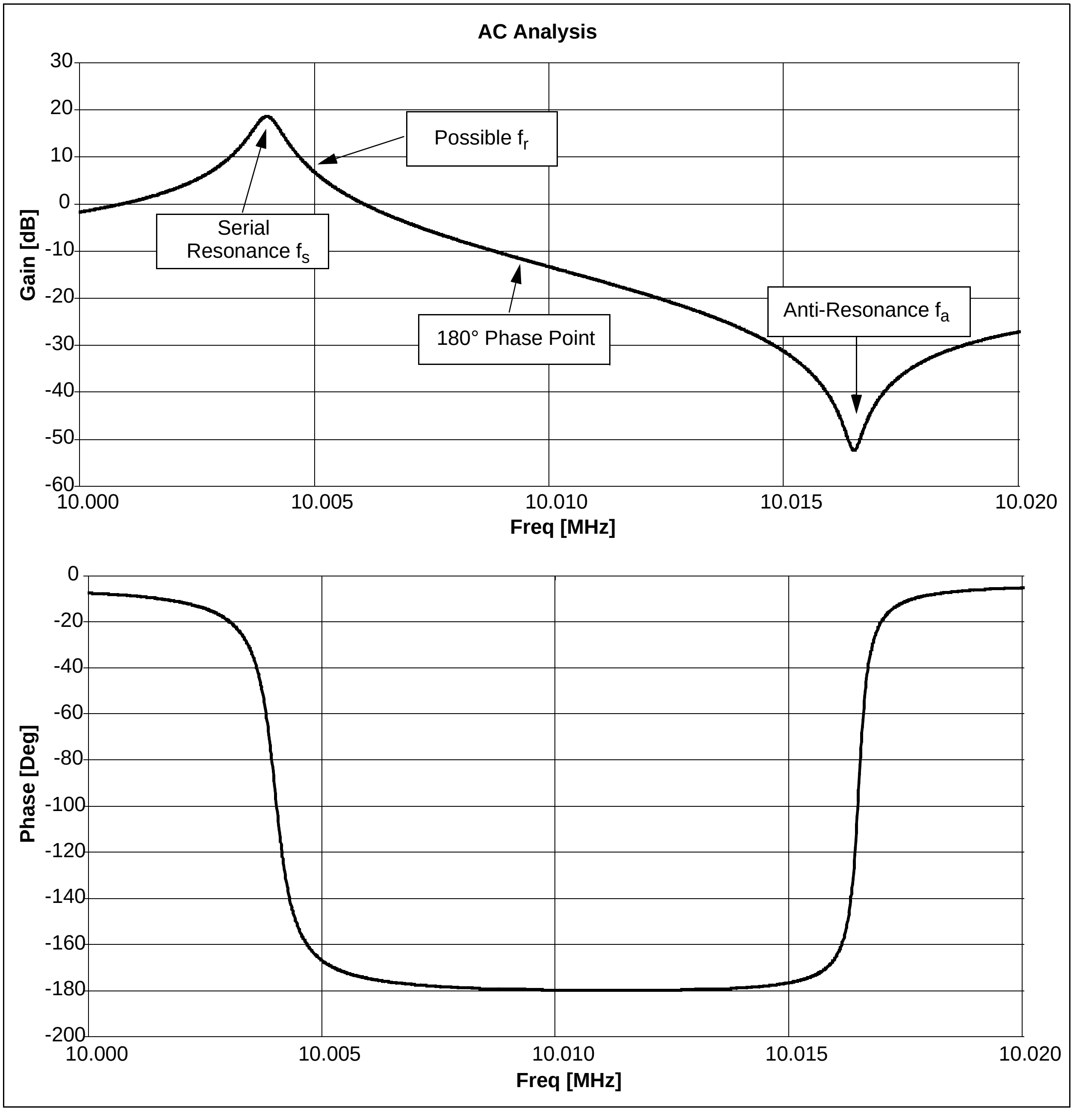
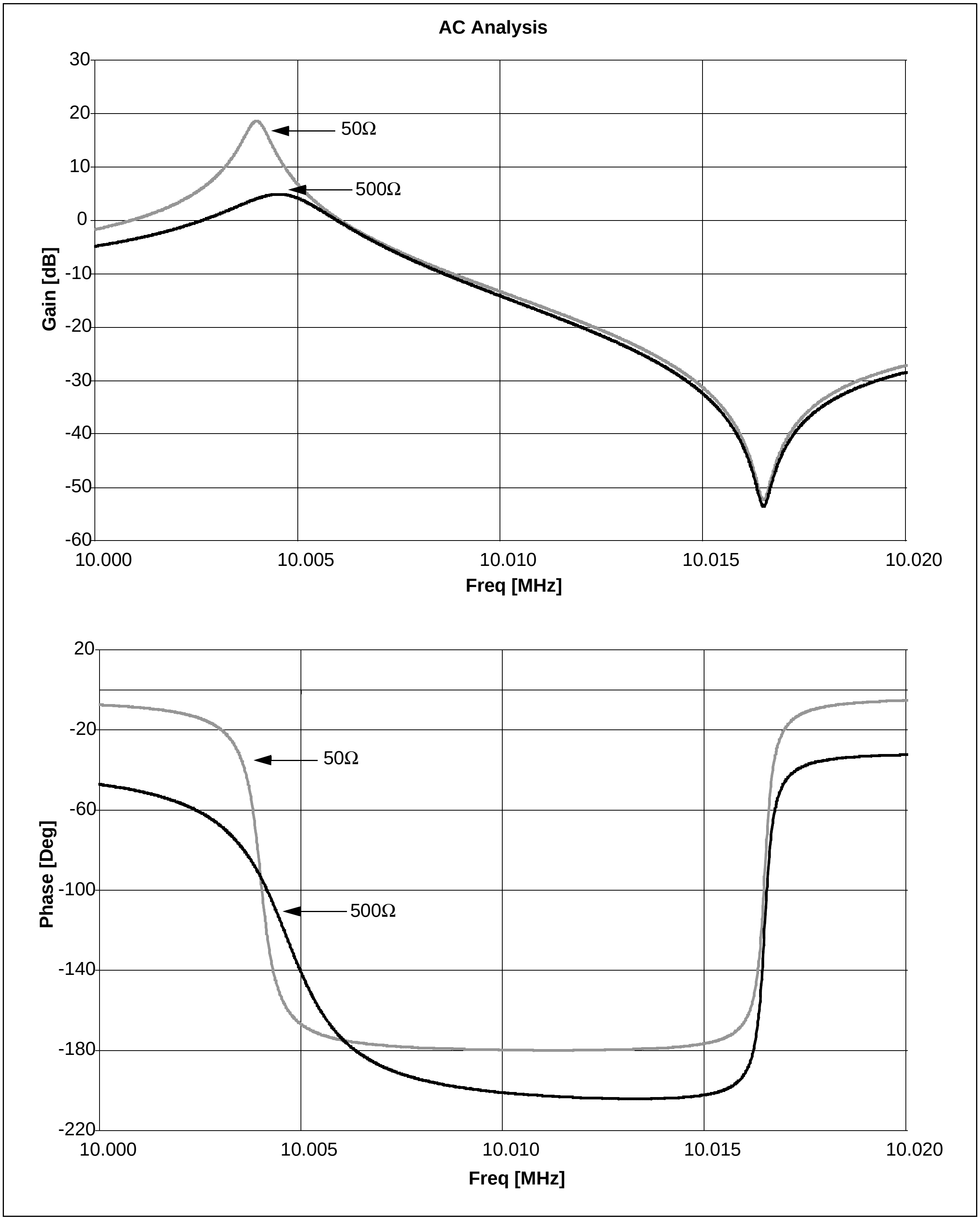


FIGURE 6: INFLUENCE OF SOURCE IMPEDANCE ON RESONANT TANK



ESR

An important, but often misunderstood subject, is referred to as the tank's Equivalent Series Resistance (ESR). The ESR is the resistance that the tank exhibits at the true series resonant frequency of the crystal or f_S. The ESR is translated to the motional resistance R_m of the crystal, as shown in Equation 1.

EQUATION 1:

$$ESR = R_m (1+C_O/C_L)^2$$

The ESR is translated as a function of the tank load capacitance C_L and the shunt capacitance C_0 of the crystal. The load capacitance C_L, as shown in Equation 1, is the serial combination of C_1 and C_2, as shown in Equation 2.

EQUATION 2:

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2}$$

ESR is often used in evaluations instead of the motional resistance R_m or R1. The exact positioning of the ESR is shown in Figure 7. The crystal's motional resistance R_m and ESR are directly related to the Q of the tank. It is important to understand that an increasing Q (decreasing R_m) will increase the tanks passive gain and, therefore, gain headroom. Later in this document Negative Resistance Testing (NRT) is introduced where some test resistance, RTEST, is deliberately placed in this position to evaluate the performance of the total resonator.

The ESR for the circuit in Figure 7 is calculated to be 74.25Ω at f_S using Equation 1. However, this is not the resistance that the driver circuit is loaded by at the resonant frequency f_r. The tank load at f_r is typically an order of magnitude larger than the ESR in this frequency range, as shown in **Section "The Driver Circuit"**.

THE DRIVER CIRCUIT

The PICmicro microcontroller's oscillator circuit typically has three separate gain or mode settings; LP, XT and HS. The LP mode is normally used with tuning fork crystals in the low frequency ranges such as 32 kHz watch crystals. The XT and HS modes have progressively more gain and are typically used for crystals in the megahertz ranges. The perception is that XT mode should be used in mid-frequency range, up to 4 MHz and HS, in the higher megahertz frequency ranges. This should be seen as a guideline and not as a hard-set rule. The data sheet for each device should be consulted for supply voltage and temperature ranges associated with each mode.

The small signal model for a typical(1) HS oscillator is shown in Figure 8. It can be thought of as an inverting amplifier, not a logic gate, with a gain(2) G_d of -20 or 26 dB. It also has a low-pass filter in the output path that causes the output gain to drop with frequency. The output pole also causes a phase delay in the output voltage. The simulated output response of the driver (see Figure 9) is given when driven by a low-impedance source into OSC1 and the output is taken at OSC2.

> **Note 1:** This is only a typical model and the model changes between different types of PICmicro devices. The model also varies from part-to-part as a function of manufacturing, supply voltage, temperature, etc.
>
> **2:** Gain is expressed as either a dimensionless number such as "10" or in dB where G[dB] = 20 • Log(VIN/VOUT).

FIGURE 7: PLACEMENT OF THE ESR AND THE MOTIONAL RESISTANCE

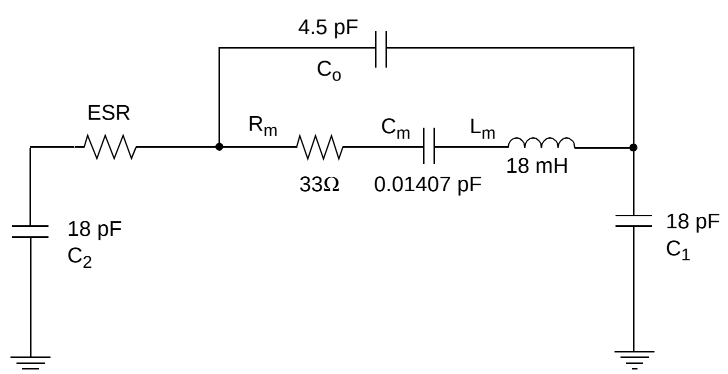


FIGURE 8: TYPICAL OSCILLATOR DRIVER EQUIVALENT MODEL – HS MODE

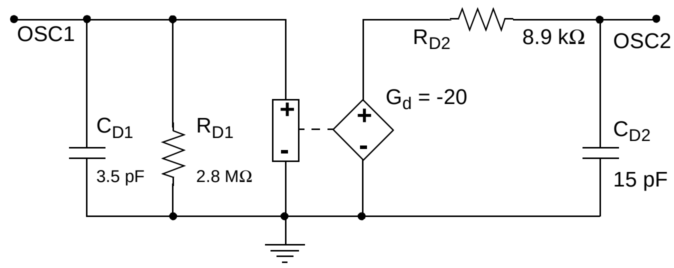
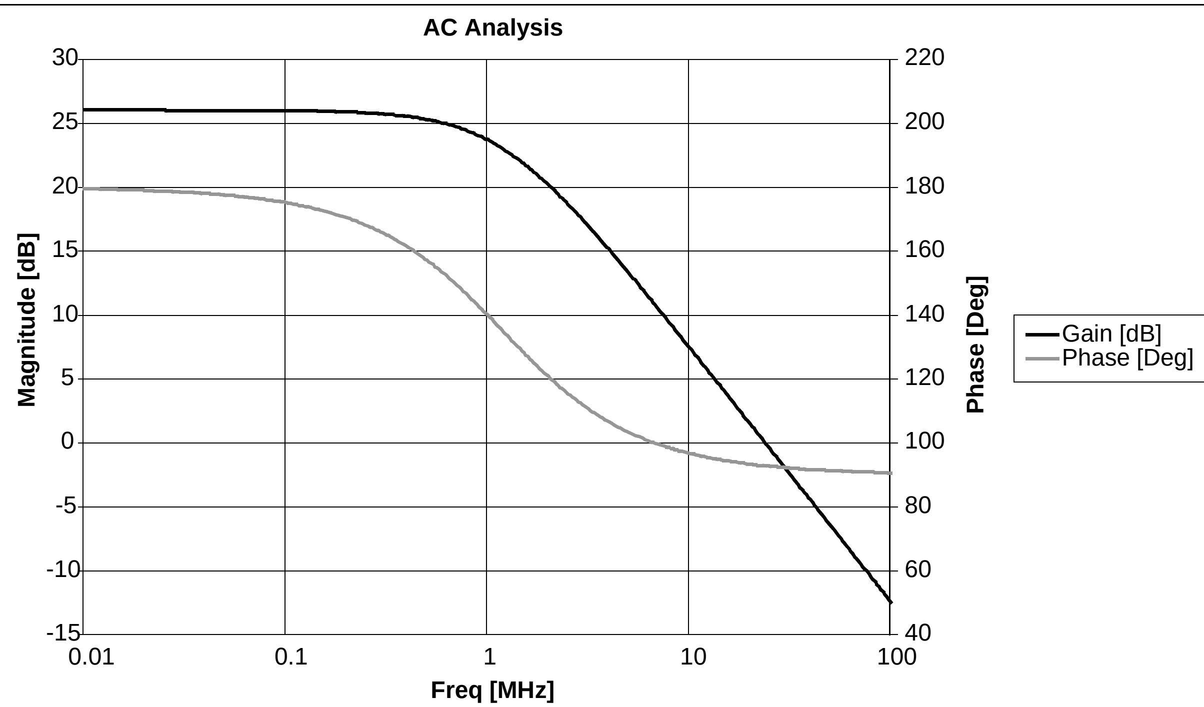
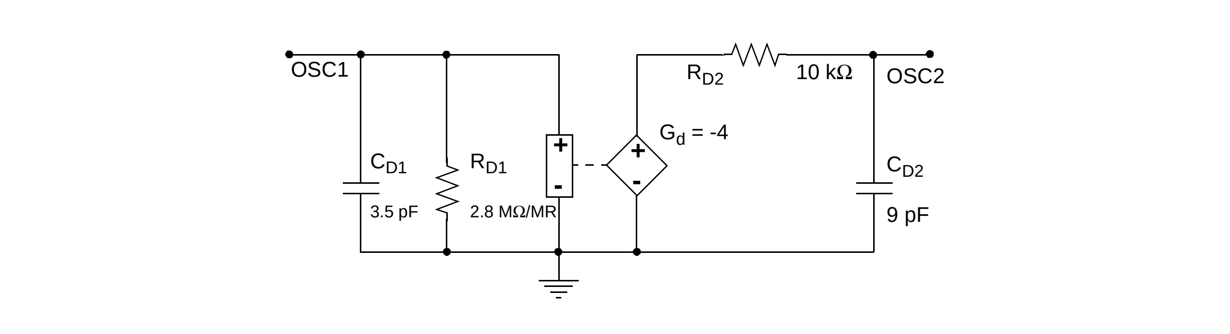


FIGURE 9: SIMULATED AC RESPONSE OF DRIVER – SMALL SIGNAL CASE IN HS MODE



The AC response and the model shown in Figure 8 and Figure 9 are for the small signal case only. The driver is based on a voltage amplifier with a low frequency gain of -20. The output gain of the driver is reduced with increasing frequency due to the output pole formed by a C_{D2}. The gain of the driver also falls off as the amplitude increases. This is an important aspect of the driver, because gain is needed under start-up conditions to increase the oscillation amplitude. The gain of the driver gradually decreases with increasing oscillation amplitude until the oscillator (driver and resonant tank) reaches unity gain. The large signal amplitude, where the oscillator reaches unity, is referred to as the Steady State Amplitude (SSA). The output pole results in a 3 dB cutoff frequency at 1.2 MHz. Any load that is connected to the output of the driver will change the impedance of the system and thus change its output characteristics. As an example, the unloaded gain at 10 MHz is about 7.5 dB, but is reduced to unity gain with a 550Ω load. The resistive load also reduces the phase shift relative to the open-loop phase response.

FIGURE 10: TYPICAL OSCILLATOR DRIVER EQUIVALENT MODEL – XT MODE



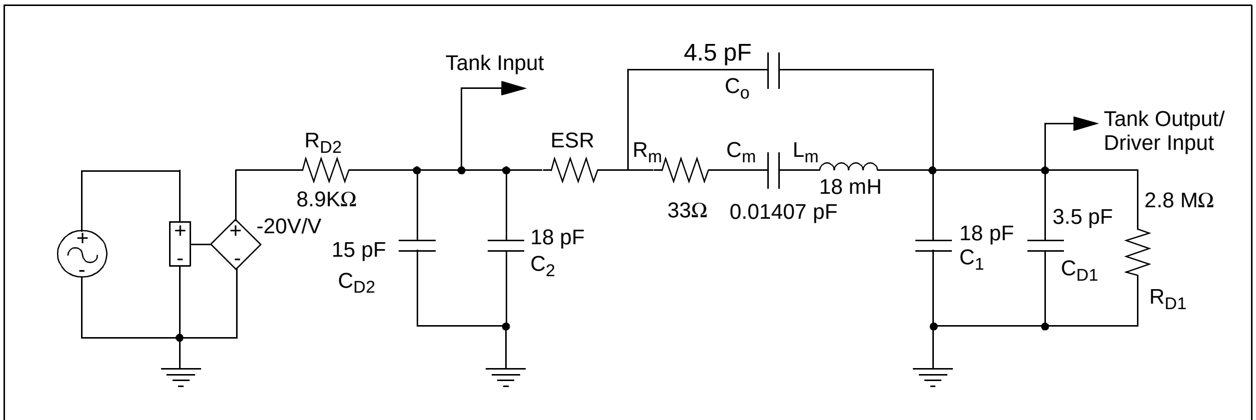
A typical(1) XT driver's equivalent model is shown in Figure 10. It is interesting that the gain is lower than the HS driver's gain, but it has a higher 3 dB frequency of about 1.8 MHz. This leads into the next stage of the analysis, which is to connect the tank and the driver to study the open-loop response of the oscillator.

Note 1:	This is only a typical model, and the model changes between different types of PICmicro devices. The model also varies from part-to-part as a function of manufacturing, supply voltage, temperature, etc.

SIMULATION OF THE OSCILLATOR'S OPEN-LOOP RESPONSE

Figure 11 shows the simulation model for analyzing the open-loop response of the oscillator under small signal start-up conditions. The loop is opened at load capacitor C_1, normally connected to the driver's input on pin OSC1. The input impedance of OSC1, consisting of C_{D1} and R_{D1}, is connected to C_1 from where the output is taken. The addition of the driver's input and output impedance needs to be taken into account as far as the ESR is concerned. The ESR recalculates to about 60Ω with a new C_L of 13 pf, that was previously 9 pF.

FIGURE 11: OPEN-LOOP SIMULATION MODEL OF THE OSCILLATOR



The response of the open-loop model is shown in Figure 12. The black curve is the output and the gray curve is the tank-input signal. The resonant frequency f_r, at start-up, is greater where the phase is zero and the gain is unity or more, in accordance with the Barkhausen criteria. It is interesting to compare the output signal to the tank-input signal, as it shows the predicted low ESR at f_s, where the tank loads the output driver. Figure 12 shows that at f_r, the tank's input impedance is significantly higher than the ESR. From the simulation results, one can calculate the tank's input impedance at f_r to be in the order of 1 kΩ, which is significantly higher than the ESR at f_s of 60Ω.

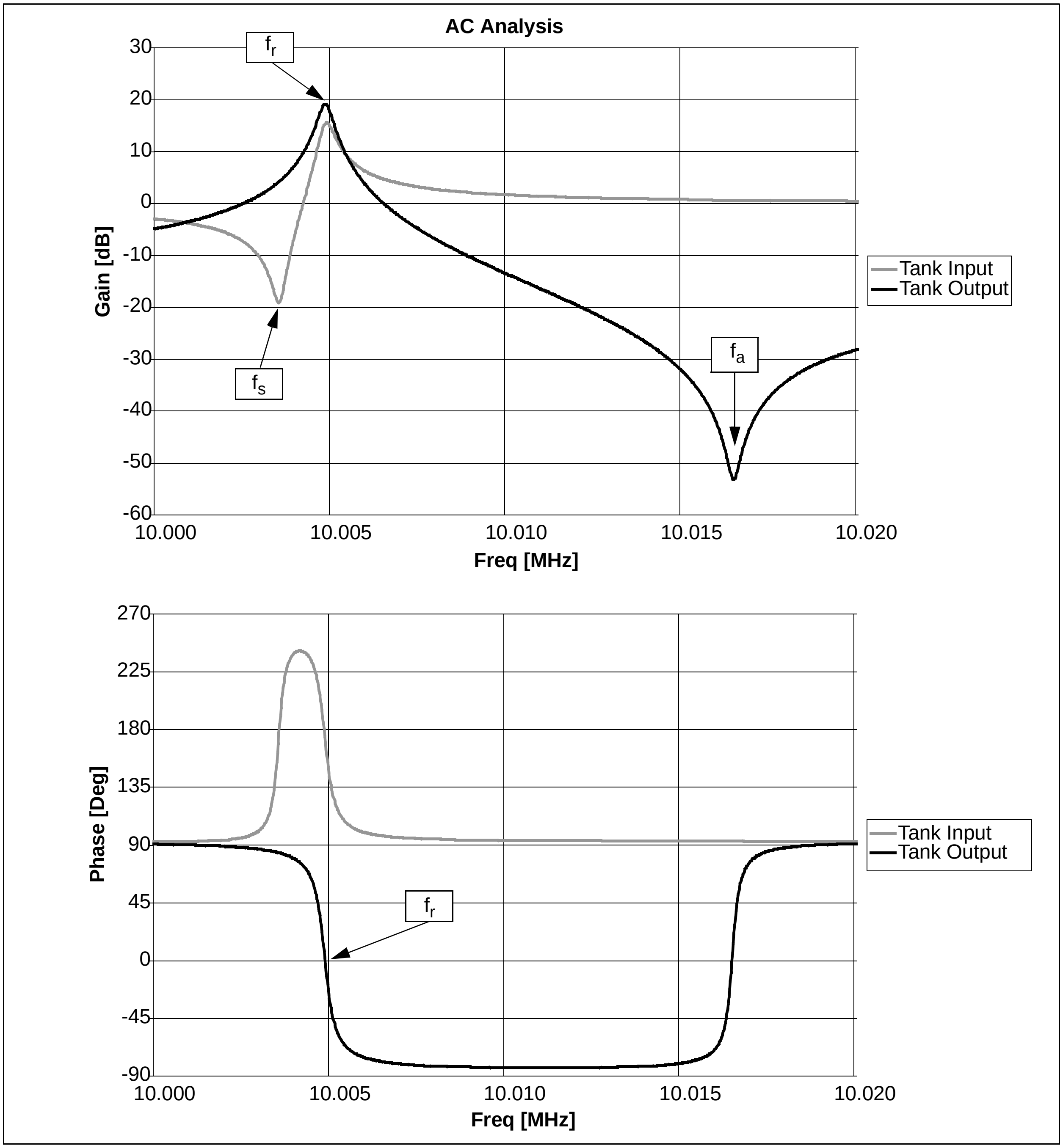
The analysis can be performed in the lab to validate the simulation. It is important to realize that the circuit is very sensitive to any loading by measurement probes or sockets. Therefore, it is necessary to use either active probes or dedicated buffers when measurements are taken. Even very high input impedance buffers have 1 or 2 pF of input capacitance, and this must be taken into account by subtracting the buffer's impedance from C_1 and C_2, as is necessary. One solution is to use a TI Burr-Brown OPA655 or OPA354 operational amplifier as a unity gain buffer. The traces from the point of measurement to the input of the buffer should be kept as short as possible. Try to make the trace less than 1 cm.

Gain Headroom

The simulation in Figure 12 shows that there is about 20 dB of gain headroom at the resonant frequency. Any gain above unity will cause the oscillation amplitude to increase, or grow, and the higher the gain, the sooner one will reach the SSA where the gain is unity. The gain headroom of the oscillator will be affected if any part of the oscillator changes, that has an affect on gain. The resonant tank's gain is reduced to 14 dB for a worst case part (from a typical 20 dB), if it is known that the worst case driver is 6 dB lower than the typical driver.

It would seem as if the goal of designing the oscillator is to get the maximum gain headroom, yet it is undesirable to have too much gain. Excessive gain may cause the crystal to resonate at one of the crystal's overtone frequencies. It can also result in an excessively large SSA, exceeding the crystals drive level. A large SSA can further cause unwanted distortion, noise and radiation. The goal is to have just enough gain to ensure operation.

FIGURE 12: AC RESPONSE OF THE OSCILLATOR'S OPEN-LOOP ANALYSIS

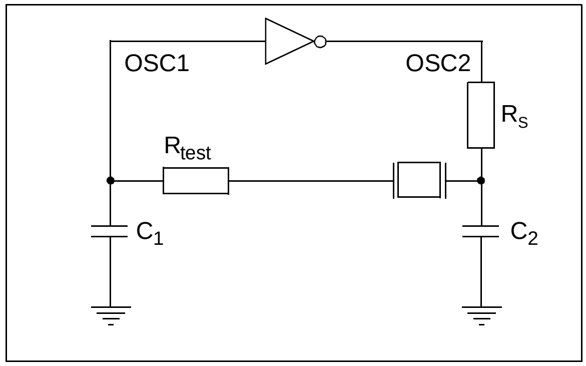


Limiting Gain Headroom And The Steady State Amplitude

A very effective method to reduce the maximum gain, and/or the SSA, is to add a series resistor R_S between the output of the driver and the tank, as shown in Figure 13. Adding a voltage divider on the output reduces the SSA and the unwanted effects of over driving the crystal where this may be an issue. It also increases the drive impedance to the tank, reducing its Q and passive gain. The gain can again be increased if the requirement is only to reduce the SSA by impedance matching of the tank. The tank impedance matching is done by changing the size of C_2, and typically involves increasing the value of C_2, thus lowering the source impedance to the tank. Increasing the value of C_2 requires that the value of C_1 be decreased. This is to maintain CL, as specified by the crystal manufacturer. Increasing the size of C_2 beyond the ideal impedance will reduce the gain because it will overload the driver. A rule of thumb is to not make C_2 more than twice the size of C_1 while maintaining C_L. With the addition of R_S, one can ignore the influence of C_{D2} on C_L, assuming that $R_S > 1/(2\pi \bullet f_s \bullet C_L)$.

Another advantage of adding R_S is that it forms a low-pass filter with C_1, reducing the chances of overtone oscillation. It can also reduce the start-up period of the tank because it adds thermal noise and increases the phase delay to the tank. Decreasing the start-up period with the addition of R_S will be more noticeable with lower frequency designs that operate below the 3 dB frequency of the driver's output pole.

FIGURE 13: THE POSITION OF RS AND RTEST IN THE RESONANT TANK



It is strongly advised to add R_S to the standard oscillator circuit in the final application, even if it is populated with a zero ohm resistor. Having the ability to add it to a future design can prove helpful when migrating to a different microprocessor or changing the crystal. The resistor RTEST is only needed when doing open-loop analysis and NRT.

Choosing Gain Headroom

The preceding text explained the general behavior of the oscillator and how it is possible to change the oscillator's gain, frequency, phase and amplitude response. The next part of the text will focus on choosing a typical gain headroom. The two variable factors that dictate the gain headroom requirement are the drivers gain G_d and the crystal's motional resistance R_m. Practical devices have fairly consistent values for G_d and R_m, but some parts do deviate from the typical values within some limits. It is possible that some worst case oscillators have a driver with a lowest possible G_d and a crystal with the highest possible R_m. The oscillator's gain headroom, or Gh_O, should be high enough to ensure that the oscillator is able to operate and start-up reliably with worst case devices. The Gh_O is the product of both the amplifier's gain headroom requirement Gh_D and the crystal's gain headroom requirement Gh_C, as per Equation 3.

EQUATION 3:

$$Gh_O = Gh_D \times Gh_C$$

Driver Gain Headroom Guidelines

Microchip maintains matrix characterization parts for some devices that go through deliberately skewed processes to determine the extremes of product variation. One specific product's matrix variation in amplifier trans conductance is shown in Table 1 below.

TABLE 1: EXAMPLE GAIN VARIATION AND GAIN HEADROOM OF A SPECIFIC HS DRIVER DATA AT 5 VDD(1)

Temp °C	Variation			Typical Gain Headroom Gh_D			Maximum Gain Headroom Gh_D		
	Minimum	Median	Maximum	Minimum	Median	Maximum	Minimum	Median	Maximum
-40	1.17	1.41	1.6	N/A	N/A	N/A	N/A	N/A	N/A
25	0.81	1	1.12	1.23	N/A	N/A	1.38	1.12	N/A
125	0.65	0.79	1	1.54	1.27	N/A	1.72	1.42	1.12

Note 1: The values given in this table are for example only.

One can make the generalized assumption that the typical driver in Figure 8 has a mean G_d at room temperature of -20. The worst case G_d at 125°C would be the typical G_d times the variation, or -20 x 0.65 = -13, and the best would be at -40°C being -20 x 1.6 = -32.

The driver's Gh_D, from a typical room temperature part to a worst case part at 125°C, is the inverse of the variation as 1/0.65 or 1.54. This means that if one ignores the variation of the crystal that a typical oscillator with gain headroom of 1.54 (3.75 dB) will still meet the Barkhausen criteria if replaced by a worst case part at 125°C. The “Typical Gain Headroom” values are to be used if one uses a couple of truly typical parts for analysis that have been randomly selected from different manufacturing lots. However, if one only has a small number of parts, then it is safer to use the ”Maximum Gain Headroom” values that assume the analysis was done with maximum gain parts.

There are two methods to account for the gain reduction from the typical oscillator. The first is well suited for analysis, and that is to simply change G_d in the equivalent model. The second method is well suited for lab analysis, and that is to introduce RTEST. The gain of the tank is inversely proportional to ESR. One needs to add RTEST, as per Equation 4, which will reduce a typical oscillator's gain by the appropriate value.

EQUATION 4: USED TO CALCULATE RTEST VALUE TO ADD A TYPICAL OSCILLATOR

$$R_{TEST} = R_{MTYPICAL}\,(Gh_D - 1)(1 + C_O/C_L)^2$$

RMTYPICAL – Typical motional resistance of crystal
Gh_D – Gain headroom from Table 1

Example: A typical oscillator, with a crystal that has a R_m = 33Ω, C_O = 4.5 pf and C_L = 13 pf. Calculate the RTEST value that will result in the same gain as a 125°C lowest gain device.

From Table 1, Gh_D = 1.54, Equation 4 is then calculated as in Equation 5.

EQUATION 5:

$$R_{TEST} = 33(1.54 - 1)(1 + 4.5\ pF/13\ pF)^2 = 32.3\Omega$$

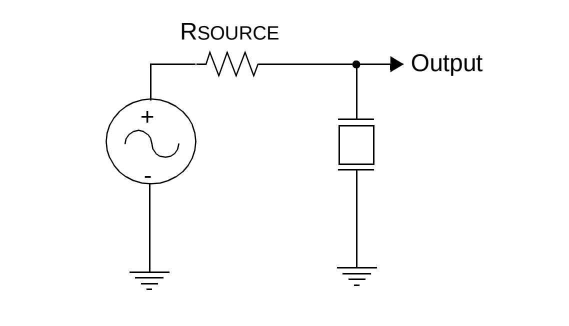
Crystal Gain Headroom Guidelines

The crystal's gain headroom requirement Gh_C can be broken up into two parts; the first part is needed to compensate for RM deterioration and the second is to ensure good start-up. Crystal manufacturers have different guidelines for variations in R_m. One reputable manufacturer claims that the worst case values are no more than 30% higher than the typical value. The manufacturer also recommended that a total crystal, $Gh_C = 3$, be used to compensate for the 30% R_m deterioration and start-up. This means that a gain headroom of about 2 is sufficient for crystal start-up with a comfortable safety margin, because it is not wise to operate on the filter to oscillator margin. Equation 4 is used in a similar manner to add RTEST when analyzing the crystal performance. Just the R_m deterioration component can be studied by using $Gh_C = 1.3$. Make sure that the oscillator still has a gain of 2 left over for start-up. The alternative is to use the full $Gh_C = 3$ to calculate RTEST, but then the oscillator should have unity gain or greater.

The total oscillator Gh_O would thus be about 4.6 when using typical parts and approximately 5.2 when using a small sample of parts. This would ensure proper operation at up to 125°C with a worst case driver and crystal. This guideline is on par with some other reputable crystal manufacturers' guidelines to have a Gh_O of 5 to account for temperature and worst case part deviations.

One problem is that most crystal manufacturers only specify the worst case value for R_m, but the typical value can be measured, as shown in Figure 14. Place a known source resistor in series with a signal generator that can be swept in 1 or 2 hertz steps around the crystals operating frequency. A high-impedance probe is used to find the lowest output voltage, VOUT-MIN, at crystal's serial resonant frequency f_S. The value for RSOURCE should have a similar value as the expected value for R_m. Using Equation 5, the value for R_m can then be calculated from VSOURCE, RSOURCE and VOUT-MIN.

FIGURE 14: SETUP TO DETERMINE R_m



EQUATION 6:

$$R_m = \frac{V_{OUT} \cdot R_{SOURCE}}{V_{IN} - V_{OUT}}$$

NEGATIVE RESISTANCE TESTING (NRT)

Negative Resistance Testing (NRT) is a very simple and reliable test that can be performed without the need for specialist equipment. NRT is done to validate an oscillator design, or used as a design basis.

To evaluate if an existing design or product has enough gain headroom, one would add a resistor RTEST in series with the crystal, as shown in Figure 13. It is not necessary to make special provisions for the resistor; one can lift a lead or the side of the crystal package and place a small 0603 surface mount resistor between the lead and the PCB pad. The resistor is then iteratively increased until the maximum value is reached where the oscillator starts up reliably. With RTESTMAX, calculate Gh_O. To do this, one needs the ESR, the translated motional resistance R_m (see Equation 1). The calculation is summarized in Equation 7 by the reordering of Equation 5.

Note:	A tuning pot is not recommended as it has too much parasitic capacitive and inductive loading. However, it can be used to get within the right range.

EQUATION 7:

$$Gh_O = \frac{R_{TEST}}{ESR} + 1 = \frac{R_{TEST}}{R_{MTYPICAL}\,(1 + C_0/C_L)^2}$$

RMTYPICAL – Typical motional resistance of crystal
Gh_O – Oscillator gain headroom

The load capacitance calculation should also include the board capacitance (about 2-3 pF) and the driver's capacitance, as shown in Equation 8.

Note:	One can ignore the influence of C_{D2} on C_L assuming that $R_S > 1/(2\pi \cdot f_s \cdot C_L)$.

EQUATION 8:

$$C_L = \frac{(C_1 + C_{D1}) \cdot (C_2 + C_{D2})}{C_1 + C_{D1} + C_2 + C_{D2}} + C_B$$

The test can then be repeated with a number of different parts and the results averaged to get typical results. The tests should be conducted with the lowest expected supply voltage because the driver's gain is supply voltage dependent. The tests can be done at room temperature or at the highest expected temperature, noting that the high temperature gain headroom will be affected, as was discussed in the **Section "Driver Gain Headroom Guidelines"**. One can further consider simulating other environmental conditions, such as humidity or radiation that the circuitry may be exposed to.

To test proper start-up, it is best to write a firmware routine that periodically puts the part in Sleep mode and then uses an interrupt, via a button push or Watchdog Time-out, to reset the part and go through a start-up routine. Make sure that there is enough Sleep time to have the oscillator completely stop. Do not simply switch the whole circuit off and on because this introduces a sharp transient that helps the start-up process. Another practical tip is to not use sockets unless the final product uses a socket for the PICmicro device.

Some crystal manufacturers use the following terminology with NRT:

- $R_{TESTMAX}$ is referred to as the "safety margin"
- "Oscillation allowance" is referred to as the "safety margin" plus ESR

A ratio is specified between oscillation allowance and ESR, which is the same as the definition for gain headroom or Gh_O in this document.

Negative Resistance Testing (NRT) as a Design Tool

NRT can be used very effectively during the design process. The first step is to choose a specific frequency crystal from a reputable crystal manufacturer. Choose a Gh_C based on the crystal manufacturer's specifications in R_m and start-up requirements, that also incorporate some safety buffer. Next, choose a Gh_D based on the driver variations for the specific PICmicro MCU used. The values in Table 1 are good guideline values. With a total target gain headroom, one can calculate R_{TEST}, a rule of thumb; $Gh_D \approx 5$. Capacitors C_1 and C_2 are calculated using Equation 7, based on the crystal manufacturers recommended C_L value. Make C_1 and C_2 equal in value, but do not include C_{D2} in the calculation because R_S will be used. With the calculated values for R_{TEST}, C_1 and C_2 and the data sheet recommended Oscillator mode, find the maximum R_S resistor value with R_{TEST} in place where the oscillator starts up reliably. If $R_{SMAX} > 1/(2\pi \bullet f_s \bullet C_L)$, then the process design is done. If not, use the impedance matching guidelines under the **Section "Limiting Gain Headroom And The Steady State Amplitude"** to increase the gain. Also, try a higher gain mode if possible, as an example try using HS instead of XT.

CONCLUSION

It is possible to analyze in simulation and in the lab what the small signal gain or gain headroom of an oscillator is. It is important that the oscillator have enough gain to ensure reliable start-up and operation even with worst case devices. A method is given to choose a safe gain headroom and how one can simulate the effects of worst case devices by introducing a test resistor in the resonant tank. The design can be verified by a simple but effective negative resistance test, which can also be used during the design of the oscillator tank.

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Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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