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APPLICATION NOTE

GATE DRIVE DESIGN FOR LARGE DIE MOSFETS

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Presents design rules for proper design and layout of gate drive circuitry.

GATE DRIVE DESIGN FOR LARGE DIE MOSFETS

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ABSTRACT

The important criteria and parameters for designing MOS gated devices are identified. Design rules for proper layout are described. Discrete driver circuits such as complimentary bipolar and MOSFET totem pole topologies are evaluated. Test results of the discrete solutions and several integrated circuit drivers are compared. The pros and cons of each driver, as related to driving high input capacitance large die MOS devices, are discussed. A computer analysis technique is presented which predicts the performance of the drive circuitry and how the performance will be affected by layout. An example of a layout induced problem, slow switching speed, is predicted using the computer program.

Introduction

The trend in today's power conversion market towards higher power density, requiring higher frequency operation and improved efficiency, has lead to the need for using parallel MOSFETs or larger die MOSFETs. The foray into using these high capacitance devices and circuits have left some designers with an uneasy feeling about what approach to use.

The successful design of robust gate drive circuitry for high voltage, very high current MOSFET devices is no different than designing driver circuitry for smaller devices and depends on an understanding of the drive requirements, a good model to predict the results, careful attention to the physical layout of the driver board and the selection of the proper circuit topology.

Figure 1 represents a generic gate driver circuit where the switching speed is controlled by the total gate impedance (R_G), the total source inductance (L_S), the load resistance and the device characteristics. Once the load is defined and the power switching device is selected, fast switching speed is achieved by minimizing the two remaining parameters, R_G and L_S.

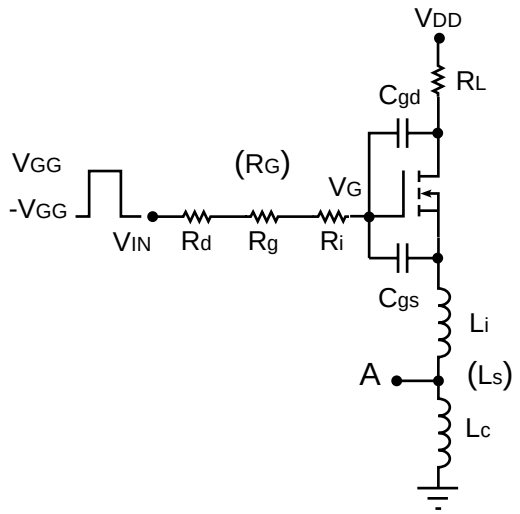

Figure 1

The following discussion is done using a single MOSFET device. However, the equations can be extended to parallel devices by combining the parameters of the parallel combination and treating the parallel devices as a single lumped device.

Turn-On

The resistive load turn-on waveforms of a Power MOSFET, Figure 2, can be divided into 3 intervals. The first interval is the period it takes for the gate voltage to rise to a value where the device just begins to conduct and is controlled by the input capacitance and input impedance. The second interval is the period it takes the drain voltage to reach its minimum and the drain current to reach its maximum. This period is controlled by the input impedance, the gate-drain and gate-source capacitances, the source inductance, the G_M of the device and the load current. This period is the most complex and represents the turn-on power losses. The third interval is the period it takes the gate voltage to complete its rise to the gate drive supply voltage and is controlled by the input impedance and the input capacitance.

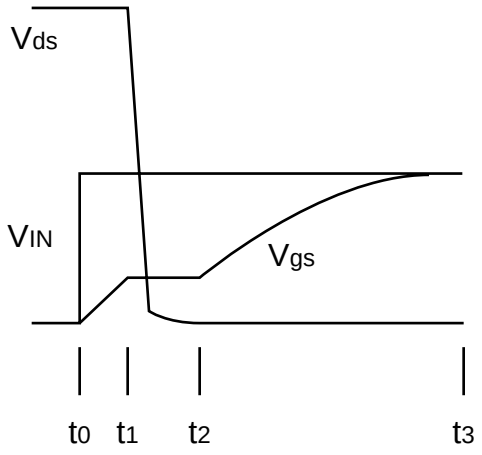

Figure 2

Interval 1 (t_0 - t_1)

This period begins with the transition of the input voltage (V_{IN}) from the low value of the gate drive voltage ($-V_{GG}$) to the high value of the gate drive voltage (V_{GG}) and ends when the gate voltage reaches a value where drain current begins to flow ($V_{GS(ON)}$). For this analysis the V_{IN} transition will be defined as a step function and occurs in zero time. As no Drain current flows during this period, the Drain voltage will remain at the supply voltage (V_{DD}).

The equivalent circuit for this period, shown in Figure 3, is an R-C network made up of the input impedance (R_G) and the input capacitance C_{iss}. R_G is the sum of the driver impedance, the gate resistor and the internal gate impedance.

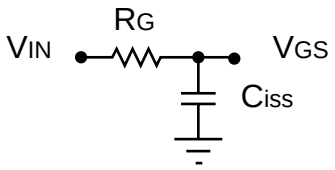

Figure 3

The time of the period and the waveform can be calculated from the R-C time constant formula:

$$V_{GS(ON)} = \Delta V_{GG}\left(1 - e^{\frac{-t}{R_G \cdot C_{iss}}}\right) \qquad (1)$$

Solving equation (1) for t:

$$t = R_G \cdot C_{iss} \cdot \ln\left(\frac{\Delta V_{GG}}{\Delta V_{GG} - V_{GS(ON)}}\right) \qquad (2)$$

Where ΔV_{GG} is the total voltage swing of V_{IN}.

From equation (2) the device in Figure 1 would have an interval of 1 of:

$$t = 58 \cdot 2890E - 12 \cdot \ln\left(\frac{15}{15 - 4.2}\right)$$

t = 55nsec

Where C_{iss} is the typical value from the data sheet and $V_{GS(ON)}$ is from the TRANSFER CHARACTERISTICS curve from the data sheet Figure 4.

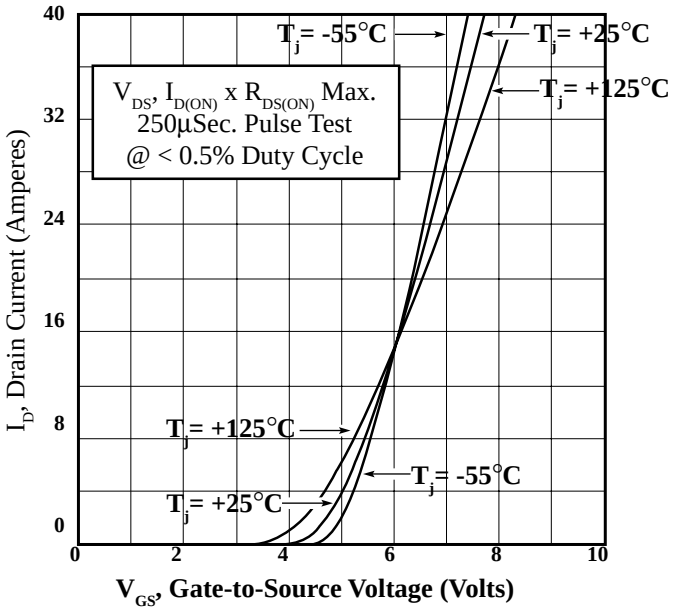

Figure 4
Typical Transfer Characteristics

Interval 2 (t_1 - t_2)

This period begins when drain current starts to flow, at the end of interval 1, and ends when the drain current (I_D) reaches its maximum value. The period is marked by the gate voltage plateau caused by the Gate-Drain capacitance C_{gd} in conjunction with the falling Drain voltage, known as the Miller Effect.

Reading some papers on MOSFET gate drive and switching performance leads one to believe that the rise time of the drain current lasts for the same time as the gate voltage is showing the Miller Effect. The following analysis will show this is not true.

Using Kirchoff's Law, an approximate equation for the gate node (when the rate of change of V_{gs} is much less than the rate of change of V_{ds}) is:

$$\frac{V_{IN} - V_G}{R_G} - C_{gd}\frac{dV_{ds}}{dt} - C_{gs}\frac{dV_{gs}}{dt} = 0 \qquad (3)$$

Solving equation 3 for dt:

$$dt = \frac{R_G(C_{gd}\cdot dV_{ds} + C_{gs}\cdot dV_{gs})}{V_{IN} - V_G} \qquad (4)$$

The change in gate voltage is related to the change in drain voltage by:

$$dV_{gs} = \frac{d_{id}}{G_M} = \frac{dV_{ds}}{G_M \cdot R_L} \qquad (5)$$

Combining (4) and (5):

$$dt = \frac{R_G\left(C_{gd} + \frac{C_{gs}}{G_M \cdot R_L}\right)dV_{ds}}{V_{IN} - V_G} \qquad (6)$$

Also:

$$V_G = V_{GS(ON)} + \frac{I_D}{G_M} + L_S\frac{di_d}{dt} \qquad (7)$$

And the rate of change of drain current is related to the rate of change of Drain voltage by:

$$\frac{di_d}{dt} = \frac{1}{R_L}\frac{dV_{ds}}{dt} \qquad (8)$$

Combining (6) (7) and (8):

$$dt = \frac{R_G\left(C_{gd} + \frac{C_{gs}}{G_M \cdot R_L}\right)dVds}{V_{IN} - V_{GS(ON)} - \frac{I_D}{G_M} - \frac{L_S}{R_L}\frac{dV_{ds}}{dt}} \qquad (9)$$

Solving equation (9) for dt:

$$dt = \frac{\frac{L_S}{R_L} + R_G\left(C_{gd} + \frac{C_{gs}}{G_M \cdot R_L}\right)}{V_{IN} - V_{GS(ON)} - \frac{I_D}{G_M}} \cdot dV_{ds} \qquad (10)$$

The solution of equation (10) is not straight forward as C_{gd} is voltage dependent and varies as a function of the drain-Source voltage and G_M is a function of the drain current. An incremental solution of equation (10) can easily be done using a spreadsheet and 25 Volt incremental values for dV_{ds}.

Interval "3" (t_2 - t_3)

This period begins when (I_D) reaches its maximum value and ends when C_{iss} is fully charged. Like the first period the equivalent circuit is an R-C network made up of R_G and C_{iss}. The time of the period and the waveform can again be calculated from the R-C time constant formula equation (2). However, the value for C_{iss} is much larger than in the first interval as the drain-source voltage is much lower. This interval is not of major concern as all activity with the drain voltage and current has been completed before this interval starts.

Turn-Off

The resistive load turn-off waveforms of a Power MOSFET, shown in Figure 5, can be divided into three intervals, like the turn-on. The equations for calculating the periods and waveforms are simply the reverse of the turn-on where interval "1" will be interval "3", interval "2" is interval "2" and interval "3" will be interval "1".

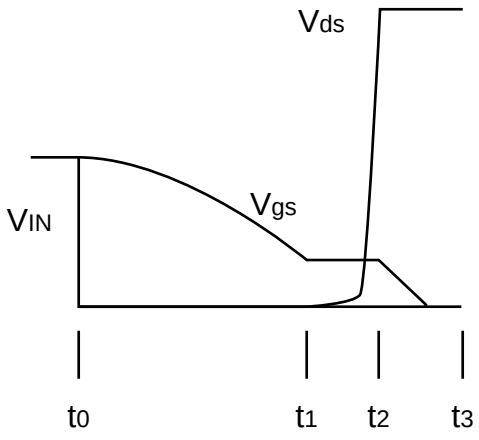

Figure 5

Figures 6 and 7 show actual switching waveforms from an APT5020BN switching a 10.5 ohm load, 250 volts with a 51 ohm gate resistor. Four (4) ohms was used for R_d and 3 ohms was used for R_i. The calculated switching waveforms are overlaid with dots. The correlation between calculated and measured is very good, proving the validity of equations (2) and (10).

Layout Considerations

As the preceding section illustrated, switching a MOSFET on and off only requires the charging and discharging of the input capacitance. The ease of charging and discharging this capacitance leads to "simple gate drive". However, this seemingly simple circuitry is not without its problems and pitfalls. It is simple only when compared to bipolar drives.

Problems most often encountered with the gate drive circuit are voltage spikes large enough to rupture the gate oxide, oscillation, ringing or false turn-on. Usually, these problems are with the layout and not in the electrical design of the driver circuit. To minimize these problems, the following design rules and precautions should be followed when designing and laying out driver circuits.

As illustrated in the previous section, the source inductance, acting as a negative feedback to the gate drive, plays a significant role in the switching speed. The source inductance in the package (L_s) of the device cannot be reduced by the user but the inductance relating to the connecting circuitry (L_c) can be mitigated. The problem section is where the gate signal and the load current share the same conduction paths, Figure 1. Therefore, the load current should be diverted from the gate signal path as soon as possible. The closer to the source terminal of the device the better.

Connecting the gate driver return to ground, instead of point A, Figure 1, adds the inductor L_c to the L_s term of the switching speed equation (10) causing the switching time to increase. Each additional inch of circuity will add as much as 20 nanoHenrys. Adding 20 nH to the switching speed calculation changed the results from a 20 nsec rise time to a 70 nsec rise time, a 350% increase.

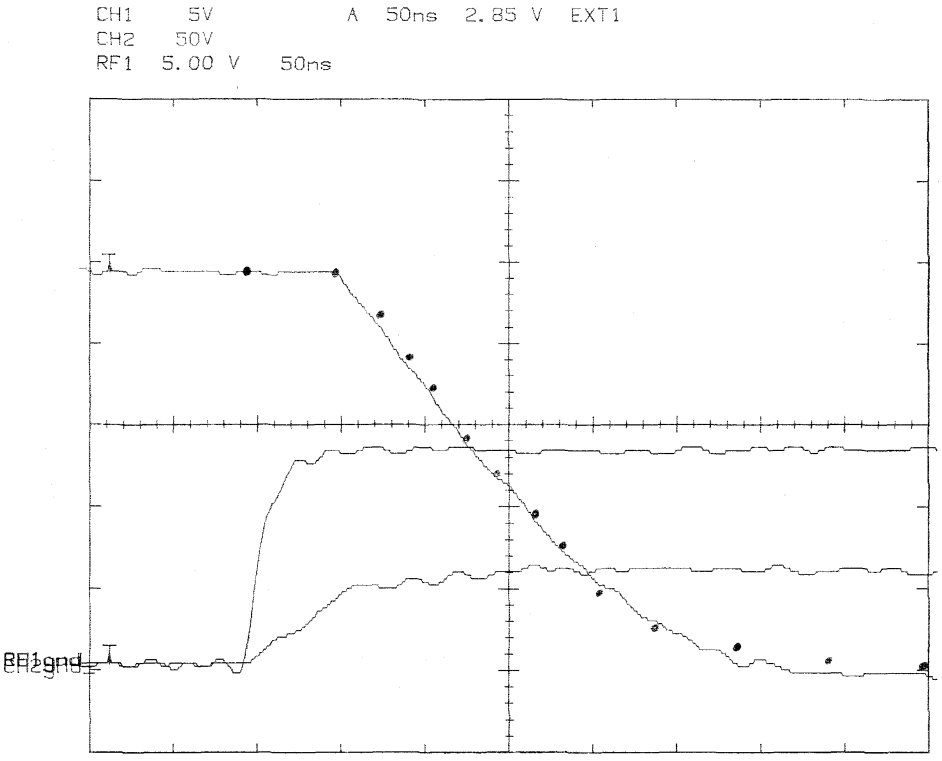

Figure 6

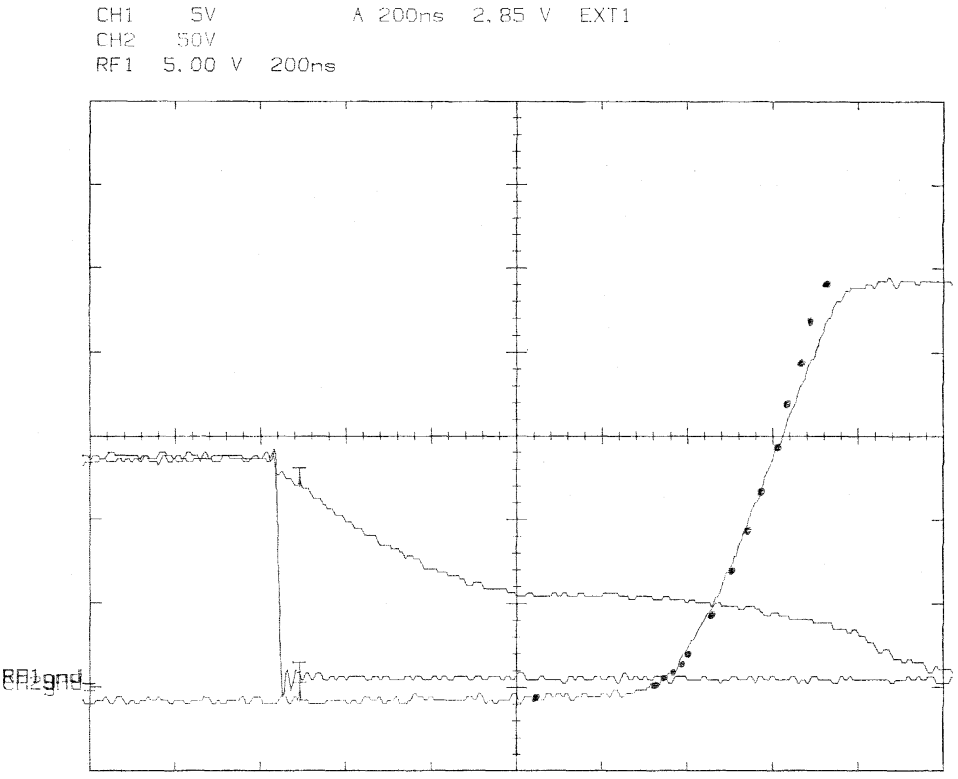

Figure 7

A ground loop is an often over looked mistake in the gate driver circuitry layout. A ground loop occurs when the gate driver circuitry is tied to the power ground in more than one place resulting in load current flowing in the gate driver ground, Figure 8. This not only results in slower switching speeds but can cause excessive ringing on the gate, false triggering of the power device and oscillations.

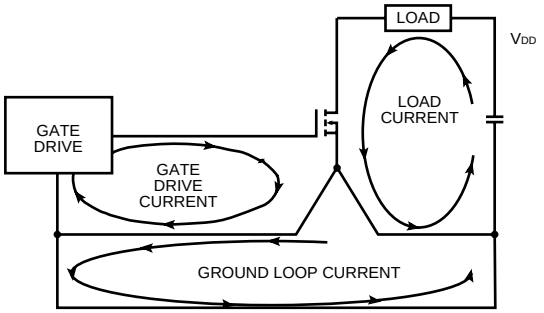

Figure 8

Minimize the area of the gate driver circuitry loop as shown in Figure 9. This will reduce the inductance in the loop and lower the driver impedance.

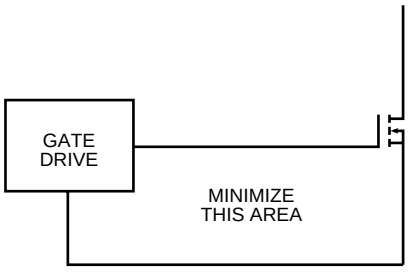

Figure 9

A ground plane, under the gate driver circuitry, is helpful in reducing noise injection into the drive circuitry. However, the ground plane should only be tied to the power ground at point A, Figure 1. Great care should be taken not to create ground loops by multiple tie points to the power ground. For a high side driver the ground plane should tie to the source of the high side device, not to the power ground.

Do not intermix gate driver circuitry and high current carrying load circuitry. Noise can be coupled into the gate driver circuitry through stray capacitance or induced by radiated fields. The results of the injected noise could cause excessive ringing on the gate, false triggering of the power device or oscillations.

The gate driver power supply should be bypassed with good quality, high frequency capacitors, as the power supply impedance is a part of the driver impedance R_g. The capacitors should be connected as close as possible to the driver to minimize the inductance.

Gate Drivers

To this point we have not indicated what type of driver was being used only that it represented 4 ohms of the total gate drive impedance R_g. Once the source inductance is under control, through proper layout, it is clear from the model, Figure 1, that the next way to improve switching speed is to reduce the driver resistance. This is accomplished through the selection of the proper gate driver circuit topology.

Gate drivers can be divided into two categories; discrete and integrated circuit (IC). In the past the discrete type drivers have dominated but IC types are being used more ad more due to their improved performance and lower prices. The author favors the IC driver over the discrete driver because with fewer components, associated with the IC driver, it is easier to achieve the optimum layout.

Discrete Drivers

There are two types of discrete drivers in common use today. The complimentary pair bipolar NPN-PNP emitter follower, Figure 10a and the complimentary pair MOSFET P-channel N-channel, Figure 10b. Both types are referred to as Totem Poles.

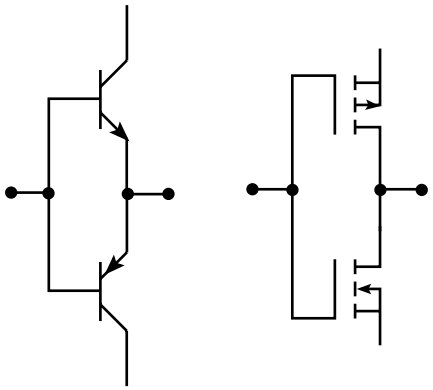

Figure 10

The bipolar Totem Pole is non-inverting and offers no voltage gain to improve the pre-driver rise or fall times. It does provide current gain to reduce the driver impedance to speed the charge and discharge of the device capacitances. Once the input capacitances are charged and the power device has been switched, the driver does not require holding current. It has medium speed and does not perform well at higher conversion frequencies.

To facilitate higher frequency operation and faster switching, the P and N channel complimentary pair MOSFET driver is used. Unlike the Bipolar solution, the MOSFET Totem Pole is inverting and offers voltage gain to improve on the pre driver rise and fall times. This driver suffers from shoot through current, caused by the threshold voltage overlap during on and off transitions, resulting in increased drive power requirements. Because of the inverting nature of the driver, it may cause false turn-on of the power device during power up and power down, requiring under voltage detection and hold off circuity.

IC Drivers

In the past, several companies had introduced IC drivers with reasonable performance and relatively high cost. Recently these and other companies have continued to improve the performance and reduce the cost of the IC driver, making them more cost competitive with the discrete driver. The IC driver is a better solution when you consider the fact they require fewer total components, making it easier to meet the layout design rules.

Driver Comparison

Table 1 shows a comparison between the two discrete drivers and several IC drivers driving an APT5020BN device (0.2 ohms, 28 amp, 500 volts) switching a 10.5 ohm load, 250 volts with no gate resistor R_g. Shown in the table several of the IC drivers equal the MOSFET Totem Pole and the remainder range between the MOSFET and bipolar Totem Pole drivers.

Driver	Rise Time nsec	Fall Time nsec
MOS	20	20
UC3710	20	20
MIC4451	20	20
MIC4429	30	30
UC3708	30	30
UC3711	30	40
Bipolar	60	70

Table 1

Driving Large Die

To this point we have been testing with the APT5020BN, a relatively large device. However, in today's world there are even larger devices such as the APT50M60JN (0.06 ohms, 71 amps, 500 volts). This device was switched with a 3.5 ohm load, 250 volts with 0, 1.5 and 3 ohms gate resistor Rg. The gate resistors were added to control excess ringing, caused by inductance in the load,

on the 3 faster devices. The APT50M60JN is four times as large as the APT5020BN and it would seem to present a much more difficult gate drive problem. However, Table 2 shows if we adhere to the layout design rules, as previously discussed, driving this device is not much more difficult than driving the smaller device.

Driver	Rg ohms	Rise nsec	Fall nsec
MOS	0	20	20
4451	0	20	20
3710	0	30	40
3711	0	40	50
4451	1.5	40	70
4451	3.0	60	100

Table 2

Conclusions

Successful design of a MOSFET gate driver not only depends on the selection of a low impedance driver circuit topology but also is strongly dependent on the layout of the circuit board containing the driver circuit.

If a low impedance driver circuit is employed and proper attention is given to the layout, fast switching of large die MOSFETs is not more difficult than driving smaller devices.

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