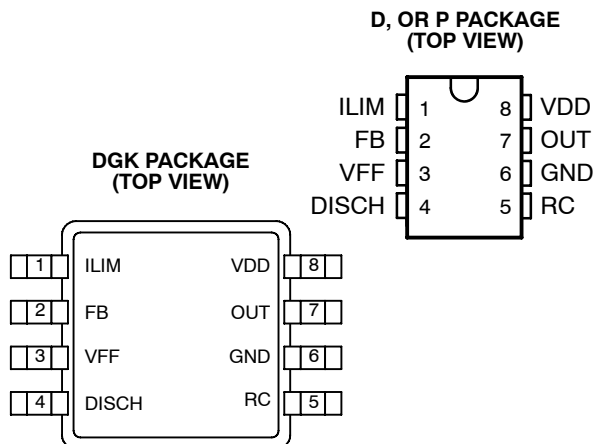


UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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- Greater Than 4-MHz Operation
- Integrated Oscillator / Voltage Feed Forward Compensation
- >4:1 Input Voltage Range
- 25-ns Current Limit Delay
- Programmable Maximum Duty Cycle Clamp
- Optocoupler Interface
- 50- μ A Start-Up Current
- 4.2-mA Operating Current @ 1 MHz
- Smallest Footprint of the 8-pin MSOP Package Minimizes Board Area and Height



description

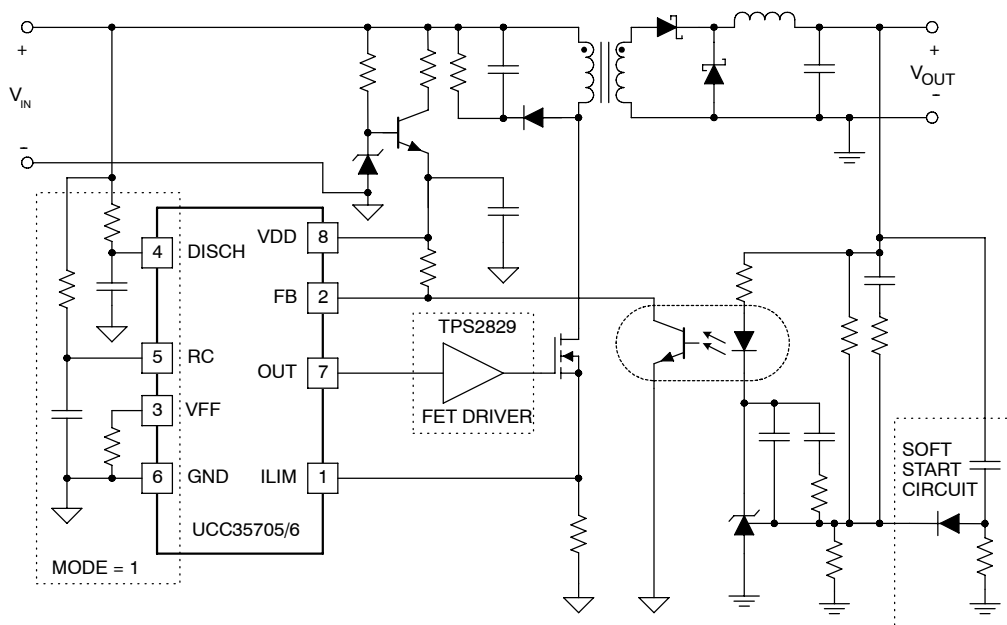
The UCC35705 and UCC35706 devices are 8-pin voltage mode primary side controllers with fast over-current protection. These devices are used as core high-speed building blocks in high performance isolated and non-isolated power converters.

UCC35705/UCC35706 devices feature a high speed oscillator with integrated feed-forward compensation for improved converter performance. A typical current sense to output delay time of 25 ns provides fast response to overload conditions. The IC also provides an accurate programmable maximum duty cycle clamp for increased protection which can also be disabled for the oscillator to run at maximum possible duty cycle.

Two UVLO options are offered. The UCC35705 with lower turn-on voltage is intended for dc-to-dc converters while the higher turn-on voltage and the wider UVLO range of the UCC35706 is better suited for offline applications.

The UCC35705/UCC35706 family is offered in 8-pin MSOP (DGK), SOIC (D) and PDIP (P) packages.

typical application schematic



UDG-99181



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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UCC25705, UCC25706, UCC35705, UCC35706

HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{†‡}

Supply voltage	15 V
Input voltage (VFF,RC,ILIM)	7 V
Input voltage (FB)	15 V
Input current (DISCH)	1 mA
Output current (OUT) dc	±20 mA
Storage temperature, T _{stg}	–65°C to 150°C
Junction temperature, T _J	–55°C to 150°C
Lead temperature (soldering, 10 sec.)	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Power Supply Control Data Book* (TI Literature Number SLUD003) for thermal limitations and considerations of packages.

AVAILABLE OPTIONS

T _A = T _J	Packaged Devices			
	UVLO Option	SOIC-8 Small Outline (D) [†]	PDIP-8 Plastic Dip (P)	MSOP-8 Small Outline (DGK) [†]
–40°C to 85°C	8.8V/8V	UCC25705D	UCC25705P	UCC25705DGK
	12V/8V	UCC25706D	UCC25706P	UCC25706DGK
0°C to 70°C	8.8V/8V	UCC35705D	UCC35705P	UCC35705DGK
	12V/8V	UCC35706D	UCC35706P	UCC35706DGK

[†] D (SOIC-8) and DGK (MSOP-8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC35705DR) to order quantities of 2500 devices per reel for SOIC-8 and 2000 devices per reel for the MSOP-8.

electrical characteristics, V_{DD} = 11 V, V_{IN} = 30 V, R_T = 47 k, R_{DISCH} = 400 k, R_{FF} = 14 k, C_T = 220 pF, C_{VDD} = 0.1 μF, and no load on the outputs, 0°C ≤ T_A ≤ 70°C for the UCC3570x and –40°C ≤ T_A ≤ 85°C for the UCC2570x, T_A = T_J, (unless otherwise specified)

UVLO section (UCCx5705)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold		8.0	8.8	9.6	V
Stop threshold		7.4	8.2	9.0	V
Hysteresis		0.3	0.6	1.0	V

UVLO section (UCCx5706)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold		11.2	12.0	12.8	V
Stop threshold		7.2	8.0	8.8	V
Hysteresis		3.5	4.0	4.5	V

supply current section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start-up current	V _{DD} = UVLO start – 1 V, V _{DD} comparator off		30	90	μA
I _{DD} active	V _{DD} comparator on, oscillator running at 1 MHz		4.2	5.0	mA

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HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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electrical characteristics, $V_{DD} = 11\text{ V}$, $V_{IN} = 30\text{ V}$, $R_T = 47\text{ k}$, $R_{DISCH} = 400\text{ k}$, $R_{FF} = 14\text{ k}$, $C_T = 220\text{ pF}$, $C_{VDD} = 0.1\text{ }\mu\text{F}$, and no load on the outputs, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for the UCC3570x and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the UCC2570x, $T_A = T_J$, (unless otherwise specified)

line sense section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Low line comparator threshold		0.95	1.00	1.05	V
Input bias current (VFF)		-100		100	nA

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	VFF = 1.2 V to 4.8 V	0.9	1.0	1.1	MHz
CT peak voltage	VFF = 1.2 V, See Note 1		1.2		V
	VFF = 4.8 V, See Note 1		4.8		V
CT valley voltage	See Note 1		0		V

NOTE 1: Ensured by design. Not production tested.

current limit section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current		0.2	-0.2	-1	μA
Current limit threshold		180	200	220	mV
Propagation delay, ILIM to OUT	50 mV overdrive		25	35	ns

pulse width modulator section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FB input impedance	$V_{FB} = 3\text{ V}$	30	50	90	$\text{k}\Omega$
Minimum duty cycle	$V_{FB} < 2\text{ V}$			0	%
Maximum duty cycle	$V_{FB} = V_{DD}$, $F_{OSC} = 1\text{ MHz}$	70	75	80	%
	$V_{DISCH} = 0\text{ V}$, $F_{OSC} = 1\text{ MHz}$		93		%
PWM gain	VFF = 2.5 V, MODE = 1		12		%/V
Propagation delay, PWM to OUT			65	120	ns

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOH	$I_{OUT} = -5\text{ mA}$, V_{DD} - output		0.3	0.6	V
VOL	$I_{OUT} = 5\text{ mA}$		0.15	0.4	V
Rise time	$C_{LOAD} = 50\text{ pF}$		10	25	ns
Fall time	$C_{LOAD} = 50\text{ pF}$		10	25	ns

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pin descriptions

DISCH: A resistor to VIN sets the oscillator discharge current programming a maximum duty cycle. When grounded, an internal comparator switches the oscillator to a quick discharge mode. A small 100-pF capacitor between DISCH and GND may reduce oscillator jitter without impacting feed-forward performance. I_{DISCH} must be between 25 μ A and 250 μ A over the entire V_{IN} range.

FB: Input to the PWM comparator. This pin is intended to interface with an optocoupler. Input impedance is 50-k Ω typical.

GND: Ground return pin.

ILIM: Provides a pulse-by-pulse current limit by terminating the PWM pulse when the input is above 200 mV. This provides a high speed (25 ns typical) path to reset the PWM latch, allowing for a pulse-by-pulse current limit.

OUT: The output is intended to drive an external FET driver or other high impedance circuits, but is not intended to directly drive a power MOSFET. This improves the controller's noise immunity. The output resistance of the PWM controller, typically 60 Ω pull-up and 30 Ω pull-down, will result in excessive rise and fall times if a power MOSFET is directly driven at the speeds for which the UCC35705/6 is optimized.

RC: The oscillator can be configured to provide a maximum duty cycle clamp. In this mode the on-time is set by RT and CT, while the off-time is set by RDISCH and CT. Since the voltage ramp on CT is proportional to VIN, feed-forward action is obtained. Since the peak oscillator voltage is also proportional to VIN, constant frequency operation is maintained over the full power supply input range. When the DISCH pin is grounded, the duty cycle clamp is disabled. The RC pin then provides a low impedance path to ground CT during the off time.

VDD: Power supply pin. This pin should be bypassed with a 0.1- μ F capacitor for proper operation. The undervoltage lockout function of the UCC35705/6 allows for a low current startup mode and ensures that all circuits become active in a known state. The UVLO thresholds on the UCC35705 are appropriate for a dc-to-dc converter application. The wider UVLO hysteresis of the UCC35706 (typically 4 V) is optimized for a bootstrap startup mode from a high impedance source.

VFF: The feed-forward pin provides the controller with a voltage proportional to the power supply input voltage. When the oscillator is providing a duty cycle clamp, a current of $2 \times I_{DISCH}$ is sourced from the VFF pin. A single resistor RFF between VFF and GND then set VFF to:

$$VFF \approx VIN \times \left(\frac{2 \times R_{FF}}{2 \times R_{FF} + R_{DISCH}} \right)$$

When the DISCH pin is grounded and the duty cycle clamp is not used, the internal current source is disabled and a resistor divider from VIN is used to set VFF. In either case, when the voltage on VFF is less than 1.0 V, both the output and oscillator are disabled.

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The schematic diagram illustrates the internal architecture of the UCC35705/06 in current mode. The chip is divided into several functional blocks:

- MODE:** A differential amplifier with a gain of 50 mV. It receives the DISCH signal (pin 4) and the VFF signal (pin 3). Its output is connected to the VDD pin (pin 8) and the LOW LINE input of the PWM block.
- LOW LINE:** A comparator with a gain of 1.0 V. It receives the output of the MODE block and the output of the PWM block. Its output is connected to the CLK input of the PWM LATCH.
- PWM:** A pulse-width modulator with a gain of 0.7 V. It receives the output of the LOW LINE block and the output of the UVLO block. Its output is connected to the PWM LATCH.
- PWM LATCH:** A latch with S, Q, RD, and Q-bar outputs. It receives the CLK signal from the LOW LINE block and the output of the PWM block. Its Q output is connected to the OUT pin (pin 7) and the Q-bar output is connected to the ILIM pin (pin 1).
- UVLO:** An undervoltage lockout block. It receives the VDD signal (pin 8) and the GND signal (pin 6). Its output is connected to the PWM block.
- Current Limit:** A comparator with a gain of 200 mV. It receives the ILIM signal (pin 1) and the output of the PWM block. Its output is connected to the Q-bar output of the PWM LATCH.

External components and connections include:

- DISCH (pin 4):** Connected to a MOSFET gate and the MODE block.
- VFF (pin 3):** Connected to the MODE block.
- RC (pin 5):** Connected to the MODE block and the LOW LINE input.
- FB (pin 2):** Connected to the PWM block via a 30 kΩ resistor.
- VDD (pin 8):** Connected to the MODE block, LOW LINE input, and UVLO block.
- GND (pin 6):** Connected to the UVLO block and the current limit comparator.
- ILIM (pin 1):** Connected to the current limit comparator.
- OUT (pin 7):** The PWM output signal.
- Internal components:** A 50 mV differential amplifier, a 1.0 V comparator, a 0.7 V pulse-width modulator, a 200 mV current limit comparator, a 30 kΩ resistor, a 20 kΩ resistor, a 1 pF capacitor, and a MOSFET.

Figure 1. Block Diagram

oscillator and PWM

The PWM latch is set during the oscillator discharge and is reset by the PWM comparator when the C_T waveform is greater than the feedback voltage. The voltage at the FB pin is attenuated before it is applied to the PWM comparator. The oscillator ramp is shifted by approximately 0.65-V at room temperature at the PWM comparator. The offset has a temperature coefficient of approximately $-2 \text{ mV}/^\circ\text{C}$.

All reset conditions are dominant; asserting any output will force a zero duty cycle output.

The timing capacitor CT is charged from ground to VFF through RT. The discharge path is through an on-chip current sink that has a value of $30 \times I_{DISCH}$, where I_{DISCH} is the current through the external resistor RDISCH. Since the charge and discharge currents are both proportional to VIN, their ratio, and the maximum duty cycle remains constant as VIN varies.

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FUNCTIONAL DESCRIPTION

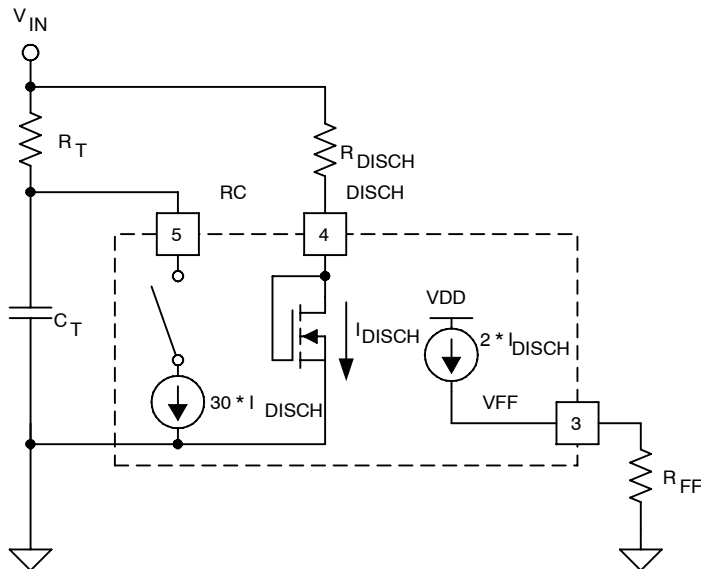


Figure 2. Duty Cycle Clamp (MODE = 1)

The on-time is approximately:

$$T_{ON} = \alpha \times R_T \times C_T \quad \text{where } \alpha = \frac{V_{FF}}{V_{IN}} \approx \frac{2 \times R_{FF}}{R_{DISCH}}$$

The off-time is:

$$T_{OFF} = \alpha \times \frac{C_T \times (R_T \times R_{DISCH})}{(30 \times R_T - R_{DISCH})}$$

The frequency is:

$$f = \left(\frac{1}{\alpha \times R_T \times C_T} \right) \times \frac{1}{1 + \frac{R_{DISCH}}{(30 \times R_T - R_{DISCH})}}$$

The maximum duty cycle is:

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \left(1 - \frac{R_{DISCH}}{30 \times R_T} \right)$$

FUNCTIONAL DESCRIPTION

component selection for oscillator with duty cycle clamp (MODE = 1)

For a power converter with the following specifications:

- $V_{IN(min)} = 18 \text{ V}$
- $V_{IN(max)} = 75 \text{ V}$
- $V_{IN(shutdown)} = 15 \text{ V}$
- $F_{OSC} = 1 \text{ MHz}$
- $D_{MAX} = 0.78 \text{ at } V_{IN(min)}$

In this mode, the on-time is approximately:

- $T_{ON(max)} = 780 \text{ ns}$
- $T_{OFF(min)} = 220 \text{ ns}$
- $V_{FF(min)} = \frac{18}{15} = 1.20 \text{ V}$

(1) Pick $C_T = 220 \text{ pF}$.

(2) Calculate R_T .

$$R_T = \frac{V_{IN(min)} \times T_{ON(max)}}{V_{FF(min)} \times C_T}$$

$$R_T = 51.1 \text{ k}\Omega$$

(3) R_{DISCH}

$$R_{DISCH} = \frac{30 \times R_T}{1 + \left[\frac{\left(\frac{V_{FF(min)}}{V_{IN(min)}} \right) \times R_T \times C_T}{T_{OFF(min)}} \right]}$$

$$R_{DISCH} = 383 \text{ k}\Omega.$$

I_{DISCH} must be between $25 \mu\text{A}$ and $250 \mu\text{A}$ over the entire V_{IN} range.

With the calculated values, I_{DISCH} ranges from $44 \mu\text{A}$ to $193 \mu\text{A}$, within the allowable range. If I_{DISCH} is too high, C_T must be decreased.

(4) R_{FF}

$$R_{FF} = \frac{V_{FF(min)} \times R_{DISCH}}{2 \times (V_{IN(min)} - 1)}$$

The nearest 1% standard value to the calculated value is 13.7 k .

UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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FUNCTIONAL DESCRIPTION

oscillator without duty cycle clamp (MODE = 0)

In this mode, the timing capacitor is discharged through a low impedance directly to ground. The DISCH pin is externally grounded. A comparator connected to DISCH senses the ground connection and disables both the discharge current source and VFF current source. A resistor divider is now required to set VFF.

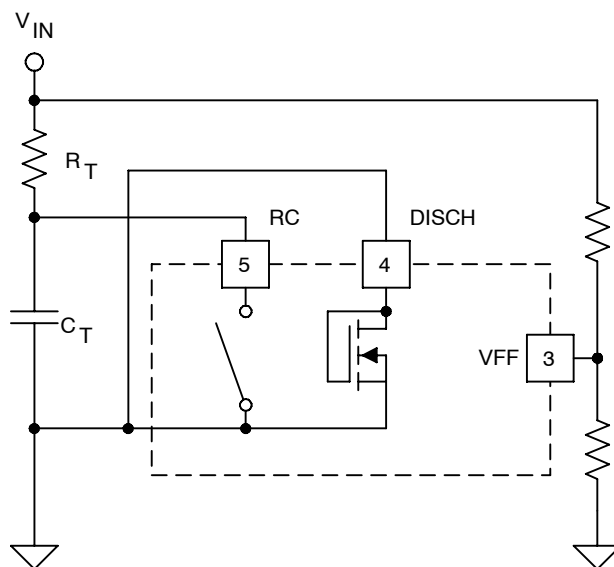


Figure 3. Oscillator Without Clamp (MODE = 0)

In this mode, the on-time is approximately:

$$T_{ON} = \alpha \times R_T \times C_T \quad \text{where } \alpha = \frac{V_{FF}}{V_{IN}}$$

The off-time is:

$$T_{OFF} \approx 75 \text{ ns}$$

The frequency is:

$$f = \frac{1}{\alpha \times R_T \times C_T + 75 \text{ ns}}$$

FUNCTIONAL DESCRIPTION

component selection for oscillator without duty cycle clamp (MODE = 0)

For a power converter with the following specifications:

- $V_{IN(min)} = 18 \text{ V}$
- $V_{IN(max)} = 75 \text{ V}$
- $V_{IN(shutdown)} = 15 \text{ V}$
- $F_{OSC} = 1 \text{ MHz}$

With these specifications,

$$V_{FF(min)} = \frac{18}{15} = 1.2 \text{ V}$$

(1) Pick $C_T = 220 \text{ pF}$

(2) Calculate R_T .

$$R_T = \frac{\frac{V_{IN(min)}}{V_{FF(min)}} \times \left(\frac{1}{F_{OSC}} - 75 \text{ ns} \right)}{C_T}$$

TYPICAL CHARACTERISTICS

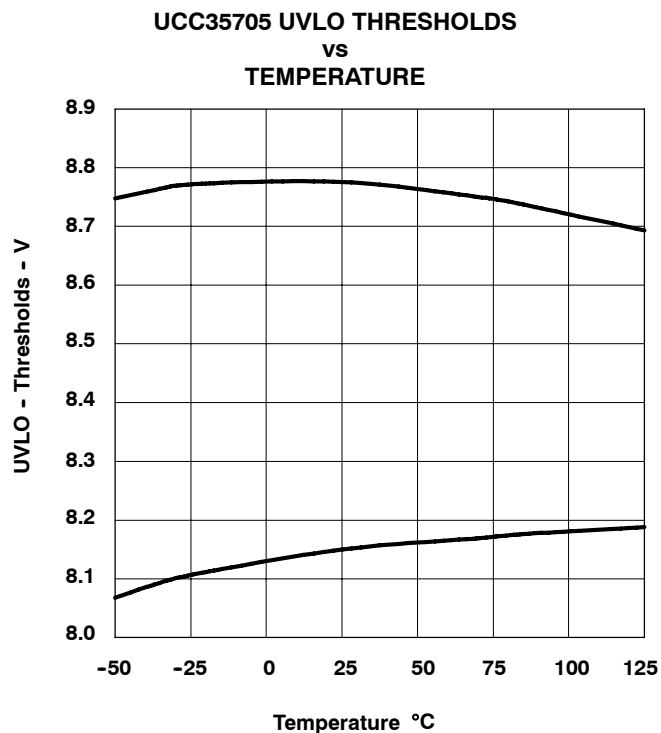


Figure 4

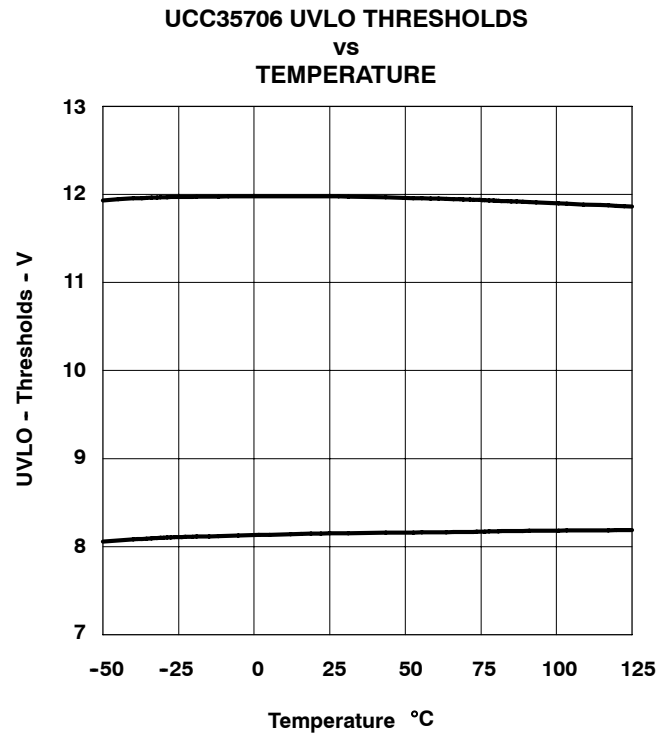


Figure 5

UCC25705, UCC25706, UCC35705, UCC35706
HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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TYPICAL CHARACTERISTICS

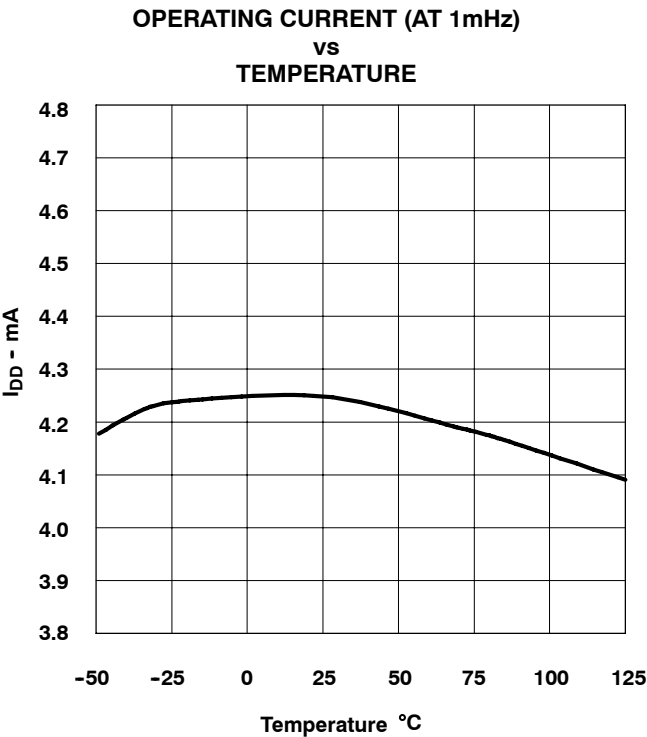


Figure 6

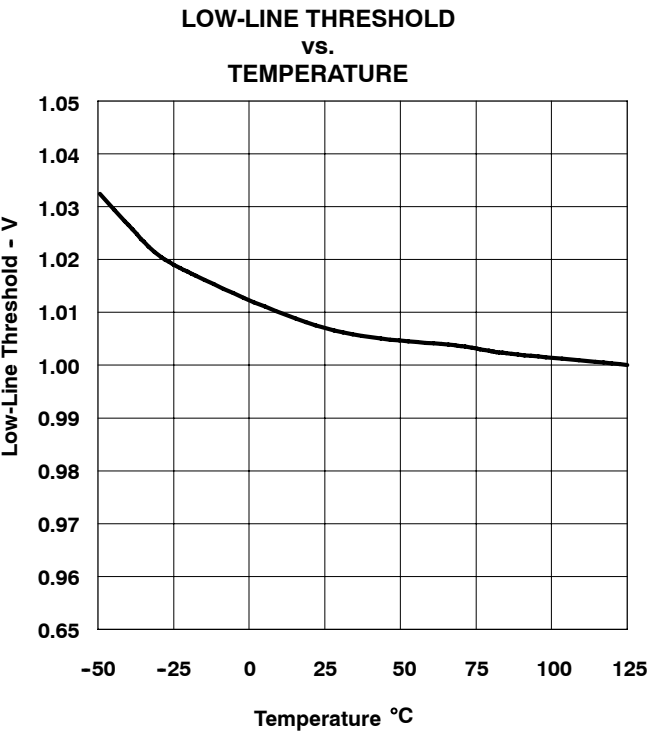


Figure 7

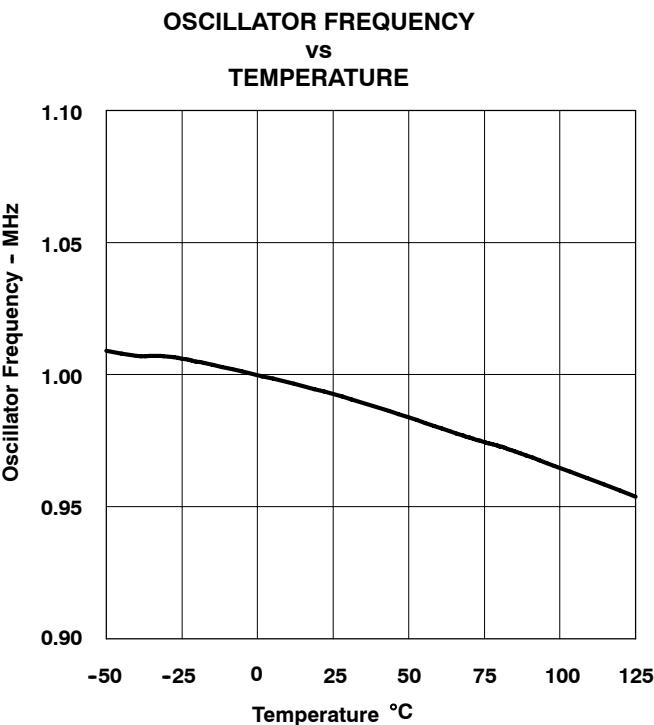


Figure 8

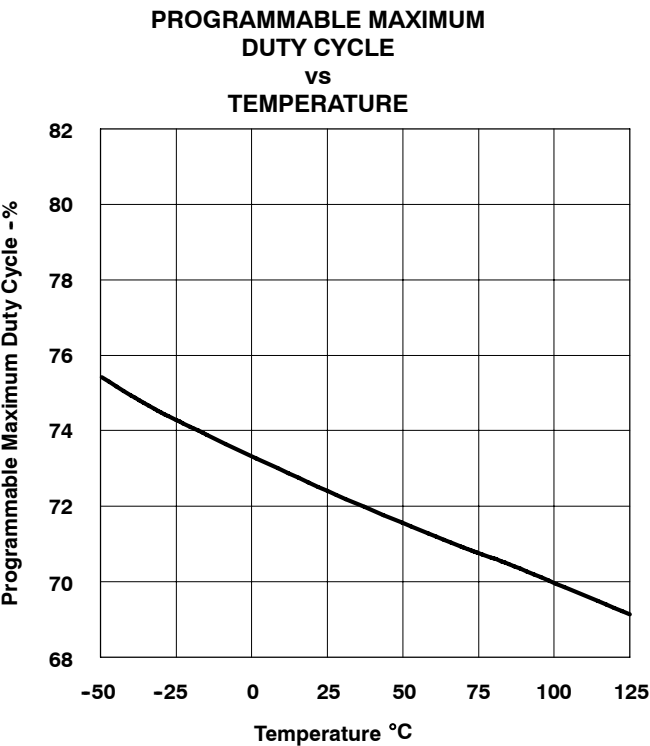


Figure 9

UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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TYPICAL CHARACTERISTICS

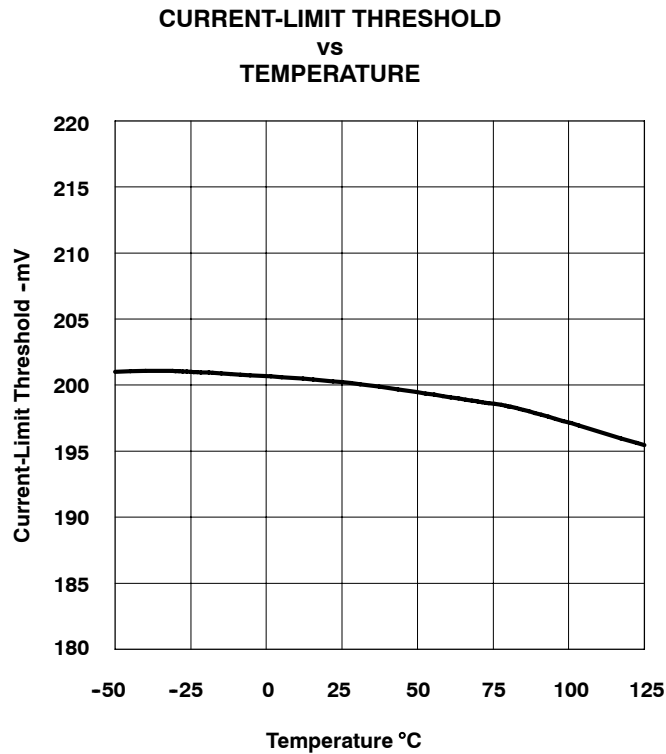


Figure 10

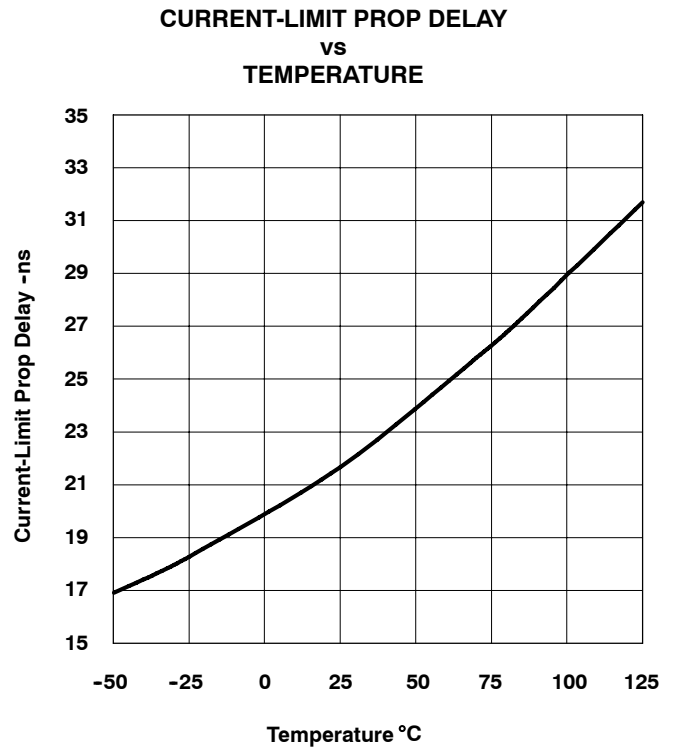


Figure 11

Revision History

Revision SLUS473A, March 2001 to SLUS473B:

- Modified "T_{OFF}" and "f" equation on page 6.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC25705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25705DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25705DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25705DGKTR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC25705DGKTRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC25705DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25705DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25705P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC25705PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC25706D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25706DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC25706DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC25706DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC25706P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC25706PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC35705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC35705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC35705DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC35705DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC35705DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC35705DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC35705P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC35705PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC35706D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC35706DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC35706DGK	ACTIVE	MSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC35706DGKG4	ACTIVE	MSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC35706P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC35706PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF UCC25706 :

- Automotive: [UCC25706-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25705DGKTR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC25705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC35705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25705DGKTR	MSOP	DGK	8	2500	346.0	346.0	29.0
UCC25705DTR	SOIC	D	8	2500	346.0	346.0	29.0
UCC35705DTR	SOIC	D	8	2500	346.0	346.0	29.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

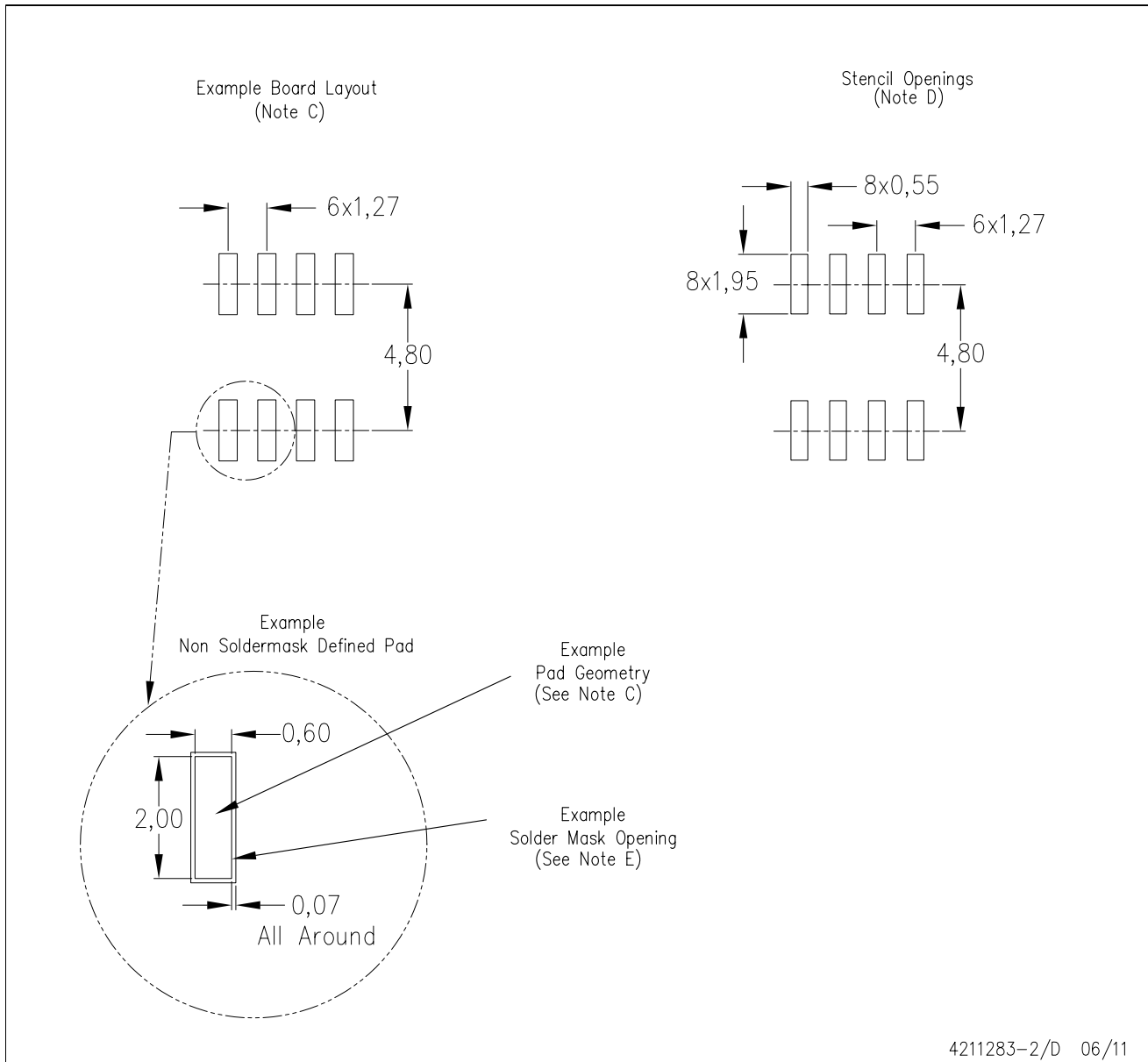


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/D 06/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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