Circuit protects FPGAs from killer spikes

NELSON NGUYEN, ANRITSU CORP, MORGAN HILL, CA

A project using Xilinx FPGAs brought an interesting problem to light. When you turn on the board, one FPGA in three succumbs to this problem. A lot of frustration and testing uncovered a negative-going spike (**Figure 1**) in the 5V line from the dc/dc converter. The system uses a dc/dc converter to convert –48V to 5V and other voltages. The spike occurs before the converter delivers its intended 5V. Spikes greater than 5V would kill the FPGA with the shortest path to the converter. The circuit in **Figure 2** solves the problem.

Because the spike occurs before the 5V supply line turns on, to prevent the spike from destroying the FPGA, you should open the 5V path when you turn on the power switch and then close the path when the 5V supply voltage is present. The R_{19}-C_{13} RC network provides a delay in turning relay K_1 on. The turn-on voltage for K_1 is approximately 3.7V. The voltage divider comprising R_{19} and K_1's coil resistance (approximately 780Ω for an NEC EA2-5NU) provides a voltage at the junction of C_{13} and R_{19} sufficient to turn K_1 on. The value of C_{13} sets the delay at approximately 2 msec. (DI #2181) EDN

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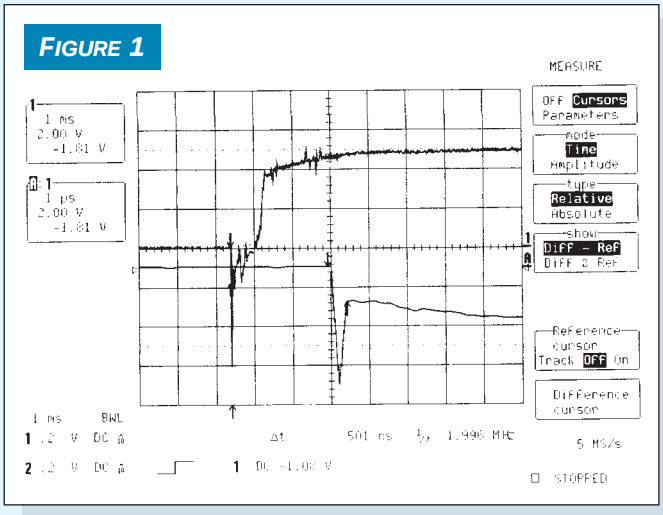
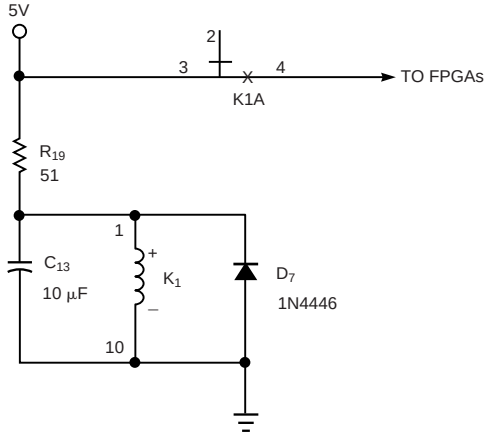
FIGURE 1



A large negative spike (top waveform) in the turn-on waveform of the 5V supply line is an effective FPGA destroyer.

FIGURE 2



NOTE: K_1 = NEC EA2 – 5NU.

A simple RC network and a relay provide a 2-msec turn-on delay in the power-supply line to the FPGAs, thereby blocking the killer negative spike.

Bootstrapped boost converter operates at 1.8V

TOM GROSS, LINEAR TECHNOLOGY, MILPITAS, CA

Many circuits, such as those that use batteries or solar cells, must operate in the face of decreasing supply voltages. The circuit in **Figure 1** maintains the maximum load current as the supply voltage drops. The regulator boosts a 2.5 to 4.2V input to 5V and provides 2A load current, for 10W of output power. The circuit is a bootstrapped synchronous boost regulator that uses an LTC1266 synchronous-regulator controller. Diodes D_1 through D_5 allow the circuit to start up using the low input voltage and then to receive its power from the higher output voltage during normal operation. The crucial elements in the circuit are the switches: two IRF7401 n-channel MOSFETs. The MOSFETs receive full enhancement at low gate-source voltages. (At V_{GS}=2V, the peak drain current is 15A.) The low enhancement voltages allow the circuit to start with low input voltages.

This low-voltage capability is important for low-series-cell-count, battery-powered systems. Diodes D_3 and D_4, along with capacitor C_2, form a charge-pump circuit, which the controller uses for the MOSFETs' gate drive. Because the circuit receives its power from the 5V output voltage, the cir-

cuit still operates if the input supply voltage drops below the IC's minimum input voltage. This bootstrapping allows the circuit to start up when the input voltage is below the IC's 3.5V minimum input spec. With a 1A load, the regulator operates with inputs as low as 1.8V. **Figure 2** shows the regulator's efficiency vs the input voltage with three load currents. With 2A load current, the efficiency drops as the input voltage decreases, because of the higher power losses in the inductor. A larger inductor would provide increased efficiency or allow for greater load currents. (DI #2185) EDN

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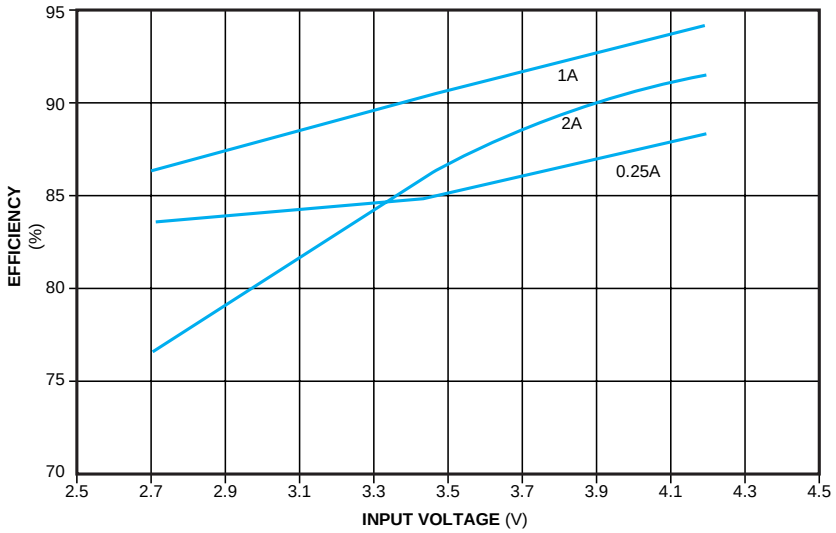
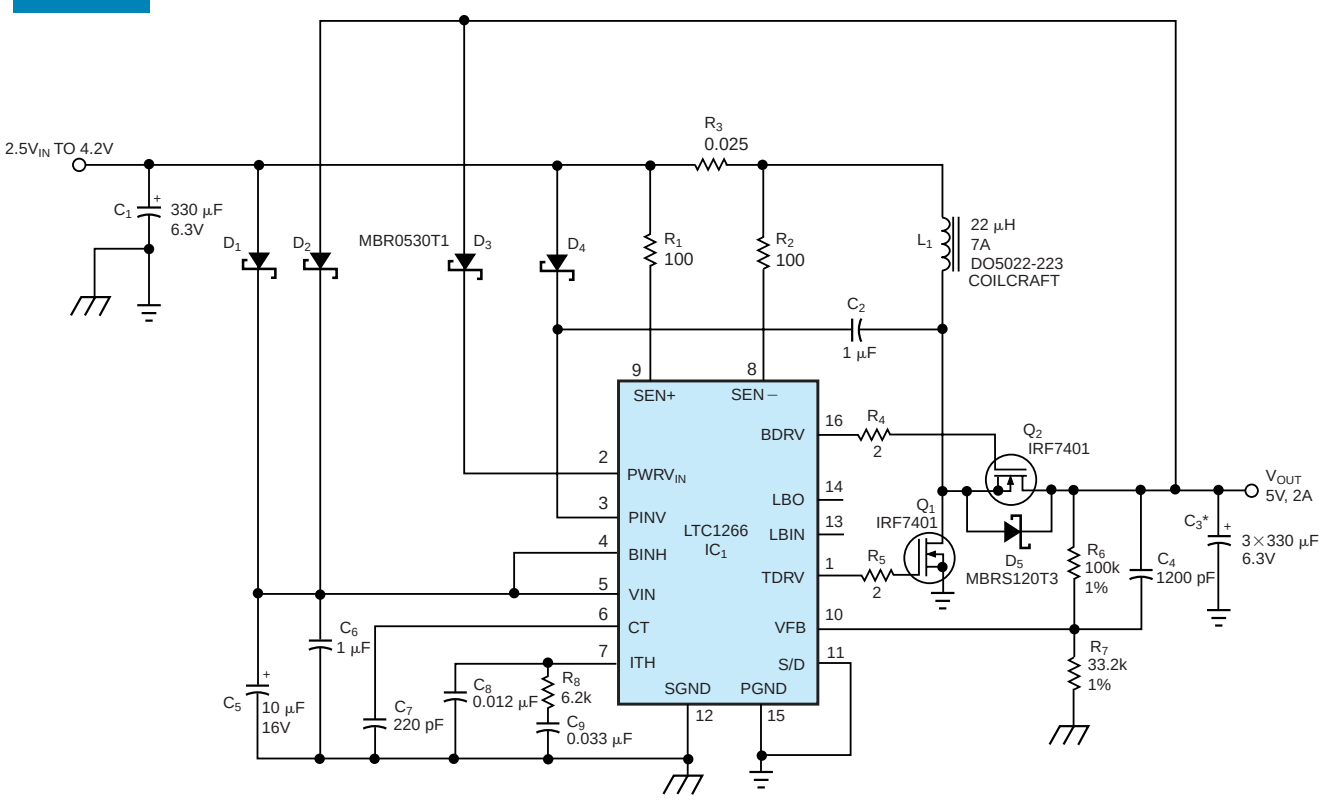
FIGURE 2



The conversion efficiency for the boost regulator in Figure 1 averages 87% overall. The circuit provides its best efficiency for all input voltages with a 1A load.

FIGURE 1



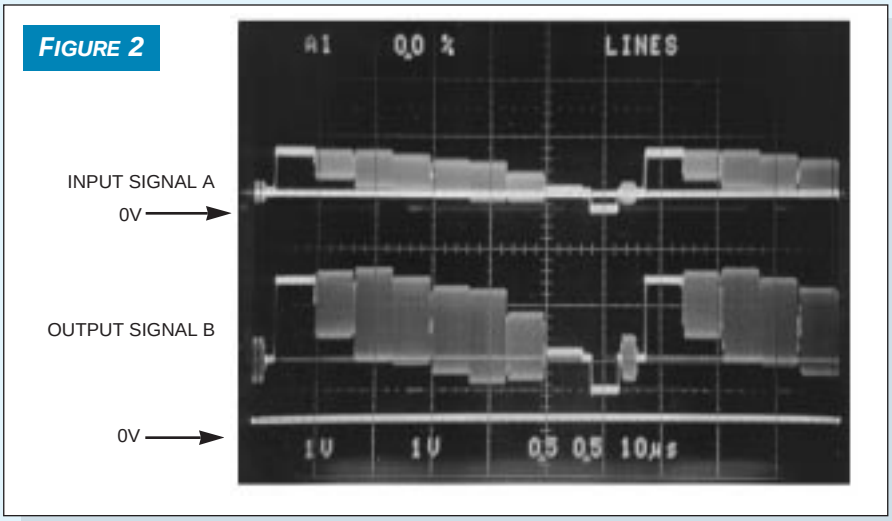
A charge-pump arrangement allows this boost regulator to operate with input voltages far below the minimum specified value for the regulator IC.

Video circuit clamps under all conditions

NICHOLAS GRAY AND TERRANCE SMITH, NATIONAL SEMICONDUCTOR, SANTA CLARA, CA

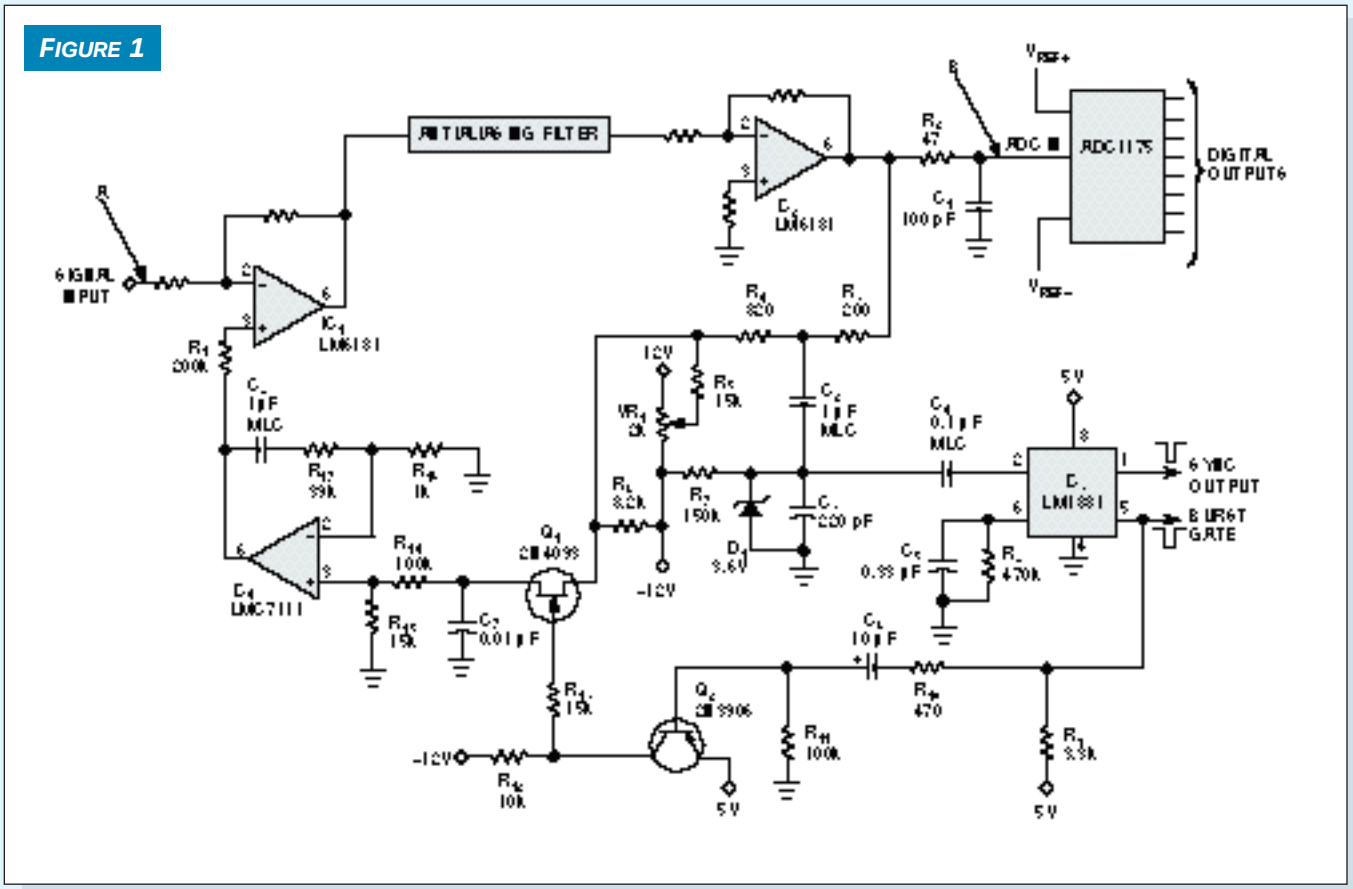
Many video-circuit clamps operate well in the presence of a composite-video signal but cannot achieve a clamp level with signals other than composite video or in the absence of an input signal. The circuit in **Figure 1**, developed for the ADC1175 (a popular and inexpensive, high-performance, 8-bit, 20M-sample/sec ADC), provides the normal back-porch clamp function to the input of the ADC in the presence of a composite-video signal. The circuit further ensures that the voltage presented to the ADC is within its correct operating

FIGURE 2



This scope photo shows the offset at Point B relative to Point A in Figure 1. Note also the gain the circuit provides.

FIGURE 1



The clamp level at Point B in this circuit is independent of the average level at Point A. The circuit thus keeps signal levels with the ADC's input range.

range in the absence of an input signal and forces any signal other than composite video to be within the ADC's input common-mode range.

The circuit accomplishes video clamping by building a control loop that forces the dc voltage at IC_2's output to a desired level during the blanking period. This level, approximately 25% of full scale for a composite-video signal, forces the ADC's output-pedestal (blanking) level to an 8-bit code of approximately 64. The simple filter comprising R_3 and C_3 bandlimits the signal at the output of IC_2. This high-frequency attenuation is necessary to prevent noise spikes from upsetting the operation of the LM1881. The LM1881 is a video sync-separator chip that produces burst-gate pulses at its Pin 5 when a composite-video signal is present at Pin 2.

The burst-gate output of the LM1881 serves to sample the blanking level of the video signal. Potentiometer VR_1 and R_5 produce an adjustable offset in the signal path when Q_1 gates on. During the blanking period, the ac-coupled burst-gate signal pulls Q_2's base low (to approximately 4V), thus pulling Q_1's gate high, thereby sampling and storing the sum of the video-blanking level and the dc offset from VR_1 onto C_7. At times other than the back-porch interval, Pin 5 of the LM1881 is high, and Q_2 is off, thereby turning Q_1 off. Divider R_{14}-R_{15} attenuates the voltage on C_7 to ensure sufficient phase margin in the clamp loop. IC_4 is an integrator that averages the attenuated dc value over many samples. This average sums with the input signal in IC_1.

If the integration time is too small, the result could be shading across the display. A long integration results in slow, perceptible adjustments when switching between fields with large differences in average brightness. The dc feedback path for IC_4 is through IC_1 and IC_2. If no video signal exists or if the input signal has no sync, R_{11} holds Q_2 on, thus holding the video output of the circuit within the ADC's operating range. With VR_1 centered, the level halfway between the positive and negative peaks of the input signal clamps at approximately 1.6V, or approximately halfway between the high and low reference voltages (2.6 and 0.6V, respectively) of the ADC1175. The circuit achieves an effective number of bits of 7.5, corresponding to a signal-to-noise and distortion of 47 dB. **Figure 2** shows the offset at Point B in **Figure 1**, relative to the voltage at Point A. (DI #2184) EDN

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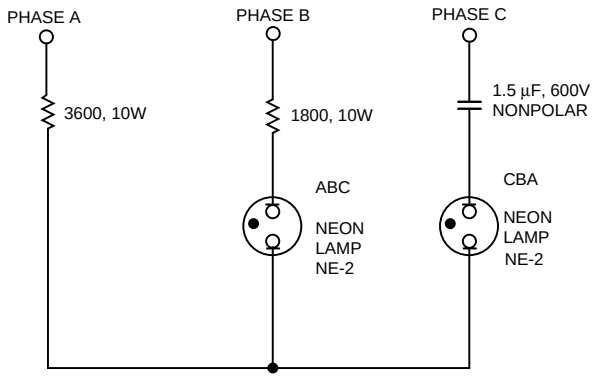
$5 junk-box circuit determines phase sequence

HUGH ADAMS, FORT WALTON BEACH, FL

Have you ever wondered which way a blower motor is going to turn when you plug it into another socket, or have you ever inherited the task of modifying three-phase wiring in your plant? The circuit in **Figure 1** is a simple, approximately $5 phase sequencer that you can probably build from parts in your junk box and save approximately $50 to boot. The component values reflect 60-Hz operation, but the design equations in **Figures 2** and **3** allow you to select values for other frequencies. The equations are in MathCAD spread-

FIGURE 1



The brighter of the two neon lamps indicates the phase sequence, either ABC or CBA.

FIGURE 2

$$f=60 \quad C=1.5\cdot10^{-6} \quad V=0 \quad R1=3600 \quad R2=1800$$

$$x=\frac{1}{2\cdot\pi\cdot f\cdot C} \qquad x=1.768\cdot10^{3}$$

$$IA=\frac{1}{R1}\cdot(120\cdot\cos(2\cdot\pi\cdot f)-V)$$

$$IB=\frac{1}{R2}\left(120\cdot\cos\left(2\cdot\pi\cdot f-2\cdot\frac{\pi}{3}\right)-V-90\right)$$

$$IC=\frac{1}{\left[\left(\frac{1}{2\cdot\pi\cdot f\cdot C}\right)^{2}\right]^{wQ}}\cdot\left(120\cdot\cos\left(2\cdot\pi\cdot f-4\cdot\frac{\pi}{3}-\frac{\pi}{4}\right)-V-90\right)$$

$$IA=0.033 \quad IB=-0.083 \quad IC=-0.033$$

MathCAD spreadsheet equations show a higher current in Phase B than in Phase C of the circuit in Figure 1; therefore, the phase sequence is ABC.

sheet format, but almost any other spreadsheet would do.

Referring to **Figure 1** and the equations, you can see that the neon bulb that glows brighter indicates the phase sequence, or phase-rotation order, ABC or CBA. The bulb glows brighter because it carries more current because of the phase shift the 1.5-μF capacitor provides. You can verify this assertion by examining the two sets of equations. Note that the two sets of equations have different expressions for I_B and I_C. In one, I_B lags I_A by $2\pi/3$; in the other, it lags by $4\pi/3$, and vice versa for I_C. The equations provide the mathematical way of reversing the phase sequence, and, as you can see, the two currents I_B and I_C reverse their relative magnitudes as the phase rotation reverses. (DI #2180) EDN

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FIGURE 3

$f=60$
$C=1.5\cdot10^{-6}$
$V=0$
$R1=3600 \quad R2=1800$

$x=\frac{1}{2\cdot\pi\cdot f\cdot C}$

$x=1.768\cdot10^{3}$

$IA=\frac{1}{R1}\cdot(120\cdot\cos(2\cdot\pi\cdot f)-V)$

$IB=\frac{1}{R2}\cdot\left(120\cdot\cos\left(2\cdot\pi\cdot f-4\cdot\frac{\pi}{3}\right)-V-90\right)$

$IC=\frac{1}{\left[\left(\frac{1}{2\cdot\pi\cdot f\cdot C}\right)^2\right]^{wQ}}\cdot\left(120\cdot\cos\left(2\cdot\pi\cdot f-2\cdot\left(\frac{\pi}{3}-\frac{\pi}{4}\right)\right)-V-90\right)$

$IA=0.033$
$IB=-0.083$
$IC=-0.116$

A CBA phase sequence produces a higher current, thus a brighter neon lamp, in Phase C of the circuit in Figure 1.

Piezo device generates buzz, beep, or chime

DENNIS EICHENBERG, PARMA HEIGHTS, OH

Piezoelectric buzzers, such as the Murata (Smyrna, GA) PKB5-3A in **Figure 1**, make excellent alarms. They're compact, lightweight, efficient, and reliable. However, a piezo alarm is a dc device; it requires additional circuitry to operate from an ac source. The circuits in **Figure 1** provide a simple and inexpensive way to obtain the dc drive. The W04G full-wave bridge rectifier produces a full-wave dc waveform from the 120V ac line. The 100Ω resistor protects the circuit from surges when you first apply power. The 5.5V 1N4733 zener diode protects the buzzer against high-voltage excursions. The 1-μF capacitor provides filtering for the buzzer.

The circuit in **Figure 1a** produces a true buzzer sound. The addition of an F336HD flashing LED (part number 276-036 at Radio Shack) in **Figure 1b** changes the alarm to a beeper, and it also provides a visual alarm. The LED produces a constant pulse of light at approximately 1 Hz without the addition of a time-constant capacitor. The LED starts immediately when you apply power, and it's insensitive to temperature variations. The addition of a 35-μF capacitor in parallel with the buzzer (**Figure 1c**) changes the audible alarm to a pleasing chime. The value of the capacitor is not critical; you can obtain various sound effects by varying it. (DI #2194) EDN

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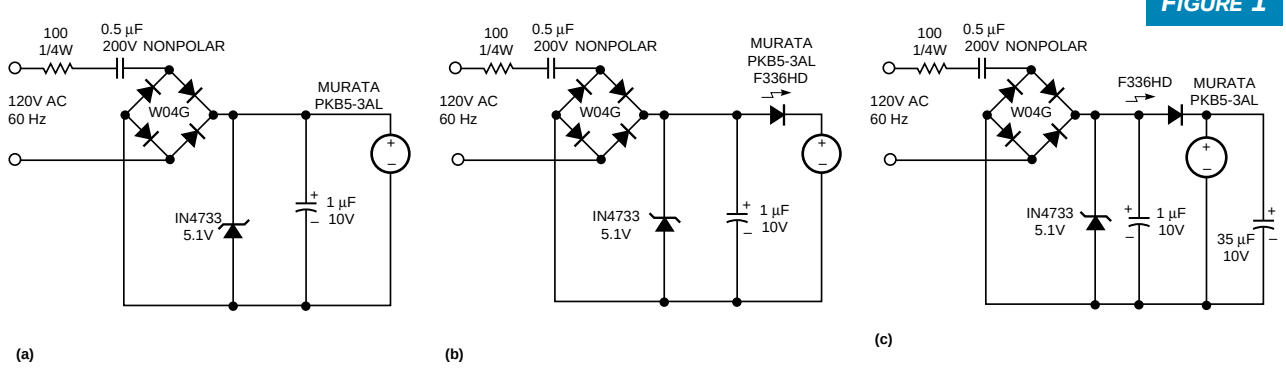
FIGURE 1



A handful of inexpensive components configures a piezo alarm device as a buzzer (a), a beeper (b), or a chime (c).

Smart switch cuts transformer turn-on current

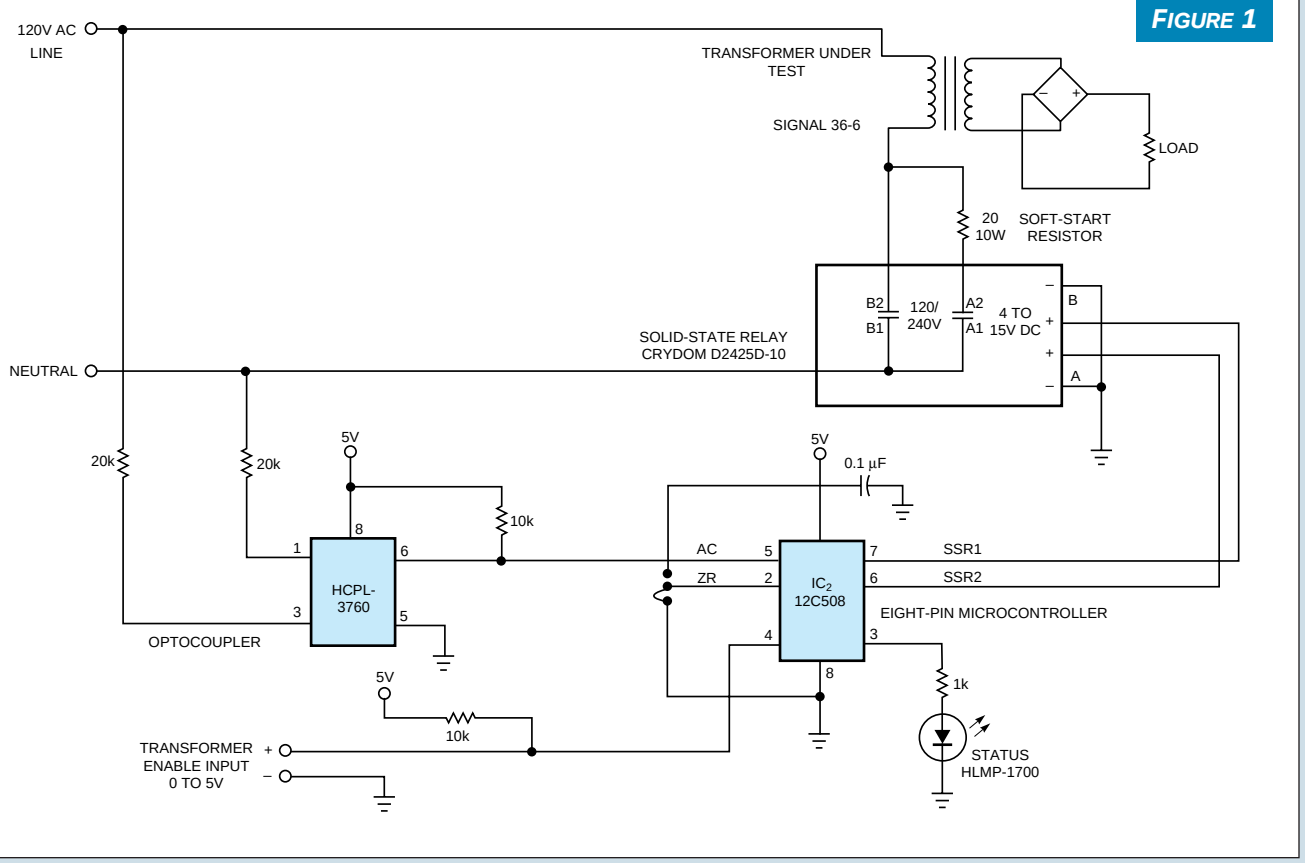
ROBERT LINDSEY, HANSVEDT EDM, URBANA, IL

Transformer-core saturation can cause inexplicable fuse blowing, system crashes, or premature switch and relay failure. When a core saturates, it loses its inductive characteristics; primary winding current can then reach extremely high values for several ac cycles. Turning on a transformer may seem fundamental, but in some power-supply designs and control applications, it can be a game of Russian roulette. Because transformers remain polarized when turned off, saturation occurrence is a function of the polarity and phase angle of the ac cycle when you switch the circuit on and off. The smart-switch circuit in **Figure 1** eliminates saturation, improves relay reliability, and provides a tool for determining transformer and relay performance.

The circuit goes beyond typical configurations using zero-crossing or peak-switching relays, by using the polarity of the ac cycle, known phase angles, and soft-starting techniques. **Figure 2** shows that the primary turn-on current of a 220-VA transformer can be disastrous when you use a zero-crossing relay. Trace R1 shows 46A peak with a saturated core. Trace 1 shows only a few amps with use of the smart-switch circuit. This large difference in current demonstrates the value of the smart switch in controlling transformer magnetization. Switching on during a positive half cycle and off during a negative half cycle or vice versa prevents most core saturation.

Peak switching of the ac voltage during turn-on and -off further reduces the susceptibility to core saturation, regardless of ac polarity. This reduction is an important consideration in the event of an uncontrolled power outage. **Figure 3**, trace R, shows the primary current with peak and same-polarity switching. The vertical scale in **Figures 2** and **3** is 10A per division, and Trace 2 is the relay control voltage. The primary current in **Figure 3** causes some core saturation (note that the current is not bipolar), but the saturation is much lower than that in **Figure 2**. Trace 1 shows the reduced primary current with the use of peak and opposite-polarity switching. Note that transformer designs vary widely; some may favor particular phase angles.

FIGURE 1



A µC-controlled smart switch prevents transformer-core saturation, thus averting system crashes and prolonging the life of power-supply relays.

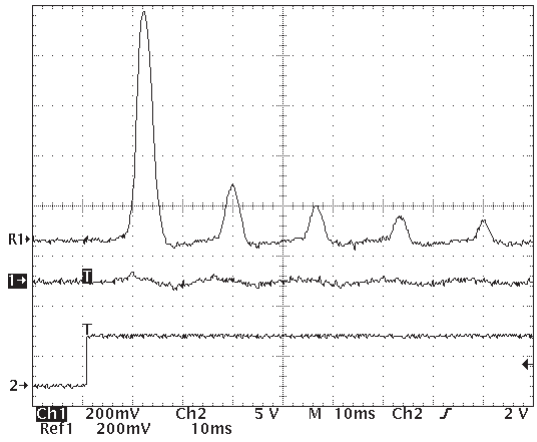
Inrush current from power-supply filter capacitors is also an important design consideration. By using a resistor, an inrush device, or an inductive input filter in the secondary winding, you can reduce this inrush surge. Another solution is to soft-start the transformer by using a resistor in the primary to limit inrush and saturation currents to an acceptable level. After a brief delay, a second solid-state relay shunts the resistor. The Microchip 12C508 µC uses its internal 4-MHz RC oscillator for all timing. The chip is simple, inexpensive, reliable, and well-suited for this application. For wide temperature variations, you can obtain more accurate timing by using a 32-kHz crystal. You can download **Listing 1**, the source code for the µC's operation, from *EDN*'s Web site www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2170.

You can use either zero-crossing or random relays, but the random type works better for transformers. Set Pin 4 high for zero-crossing relays and low for random-turn-on relays. The HCPL-3760 optocoupler determines the polarity and phase of the ac line. The coupler is configured as a near-zero detector. Its output is set to switch on at 50V ac and off at 25V ac.

LISTING 1—SOURCE CODE FOR TRANSFORMER SOLID-STATE-RELAY CONTROLLER

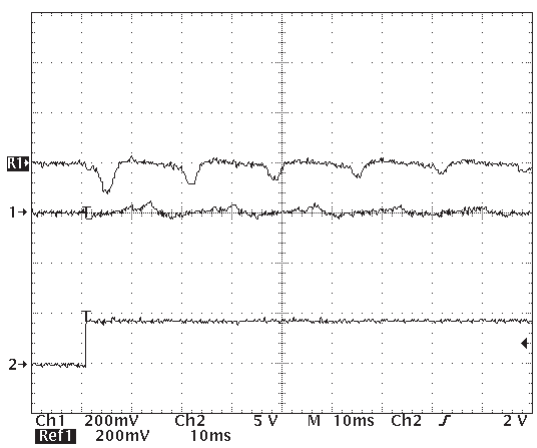
```
;
; ROBERT LINDSEY
; 1908 KENNY AVE, CHAMPAIGN, IL  61821
; 217 384-5900

; This is a smart switch for controlling a solid state relay that is used
; for controlling the AC primary power to a large transformer.  Transformers
; are noted for having extremely high inrush currents due to momentary
; core saturation if the polarization is correct. This version has an optional
; soft start switch that uses a resistor in the primary to limit current
; from the power supply filter capacitors and core saturation. The primary
; function of the code is to always turn the transformer on on the positive
; half of the ac cycle and turn it off on the negative half of the ac cycle.
; Random turn on solid state relays or zero crossing relays can be used.


 title "Transformer SSR Controller"
 list p=pic12C508, st=off, x=on, n=75, r=dec
 include "p12c508.inc"
 __CONFIG B'000000001010'

;------------------------------ RAM REGISTERS -----------------------------

 cblock H'0007'
 COUNT1  ;test counter
 COUNT2  ;test counter
 endc

;---------------------------- PORT PIN ASSIGNMENTS --------------------------

#define  SSR1 GPIO,0  ;pin 7, output, SS relay 1
#define  SSR2 GPIO,1  ;pin 6, output, SS relay 2
#define  AC GPIO,2  ;pin 5, input, AC polarity, HCPL-3760
#define  TE GPIO,3  ;pin 4, input, transformer enable
#define  BLEEDER GPIO,4  ;pin 3, output, bleeder resistor
#define  ZR GPIO,5  ;pin 2, input, zero crossing or random
     ;1=Zero crossing, 0=Random turn on

;-------------------------------------------------------------------------------
 org 0
 movlw 0
 movwf OSCCAL  ;int RC oscillator calibration value

 movlw B'10000110' ;wake-up off, pull-ups on, T0 int clk,
 option   ;T0 prescaler, =128

;------------------------------- MAIN ------------------------------------
 bcf SSR1  ;set pin 7 latch low
 bcf SSR2  ;set pin 6 latch low
 bcf BLEEDER  ;set pin 3 latch low

main movlw B'00101100' ;GPIO, 0 = output pin
 tris GPIO  ;set I/O pin functions

 bcf SSR2  ;ssr2 is off
 bsf BLEEDER  ;bleeder is on
 btfss TE  ;is TE enable signal high
 goto TX0  ;no, so keep checking

 movlw 50  ;yes, make sure it was not a glitch
 movwf COUNT2
 call wait  ;wait 50ms
 btfss TE  ;is TE enable still high
 goto TX0  ;no, it was a glitch, keep waiting

 bcf BLEEDER  ;yes, turn off bleeder resistor
 clrf COUNT2  ; 1/4 second delay
 call wait  ;

 movlw 4  ;load COUNT2 with 4ms wait after zero crossing
 movwf COUNT2  ;which will be near AC peak
 call ACtrig  ;wait for +zero crossing of AC voltage
 call wait

 bsf SSR1  ;turn on SS relay 1 (soft start resistor)
 clrf COUNT2  ;load ms counter for 1/4 second delay
 call wait  ;allow power supply caps to charge

 movlw 4  ;load COUNT2 with 4ms wait after zero crossing
 movwf COUNT2  ;which will be near AC peak
 call ACtrig  ;wait for +zero crossing of AC voltage
 call wait
 bsf SSR2  ;turn on SS relay 2 (main)

;------------------------------ TURN OFF ---------------------------------
; turn off transformer at negative peak

TX1 bsf SSR1  ;ssr1 is on
 bsf SSR2  ;ssr2 is on
 bcf BLEEDER  ;bleeder is off
 btfsc TE  ;is TE enable signal low
 goto TX1  ;no, it is still high, so keep checking

 movlw 50  ;yes, make sure it was not a glitch
 movwf COUNT2
 call wait  ;wait 50ms
 btfsc TE  ;is TE enable still low
 goto TX1  ;no, it was a glitch, keep waiting

 movlw 12  ;yes, load 12ms wait after zero crossing
 btfsc ZR  ;using zero crossing SS relay?  ZR=1?
 movlw 4  ;yes, load 4ms wait after zero crossing
 movwf COUNT2  ;which will be near AC peak
 call ACtrig  ;wait for +zero crossing of AC voltage
 call wait
 bcf SSR2  ;turn off solid state relay 2
 clrf COUNT2  ;1/4 second delay
 call wait  ;
 movlw 12  ;load 12ms wait after zero crossing
 btfsc ZR  ;using zero crossing SS relay?  ZR=1?
 movlw 4  ;yes, load 4ms wait after zero crossing

 movwf COUNT2  ;which will be near AC peak
 call ACtrig  ;wait for +zero crossing of AC voltage
 call wait
 bcf SSR1  ;turn off SS relay 1

 clrf COUNT2  ;1/4 second delay
 call wait  ;

 bsf BLEEDER  ;turn on bleeder resistor
 clrf COUNT2  ;1/4 second delay for power supply bleed down
 call wait  ;
 goto main  ;wait for turn-on

;------------------------------ AC TRIGGER -------------------------------

;wait for a low  to high transition from the HCPL-3760 opto-coupler

ACtrig:
ac1 btfsc AC  ;is AC input signal low
 goto  ac1  ;no, it is high, keep waiting until low
 nop   ;yes, it is low now

ac0 btfss AC  ;is AC input signal high
 goto ac0  ;no, it is low, keep waiting until high
 nop   ;yes, it is high now
 return

;------------------------------ MS WAIT DELAY ----------------------------
;enter with milli-second value in COUNT2 register
;exits with COUNT1 and COUNT2 =0

wait:
wait1 clrf  COUNT1
wait2 nop
 decfsz COUNT1,1
 goto wait2
 decfsz COUNT2,1
 goto  wait1
 return
;-------------------------------------------------------------------------------

end
```

FIGURE 2



Using only a zero-crossing relay results in core saturation and a disastrous 46A peak current in the transformer's primary winding.

FIGURE 3



The smart-switch circuit in Figure 1 greatly reduces core saturation, resulting in well-behaved primary current. Trace R1 results from peak and same-polarity switching; trace 1 represents peak and opposite-polarity switching.

One internal diode in the optocoupler rectifies the ac signal to indicate the positive half cycle. The µC has two solid-state-relay outputs: SSR1 and SSR2. When the Transformer Enable input goes high, the µC waits 250 msec, detects the next positive edge from the optocoupler, waits 12 msec, and then turns off SSR1. SSR2 has a 250-msec delay from SSR1 and operates as a last-on, first-off output to shunt a soft-start resistor. Pin 3 is an optional output for a power-supply bleeder switch or a status indicator. (DI #2170) EDN

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