Analog Sample and Hold

This Sample and Hold design incorporates quite a number of features while using only six active devices – three general purpose opamps, one FET op amp, one N-FET and one PNP transistor. Here are some of the features:

Voltage Controlled Sample Clock
External Clock Input with Threshold Control
Single Sample Pushbutton
Wide Input Signal Range of –10 to +10volts
Wide Sample Clock Rate of 0.5 Hz to 8 Khz
Low Sample Droop Rate of less than 0.5% per second

The Sample and Hold

Referring now to the circuit diagram, the basic Sample and Hold Circuit is built around the op amp buffers labeled A and B, and the 2n5951 NFET switch. Op amp A can be any general purpose op amp such as a 741. It is used to buffer the input signal. Op amp B must be a FET type device, such as the LM351, used for its high input impedance. It acts as an output buffer for the sampled voltage held on the capacitor C1. The NFET serves as a switch that closes whenever op amp D outputs its 100 usec. pulse. During this 100useconds the NFET switch is closed and capacitor C1 charges or discharges to the input voltage level output from op amp A. At all other times the NFET switch is open so that the charge accumulated on C1 is effectively trapped between the two high FET resistances. Of course, nothing is perfect, so there is a slow leakage of C1's charge through op amp B's input resistance. For an LM351 this droop rate is less than 0.5% drop in voltage for every second.

The Pulse Generator

The circuitry around op amp D forms a pulse generator. The op amp itself acts as a comparator. The op amp output normally rests at –15v with the negative input at a diode drop of about –0.6v and the positive input at –7.5v as determined by resistors R6 and R7. Any sufficiently large positive voltage transition at the pulse generator's input will be coupled through capacitor C4 and diode D1 to drive the positive input above the negative input's –0.6v. With this change in the op amp's positive input, the output immediately goes high to +15v and the positive input's rest voltage is brought to +7.5v. The negative input, in the meantime, reacts slower as capacitor C3 charges toward +15v through R5. After about 100 usec., the negative input's voltage has risen to just above the positive input's +7.5v. The output then goes low to its original state of –15v.

The output pulse width is set by R6, R7, R5, and C3. The sampling time of 100us was chosen to be as short as possible while still allowing time for the holding capacitor

C1 to charge or discharge to the new input voltage. This pulse width limits the maximum sampling clock rate to about 8 KHz.

A full –15v to +15v pulse was used to switch the NFET in order to accommodate a large input signal voltage range. Input signals can range from –10v to +10v. This allows sampling of synthesizer control voltages as well as audio signals.

The Sampling Clock

Op amp C is used to form the sampling clock. The 2-position switch, in the position shown in the circuit diagram, completes a positive feedback path from the op amp's output to its positive input. This results in a voltage-controlled clock.

The op amp C itself functions as a comparator. Its negative input is set at about 0.6v by resistors R8 and R9 when there is no CV Input. When a Control Voltage Input is present, the negative op amp input is set slightly below the actual CV input voltage. As a starting point for our sequence of events, consider op amp C's output at –15v. The PNP transistor is in saturation with its collector at +15v. Capacitor C2 is quickly charged to +15v through R3 and the diode D3. Ideally, this charging should be as fast as possible so that C2 is fully charged to 15v before the op amp switches to +15v. However, the current limiting R3 has been inserted to prevent glitches on the supply lines and subsequent coupling of the sampling clock to the Sample and Hold output. The additional time required to allow C2 to fully charge is bought by inserting a 100pf capacitor and a 2M resistor between the output and positive input. This couples the high-to-low transition of the comparator output to the positive input, which brings it below the negative input for the necessary time. After the comparator's output goes high the transistor goes into cutoff and C2 slowly discharges toward ground through R2, R3, and R4. R2 is made variable to act as a clock rate control. The comparator does not switch to –15v again until the capacitor's voltage drops below the voltage as seen by the negative input, making the CV input act as a second clock rate control. High CV Input voltages effectively shorten the discharge time of C2 and thus increase the sampling clock's frequency. The resulting waveform at C's output is a pulse oscillator and the waveform at the positive input is a sawtooth.

The two switches provide a number of additional operating modes for the Sample Clock. When the clock is in its free running mode, the pushbutton can stop the clock. It stops it by holding the positive input of the comparator high for as long as the pushbutton is pressed.

When the 2-positive switch is switched to External Clock, the operation of the positive feedback path is broken and the op amp acts as a simple comparator with the External signal as an input. The CV Input now acts as a switching threshold control. One application would be to use a noise source as the External clock Input. In such a setup the sampling becomes random with an overall rate controlled by the CV Input threshold setting.

With no External Clock Input, the pushbutton can be used for single sample triggering.

Control Voltage Noise Generator

A second circuit provides a randomly varying signal for either the Sample and Hold's main input or its external clock input.

The 3080 chip is a transconductance device. The noise signal from the 2N967 transistor junction is amplified by about 1000 (220K/220). The output of the 3080 is a current that charges and discharges the 1.0uF capacitor with the amplified noise signal. The amount of current available for this process is determined by the Rate control 741 op amp. A smaller rate means that less current is available to charge and discharge the capacitor so that it is unable to keep up with the fast changes of the noise signal. A larger rate input voltage translates into more current at the output of the 3080 allowing the changing voltage on the capacitor to keep up with the amplified noise signal. Finally, the output 741 provides a means to adjust the final voltage offset and gain with trimmers.

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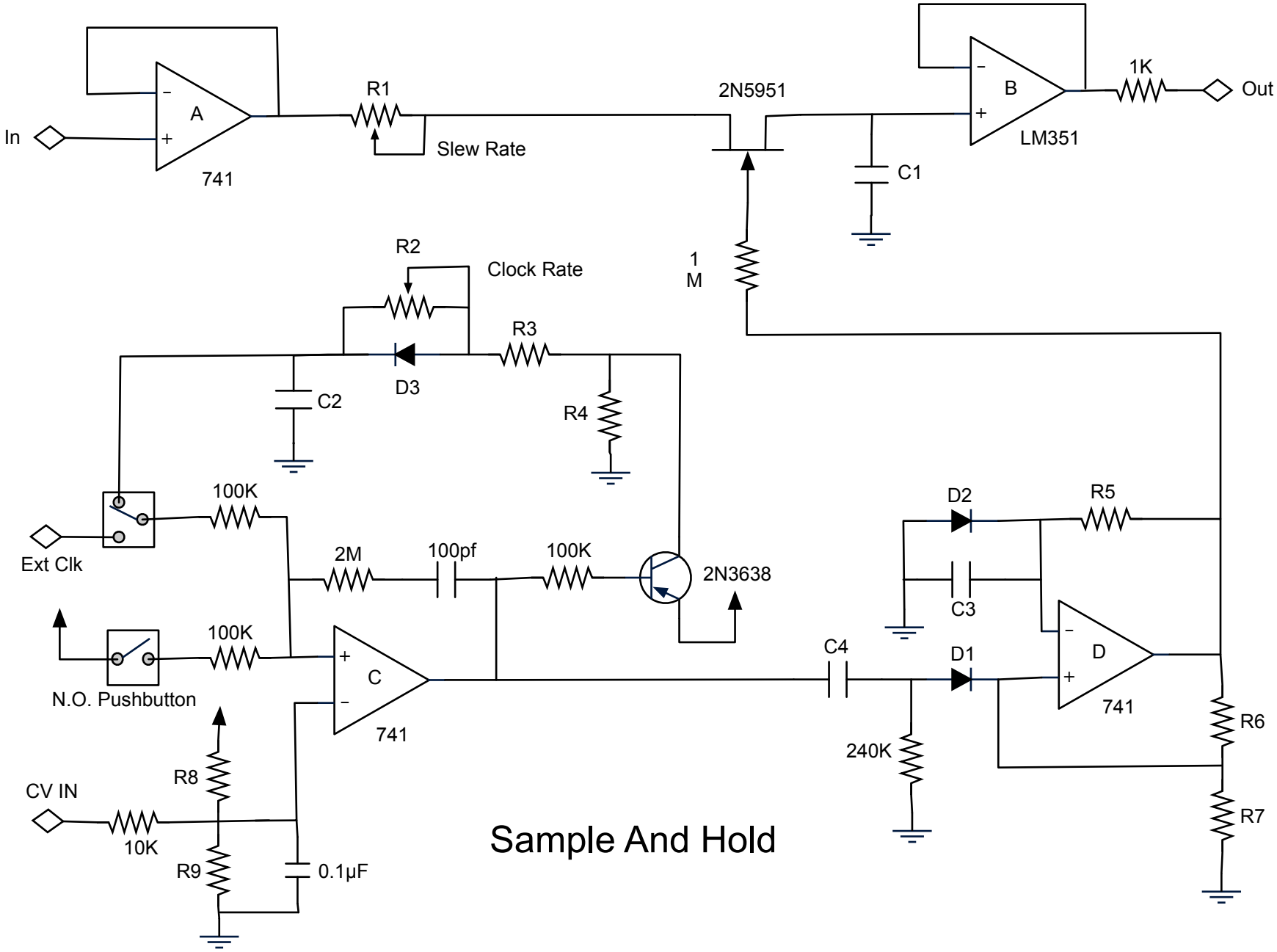
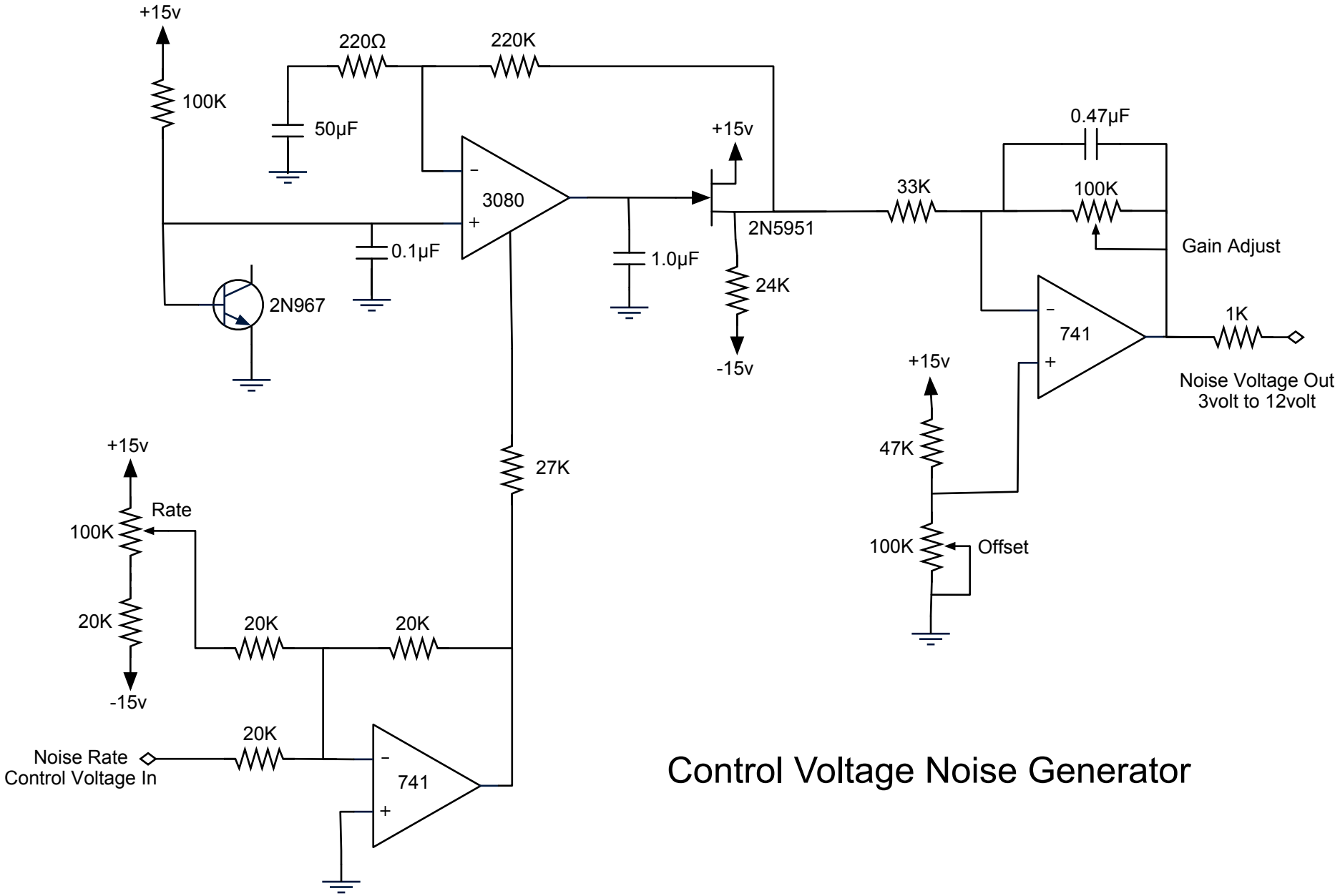

In
A
741
R1
Slew Rate
2N5951
B
LM351
1K
Out
C1
R2
Clock Rate
1
M
R3
D3
C2
R4
100K
Ext Clk
2M
100pf
100K
2N3638
D2
R5
C3
100K
N.O. Pushbutton
C
741
C4
D1
D
741
240K
R6
R7
R8
CV IN
10K
R9
0.1µF
Sample And Hold



Control Voltage Noise Generator