Revision A

DN 6000322A

TECHNICAL MANUAL
MODEL 521VA
• REAL TIME DATA STORAGE SYSTEM •

Acroamatics, Inc.
70 South Kellogg Avenue
Goleta, CA 93117-3476
February 15, 2001

ACROAMATICS DOCUMENT HISTORY

The following table indicates major changes made to *Engineering Specification - Model 521V Data Storage & Recovery System*, Acroamatics Document Number 6000322, released on June 5, 2000, and contains a record of all revisions made since that date.

DN6000322 CHANGE HISTORY			
Rev	**Date**	**Action**	**Name**
	6-5-00	Original Issue	DJM
A	2-14-01	Updated to 521VA	DJM

TECHNICAL MANUAL
MODEL 521VA
• REAL TIME DATA STORAGE SYSTEM •

TABLE OF CONTENTS

TECHNICAL MANUAL
MODEL 521VA
• REAL TIME DATA STORAGE SYSTEM •

SECTION 1
INTRODUCTION

1.1 DESCRIPTION

The Real-time Data Storage System records data input from either the processed telemetry data bus (the TDP A-bus) or the VMEbus. Recording is initiated by commands from the TDP internal computer to VMEbus-addressable registers on the *521VA Real Time Data Storage (RTDS)* VMEbus card. The recording operation archives data at sustained rates up to 20 MBytes/sec without intervention from the host processor. This rate is consistent with the maximum data message rate that the VME TDP can generate. Although higher rates can be achieved with much more complex hardware, the higher rates would not be beneficial in typical applications.

A single drive cannot sustain the 20 Mbyte carry-away rate the Fast SCSI bus supports for synchronous transfers. Disk drives have overhead that offsets their instantaneous transfer rates so that the sustainable rate is a fraction of the instantaneous rate. To achieve higher transfer rates typically requires a system to operate with four drives per SCSI bus, filling these buffers at the 10 Mbyte rate, then moving to the next drive and filling its buffer, and so-on. This process is called *striping of the data* and it is a conventional method for improving sustained disk transfer rates.

The basic Real-time Data Storage System consists of the 521VA RTDS card and internal cabling for an appropriate Acroamatics TDP. You can use this base system in your TDP with two internal disk drives (for systems requiring only limited storage) or with external disks in an expansion unit.

1.1.1 Data Storage & Expansion Unit

The Data Storage System *Expansion Unit* is an expansion chassis with power supply, internal cabling and up to eight removable hard disk drives. The removable disk drives are industry standard disk drives installed in the carrier assembly in the Expansion unit. The recording system provides storage up to eight times the capacity of a single drive (all drives must be the same capacity) when configured with either six external and two internal drives - or with eight external drives. For instance, using 9GB drives will provide 72GB of storage. The upper storage limit per eight drives (per controller) is one Terabyte.

The rack mountable expansion chassis is a seven inch high rack mountable chassis, and includes the pair of SCSI cables required to connect the expansion chassis to the TDP.

You can configure this system to meet particular recording needs. For field operations requiring lower total bandwidth and less recording capacity you can use the system with only the two drives installed in the TDP. For use with systems that have no room in the TDP for the two drives, you can use the external

chassis alone with all eight drives installed there.

1.1.2 521VA A-Bus Recording

During a telemetry data acquisition the 521VA RTDS card buffers data received from the A-bus stream into a hardware-managed 1MB memory. An option is available to expand the buffer memory to 4MB. The memory is divided into four memory pages (two for input message formation and two for completed data records) which are transferred to or from the two SCSI controllers to the disk drives. The card divides the incoming data stream into frame buffer messages, usually containing a fixed number of telemetry samples, proceeded by a time header. The number of words in the buffer is determined by the frame buffer size, which is a programmable number of 16-bit sequential data stream data words. The maximum transfer rate block size is a function of the disk drives used, and should be as large as the disk cache memory. The disk is addressed as clusters of sectors, and maximum disk utilization occurs when the buffer size is evenly divisible by the cluster size. Block sizes up to 256kB are supported with the 1MB memory, and up to 1MB with the optional 4MB memory. There is a separate transfer path for each of the two SCSI busses. When you select dual bus operation the memory manager hardware directs the data blocks alternately between the two busses. The embedded processor controlling this operation receives an interrupt at the completion of each new block, at which time it issues the commands that cause the record to be output on the appropriate SCSI bus. If the associated disk drive on the selected SCSI bus is ready, it will initiate the transfer to that SCSI bus and disk drive. The processor then commands the memory control hardware to transfer the block of data to the selected SCSI bus. When a SCSI transfer completes, the processor determines whether another buffer is complete and, if so, selects the next disk drive or alternate SCSI bus to receive data, and initiates the transfer. Each SCSI bus will service one to four high performance 3.5 inch disk drives, depending on the system configuration. SCSI Bus One feeds disk drives 1-3-5-7, and SCSI Bus Two feeds drives 2-4-6-8. A sequence of block transfers is as follows: first block to SCSI 1, drive 1, second block to SCSI 2 drive 2, third to SCSI 1 drive 3, fourth to SCSI 2 drive 4, etc. If you do not require high transfer rates, you can configure the controller to operate with a single SCSI bus.

1.1.3 VMEBUS Data Recording

You can also record data from the VME bus. The system supports two methods of data transfer: conventional double-buffered DMA, and a memory mapped data transfer path. Both methods require the recording block length to be the same as the length of the record being transferred. The host processor controls DMA transfers by loading Starting and Backup address registers and Transfer Length counters. The host is interrupted at the end of each DMA transfer and controls the rate of transfer by reloading the Word Length register. The embedded 386EX processor is interrupted at the finish of each DMA so that it may transfer the block of data to the appropriate disk drive. The first complete record following the Record ON will be the first record recorded. Record OFF works similarly in that the last complete buffer following a Record OFF will be recorded and if the DMA channel is left enabled the data will be transferred to the frame buffer memory but will not be recorded on the disk drive.

When the data record memory is selected as memory mapped, the DMA starting address register specifies the VME address at which the input record page (256k bytes) starts. The DMA record length register defines the number of 32-bit words in the data record. Once the current memory page has been written with the number of words in a record, the memory page is rotated to provide a new empty page (assuming an empty page is available). The completed record is transferred to disk via the SCSI bus if the Record ON command has been received.

The recorded data is read back via the VME bus using either DMA or memory mapped operations. The host first asks for the file directly. You recover data by reading the records from programmable *START* and *STOP* times.

1.2 SYSTEM APPLICATION SOFTWARE

The RTDS card contains an embedded processor that automatically detects the number of disk drives attached to each of the SCSI busses and controls the data recording strategy to maximize the recording bandwidth. It also initiates the transfer of data to and from the SCSI channels, and it keeps records of the relationship between IRIG time and data record blocks. This feature enables a rapid search of large volumes of recorded data. You can start and stop data recording using either IRIG times or Start/Stop Immediate commands. The Host processor can read the recorded data through a dual-ported memory (memory-mapped into the VME address space) and also addressable by the disk recording logic.

TDP software running on the PC VME Host in the TDP supports the following tasks:

1. Initiate and stop data recording independently of the TDP running and stopping.

   Data recording on a Real Time Data Storage Device (RDSD) uses an entirely different data path from data recording on the local hard disk drive and you can continue to record data there as well as on the RDSD. Recording on the RDSD does not use the VME Host DMA channel but connects to a different A-bus device address. This means that anything you want to record on the RDSD requires additional Distribution programming. For example, to record on both the local disk drive and the RDSD you need to have the programming:

   ```
   idtag:  PAS
           PAS DV2
   ```

   That sends the data to both ports. On the other hand, to send data only to the RDSD, you can just add the command

   ```
   OUT DV2
   ```

   At the start of your distribution program and all data you output will go there.

2. Recover data from the disk system and transfer it to a file on the Host computer disk drive.

   Software also transfers data from the RDSD, selected according to a time window, to a file on the VME host computer. From there, you can use existing software to analyze or transmit the data to other systems by way of the Ethernet link. This software moves the data from the RDSD to any

file accessible device on the VME host, including tape drives, optical disk recorders, and network files on other systems. There are also library functions that user-written software can use to access data on the RDSD.

3. Reconstruct recorded data

   Software also accesses data on the RDSD selected by the time window. This transmits to the reconstructor section, allowing you to play back recorded data through the TDP front end for real-time display, output to DACs, and further pre-processing. To use this feature you must format the data in a form acceptable to the reconstructor.

SECTION 2
INSTALLATION

2.1 GENERAL

This section contains installation information for the Acroamatics Model 521VA RTDS. The card part number is 6011521.

2.2 UNPACKING

Using proper ESD-protection procedures, open the cardboard shipping container and remove the card from the anti-static bag. Retain the container, anti-static bag, and foam packaging material for use if you must return the card.

2.3 FACTORY RETURN

When you return a card to the factory for repair or modification, include as much information as possible describing the failure mode or the modification/update you want.

Pack the card for shipment by wrapping it in the anti-static bag. Place the card into the shipping container, protecting it with the foam packing, and secure the container with reinforced tape. Provide the name and phone number of a technical contact we can talk to regarding the card.

Call Acroamatics at (805) 967-9909 to get an RMA number before returning any equipment to the factory, and include the number in any correspondence or shipments to Acroamatics.

2.4 INSTALLING

The RTDS card mounts in a standard VMEbus chassis. Mounting dimensions are shown in the assembly Drawing in Section 6 of this manual. Slide the card into one of your system VME chassis slots and seat the card firmly by pressing against the ears. Make the front panel cable connections appropriate to your system. Remove the board by pulling firmly on the outside of the ears.

2.5 CONNECTORS

The following pages contain tables of information on all the connections into and out of the RTDS card.

TABLE 2-1. MATING CONNECTOR LIST FOR MODEL 521VA

CONN.	FUNCTION	MATING CONNECTOR
P01	VMEbus	603-2-IEC-C096
P02	VMEbus	603-2-IEC-C096
J01	A BUS	7964-656EC
J02	HSL OUT	
J03	HSL IN	
J04	WIDE SCSI	

TABLE 2-2. CONNECTOR LIST
MODEL 521VA BACKPLANE CONNECTOR P01-ROW-A

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED00	Data Bus 00
02	4VMED01	Data Bus 01
03	4VMED02	Data Bus 02
04	4VMED03	Data Bus 03
05	4VMED04	Data Bus 04
06	4VMED05	Data Bus 05
07	4VMED06	Data Bus 06
08	4VMED07	Data Bus 07
09	GND	Ground
10	SYSCLK ($)	System Clock
11	GND	Ground
12	9VMEDS1	Data Strobe 1
13	9VMEDS0	Data Strobe 0
14	9VMEWRT	Write
15	GND	Ground
16	9VMDACK	Data Transfer Acknowledge
17	GND	Ground
18	9VMASTB	Address Strobe
19	GND	Ground
20	9VMIACK	Interrupt Acknowledge
21	9VMIAIN	Interrupt Acknowledge IN
22	9VMIAOT	Interrupt Acknowledge OUT
23	4VMAM04	Address Modifier 4
24	4VMEA07	Address Bus 07
25	4VMEA06	Address Bus 06
26	4VMEA05	Address Bus 05
27	4VMEA04	Address Bus 04
28	4VMEA03	Address Bus 03
29	4VMEA02	Address Bus 02
30	4VMEA01	Address Bus 01
31	-12 VDC ($)	-12 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-3. CONNECTOR LIST
MODEL 521VA BACKPLANE CONNECTOR P01-ROW-B

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	9VMBSBY	Bus Busy
02	9VMBCLR	Bus Clear
03	ACFAIL ($)	AC Power Fail
04	9VMBGI0	Bus Grant 0 IN
05	9VMBGO0	Bus Grant 0 OUT
06	9VMBGI1	Bus Grant 1 IN
07	9VMBGO1	Bus Grant 1 OUT
08	9VMBGI2	Bus Grant 2 IN
09	9VMBGO2	Bus Grant 2 OUT
10	9VMBGI3	Bus Grant 3 IN
11	9VMBGO3	Bus Grant 3 OUT
12	9VMBRQ0	Bus Request 0
13	9VMBRQ1	Bus Request 1
14	9VMBRQ2	Bus Request 2
15	9VMBRQ3	Bus Request 3
16	4VMAM00	Address Modifier 0
17	4VMAM01	Address Modifier 1
18	4VMAM02	Address Modifier 2
19	4VMAM03	Address Modifier 3
20	GND	Ground
21	SERCLK ($)	Serial Clock
22	SERDAT ($)	Serial Data
23	GND	Ground
24	9VMIRQ7	Interrupt Request 7
25	9VMIRQ6	Interrupt Request 6
26	9VMIRQ5	Interrupt Request 5
27	9VMIRQ4	Interrupt Request 4
28	9VMIRQ3	Interrupt Request 3
29	9VMIRQ2	Interrupt Request 2
30	9VMIRQ1	Interrupt Request 1
31	+5 VSTDBY ($)	Stand-by +5 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-4. CONNECTOR LIST
MODEL 521VA BACKPLANE CONNECTOR P01-ROW-C

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED08	Data Bus 08
02	4VMED09	Data Bus 09
03	4VMED10	Data Bus 10
04	4VMED11	Data Bus 11
05	4VMED12	Data Bus 12
06	4VMED13	Data Bus 13
07	4VMED14	Data Bus 14
08	4VMED15	Data Bus 15
09	GND	Ground
10	SYSFAIL ($)	System Failure
11	9VMBERR	Bus Error
12	9VMPRST	System Reset
13	9VMELWD	Long Word
14	4VMAM05	Address Modifier 5
15	4VMEA23	Address Bus 23
16	4VMEA22	Address Bus 22
17	4VMEA21	Address Bus 21
18	4VMEA20	Address Bus 20
19	4VMEA19	Address Bus 19
20	4VMEA18	Address Bus 18
21	4VMEA17	Address Bus 17
22	4VMEA16	Address Bus 16
23	4VMEA15	Address Bus 15
24	4VMEA14	Address Bus 14
25	4VMEA13	Address Bus 13
26	4VMEA12	Address Bus 12
27	4VMEA11	Address Bus 11
28	4VMEA10	Address Bus 10
29	4VMEA09	Address Bus 09
30	4VMEA08	Address Bus 08
31	+12 VDC ($)	+12 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-5. CONNECTOR LIST
MODEL 521VA BACKPLANE CONNECTOR P02-ROW-A

PIN	SIGNAL	FUNCTION
01	9CHBRCV	RS-232 Receive Data
02	9CHBXMT	RS-232 Transmit Data
03	9SC1D12	Data Bus Bit 12
04	9SC1D13	Data Bus Bit 13
05	9SC1D14	Data Bus Bit 14
06	9SC1D15	Data Bus Bit 15
07	9SC1P1	Data Parity -
08	9SC1D0	Data Bus Bit 00
09	9SC1D1	Data Bus Bit 01
10	9SC1D2	Data Bus Bit 02
11	9SC1D3	Data Bus Bit 03
12	9SC1D4	Data Bus Bit 04
13	9SC1D5	Data Bus Bit 05
14	9SC1D6	Data Bus Bit 06
15	9SC1D7	Data Bus Bit 07
16	9SC1P0	Data Parity +
17	GND	Ground
18	4TR1PWR	Terminator Power
19	9SC1ATN	Bus Attentation
20	GND	Ground
21	9SC1BSY	Bus Busy
22	9SC1ACK	Bus Acknowledge
23	9SC1RST	Bus Reset
24	9SC1MSG	Bus Message
25	9SC1SEL	Bus Select
26	9SC1CDT	Bus Command
27	9SC1REQ	Bus Request
28	9SC1IOT	Input_Output
29	9SC1D8	Data Bus Bit 08
30	9SC1D9	Data Bus Bit 09
31	9SC1D10	Data Bus Bit 10
32	9SC1D11	Data Bus Bit 11

TABLE 2-6. CONNECTOR LIST
MODEL 521VA BACKPLANE CONNECTOR P02-ROW-B

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	+5 VDC	+5 Volts DC
02	GND	Ground
03	RESERVED ($)	
04	4VMEA24	Address Bus 24
05	4VMEA25	Address Bus 25
06	4VMEA26	Address Bus 26
07	4VMEA27	Address Bus 27
08	4VMEA28	Address Bus 28
09	4VMEA29	Address Bus 29
10	4VMEA30	Address Bus 30
11	4VMEA31	Address Bus 31
12	GND	Ground
13	+5 VDC	+5 Volts DC
14	4VMED16	Data Bus 16
15	4VMED17	Data Bus 17
16	4VMED18	Data Bus 18
17	4VMED19	Data Bus 19
18	4VMED20	Data Bus 20
19	4VMED21	Data Bus 21
20	4VMED22	Data Bus 22
21	4VMED23	Data Bus 23
22	GND	Ground
23	4VMED24	Data Bus 24
24	4VMED25	Data Bus 25
25	4VMED26	Data Bus 26
26	4VMED27	Data Bus 27
27	4VMED28	Data Bus 28
28	4VMED29	Data Bus 29
29	4VMED30	Data Bus 30
30	4VMED31	Data Bus 31
31	GND	Ground
32	+5 VDC	+5 Volts DC

TABLE 2-7. CONNECTOR LIST
MODEL 521VA BACKPLANE CONNECTOR P02-ROW-C

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	GND	Ground
02	GND	Ground
03	4SC1D12	Data Bus Bit 12
04	4SC1D13	Data Bus Bit 13
05	4SC1D14	Data Bus Bit 14
06	4SC1D15	Data Bus Bit 15
07	4SC1P1	Data Parity 1
08	4SC1D0	Data Bus Bit 00
09	4SC1D1	Data Bus Bit 01
10	4SC1D2	Data Bus Bit 02
11	4SC1D3	Data Bus Bit 03
12	4SC1D4	Data Bus Bit 04
13	4SC1D5	Data Bus Bit 05
14	4SC1D6	Data Bus Bit 06
15	4SC1D7	Data Bus Bit 07
16	4SC1P0	Data Parity 0
17	4SC1SEN	DIFF Sense
18	4TR1PWR	Terminator Power
19	4SC1ATN	Bus Attentation
20	GND	Ground
21	4SC1BSY	Bus Busy
22	4SC1ACK	Bus Acknowledge
23	4SC1RST	Bus Reset
24	4SC1MSG	Bus Message
25	4SC1SEL	Bus Select
26	4SC1CDT	Bus Command
27	4SC1REQ	Bus Request
28	4SC1IOT	Input_Output
29	4SC1D8	Data Bus Bit 08
30	4SC1D9	Data Bus Bit 09
31	4SC1D10	Data Bus Bit 10
32	4SC1D11	Data Bus Bit 11

TABLE 2-8. CONNECTOR LIST
MODEL 521VA FRONT PANEL CONNECTOR J01

PIN	SIGNAL	FUNCTION
01		Not Used
02	9AWORD1	A Bus Last Word Flag
03	4SFLAG1	A Bus Last Transfer Flag
04	4APORT1	A Bus Port Select 1
05	GND	Ground
06	4APORT0	A Bus Port Select 0
07	4ADEST2	A Bus Destination Select 2
08	4ADEST1	A Bus Destination Select 1
09	4ADEST0	A Bus Destination Select 0
10	4AOUT15	A Bus 15
11	4AOUT14	A Bus 14
12	GND	Ground
13	4AOUT13	A Bus 13
14	4AOUT12	A Bus 12
15	4AOUT11	A Bus 11
16	4AOUT10	A Bus 10
17	GND	Ground
18	4AOUT9	A Bus 09
19	4AOUT8	A Bus 08
20	4AOUT7	A Bus 07
21	4AOUT6	A Bus 06
22	4AOUT5	A Bus 05
23	4AOUT4	A Bus 04
24	GND	Ground
25	4AOUT3	A Bus 03
26	4AOUT2	A Bus 02
27	4AOUT1	A Bus 01
28	4AOUT0	A Bus 00
29	GND	Ground
30		
31		
32	GND	Ground
33		
34		
35	GND	Ground
36		
37		
38	GND	Ground
39		
40		

TABLE 2-8. (continued) CONNECTOR LIST
MODEL 521VA FRONT PANEL CONNECTOR J01

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
41	GND	Ground
42	4AOWAIT	A Bus Wait
43	4AOREST	A Bus Reset
44	GND	Ground
45	4AOUT31	A Bus 31
46	4AOUT30	A Bus 30
47	4AOUT29	A Bus 29
48	4AOUT28	A Bus 28
49	4AOUT27	A Bus 27
50	4AOUT26	A Bus 26
51	4AOUT25	A Bus 25
52	4AOUT24	A Bus 24
53	4AOUT23	A Bus 23
54	4AOUT22	A Bus 22
55	4AOUT21	A Bus 21
56	4AOUT20	A Bus 20
57	4AOUT19	A Bus 19
58	4AOUT18	A Bus 18
59	GND	Ground
60	4AOSTRB	A Bus Data Strobe
61	4ALWORD	A Bus Last Word
62	GND	Ground
63	4AOUT17	A Bus 37
64	4AOUT16	A Bus 36

TABLE 2-9. CONNECTOR LIST
MODEL 521VA FRONT PANEL CONNECTOR J02

PIN	SIGNAL	FUNCTION
01	9HLWAIT	Hot Link Wait
02		Ground
03	9HLXMTA	Hot Link Transmit -
04	4HLXMTA	Hot Link Transmit +
05		
06		
07		0 OHM
08		0 OHM
09		0 OHM

TABLE 2-9. CONNECTOR LIST
MODEL 521VA FRONT PANEL CONNECTOR J03

PIN	SIGNAL	FUNCTION
01		
02		Ground
03		
04		
05	9HLRCVA	Hot LinkReceive -
06	4HLRCVA	Hot LinkReceive +
07		0 OHM
08		0 OHM
09		0 OHM

TABLE 2-10. CONNECTOR LIST
MODEL 521VA FRONT PANEL CONNECTOR J04

PIN	SIGNAL	FUNCTION
01	4SC2D12	Data Bus Bit 12
02	4SC2D13	Data Bus Bit 13
03	4SC2D14	Data Bus Bit 14
04	4SC2D15	Data Bus Bit 15
05	4SC2DP1	
06	GND	Ground
07	4SC2D0	Data Bus Bit 00
08	4SC2D1	Data Bus Bit 01
09	4SC2D2	Data Bus Bit 02
10	4SC2D3	Data Bus Bit 03
11	4SC2D4	Data Bus Bit 04
12	4SC2D5	Data Bus Bit 05
13	4SC2D6	Data Bus Bit 06
14	4SC2D7	Data Bus Bit 07
15	4SC2DP0	
16	4SC2SEN	
17	4TR2PWR	Terminator Power
18	4TR2PWR	Terminator Power
19		
20	4SC2ATN	Bus Attentation
21	GND	Ground
22	4SC2BSY	Bus Busy
23	4SC2ACK	Bus Acknowledge
24	4SC2RST	Bus Reset
25	4SC2MSG	Bus Message
26	4SC2SEL	Bus Select
27	4SC2CDT	Bus Command
28	4SC2REQ	Bus Request
29	4SC2IOT	Input_Output
30	GND	Ground
31	4SC2D8	Data Bus Bit 08
32	4SC2D9	Data Bus Bit 09
33	4SC2D10	Data Bus Bit 10
34	4SC2D11	Data Bus Bit 11

TABLE 2-10. (continued) CONNECTOR LIST
MODEL 521VA FRONT PANEL CONNECTOR J04

PIN	SIGNAL	FUNCTION
35	9SC2D12	Data Bus Bit 12
36	9SC2D13	Data Bus Bit 13
37	9SC2D14	Data Bus Bit 14
38	9SC2D15	Data Bus Bit 15
39	9SC2DP1	
40	GND	Ground
41	9SC2D0	Data Bus Bit 00
42	9SC2D1	Data Bus Bit 01
43	9SC2D2	Data Bus Bit 02
44	9SC2D3	Data Bus Bit 03
45	9SC2D4	Data Bus Bit 04
46	9SC2D5	Data Bus Bit 05
47	9SC2D6	Data Bus Bit 06
48	9SC2D7	Data Bus Bit 07
49	9SC2DP0	
50	GND	Ground
51	4TR2PWR	Terminator Power
52	4TR2PWR	Terminator Power
53		
54	9SC2ATN	Bus Attentation
55	GND	Ground
56	9SC2BSY	Bus Busy
57	9SC2ACK	Bus Acknowledge
58	9SC2RST	Bus Reset
59	9SC2MSG	Bus Message
60	9SC2SEL	Bus Select
61	9SC2CDT	Bus Command
62	9SC2REQ	Bus Request
63	9SC2IOT	Input_Output
64	GND	Ground
65	9SC2D8	Data Bus Bit 08
66	9SC2D9	Data Bus Bit 09
67	9SC2D10	Data Bus Bit 10
68	9SC2D11	Data Bus Bit 11

SECTION 3
OPERATION

3.1 INTERFACE REGISTER SET

This section describes the arrangement and functions of the register set on the 521VA card. TABLE 3-1 lists the registers in address order, showing A16 utility space allocation. The address shown is the offset address (in hexadecimal) from the card base address set by switches on the card.

A16 Utility Registers		
Addr	**Function**	**Mode**
00	Signature	Read only
02	Memory Mapped A32 Base Address	Read/Write
04	DMA Command/Status	Read/Write
06	Interrupt Vector	Read/Write
08	DMA Primary Address (A31-A16)	Read/Write
0A	DMA Primary Address (A15-A2)	Read/Write
0C	DMA Backup Address (A31-A16)	Write Only
0E	DMA Backup Address (A15-A2)	Write Only
10	DMA Primary Word Count-High	Read/Write
12	DMA Primary Word Count-Low	Read/Write
14	DMA Backup Word Count-High	Write Only
16	DMA Backup Word Count-Low	Write Only
18	Doorbell Register to 386	Read/Write
1A	Mail Box Register 1	Read/Write
1C	Mail Box Register 2	Read/Write
1E	Mail Box Register 3	Read/Write
20	Mail Box Register 4	Read/Write
22	Mail Box Register 5	Read/Write
24	Mail Box Register 6	Read/Write

TABLE 3-1. RTDS Interface A16 Registers

The registers contain 521VA *command* and *status* information. Register locations are memory-mapped in the A16 Utility Address Space on a switch-selectable 64-byte boundary. You access the registers through nonprivileged or supervisory A16/D16 memory instructions.

3.2 Signature Register (Address 00)

The Signature Register identifies the installed 521VA card for system configuration purposes. Reading this register returns a value of 0x521, that is the bit pattern `x010100100001`. The x bit identifies the installed options. You should mask these bits during any card identification function.

Signature Register		
Addr	**Description**	**Mode**
0	X521	Read

TABLE 3-2. Signature Register

Signature Register Option Bits	
Bit	**Description**
15	Not Used
14	Not Used"
13	Not Used"
12	0 = 1MB, 1 = 4MB

TABLE 3-3. Option Bits in Signature Register

3.3 A32 Base Address Register (Address 02)

The base address register establishes the A32 block address of the record formation memory when this memory is to be accessed by memory mapping the input or output record into the VME address space. The record formation memory is 1MB (4MB optional) and one quarter of the memory is accessible as an input or output record therefore the memory uses 256kB (or 1MB) of VME address space and the base address register supplies the 11 most significant addresses for all A32 data transfers. The memory mapped method of data transfer can be used as an alternate to using the RTDS DMA when the device transferring the data prefers to use its own DMA. The record length register establishes the transfer length and when it is counted down to zero it is reloaded from the backup count register and the record formation memory is rotated to provide the next buffer thus providing sustained data transfers. Data transfers can be A32/D32, A32/D32 block mode, or A32/D64 block mode.

3.4 VME DMA SYSTEM

The DMA system on the 521VA card is a bi-directional transfer of data to or from VME memory to the record formation memory for *disk storage* operations, or from the record formation memory for *disk read* operations.

A 32-bit counter register called the *Primary Address Register* always contains the address of the next location to be accessed in VME memory. Two 16-bit transfers to the Primary Address Register (at address offsets 08 and 0A) load the starting A32 address for a block transfer. The Primary Address Register indicates it is loaded (DMA Status Register bit 8 reads as 1) upon loading the least significant 16 bits into address 0A.

A 20-bit *Primary Word Count* register holds the number of 32-bit words awaiting transfer from VME memory. Two 16-bit transfers to the primary word count register (address offsets 10 and 12, respectively) load the word count. Load this register with zero for a transfer count of 262,144. When the Primary Address Register has loaded status and the DMA Interface is enabled, the DMA transfers initiate. You should load the Primary Word Count register previous to this. The 32-bit

Backup Address register (formed by addresses 0C and 0E) holds the starting A32 address for the *next* block transfer that will occur after the *primary* transfer is complete. The 20-bit *Backup Count* register (addresses 14 and 16) contain the transfer length of that next block transfer.

the Primary Address register auto-increments with each DMA transfer. The Primary Word Counter auto-decrements until it reaches zero, signifying completion of the DMA transfer. If the Backup Address register is loaded, it's contents are transferred to the Primary Address Register while, in a similar fashion, the Backup Count register contents are transferred to the Primary Count Register and the DMA transfer continues. When the Backup Address register is empty the DMA transfer stops. In either case, an interrupt occurs if the DMA Terminal Count Interrupt is enabled.

The Backup Address register becomes loaded (DMA Status Register bit 9 reads as 1) when you load the least significant half (address 0E). A reasonable loading order is Backup Count, Backup Address MSH, and then Backup Address LSH. If the Primary Address is not loaded, the DMA is idle and the Backup Registers transfer immediately to the Primary Registers. If the Primary Address is loaded, the Backup Address retains *loaded* status until the DMA block transfer completes and the Backup Registers transfer to the Primary Registers. You then reload the Backup Registers. Thus you can consider the Primary and Backup registers a two location queue. You never have to load the Primary registers directly when you are performing double-buffered data transfers. For single buffered operation it is more convenient to use the Primary registers.

3.4.1 DMA Command/Status Register (Address 04)

The DMA Command/Status Register (CSR) provides control for the DMA interface, along with *enable* and *status* signals for the interrupt structure. TABLE 3-4 lists the *command* and *status* bits of the register. To the extent possible, the DMA control is identical to that of the 504VA DIST Card.

DMA Command/Status Register		
Bit	**Function**	**Mode**
15	DMA block transfers	Read/Write
14	DMA D64 transfers	Read/Write
13	DMA Transfers from disk	Read/Write
12	DMA auto run	Read/Write
11	DMA Interface Enable	Read/Write
10	DMA Interface Reset	Write Only
9	DMA Backup Address Loaded Status	Read Only
8	DMA Primary Address Loaded Status	Read
8	Enables writing of Bit 11	Write
7	Enables writing Bits 0, 1 & 2	Write only
6	Enables clearing of Bits 3, 4 & 5	Write only
5	386 Interrupt Status	Read only
4	Interrupt Status	Read Only
3	DMA Terminal Count Interrupt Status	Read Only
2	386 Interrupt Enable	Read/Write
1	MM Data Ready Interrupt Enable	Read/Write
0	DMA Terminal Count Interrupt Enable	Read/Write

TABLE 3-4. DMA Command/Status Register

The following bit descriptions describe the condition that results when you set the specified command bit to **1**. For a status bit, the state described exists when you read the specified bit as **1**. Some bits have both a command and a status function.

Bit 15 - DMA transfers will be in block mode.

Bit 14 - DMA transfers will be in 64 bit block mode.

Bit 13 - DMA transfers will be read from the disk. If the bit is set to **0** the transfers are to the disk.

Bit 12 - if set to **1**, the DMA will be in auto run mode, which will cause the DMA to ping pong between the primary and backup address pointers automatically without host intervention.

Bit 11 - Command: enables the DMA to begin transfers.

Bit 10 - Command: clears the DMA Primary and Backup Address Loaded status.

Bit 9 - Status: the DMA Backup Address is loaded.

Bit 8 - Status: the DMA Primary Address is loaded.
Command: enables you to write to Command bit 11.

Bit 7 - Command: enables you to write bits 2, 1, & 0 of the register.

Bit 6 - Command: clears the current interrupt status, bits 5-3.

Bits 5, 4 & 3 - Status: records the source or sources of an interrupt. The bits remain set until cleared by writing **1** to bit 6. If another interrupt causing-event occurs before the Interrupt Status bits are cleared, the interrupt controller queues the second interrupt and its sources until the current interrupt status is cleared. An interrupt from a given source occurs only if the corresponding Interrupt Enable bit is set to **1**. If the Interrupt Enable bit is not **1**, the corresponding status bit cannot be set.

Bit 2 - Command: allows an interrupt when the 386 doorbell register is loaded.

Bit 1 - Command: allows an interrupt when the memory mapped frame buffer memory has data ready in Read mode - or is ready for data in Write mode.

Bit 0 - Command: allows an interrupt when DMA Primary Word Count reaches zero.

3.4.2 Interrupt Vector Register (Address 06)

The Interrupt Vector Register holds a 16-bit address that addresses the memory cell containing the address of the common interrupt service routine that services all three possible interrupts from the 521VA card.

3.4.3 Communications Port

A block of registers mediate communications between the host and the 386EX embedded processor. The first of these registers forms the *doorbell register.* The following six registers form *mailbox registers* one through six. To communicate, the host loads the necessary *command string* into the six mailbox registers. Next, a *command function* is loaded into the doorbell register, which in turn interrupts the 386EX to indicate a communication request. This action also resets the lower status byte. When the 386EX receives the command and associated command string it may initiate a response to the host, following the same protocol procedure as the host. A VME host interrupt may be enabled to check the doorbell register for a “non-zero” state in the status portion of the register. This action also resets the upper command byte.

3.4.4 Doorbell Register (Address 18)

This register is divided into two parts to provide communications protocol between the host and embedded processors. The upper byte is defined as the command register to the 386EX. The lower byte is defined as the status register from the 386EX.

Doorbell Register		
Bits	**Function**	**Mode**
15-8	Command to 386EX	Read/Write
7-0	Status from 386EX	Read Only

TABLE 3-5. Doorbell Register

3.4.5 Mailbox Registers (Addresses 1A, 1C, 1E, 20, 22, & 24)

These registers are writable (read by the 386EX) and readable (written by the 386EX).

Mailbox Registers		
Bits	**Function**	**Mode**
15-0	Data to 386EX	Write Only
15-0	Data from 386EX	Read Only

TABLE 3-6. Mailbox Registers

3.5 386EX I/O REGISTERS

386EX I/O REGISTERS		
Addr	**Function**	**Mode**
00	Disk Storage Configuration Register	Read/Write
02	Doorbell Register	Read/Write
04	Mailbox Register 1	Read/Write
06	Mailbox Register 2	Read/Write
08	Mailbox Register 3	Read/Write
0A	Mailbox Register 4	Read/Write
0C	Mailbox Register 5	Read/Write
0E	Mailbox Register 6	Read/Write
10	Formation Buffer, Low Address	Read/Write
12	Formation Buffer, High Address	Read/Write
20	Data Control Register	Read/Write
22	Time Word - Major Time 1	Read/Write
24	Time Word - Major Time 2	Read/Write
26	Time Word - Milliseconds	Read/Write
28	Frame Buffer Header Control Register	Read/Write
2A	Frame Buffer Message Control Register	Read/Write
2C	Header Fixed Word 1	Read/Write
2E	Header Fixed Word 2	Read/Write
30	Header Fixed Word 3	Read/Write

TABLE 3-7. 386EX I/O Registers

3.5.1 Disk Storage Configuration Register (Address 0)

Disk Storage Configuration Register		
Bit	**Function**	**Mode**
0	Disk Controller A Enabled	Read/Write
1	Disk Controller B Enabled	Read/Write
2	Select Data Source	Read/Write
3	Disk Data Direction	Read/Write
4	Test Mode	Read/Write
5	Enable Writing to Buffers	Read/Write
6	Mask for Interrupt	Read/Write
7	Overflow	Read
7	Overflow Clear	Write
8,9	Formation Buffer Upper Address	Read only
10	SCSI Buffer 1 Full	Read only
11	SCSI Buffer 2 Full	Read only
12	Buffer Overflow	Read/Write
13	Not Used	n/a
14	Not Used	n/a
15	Not Used	n/a

TABLE 3-8. Disk Storage Configuration Registers

Bit 0 - When set to **1** enables data to be transferred to or from SCSI Port A.

Bit 1 - When set to **1** enables data to be transferred to or from SCSI Port B.

Bit 2 - This bit defines the data source when writing to disk: 0 = A-bus data/HOTLink, and 1 = VME data. When reading the disk, the target is defined as: 0=HOTLink, 1=VME.

Bit 3 - Determines the data direction: 0 = data is written to the disk, and 1 = data is read from the disk.

Bit 4 - Test Mode - creates buffers but not sent to SCSI busses.

Bit 5 - Enables the writing of data to the formation buffers.

Bit 6 - Mask bit for Overflow Interrupt during RUN.

Bit 7 - This bit, when set to **1** causes any remaining non-full buffers to be flushed out to the SCSI drives when the next data arrives.

Bits 8,9 - These bits indicate which formation buffer is currently being serviced.

Bit 10 - This bit set to **1** indicates a buffer is ready for SCSI bus 1.

Bit 11 - This bit set to **1** indicates a buffer is ready for SCSI bus 2.

Bit 12 - This bit set to **1** indicates a buffer overflow condition occurred. Write clears flag.

3.5.2 Communications Port

A block of registers mediate communications between the 386EX embedded processor and the VME host. The first of these registers forms the *doorbell register.* The following six registers form *mailbox registers* one through six. To communicate with the host, the 386EX will wait for a command loaded by the host, which will cause an interrupt to the 386EX. The command and command string will be read by the 386EX and it may send back a respond signal. It must first load the mailbox registers and then the doorbell. register. This will reset the host status byte and signal to the host that a valid response is awaiting.

3.5.3 Doorbell Register (Address 2)

This register is divided into two parts to provide communications protocol between the host and embedded processors. The upper byte is defined as the command register to the VME host. The lower byte is defined as the status register from the VME host.

Doorbell Register (Address 2)		
Bits	**Function**	**Mode**
15-8	Command to VME host	Read/Write
7-0	Status from VME host	Read Only

TABLE 3-9. Doorbell Register

3.5.4 Mailbox Registers (Addresses 4, 6, 8, A, C, & E)

These registers are writable (read by the VME host) and readable (written by the VME host).

Mailbox Registers (Addresses 4,6,8,A,C,E)		
Bits	**Function**	**Mode**
15-0	Data to VME host	Write Only
15-0	Data from VME host	Read Only

TABLE 3-10. Mailbox Registers

3.5.5 Formation Address Counter (Addresses 10, 12)

Formation Address Counter - Low Address 10		
Bits	**Function**	**Mode**
15-0	Formation Count - Low	Read Only

TABLE 3-11. Formation Address Counter - Low

Formation Address Counter - High Address 12		
Bits	**Function**	**Mode**
2-0	Formation Count - High	Read Only

TABLE 3-12. Formation Address Counter - High

3.5.6 Data Control Registers

Data Control Register (Address 20)		
Bits	**Function**	**Mode**
15	Data Formation Enable	Read/Write
14	Startup Option 1	Read/Write
13	Startup Option 0	Read/Write
12	Time Source	Read/Write
11	Hot Link Test Mode	Read/Write
10-9	Select Data Source	Read/Write
8	Drive A-bus Wait	Read/Write
7	Hot Link Data Direction	Read/Write
6	Enable Block Mode	Read/Write
5	Data Only	Read/Write
4	A-bus Time Dest. Bit 1	Read/Write
3	A-bus Time Dest. Bit 0	Read/Write
2	A-bus Destination Bit 2	Read/Write
1	A-bus Destination Bit 1	Read/Write
0	A-bus Destination Bit 0	Read/Write

TABLE 3-13. Data Control Register

Bit 15 - Enables the transfer of data to the formation buffer.

Bits 14, 13 - Select the startup option as follows:

```
Op 1  Op 0    Mode
----  ----    ----
 0     0      Begins transfer on first Word received
              after in run
 0     1      Begins transfer on first Framed Word received
              after in run
 1     0      Begins transfer on first Time Word received
              after in run
 1     1      Reserved
```

Bit 12 - Defines the time of day source for header stamping: 0 = time is loaded from the A-bus by time DITs; 1 = the host computer presets the time and then it is put in generate mode.

Bit 11 - This bit puts the hot link receiver and transmitter in test mode for self diagnostics: 0 = normal mode; 1 = test mode.

Bits 10,9 - These bits define the data source for disk writing as follows:

Bit 10	Bit 9	Description
0	0	Select A-Bus
0	1	Select HOTLink
1	X	Select VME

Bit 8 - This bit allows the A-bus FIFO not to drive the wait signal: 0 = drive wait; 1 = Do not drive wait.

Bit 7 - Selects the hot link data direction: 0 = data is received by hot link; 1 = data is transmitted by hot link.

Bit 6 - Enables Block Mode.

Bit 5 - Enables Data Only Mode.

Bits 4, 3 - A-bus device selection bits to recover time and Q word.

Bits 2, 1, 0 - A-bus device selection bits for all data types.

3.6 TIME BASE GENERATOR FEATURE

The Model 521VA has a Time Base Generator that delivers time messages to the 386EX, which uses the time to annotate the start of each recorded block of data so that data can be recovered using a user supplied start and stop time. By using a bit in the data control register, the host computer can preset the time and then generate from that time, or the time register can be loaded from the A-bus by time dits.

3.6.1 Time-Of-Year Data Registers (Addresses 22, 24, 26)

The three registers at addresses 22, 24, and 26 preset a time of year counter that computes the current time-of-year in BCD.

Time Words				
Data Bits				Description
15 - 12	11 - 8	7 - 4	3 - 0	
TIME Word 1 - Address 22				
x x x x	x x x x	x x x x	x x x x	MAJOR TIME: DAYs, HOURs
x x x x				Tens of Days (BCD)
	x x x x			Units Days (BCD)
		x x		Tens of Hours (0-2)
		x x	x x	Units Hours (BCD)
			x x	Hundreds of Days (0-3)
TIME Word 1 - Address 24				
x x x x	x x x x	x x x x	x x x x	MAJOR TIME: MINs, SECs
x x x x				Tens of Minutes (0-5)
	x x x x			Units Minutes (BCD)
		x x x x		Tens of Seconds (0-5)
			x x x x	Units Seconds (BCD)
TIME Word 1 - Address 26				
x x x x	x x x x	x x x x	x x x x	MILLISECONDS WORD
x x x x				Milliseconds Hundreds (BCD)
	x x x x			Milliseconds Tens (BCD)
		x x x x		Milliseconds Units (BCD)
			x x x x	Milliseconds Tenths (BCD)

TABLE 3-14. Time-Of-Year Register Formats

TIME DIT ID OF 1FFC			
31	Bit Position		16
Milliseconds		ID	
15	Bit Position		0
Days & Hours		Minutes & Seconds	

TABLE 3-15. 64 Bit Millisecond Time Message

3.6.2 Frame Buffer Header Control Register (Address 28)

The frame buffer message may be preceded by up to seven words of header messages. The header words are shown in **TABLE 3-16** below. The header message is constructed by scanning the header message control register defining the first five header words, and the header control register (Address 2A) that defines the last two header words, while outputting the appropriate word for each position. Up to seven header words may be included in the message prefix. The message is terminated when header word 0 is addressed. Should message 0 be specified for header position one (as selected by bits 0-2 in the header control register) no header message is generated.

Header Word Selection	
Word	Description
7	Header Fixed Word 3
6	Header Fixed Word 2
5	Header Fixed Word 1
4	Record Message
3	Frame Counter
2	Q Word
1	Time Message
0	End of Header

TABLE 3-16. Header Word Numerical Selection

The bit allocations in the Header Control Register are shown in **TABLE 3-17** below.

Header Control Registers	
Bits	Description
15	Not used
14-12	Header Word 5 Control
11-9	Header Word 4 Control
8-6	Header Word 3 Control
5-3	Header Word 2 Control
2-0	Header Word 1 Control

TABLE 3-17. Frame Buffer Header Control Word

Bit 15 is not used

Bits 14-0 of the Header Control Register are broken into five 3-bit fields, each selecting a specific header word. The first field containing a zero will terminate the header message. The messages are scanned from Word 1 through Word 7.

Bits 0-5 of the frame buffer message counter register control the header message words six and seven.

3.6.3 Frame Buffer message Control Register (Address 2A)

This register controls the format of the messages and defines the fifth and sixth words of the header message. The bit allocations in the frame buffer message control register are shown in **TABLE 3-18** below.

Message Control Register		
Bit	**Function**	**Mode**
6	Force Header	Write only
5-3	Header Word 7 Control	Read/Write
2-0	Header Word 6 Control	Read/Write

TABLE 3-18. Frame Buffer Message Control Register

Bit 6 - This bit set to **1** will force a header block to be used in conjunction with the force mode in Register 0.

Bits 5-0 - control the selection of Header Message Words 6 and 7. The messages you can insert are shown in TABLE 3-7. The header message is terminated when a zero message is selected, or at the end of word seven.

3.6.4 Header Fixed Words 1 - 3 (Addresses 2C, 2E, 30)

You write Header Fixed Word 1 through 3 into registers 2C - 30 when fixed words will be included in a header block preceding a DMA or memory mapped frame buffer transfer.

3.7 FILE SYSTEM

We have enabled multiple file recording on the data storage system by creating a simple file system to manage the disk space. This section describes the file system maintained by the firmware on the data storage card.

3.7.1 File System Types

The file system contains up to eight partitions on the system SCSI disks. There are two types of file systems, depending on the SCSI hardware detected. In a **Striped** file system, both SCSI controllers have at least one disk attached. When data is written to a partition, it is striped onto the disks of both controllers. Data buffers are written alternately on the active disk of each controller. For example, the 1st buffer is written to SCSI controller 0, disk 0 (c0d0), the 2nd buffer to c1d0, the third to c0d0, the 4th to c1d0, and so on until the partition boundary is encountered. If the partition spans more than one disk, recording continues on the next disk pair. For example, if the disk pair 0 was filled after writing the Nth buffer, then the N+1 buffer would be written to c0d1, and the N+2 buffer would be written to c1d1. In a **NonStriped** file system only SCSI controller X has disks attached, where X is either 0 or 1. In this file system type, data written is not striped, but rather written to a single disk. The 1st buffer goes to cXd0, as does the second, and this continues until the partition boundary is encountered. If the partition spans more than one disk, then the writing continues on cXd1.

3.7.2 File System Structure

The file system is defined by a **partition table** and **partition headers** which are written on the disks. In a striped file system the partition table and partition headers are mirrored on both disks.

A partition defines a portion of contiguous disk space to which data may be recorded. Any particular archive operation can write data to only 1 partition. When that partition is full, the archive operation will automatically stop so that data on the other partitions will not be corrupted. Each partition may contain only one data file, even if that data file does not use up the entire partition.

When data is recorded, it is written to the disk in chunks of a user definable buffer size. The buffer size is set by the VME host via the DMA Primary and Backup Word Count registers. The RTDS firmware must also be informed of the buffer size by the VME host via a command through the communications port. At the beginning of each buffer is a user definable buffer header which nominally contains a time stamp, although other stamps are also possible. (See the section on the Frame Buffer Header Control Register). This header indexes the buffers allowing the user to, for example, recover data between two specified times. While a partition may span disk pair boundaries, a buffer cannot (this is a hardware limitation). Therefore, each disk pair always contains an integer number of buffers, and space leftover between the last buffer on a given disk pair and the 1st block on the next disk pair is not used.

Several ways are used to refer to a position in the file system. A triplet of numbers is required to completely specify a position in the file system: the controller number; the pair index; and the block number. The controller number specifies which disk array. The pair index specifies which disk in the disk array. The disks in the disk array are numbered by assigning zero to the disk with the lowest SCSI ID, one to the next highest SCSI ID, and so on. The block number specifies the block on that disk. The specification of all three numbers is called a Complete Block address.

To specify a position in a particular disk array (i.e. fixed controller number), two indexing schemes are used. The first scheme numbers the blocks in a particular disk array starting at 0, and the block number increases monotonically transparent to disk boundaries. This scheme of indexing is referred to as Logical Block addressing. The other scheme for indexing a block in a particular disk array is to specify the disk pair index (the disk number in that array), and the block number on that disk. This scheme of indexing is called Physical Block addressing.

3.7.3 File System Example

The diagram on the following page shows a schematic of how a striped file system works. In a non-striped file system, all of the buffers are written to the same disk array. The diagram shows a file system with three partitions. Partition 1 is empty while partitions 0 and 2 each have a data file recorded on them. None of the partitions is full, but only partition 1 is available for recording (without overwriting any data) since the other two partitions already have a data file. Note that the Disk Pair 2 contains no file system information (ie. no partition table, no partition headers). This means that if the disk on controller 0 were accidentally swapped with the disk on controller 1, the RTDS firmware would have no way of identifying the mistake, and any previously recorded data that is recovered from the incorrectly assembled disk pair would be out of order. Therefore care should be taken when disassembling and reassembling the disk arrays if there is data on the disks that needs to be recovered.

Physical Block	Logical Block	Controller 0	Controller 1	
0	0	Partition Table	Partition Table	
1	1	Partition 0 Hdr	Partition 0 Hdr	
2	2	Buffer 0	Buffer 1	
3	3			Disk
4	4	Buffer 2		Pair
5	5			0
6	6	Partition 1 Hdr	Partition 1 Hdr	
7	7			
0	8			
1	9			
2	10			
3	11			Disk
4	12	Partition 2 Hdr	Partition 2 Hdr	Pair
5	13	Buffer 0	Buffer 1	1
6	14			
7	15			
0	16	Buffer 2	Buffer 3	
1	17			
2	18			
3	19			Disk
4	20			Pair
5	21			2
6	22			
7	23			

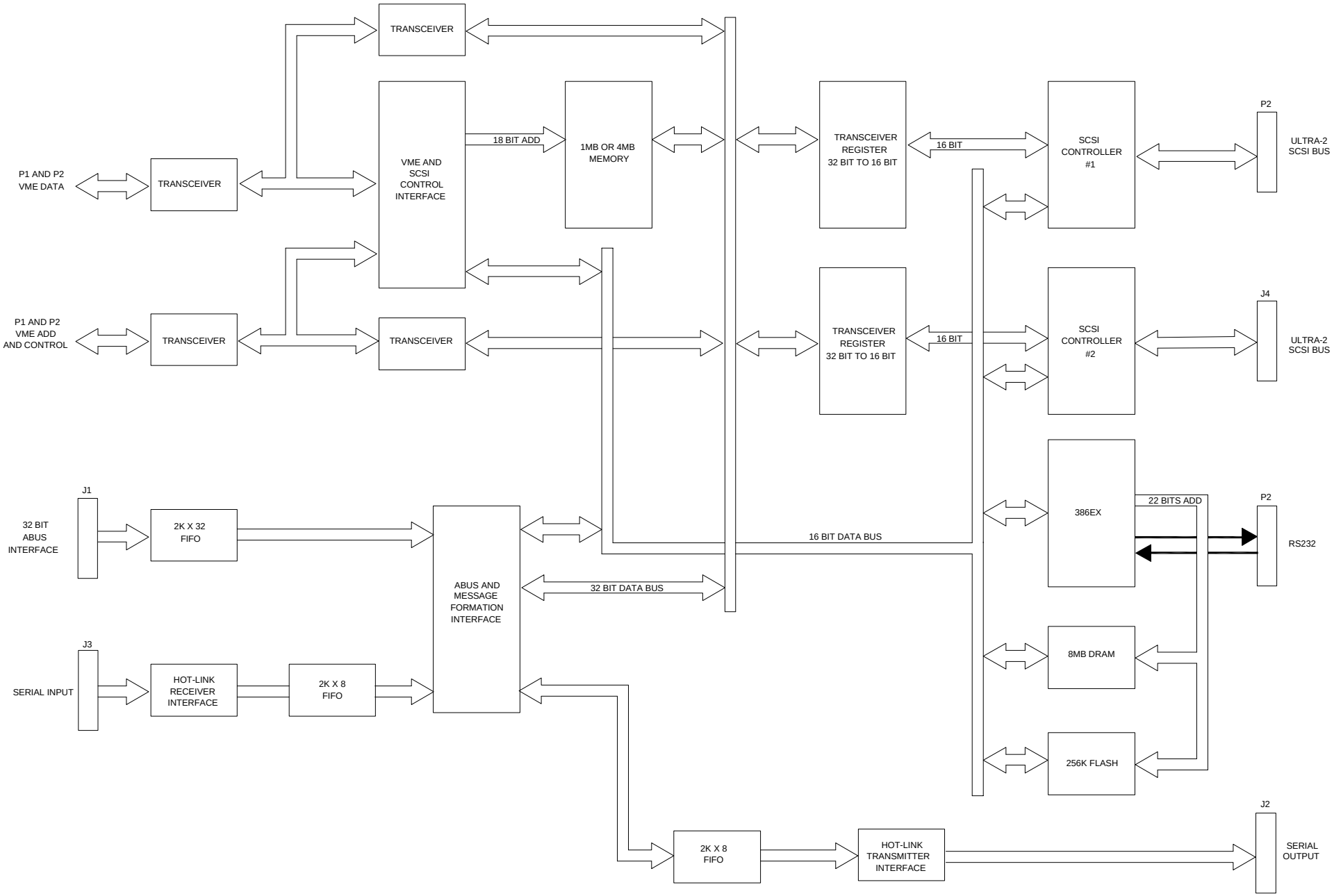
```
Disk Array Formatted 20%, 25%, 55%
NumPartitions = 3
HeaderLogBlocks = {1,6,12}
Partn[0] Buffer Size = 2 Blocks
Partn[1] Buffer Size = 3 Blocks
```

TABLE 3-19. Disk Partitioning Scheme

SECTION 4
THEORY OF OPERATION

4.1 INTRODUCTION

This section contains a block diagram of the 521V-11 RTDS card.



RTDS SIMPLIFIED BLOCK DIAGRAM

DIAG. 7000215 REV. A

SECTION 5
ADJUSTABLE SWITCH & JUMPER SETTINGS

5.1 DESCRIPTION

The paragraphs below describe the selections available on the 521V RTDS card.

5.1.1 Address Select

The switches at U29 and U30 select the base of the 64 byte block of registers in the A16:D16 address space A6 through A15.

5.1.2 JP1 & U21 - DMA Bus Grant & Request

JP1 selects the bus grant level for DMA transfers. The Bus Grant In, Bus Grant Out, and Bus Request (selected by U21) must all be set to the same level. JP1 also selects Bus Grant Passthrough, and you must place the three bus levels not used by the DMA in the Bypass position.

5.1.3 U25 & U30 - Interrupt Request and Acknowledge Level

Switch U25 selects the Interrupt Request level. Switch U30-6, 5, 4 select the Interrupt Acknowledge level. The request and acknowledge levels must match.

5.1.4 JP5 & 7 - SCSI Sense Control

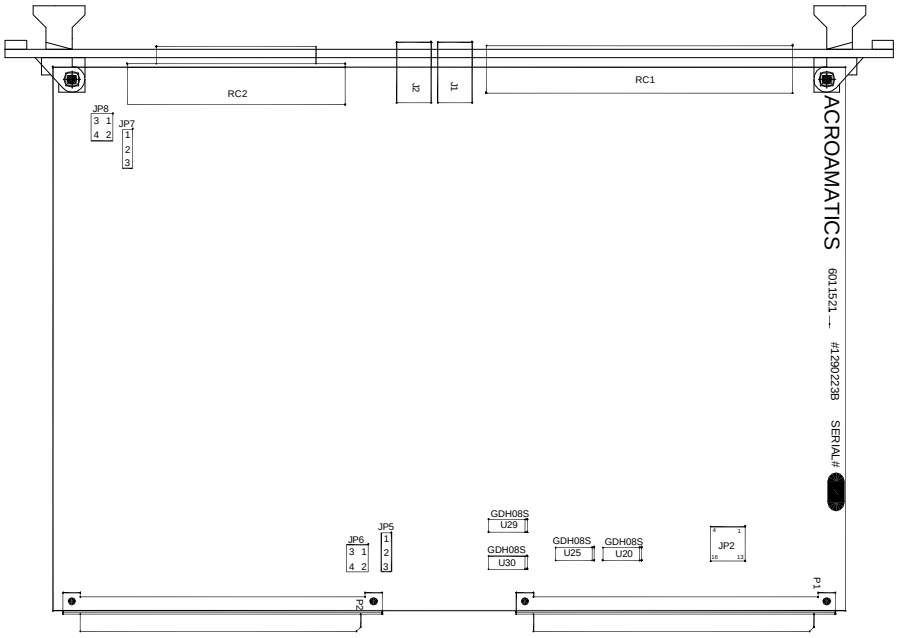
Connect these jumpers from pin 1 to pin 2 for normal operation.

5.1.5 JP 6 & 8 - Terminator Power Selection

These jumpers allow the board to drive the termination power on the SCSI bus and to select which source will drive the on-board terminators.

5.1.6 U30 - Termination Enables

Switches U30-1 & -2 enable the on board terminators for SCSI channels One and Two.

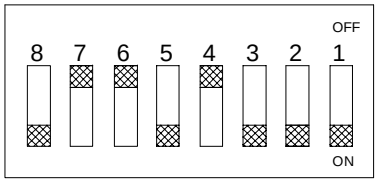


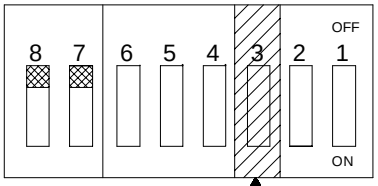
U30 - I/O Address
Interrupt acknowledge selection
SCSI Bus termination

U29 - I/O Address

OFF = 1

ON = 0

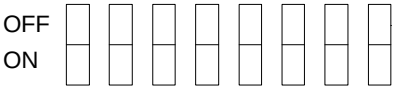


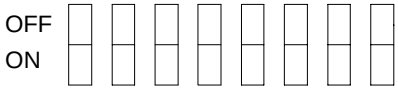


Address 68C0 shown

A15 ◄ ——— A6

NOT USED





U30 Interrupt acknowledge selection and SCSI Bus termination

6	5	4	2	1	Description
off	off	off	x	x	Reserved - Do not use
off	off	on	x	x	Interrupt acknowledge level 1
off	on	off	x	x	Interrupt acknowledge level 2
off	on	on	x	x	Interrupt acknowledge level 3
on	off	off	x	x	Interrupt acknowledge level 4
on	off	on	x	x	Interrupt acknowledge level 5
on	on	off	x	x	Interrupt acknowledge level 6
on	on	off	x	x	Interrupt acknowledge level 7
x	x	x	x	off	SCSI BUS CH. 1 IS TERMINATED ON BOARD
x	x	x	x	on	SCSI BUS CH.1 IS NOT TERMINATED ON BOARD
x	x	x	off	x	SCSI BUS CH.0 IS TERMINATED ON BOARD
x	x	x	on	x	SCSI BUS CH.0 IS NOT TERMINATED ON BOARD

THE VME INTERRUPT REQUEST LEVEL SELECTED
BY U25 MUST MATCH THE INTERRUPT ACKNOWLEDGE
LEVEL SELECTED BY U30

SHIPPED ADDRESS _____

CARD 6011521-10

SERIAL# / REV. _____

_____

CUSTOMER JOB#

_____

CONFIGURED BY DATE

_____

QC CHECK BY DATE

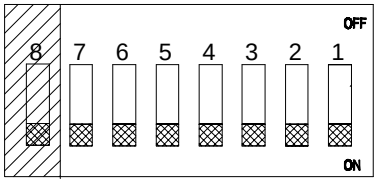
JP2 - VME BUS GRANTS

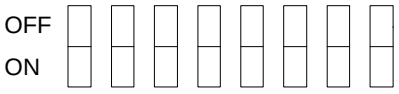
PINS	FUNCTION
1-5	BUS GRANT IN 0 SELECT
2-6	BUS GRANT IN 1 SELECT
3-7	BUS GRANT IN 2 SELECT
4-8	BUS GRANT IN 3 SELECT
9-13	BUS GRANT OUT 0 SELECT
10-14	BUS GRANT OUT 1 SELECT
11-15	BUS GRANT OUT 2 SELECT
12-16	BUS GRANT OUT 3 SELECT
5-9	BYPASS BG IN O TO BG OUT 0
6-10	BYPASS BG IN 1 TO BG OUT 1
7-11	BYPASS BG IN 2 TO BG OUT 2
8-12	BYPASS BG IN 3 TO BG OUT 3
THE THREE UNSELECTED BUS GRANTS MUST BE SET TO 'BYPASS'	

JP2

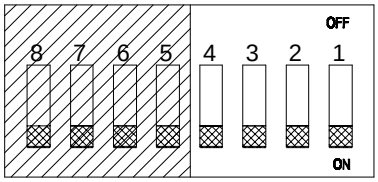
PINS	INSTALLED
1-5	
2-6	
3-7	
4-8	
9-13	
10-14	
11-15	
12-16	
5-9	
6-10	
7-11	
8-12	

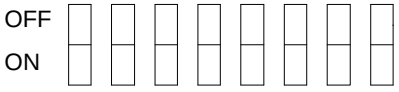
NOT USED





U20 - VME BUS REQUEST
NOT USED





U25 - VME INTERRUPT REQUEST

7	6	5	4	3	2	1	Description
off	off	off	off	off	off	on	INTERRUPT REQUEST LEVEL 1 SELECT
off	off	off	off	off	on	off	INTERRUPT REQUEST LEVEL 2 SELECT
off	off	off	off	on	off	off	INTERRUPT REQUEST LEVEL 3 SELECT
off	off	off	on	off	off	off	INTERRUPT REQUEST LEVEL 4 SELECT
off	off	on	off	off	off	off	INTERRUPT REQUEST LEVEL 5 SELECT
off	on	off	off	off	off	off	INTERRUPT REQUEST LEVEL 6 SELECT
on	off	off	off	off	off	off	INTERRUPT REQUEST LEVEL 7 SELECT

THE VME INTERRUPT REQUEST LEVEL SELECTED
BY U25 MUST MATCH THE INTERRUPT ACKNOWLEDGE
LEVEL SELECTED BY U30

U20 - VME BUS REQUEST

4	3	2	1	Description
off	off	off	on	BUS REQUEST 0 SELECT
off	off	on	off	BUS REQUEST 1 SELECT
off	on	off	off	BUS REQUEST 2 SELECT
on	off	off	off	BUS REQUEST 3 SELECT

JP6 - SCSI CHANNEL 0

PINS	FUNCTION
1-3	BOARD SOURCES PWR TO SCSI BUS
2-4	BOARD SOURCES PWR TO BOARDS TERMINATORS
1-2	SCSI BUS SOURCES PWR TO BOARDS TERMINATORS

JP8 - SCSI CHANNEL 1

PINS	FUNCTION
1-3	BOARD SOURCES PWR TO SCSI BUS
2-4	BOARD SOURCES PWR TO BOARDS TERMINATORS
1-2	SCSI BUS SOURCES PWR TO BOARDS TERMINATORS

JP5 CH.0 TERMINATION POWER SELECT

PINS	FUNCTION
1-2	ON BOARD TERMINATORS SENSE ENABLED
2-3	ON BOARD TERMINATORS SENSE DISABLED

JP7 CH.1 TERMINATION POWER SELECT

PINS	FUNCTION
1-2	ON BOARD TERMINATORS SENSE ENABLED
2-3	ON BOARD TERMINATORS SENSE DISABLED

SECTION 6
DRAWINGS

6.1 INTRODUCTION TO THE DRAWINGS

Section 6 contains a complete technical drawing package describing your VME card. the drawings in this section are keyed to your specific serial numbered card.

6.1.1 Drawing System

Acroamatics Drawing numbers are seven digit numbers which can also have a two digit dash number. The first four digits represent a drawing class, and wherever a drawing may be part of a standard drawing package, drawing numbers are issued so that all drawings which are part of the package share the same last three digits. In the following discussion “xxx” represents the number keyed to the the card part number (6011xxx). Individual parts are classified within the same drawing system, but are assigned serially without regard to other assemblies.

The PC Card Reference package includes the following drawings:

FOR CARD PART NUMBER 60115xx:

60115xx	Card Assembly Drawing
81115xx	Card List of Materials
21115xx	Card Schematic Drawing

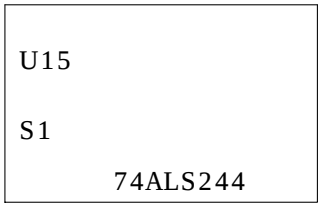
6.1.2 Drawing Package Organization

This section of the manual contains the physical drawings, called *Drawings*, as opposed to the schematic drawings, called *Schematics*, which are found in Section 7.

The Drawings section includes the card component assembly drawing 60115nn and the card List Of Materials (LOM). LOM’s include sufficient information to facilitate ordering replacement parts either from Acroamatics or from the original component manufacturer. LOMs list parts by Acroamatics Part Number in the column headed *PART NO* . The component manufacturer is identified as *VENDOR*. Parts for which ACROAMATICS is listed as vendor are proprietary components available only from Acroamatics, Inc. Integrated Circuits which are industry standard are listed as GENERIC, and may be obtained from any reliable vendor. Other parts for which a specific source is listed may be available from other sources. When substituting parts from vendors other than those specifically listed, be certain that the components are truly interchangeable.

The last column (Reference) of the List of Materials lists the assembly location or locations. An assembly location can contain a socket as well as the component plugged into the socket.

For example



This example shows that location U15 contains socket S1 and an IC of type 74ALS244. Resistors, capacitors, and other components are shown in a similar fashion, and are referenced using common industry abbreviations.

6.1.3 Programmed Parts

The VME card can include programmed parts such as PROMs, EPROMs, EEPROMs, PALs, GALs, FPGAs, etc. If these are a permanent part of the hardware, they are documented on the List Of Materials for the PC card on which they are installed. Programmed parts are listed on the LOM twice; once as the unprogrammed part, with the Manufacturers Part Number, and also under the Acroamatics program number (606xxxx) with which they must be programmed to become the correct programmed part.

Programs for PROMs have part numbers in the series 6061xxx
Programs for EPROMs and EEPROMs have part numbers in the series 6062xxx
Programs for PALws and GALs have part numbers in the series 6064xxx
Programs for FPGAs have part numbers in the series 6067xxx

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASED SEE ECR 4540		BL		5/00
B	SEE ECR 4652		BL		8/00
C	SEE ECR 4672		BL		10/00
D	SEE ECR 4734		BL		5/01
E	SEE ECR 4738		BL		6/01
F	SEE ECR 4741		BL		6/01
G	SEE ECR 4771		BL		1/02
H	SEE ECR 4799		BL		2/02

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X	X	X	X	X	X																		

LIST OF MATERIALS 8111521-10

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	1																								

PC CARD 1290223

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X	X	X																					

SCHEMATICS 2111521-10

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

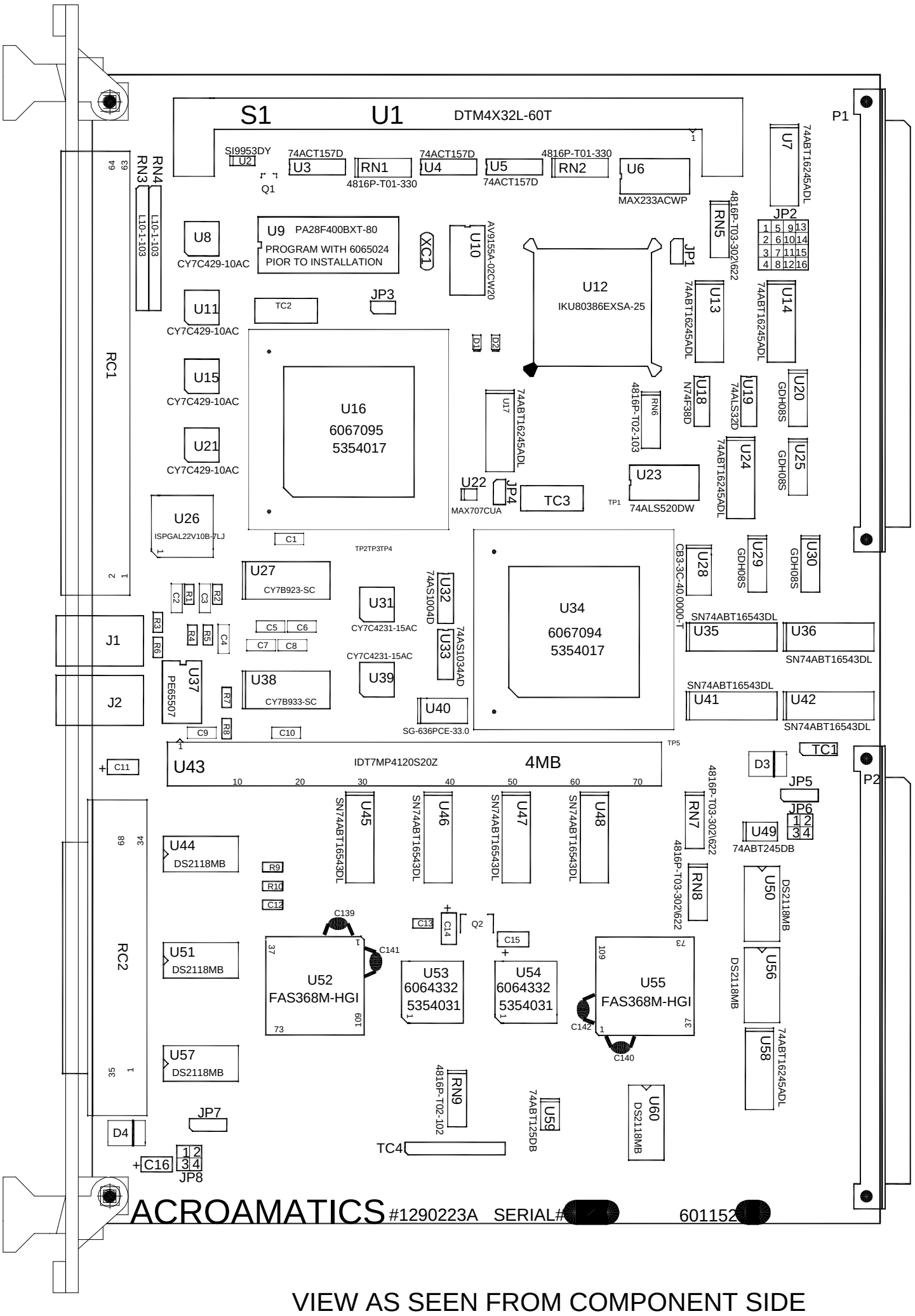
DR	B. GALAZIOS	2/02
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME REAL TIME DATA STORAGE 4MB

SIZE	SCALE	DWG NO.
B	NTS	6011521-10
SHEET 1 OF 3		REV H



VIEW AS SEEN FROM COMPONENT SIDE

NOTE:
1) SOLDER CAPACITOR C139 ON THE PINS 2 AND 5 OF LOCATION U52
2) SOLDER CAPACITOR C140 ON THE PINS 2 AND 5 OF LOCATION U55
3) SOLDER CAPACITOR C141 ON THE PINS 139 AND 141 OF LOCATION U52
4) SOLDER CAPACITOR C142 ON THE PINS 139 AND 141 OF LOCATION U55

DR	B. GALAZIOS	2/02
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

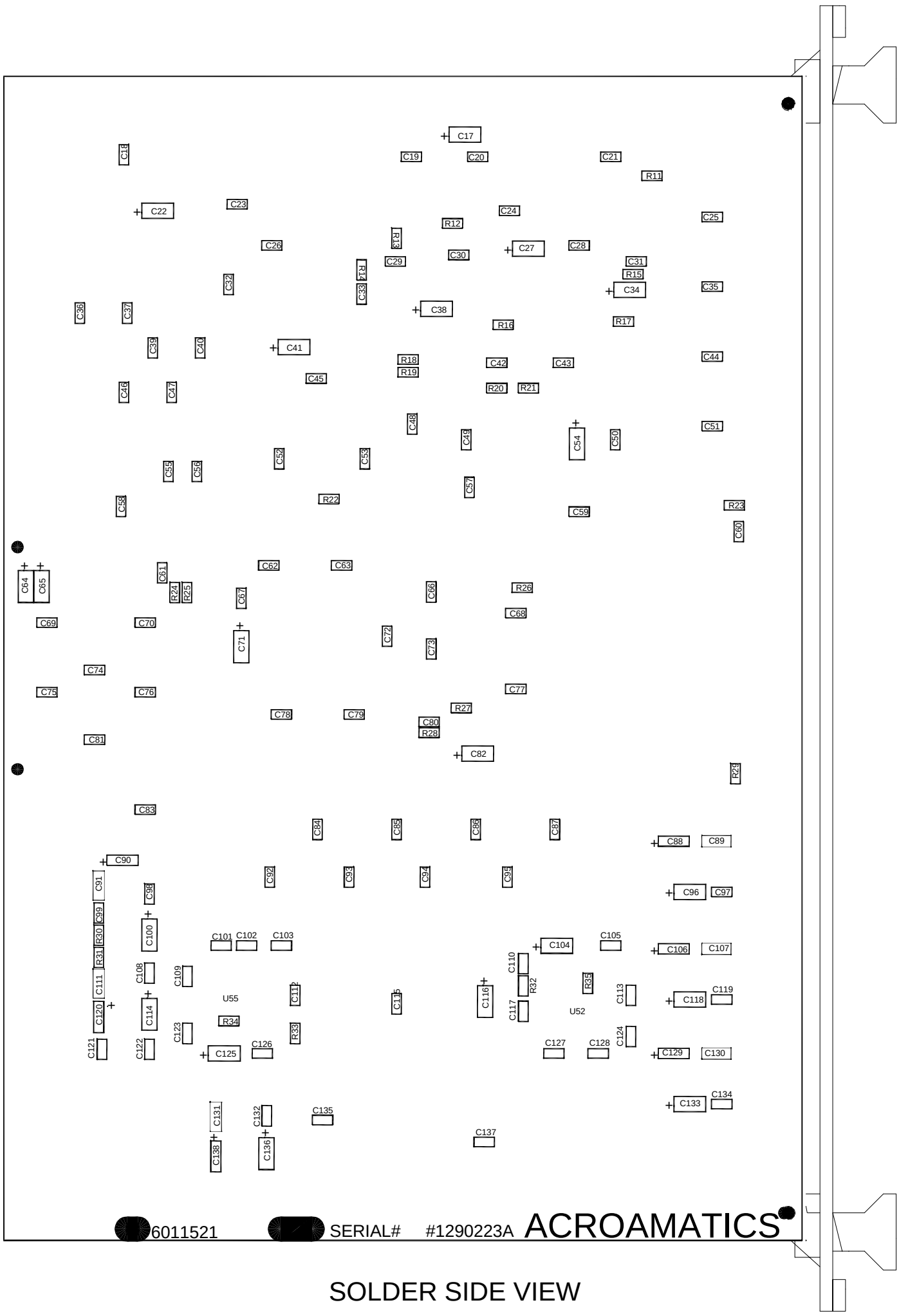
ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME REAL TIME DATA STORAGE 4MB

SIZE	SCALE	DWG NO.	REV
B	NTS	6011521-10	H

SHEET 2 OF 3



6011521 SERIAL# #1290223A ACROAMATICS

SOLDER SIDE VIEW

DR	B. GALAZIOS	2/02
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME REAL TIME DATA STORAGE 4MB

SIZE	SCALE	DWG NO.	REV
B	NTS	6011521-10	H

SHEET 3 OF 3

LIST OF MATERIALS 8111521-10 PAGE 1 OF 3
VME RT DATA STORAGE 4MB

ASSEMBLY PN 6011521-10 DRAWN BY Bryan Jul 8 16:57

REVISION H ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290223	1	PCB REAL TIME DATA STORAGE	1290223	ACROAMATICS	
2	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1,P2
3	2796060	1	CONN PC 64P SDR RTANGL	2564-5002UB	3M	RC1
4	2796106	1	CONN PC 68P .05 SUB-D RTANGL	787082-7	AMP	RC2
5	2796104	2	CONN PC 7PIN 1.25 HEADER SMT	53398-0790	MOLEX	TC2,TC3
6	2796128	2	CONN PC 6P 1394 RTNGL UPRIGHT	53460-0611	MOLEX	J1,J2
7						
8	8542094	1	SOCKET RGHT ANGLE 72 PIN SIMM	7-382486-2	AMP	S1
9						
10	1904018	4	CAP NPO 39pF	5018E050RD390J	KYOCERA	C139,C140,C141,C142
11	1903069	91	CAP X7R .1uF 5% 50V SMT-805	C0805C104J5RAC	KEMET	C12,C13,C18-C21,C23-C26,C28-C33
11						C35-C37,C39,C40,C42-C53,C55-C63
11						C66-C70,C72-C79,C81,C83-C87,C92-C95
11						C97-C99,C101-C103,C105,C108-C110
11						C112,C113,C115,C117,C119,C121-C124
11						C126-C128,C132,C134,C135,C137
12	1903063	6	CAP TMP STBL (X7R) .022uF SMT	ECU-V1H223KBM	PANASONIC	C1,C5-C8,C10
13	1903064	7	CAP TMP STBL (X7R) .01uF SMT	ECU-V1H103KBM	PANASONIC	C4,C89,C91,C107,C111,C130,C131
14	1904101	2	CAP NPO 1000pF 50V SMT 1206	ECU-V1H102JCH	PANASONIC	C2,C3
15	1904103	1	CAP NPO 39pF 5% 50V SMT	ECU-V1H390JCG	PANASONIC	C80
16	1922656	24	CAP TA 10uF 10% 20V SMT	T491B106K020AS	KEMET	C11,C14-C17,C22,C27,C34,C38,C41,C54
16			Acceptable substitute is:	ECS-T1DX106R	PANASONIC	
16						C64,C65,C71,C82,C96,C100,C104,C114
16						C116,C118,C125,C133,C136
17	1922646	6	CAP TA 2.2uF 10% 16V SMT	T491A225K016AS	KEMET	C88,C90,C106,C120,C129,C138
18	7680968	2	RES 49.9 OHM .1W 1% SMT-0805	ERJ-6ENF49.9	PANASONIC	R32,R33
19	7680971	2	RES 200K .1W 1% SMT-0805	ERJ-6ENF200K	PANASONIC	R9,R31
20	7680973	2	RES 18.7K .1W 1% SMT-0805	ERJ-6ENF18.7K	PANASONIC	R10,R30
21	7680980	9	RES 33.2 OHM .1W 1% SMT-0805	ERJ-6ENF33.2	PANASONIC	R12-R14,R20,R21,R23-R26
22	7680981	5	RES 10K .1W 1% SMT-0805	ERJ-6ENF10.0K	PANASONIC	R16,R17,R22,R27,R29
23	7680983	2	RES 100K .1W 1% SMT-0805	ERJ-6ENF100K	PANASONIC	R11,R15
24	7680988	4	RES 267 OHM .1W 1% SMT-0805	ERJ-6ENF267	PANASONIC	R1,R2,R18,R19
25	7680912	2	RES 75 OHM .1W 1% SMT-0805	ERJ-6ENF75	PANASONIC	R7,R8
26	7680922	2	RES 3.01K .1W 1% SMT-0805	ERJ-6ENF3.01K	PANASONIC	R34,R35
27	7680986	1	RES 681 OHM .1W 1% SMT-0805	ERJ-6ENF681	PANASONIC	R5
28	7680987	1	RES 1.5K .1W 1% SMT-0805	ERJ-6ENF1501	PANASONIC	R4
29	7680999	3	RES 0 OHM .1W SMT-0805	ERJ-6GEY0R00	PANASONIC	R3,R6,R28
30	7690103	1	RES DIP 10K OHM 15R 16P SMT	4816P-T02-103	BOURNS	RN6
31	7690104	3	RES DIP 3K/6.2K 16 PIN SMT	4816P-T03-302622	BOURNS	RN5,RN7,RN8
32	7690107	1	RES DIP 1K OHM 15R 16P SMT	4816P-T02-102	BOURNS	RN9
33	7690106	2	RES DIP 33 OHM 8R 16P SMT	4816P-T01-330	BOURNS	RN1,RN2
34	7700026	2	RES SIP 10K 9RES 10-PIN	L10-1-103	BECKMAN	RN3,RN4
35						
36	3570032	1	LED RED SMT 0603	LNJ208R8ARA	PANASONIC	D2
37	3570033	1	LED GRN SMT 0603	LNJ308R8LRA	PANASONIC	D1

VME RT DATA STORAGE 4MB

ASSEMBLY PN 6011521-10 DRAWN BY Bryan Jul 8 16:57

REVISION H

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
38	3573002	2	DIODE SCHOTTKY SWITCH 3A SMT	B320	LITEON	D3,D4
39	3070025	1	CRYSTAL 14.318MHZ	ECS-143-S-4	ECS	XC1
39			Acceptable substitute is:	ATS143	CTS	
40						
41	5300004-42	1	IC HEX INVERTER (SMD)	74AS1004D	GENERIC	U32
42	5300032-39	1	IC QUAD 2-INP OR GATE SMT	74ALS32D	GENERIC	U19
43	5300034-37	1	IC HEX DRIVER +-48ma SMT	74AS1034AD	GENERIC	U33
44	5300038-39	1	IC QUAD 2-INP NAND BUFF(SMD)	N74F38D	GENERIC	U18
45	5300125-49	1	IC QUAD BUF NI INDEP-TS SMT	74ABT125DB	GENERIC	U59
46	5300157-63	3	IC QUAD 2-TO-1 DATA SEL/MUX	74ACT157D	GENERIC	U3,U4,U5
47	5300245-55	6	IC 16BIT BUS XCVR SMT NI TS	74ABT16245ADL	GENERIC	U7,U13,U14,U17,U24,U58
48	5300245-91	1	IC OCT BUS XCVR NI TS SMT	74ABT245DB	GENERIC	U49
49	5300520-32	1	IC 8-BIT MAG COMP SMT	74ALS520DW	GENERIC	U23
50	5300543-55	8	IC 16 BIT REGISTERED XCVR	SN74ABT16543DL	TI	U35,U36,U41,U42,U45-U48
51	5302155	1	IC FREQUENCY GENERATOR	AV9155A-02CW20	ICS	U10
52	5302233-01	1	IC DUAL RS-232 XMTR/RCVR SMT	MAX233ACWP	MAXIM	U6
52			Acceptable substitute is:	SP233ACT/SP233AET	SIPEX	
53	5302707	1	IC POWER UP RESET	MAX707CUA	MAXIM	U22
54	5308003	1	IC 160-330MBPS SERIAL XMIT	CY7B923-SC	CYPRESS	U27
55	5308004	1	IC 160-330MBPS SERIAL RCVR	CY7B933-SC	CYPRESS	U38
56	5308005	6	IC LVD/SE SCSI TERM RESISTOR	DS2118MB	DALLAS	U44,U50,U51,U56,U57,U60
57						
58	5308429-10	4	IC 2Kx9-BIT FIFO (QFP)	CY7C429-10AC	CYPRESS	U8,U11,U15,U21
59	5308423-15	2	IC 2Kx9 SYNCHRONOUS FIFO SMT	CY7C4231-15AC	CYPRESS	U31,U39
59			Acceptable substitute is:	IDT72231L15PF	IDT	
60	5352400-80	1	IC 256KX16 FLASH 80ns	PA28F400BXT-80	INTEL	U9,Program with 6065024 prior
60			Acceptable substitute is:	MT28F400B5SG-8	MICRON	
60						to installation. Program with
60						6068003 after installation.
61	5353031	3	IC (ISP) GAL 22V10 7ns PLCC	ISPGAL22V10B-7LJ	LATTICE	U26,U53,U54, Program after
61						installation
62	5354017	2	FPGA 24000 M-GATE PQFP	A42MX24-PQ208C	ACTEL	unprogrammed FPGA
63	6031096	1	ZIP SRAM 1MX32 20ns	IDT7MP4120S20Z	IDT	U43
64	6031123	1	SIMM DRAM 16MB 4MX32 60ns	DTM4x32L-60T	MEMORY4LESS	U1
65	6064332	2	VME RDSD PARITY GENERATOR	5353031-REV.A	ACROAMATICS	U53,U54 ITEM #61
66	6064333	1	VME RDSD ABUS CONTROL	5353031-REV.B	ACROAMATICS	U26 ITEM #61
67	6067094	1	VME RTDS INTERFACE	5354017-REV.C	ACROAMATICS	U34,RTDS7094 ITEM #62
68	6067095	1	VME RTDS ABUS CONTROL	5354017-REV.D	ACROAMATICS	U16,RTDS7095 ITEM #62
69	6068003	1	VME RTDS FLASH	5352400-V1.1	ACROAMATICS	U10,ITEM #60
70	6350064	1	OSCIL. XTAL 40.000MHZ SMT	CB3-3C-40.0000-T	CTS	U28
71	6350055	1	OSCIL. XTAL 33.000MHZ SMT	SG-636PCE-33.000MC	EPSON	U40
72	9543006	1	XFMR DUAL FIBRE CHNL 266MHZ	PE65507	PULSE	U37
73	9581023	1	TRANSISTOR DUAL P-CHNL MOSFET	SI9953DY	SILICONIX	U2
74	9581024	1	TRANSISTOR N-CHNL MOSFET	2N7002LT1	MOTOROLA	Q1
75						
76	6128386-25	1	IC 386 EMBEDDED PROCESSOR	IKU80386EXSA-25	INTEL	U12
76			Acceptable substitute is:	IKU80386EXTA-25	INTEL	

VME RT DATA STORAGE 4MB

ASSEMBLY PN 6011521-10 DRAWN BY Bryan Jul 8 16:57

REVISION H

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
76			Acceptable substitute is:	IKU80386EXTC-25	INTEL	
77	6129015	2	IC LVD/SE SCSI CONTROLLER SMT	FAS368M-HGI	QLOGIC	U52,U55
78	7580039	1	REGULATOR +3.3V 700ma	LT1129CST-3.3	LINEAR	Q2
78			Acceptable substitute is:	LM3940IMP-3.3	NATIONAL	
79	9070015	4	DIP SWITCH 8-POS SLIDE SMT	GDH08S	AUGAT	U20,U25,U29,U30
80	5470011	1	JUMPER PINS SINGLE ROW 50POS	MTSW-150-07-G-S-24	SAMTEC	TC1(1x3pins),TC4(1x8pins)
80						JP1(1x2pins),JP3(1x2pins)
80						JP4(1x2pins),JP5(1x3pins)
80						JP7(1x3pins)
81	5470012	1	JUMPER PINS DOUBLE ROW 50POS	MTSW-150-07-G-D-24	SAMTEC	JP2(4x4pins),JP6(2x2pins)
81						JP8(2x2pins)
82						
83						
84	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
85	5600039	1	LABEL,VME PNL, RTDS	5600039	ACROAMATICS	
86	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCR #8071214, MOD #5951142

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASED SEE ECR 4540		BL		5/00
B	SEE ECR 4652		BL		8/00
C	SEE ECR 4672		BL		10/00
D	SEE ECR 4734		BL		5/01
E	SEE ECR 4738		BL		6/01
F	SEE ECR 4741		BL		6/01
G	SEE ECR 4771		BL		1/02
H	SEE ECR 4799		BL		2/02

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X	X	X	X	X	X																		

LIST OF MATERIALS 8111521-11

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	1																								

PC CARD 1290223

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X	X	X																					

SCHEMATICS 2111521-11

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

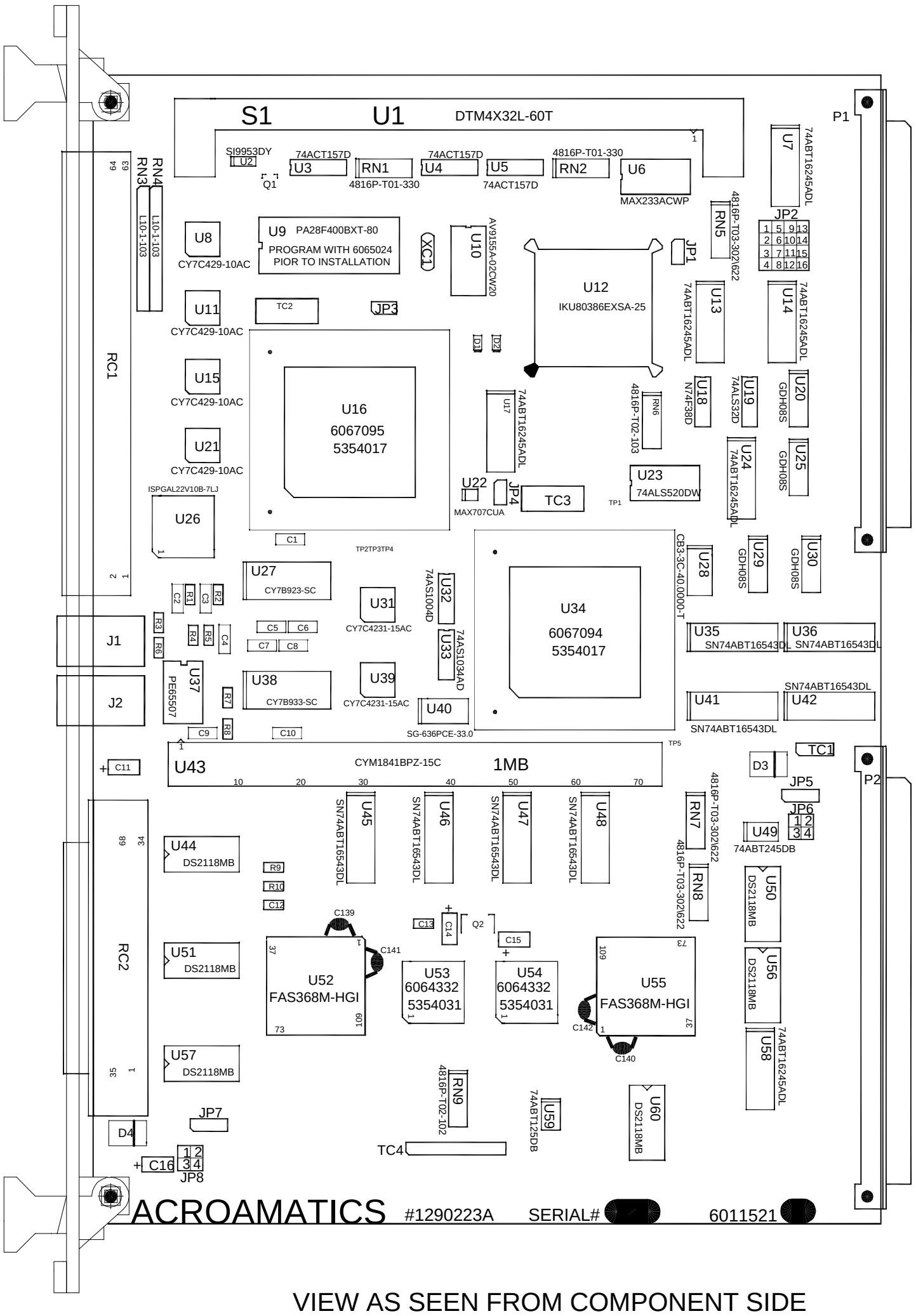
DR	B. GALAZIOS	2/02
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME REAL TIME DATA STORAGE 1MB

SIZE	SCALE	DWG NO.
B	NTS	6011521-11
SHEET 1 OF 3		REV H



VIEW AS SEEN FROM COMPONENT SIDE

NOTE: 1) SOLDER CAPACITOR C139 ON THE PINS 2 AND 5 OF LOCATION U52
2) SOLDER CAPACITOR C140 ON THE PINS 2 AND 5 OF LOCATION U55
3) SOLDER CAPACITOR C141 ON THE PINS 139 AND 141 OF LOCATION U52
4) SOLDER CAPACITOR C142 ON THE PINS 139 AND 141 OF LOCATION U55

DR	B. GALAZIOS	2/02
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

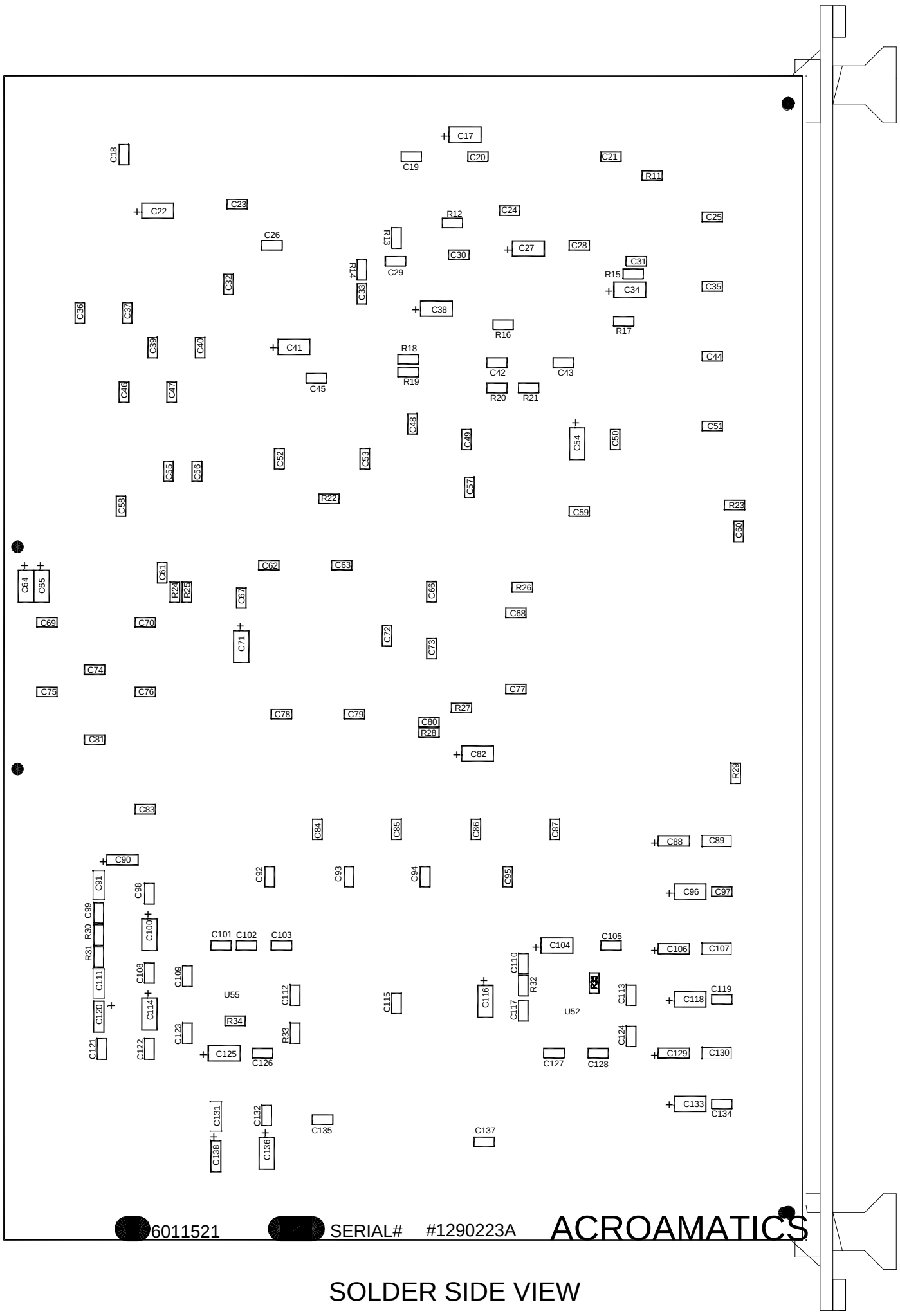
ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME REAL TIME DATA STORAGE 1MB

SIZE	SCALE	DWG NO.	REV
B	NTS	6011521-11	H

SHEET 2 OF 3



6011521 SERIAL# #1290223A ACROAMATICS

SOLDER SIDE VIEW

DR	B. GALAZIOS	2/02
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME REAL TIME DATA STORAGE 1MB

SIZE	SCALE	DWG NO.	REV
B	NTS	6011521-11	H

SHEET 3 OF 3

VME RT DATA STORAGE 1MB

ASSEMBLY PN 6011521-11 DRAWN BY Bryan Feb 20 09:21

REVISION H ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290223	1	PCB REAL TIME DATA STORAGE	1290223	ACROAMATICS	
2	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1,P2
3	2796060	1	CONN PC 64P SDR RTANGL	2564-5002UB	3M	RC1
4	2796106	1	CONN PC 68P .05 SUB-D RTANGL	787082-7	AMP	RC2
5	2796104	2	CONN PC 7PIN 1.25 HEADER SMT	53398-0790	MOLEX	TC2,TC3
6	2796128	2	CONN PC 6P 1394 RTNGL UPRIGHT	53460-0611	MOLEX	J1,J2
7						
8	8542094	1	SOCKET RGHT ANGLE 72 PIN SIMM	7-382486-2	AMP	S1
9						
10	1904018	4	CAP NPO 39pF	5018E050RD390J	KYOCERA	C139,C140,C141,C142
11	1903069	91	CAP X7R .1uF 5% 50V SMT-805	C0805C104J5RAC	KEMET	C12,C13,C18-C21,C23-C26,C28-C33
11						C35-C37,C39,C40,C42-C53,C55-C63
11						C66-C70,C72-C79,C81,C83-C87,C92-C95
11						C97-C99,C101-C103,C105,C108-C110
11						C112,C113,C115,C117,C119,C121-C124
11						C126-C128,C132,C134,C135,C137
12	1903063	6	CAP TMP STBL (X7R) .022uF SMT	ECU-V1H223KBM	PANASONIC	C1,C5-C8,C10
13	1903064	7	CAP TMP STBL (X7R) .01uF SMT	ECU-V1H103KBM	PANASONIC	C4,C89,C91,C107,C111,C130,C131
14	1904101	2	CAP NPO 1000pF 50V SMT 1206	ECU-V1H102JCH	PANASONIC	C2,C3
15	1904103	1	CAP NPO 39pF 5% 50V SMT	ECU-V1H390JCG	PANASONIC	C80
16	1922656	24	CAP TA 10uF 10% 20V SMT	T491B106K020AS	KEMET	C11,C14-C17,C22,C27,C34,C38,C41,C54
16			Acceptable substitute is:	ECS-T1DX106R	PANASONIC	
16						C64,C65,C71,C82,C96,C100,C104,C114
16						C116,C118,C125,C133,C136
17	1922646	6	CAP TA 2.2uF 10% 16V SMT	T491A225K016AS	KEMET	C88,C90,C106,C120,C129,C138
18	7680968	2	RES 49.9 OHM .1W 1% SMT-0805	ERJ-6ENF49.9	PANASONIC	R32,R33
19	7680971	2	RES 200K .1W 1% SMT-0805	ERJ-6ENF200K	PANASONIC	R9,R31
20	7680973	2	RES 18.7K .1W 1% SMT-0805	ERJ-6ENF18.7K	PANASONIC	R10,R30
21	7680980	9	RES 33.2 OHM .1W 1% SMT-0805	ERJ-6ENF33.2	PANASONIC	R12-R14,R20,R21,R23-R26
22	7680981	5	RES 10K .1W 1% SMT-0805	ERJ-6ENF10.0K	PANASONIC	R16,R17,R22,R27,R29
23	7680983	2	RES 100K .1W 1% SMT-0805	ERJ-6ENF100K	PANASONIC	R11,R15
24	7680988	4	RES 267 OHM .1W 1% SMT-0805	ERJ-6ENF267	PANASONIC	R1,R2,R18,R19
25	7680912	2	RES 75 OHM .1W 1% SMT-0805	ERJ-6ENF75	PANASONIC	R7,R8
26	7680922	2	RES 3.01K .1W 1% SMT-0805	ERJ-6ENF3.01K	PANASONIC	R34,R35
27	7680986	1	RES 681 OHM .1W 1% SMT-0805	ERJ-6ENF681	PANASONIC	R5
28	7680987	1	RES 1.5K .1W 1% SMT-0805	ERJ-6ENF1501	PANASONIC	R4
29	7680999	3	RES 0 OHM .1W SMT-0805	ERJ-6GEY0R00	PANASONIC	R3,R6,R28
30	7690103	1	RES DIP 10K OHM 15R 16P SMT	4816P-T02-103	BOURNS	RN6
31	7690104	3	RES DIP 3K/6.2K 16 PIN SMT	4816P-T03-302622	BOURNS	RN5,RN7,RN8
32	7690107	1	RES DIP 1K OHM 15R 16P SMT	4816P-T02-102	BOURNS	RN9
33	7690106	2	RES DIP 33 OHM 8R 16P SMT	4816P-T01-330	BOURNS	RN1,RN2
34	7700026	2	RES SIP 10K 9RES 10-PIN	L10-1-103	BECKMAN	RN3,RN4
35						
36	3570032	1	LED RED SMT 1.6 x 1.1mm	LNJ208R8ARA	Generic	D2
37	3570033	1	LED GRN SMT 1.6 x 1.1mm	LNJ308R8LRA	Generic	D1

VME RT DATA STORAGE 1MB

ASSEMBLY PN 6011521-11 DRAWN BY Bryan Feb 20 09:21

REVISION H

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
38	3573002	2	DIODE SCHOTTKY SWITCH 3A SMT	B320	LITEON	D3,D4
39	3070025	1	CRYSTAL 14.318MHZ	ECS-143-S-4	ECS	XC1
39			Acceptable substitute is:	ATS143	CTS	
40						
41	5300004-42	1	IC HEX INVERTER (SMD)	74AS1004D	GENERIC	U32
42	5300032-39	1	IC QUAD 2-INP OR GATE SMT	74ALS32D	GENERIC	U19
43	5300034-37	1	IC HEX DRIVER +-48ma SMT	74AS1034AD	GENERIC	U33
44	5300038-39	1	IC QUAD 2-INP NAND BUFF(SMD)	N74F38D	GENERIC	U18
45	5300125-49	1	IC QUAD BUF NI INDEP-TS SMT	74ABT125DB	GENERIC	U59
46	5300157-63	3	IC QUAD 2-TO-1 DATA SEL/MUX	74ACT157D	GENERIC	U3,U4,U5
47	5300245-55	6	IC 16BIT BUS XCVR SMT NI TS	74ABT16245ADL	GENERIC	U7,U13,U14,U17,U24,U58
48	5300245-91	1	IC OCT BUS XCVR NI TS SMT	74ABT245DB	GENERIC	U49
49	5300520-32	1	IC 8-BIT MAG COMP SMT	74ALS520DW	GENERIC	U23
50	5300543-55	8	IC 16 BIT REGISTERED XCVR	SN74ABT16543DL	TI	U35,U36,U41,U42,U45-U48
51	5302155	1	IC FREQUENCY GENERATOR	AV9155A-02CW20	ICS	U10
52	5302233-01	1	IC DUAL RS-232 XMTR/RCVR SMT	MAX233ACWP	MAXIM	U6
52			Acceptable substitute is:	SP233ACT/SP233AET	SIPEX	
53	5302707	1	IC POWER UP RESET	MAX707CUA	MAXIM	U22
54	5308003	1	IC 160-330MBPS SERIAL XMIT	CY7B923-SC	CYPRESS	U27
55	5308004	1	IC 160-330MBPS SERIAL RCVR	CY7B933-SC	CYPRESS	U38
56	5308005	6	IC LVD/SE SCSI TERM RESISTOR	DS2118MB	DALLAS	U44,U50,U51,U56,U57,U60
57						
58	5308429-10	4	IC 2Kx9-BIT FIFO (QFP)	CY7C429-10AC	CYPRESS	U8,U11,U15,U21
59	5308423-15	2	IC 2Kx9 SYNCHRONOUS FIFO SMT	CY7C4231-15AC	CYPRESS	U31,U39
59			Acceptable substitute is:	IDT72231L15PF	IDT	
60	5352400-80	1	IC 256KX16 FLASH 80ns	PA28F400BXT-80	INTEL	U9,Program with 6065024 prior
60						to installation. Program with
60						6068003 after installation.
61	5353031	3	IC (ISP) GAL 22V10 7ns PLCC	ISPGAL22V10B-7LJ	LATTICE	U26,U53,U54, Program after
61						installation
62	5354017	2	FPGA 24000 M-GATE PQFP	A42MX24-PQ208C	ACTEL	unprogrammed FPGA
63	6031116	1	ZIP SRAM 256KX32 15ns	CYM1841BPZ-15C	CYPRESS	U43
63			Acceptable substitute is:	IDT7MP4045S15Z	IDT	
63			Acceptable substitute is:	CYM1841APZ-15C	CYPRESS	
63			Acceptable substitute is:	MCM32257Z15	MOTOROLA	
64	6031123	1	SIMM DRAM 16MB 4MX32 60ns	DTM4x32L-60T	MEMORY4LESS	U1
65	6064332	2	VME RDSD PARITY GENERATOR	5353031-REV.A	ACROAMATICS	U53,U54 ITEM #61
66	6064333	1	VME RDSD ABUS CONTROL	5353031-REV.B	ACROAMATICS	U26 ITEM #61
67	6067094	1	VME RTDS INTERFACE	5354017-REV.C	ACROAMATICS	U34,RTDS7094 ITEM #62
68	6067095	1	VME RTDS ABUS CONTROL	5354017-REV.D	ACROAMATICS	U16,RTDS7095 ITEM #62
69	6068003	1	VME RTDS FLASH	5352400-80-REV.A	ACROAMATICS	U10,ITEM #60
70	6350064	1	OSCIL. XTAL 40.000MHZ SMT	CB3-3C-40.0000-T	CTS	U28
71	6350055	1	OSCIL. XTAL 33.000MHZ SMT	SG-636PCE-33.000MC	EPSON	U40
72	9543006	1	XFMR DUAL FIBRE CHNL 266MHZ	PE65507	PULSE	U37
73	9581023	1	TRANSISTOR DUAL P-CHNL MOSFET	SI9953DY	SILICONIX	U2
74	9581024	1	TRANSISTOR N-CHNL MOSFET	2N7002LT1	MOTOROLA	Q1
75						

VME RT DATA STORAGE 1MB

ASSEMBLY PN 6011521-11 DRAWN BY Bryan Feb 20 09:21

REVISION H

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
76	6128386-25	1	IC 386 EMBEDDED PROCESSOR	IKU80386EXSA-25	INTEL	U12
76			Acceptable substitute is:	IKU80386EXTA-25	INTEL	
76			Acceptable substitute is:	IKU80386EXTC-25	INTEL	
77	6129015	2	IC LVD/SE SCSI CONTROLLER SMT	FAS368M-HGI	QLOGIC	U52,U55
78	7580039	1	REGULATOR +3.3V 700ma	LT1129CST-3.3	LINEAR	Q2
78			Acceptable substitute is:	LM3940IMP-3.3	NATIONAL	
79	9070015	4	DIP SWITCH 8-POS SLIDE SMT	GDH08S	AUGAT	U20,U25,U29,U30
80	5470011	1	JUMPER PINS SINGLE ROW 50POS	MTSW-150-07-G-S-24	SAMTEC	TC1(1x3pins),TC4(1x8pins)
80						JP1(1x2pins),JP3(1x2pins)
80						JP4(1x2pins),JP5(1x3pins)
80						JP7(1x3pins)
81	5470012	1	JUMPER PINS DOUBLE ROW 50POS	MTSW-150-07-G-D-24	SAMTEC	JP2(4x4pins),JP6(2x2pins)
81						JP8(2x2pins)
82						
83						
84	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
85	5600039	1	LABEL,VME PNL, RTDS	5600039	ACROAMATICS	
86	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCR #8071214, MOD #5951142