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JFET-based dc/dc converter operates from 300-mV supply

Jim Williams, Linear Technology Corp, Milpitas, CA

You use a JFET's self-biasing characteristics to build a dc/dc converter that operates from power sources such as solar cells, thermopiles, and single-stage fuel cells, all of which deliver less than 600 mV and sometimes as little as 300 mV. Figure 1 shows the drain-to-source characteristics of an N-channel JFET under zero-bias conditions, which you can produce by connecting its gate and source together. Applying 100 mV causes a current of 10 mA to flow through the device, increasing to 30 mA at 350 mV. Exploiting the JFET's ability to conduct significant current at zero bias makes it possible to design a self-starting, low-input-voltage converter.

The circuit can supply 5V at currents as large as 2 mA—enough to serve many micropowered applications or to provide auxiliary bias for a higher power switched-mode voltage regulator. At 300-mV input, the circuit starts up at load currents of 300 µA. A load current of 2 mA requires an input of 475 mV.

In Figure 2, Q_1, a parallel-connected pair of Philips Semiconductor's (www.semiconductors.philips.com) BF862 JFETs, and Coiltronics' (www.coiltronics.com) Versa-Pac transformer, T_1, form an oscillator in which T_1's secondary winding provides feedback to Q_1's gate. When you first apply power, Q_1's gate rests at 0V, and drain current flows through T_1's primary winding. T_1's phase-inverted secondary winding responds by delivering a negative voltage to Q_1's gate, which turns off Q_1 and interrupts current flow through T_1's primary winding. In turn, T_1's secondary voltage collapses, and sustained oscillations begin. Although the BF862's published specifications do not cover the device's internal geometry, the device has a low on-resistance and maintains a low gate-turn-on threshold voltage. Using a pair of parallel-connected JFETs for Q_1 ensures the low saturation voltage for operation at low power-supply voltages.

Rectifying and filtering the positive-going flyback-voltage impulses on Q_1's drain produce a dc voltage across capacitor C_1. To assist the circuit's start-up, a P-channel MOSFET, Q_2, which requires a gate-to-source voltage of approximately 2V for conduction, initially isolates the output load from the rectifier. When Q_2 conducts, the output voltage increases toward 5V. Comparator IC_1, a Linear Technology (www.linear.com) LTC-1440, draws power from Q_2's source and imposes output-voltage regulation by comparing its internal voltage reference with a sample of the output voltage. The output

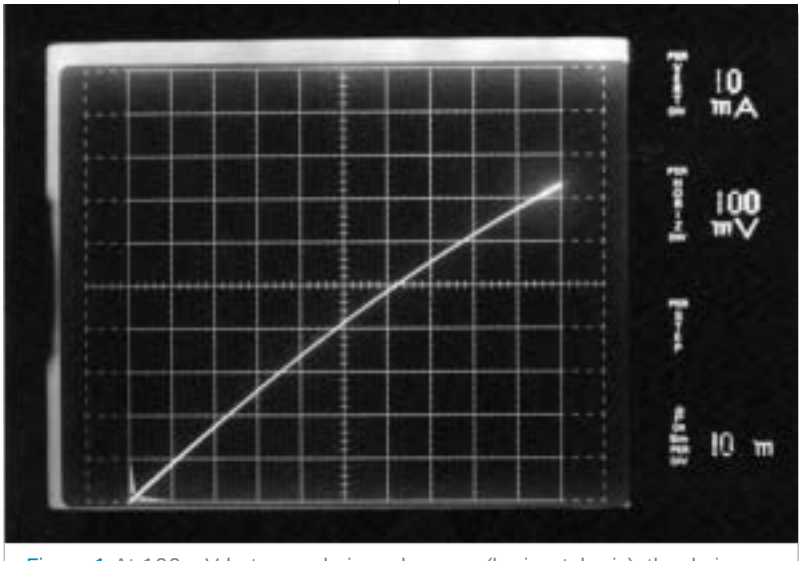

Figure 1 At 100 mV between drain and source (horizontal axis), the drain current reaches 10 mA (vertical axis) and increases to 30 mA at 300 mV.

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from IC_1 varies Q_1's on-time through Q_3 to close the control loop and maintain output-voltage regulation. Figure 3 shows the ripple voltage present at the power supply's output. When the output voltage decays, comparator IC_1 switches (Trace B, middle) and allows Q_1 to oscillate. The resulting flyback events at Q_1's drain (Trace C, bottom) restore the output voltage.

Using Q_3 as a simple but effective shunt control for Q_1's gate voltage results in a 25-mA quiescent-current drain from the power source. A modification reduces the quiescent drain to 1 mA (Figure 4). Inserting switch Q_4 in series with T_1's secondary winding more efficiently controls Q_1's gate. Bootstrapping the voltage across T_1's secondary winding produces negative-turn-off-bias voltage for Q_4. Figure 5 illustrates how to connect T_1's wind-

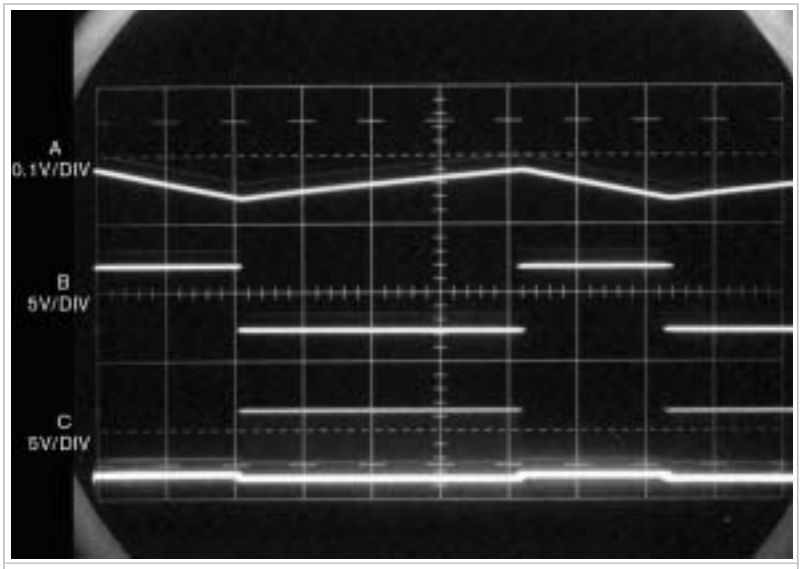
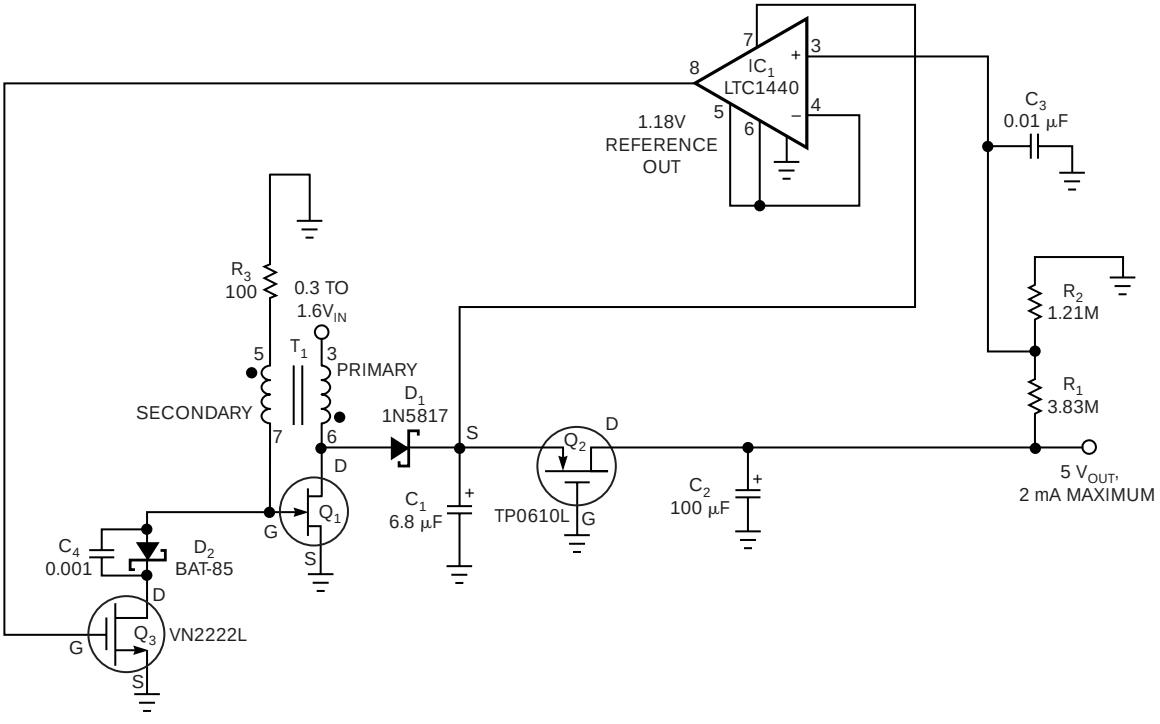


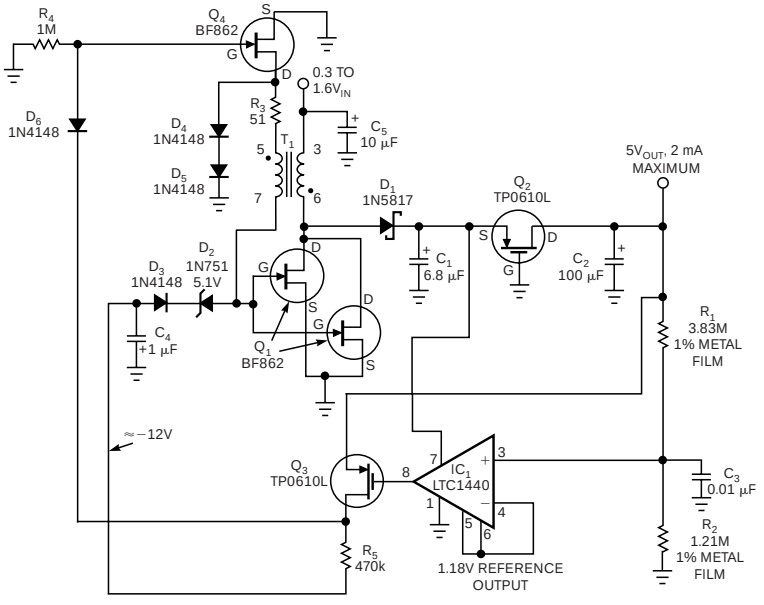
Figure 3 The dc output (Trace A), comparator IC_1's output, and the voltage at Q_1's drain (Trace C) have a horizontal-deflection factor of 5 msec.



NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.

Figure 2 A pair of parallel-connected JFETs allows this dc/dc converter to operate from power sources that supply as little as 300 mV.

ings. When Q_4 switches off, it interrupts the current flowing in T_1's secondary winding and drives T_1's Pin 5 positive. Without diodes D_4 and D_5, the peak voltage would approach 15V and reverse-bias Q_4, an undesirable condition. Under normal operating conditions, excursions of approximately 0.8V appear at Pin 5, necessitating the use of two series-connected diodes to clamp the voltage at a safe level. Zener diode D_3 holds off bias-supply loading to aid start-up during initial power application. EDN



NOTES:
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2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.
4. T_1 = COILTRONICS VP1-1400.

Figure 4 Adding Q_3, Q_4, and the bootstrapped negative-bias generator comprising D_2, D_3, and C_4 reduces the circuit's quiescent current from 25 mA to 1 mA.

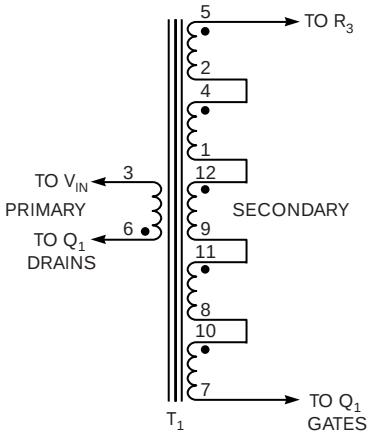

Figure 5 Comprising six independent windings that offer more than 500 configurations, Coiltronics' VP1-1400 serves as a combination feedback and flyback transformer in this application. Connect the windings as shown.

Configurable logic gates' Schmitt inputs make versatile monostables

Glenn Chenier, Allen, TX

You can assemble a pulse-generation circuit from a simple Schmitt-input AND gate plus a resistor-capacitor timing network. However, if you need a logic function that's not a standard catalog item, you need a Schmitt-input gate or inverter and an additional logic gate. Drawing from an earlier Design Idea (Reference 1) and a recent design requirement for adding pulse-generation functions to a crowded pc board, I searched Fairchild Semiconductor's Web site (www.fairchildsemi.com) for small-footprint Schmitt-input logic gates and found only "old faithfuls"—familiar Schmitt-input AND gates and Schmitt buffers.

Disappointed, I investigated other logic offerings from Fairchild and stumbled across a section of the Web site that describes "configurable logic gates." Lo and behold, I suddenly realized I was looking at the solution to my problem. The NC7SZ57 and NC7SZ58 (Reference 2) comprise tiny, six-pin surface-mount packages that you can configure as inverters or as AND, OR, or XOR gates, all of which allow the inversion of one input. These devices feature inverted outputs, overvoltage-input tolerance, and high current drive.

Every input has hysteresis, making these devices ideal for timed pulse generation. A design that combines digital logic with analog interfaces often requires timed pulses and delays, along with pulse shorteners and stretchers. For applications in which exact pulse times are not critical, the added feature of Schmitt inputs allows the delay of one input using an RC (resistance-capacitance) timing network. When the slowly changing RC circuit's output crosses the analog-level upper- or lower-trip-point thresholds, the Schmitt feature converts the slowly rising and falling voltages to fast digital edges.

Texas Instruments (www.ti.com)

offers functional equivalents—the SN74LVC1G57 and SN74LVC1G58 (Reference 3). Both companies' devices offer upper- and lower-trip-point-voltage thresholds averaging 37 and 63%, respectively, of V_{CC}, or approximately one RC time constant on the rising or the falling edges. According to the published data sheets from the manufacturers' Web sites, Texas Instruments' versions impose somewhat tighter tolerances on the analog threshold levels and thus deliver tighter timing tolerances than do the Fairchild parts.

For digital-analysis purposes, any voltage below the upper trip point for a rising edge effectively represents a logic zero, and any voltage above the lower trip point for a falling edge represents a logic one. These conditions are true only after the input crosses a respective trip point, such as a rising edge that approaches but never crosses the upper trip point. This voltage remains a logic zero, even if the voltage then drops back to ground potential on its falling edge.

Figure 1a shows some typical circuit implementations. Note that these circuits lack some of the niceties of genuine monostables. For example, a circuit doesn't retrigger until after its RC network has stabilized or about five time constants have elapsed. The RC time constant must be five times shorter than the time between triggering events. Devices from the SN74LVC1G57 family produce the waveforms in Figure 1b, and circuits using the SN74LVC1G58-family devices produce the inverse of these waveforms. The circuits' operation is straightforward. The RC circuits delay one input, so that the inputs momentarily rest at opposite states. When one RC time constant elapses, the delayed voltage crosses the Schmitt upper- or lower-trip-point thresholds, and the delayed input catches up to the straight-through input.

Of unusual interest and unlike the usual variety of monostable that triggers only from a voltage transition in one direction, the XOR implementation functions as a monostable triggered by both the rising and the falling edges, enabling it to function as a frequency doubler for generating strobe pulses on rising and falling clock edges. You can make any inverting-gate configuration into an oscillator by feeding back its inverted output to an RC-delayed Schmitt input and enabling the gate's remaining input. However, once the XOR oscillator's remaining gate switches off the oscillation, the gate's output state hangs at either a one or a zero to produce a truly random state derived from the oscillation's nonsynchronous relationship to the timing of the disabling input. EDN

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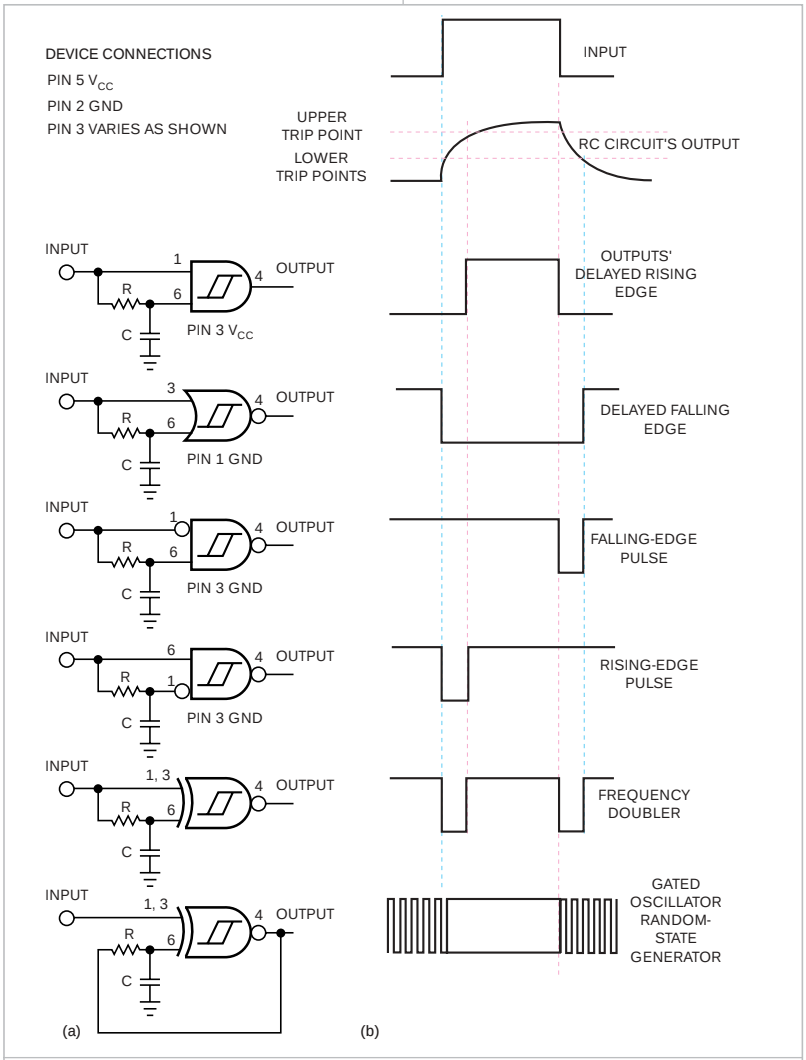

Figure 1 One gate plus an RC network (a) can deliver a range of useful timed outputs (b).

Stealth-mode LED controls itself

Howard Myers, Greensboro, NC

Since the LED's invention more than 30 years ago, its emission efficiency has steadily increased, and, although it may surprise you, the increased conversion efficiency works in two directions. Certain bright, efficient LEDs, such as Hewlett-Packard's (www.hp.com) HLMP-EG30-NR000, a red emitter molded in clear encapsulation, also exhibit significant photovoltaic action. The circuit in Figure 1 shows how you can put an LED's photovoltaic characteristics to work. Using the same components, older, red LEDs also function but with lower light output in this circuit. This Design Idea circuit describes an LED that controls itself by determining whether it's on or off without the assistance of any light sensor other than its own characteristics. When you darken the LED, it turns on, and, when you illuminate it, it turns off. The circuit's main components comprise LED D_1, micropower operational amplifier IC_1, one-shot IC_{2A}, and transistor switch Q_1 to control current through the LED.

When dark, the LED produces no photovoltaic current. When moderate lighting, such as that in an office or a lab, illuminates it, it generates 50 to 100 mV into a 4.7-MΩ load resistor. Comparator op amp IC_1 compares the voltage that the LED produces with a threshold reference voltage of approximately 50 mV. You can vary the circuit's sensitivity threshold by altering the values of resistors R_1 and R_2 in the voltage divider that connects to IC_1's Pin 2.

When ambient light decreases, the LED produces less voltage, and, when the voltage falls below the 50-mV threshold, the op amp's output goes low and triggers one-shot IC_{2A}. The one-shot turns on transistor Q_1 for an interval, lighting the LED for approximately 3 msec until the one-shot's output goes low. In a darkened room, the cycle repeats at a 200-Hz rate, and the LED blinks repeatedly with short off periods. At high flash rates, the LED appears to be continuously on.

The circuit's current drain in the daylight state mainly comprises the current driving the reference-bias network: 3.6V/162 kΩ=22 μA. In both day and night modes, with the LED drawing a few milliamperes when illuminated, a battery that can deliver 1 Ahr would power the circuit for a couple of months. You can reduce the current by increasing the values of R_1 and R_2. Given the circuit's low and intermittent current drain in a well-lighted environment, a 1-Ahr lithium cell's service life should approach its shelf life. EDN

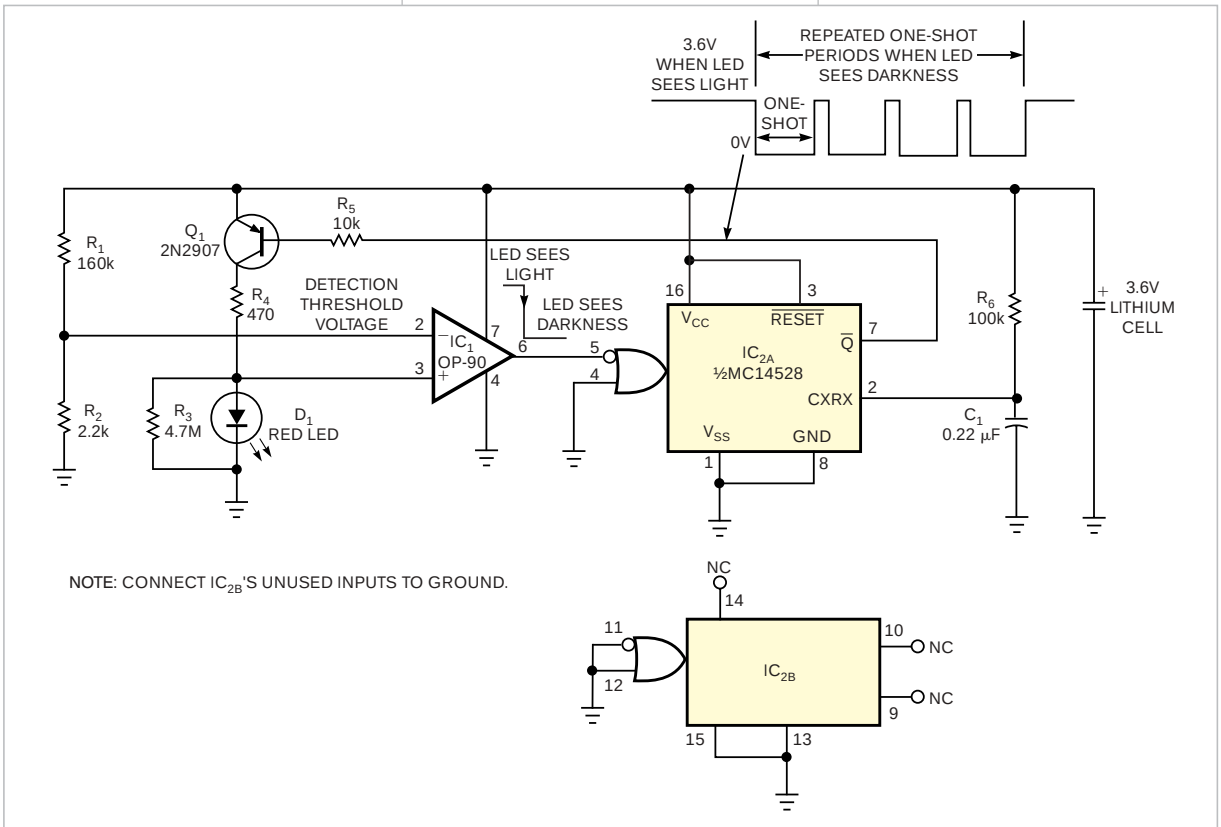

Figure 1 An efficient LED forms the heart of a light-sensitive "mystery lamp" that contains no apparent photodetector.

Data-acquisition system captures 16-bit voltage measurements using the USB

Terry Millward, Maxim Integrated Products Inc, Bionay, Switzerland

The USB has become the interface of choice for connecting to PCs. Available on all relatively modern PCs, the USB offers a standard connector and can supply power to peripherals at 5V and as much as 100 mA of current. The circuit in Figure 1 combines Maxim's (www.maxim-ic.com) MAX1168, a low-power, 16-bit ADC, with a small USB-interface module to make a simple, eight-channel, 16-bit measurement system. The MAX1168 includes eight input channels, an SPI (serial-peripheral-interface) port, a 4.096V reference, and a clock oscillator. The MAX1168 operates from a 5V supply and can convert individual channels, execute multiple conversions on one channel, or scan the channels sequentially and store measured data on-chip.

Based on a Cypress (www.cypress.com) CY7C63743 controller, USBmicro's (www.usbmicro.com) U421 USB-interface module provides as many as 16 I/O lines and an option to use some of those lines as an SPI port at selectable clock rates of 62.5 kHz, 500 kHz, 1 MHz, or 2 MHz. Firmware on the U421 allows generic access to SPI read-and-write devices, and the device's general-purpose I/O lines can serve as slave-select lines for addressing multiple SPI devices. One I/O line controls the MAX1168's chip-select input. When you use it with an

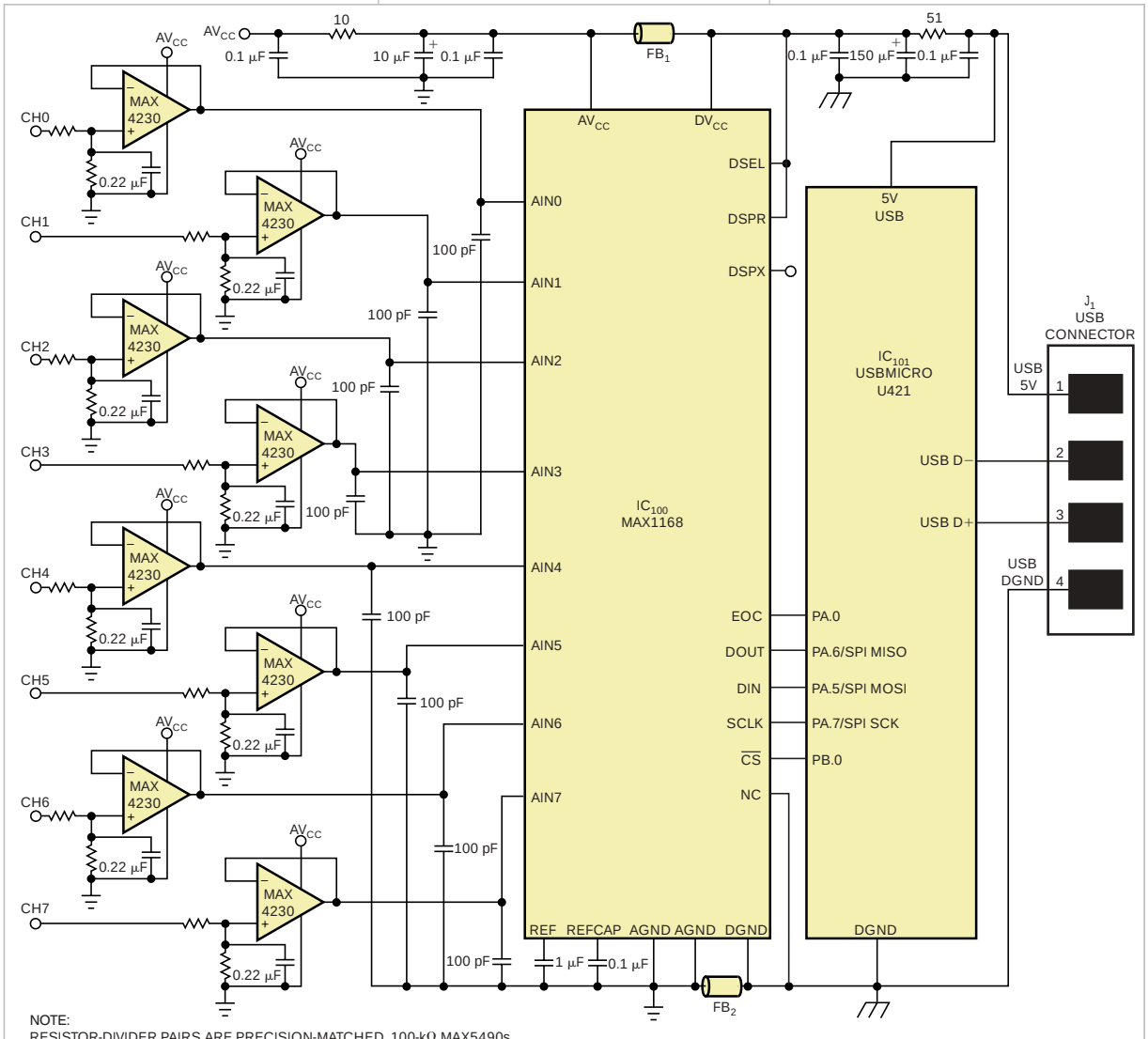

Figure 1 This simple data-acquisition system provides eight channels of 16-bit data to a host computer through a USB interface.

HID (human-interface device), the U421 USB controller can transfer data at rates as high as 800 bytes/sec. With additional filtering to reduce noise, the USB port provides 5V power to the circuit.

The MAX1168's sample-and-hold circuit must acquire the input voltage and charge its 45-pF holding capacitor in 3 μsec and thus requires a fast amplifier to minimize acquisition errors. Available in dual and quad versions, the MAX4230 provides a 10-MHz bandwidth, 2V/μsec slew rate, rail-to-rail inputs and outputs, and the ability to operate from a 5V rail or from voltages as low as 2.7V. The MAX4230's bias current—typically, 50 pA—allows significant input impedance without affecting accuracy.

To provide protection from overvoltages and apply input-voltage scaling, each buffer amplifier's input includes a 100-kΩ precision-matched resistive divider. This application uses Maxim's MAX5490VA10000 10-to-1 dividers, which provide a scaling factor of $^1/_{11}$, to allow maximum readable inputs of 45V at resolutions of 687.5 μV.

Figure 2 User-interface software for the data-acquisition system allows selection of operating parameters. In this image, the lower three channels are unselected and hence are not visible in the display.

Written in Microsoft's Visual Basic.Net, Standard Edition, the evaluation software provides commands to the U421 through the USBm.dll DLL (dynamic-linking-library) file. The demo program sets the MAX1168 to scan all eight channels and display the results. When you run the program, the Visual Basic form allows you to set the reference voltage to allow for the input divider, select the scan time, and enable any of the eight input channels for screen display (Figure 2). You can download the evaluation software at www.maxim-ic.com/MAX=1168DI. EDN

ACKNOWLEDGMENT

Thanks to Robert Severson of USBmicro for his help with the interface.