

Data sheet acquired from Harris Semiconductor SCHS031B – Revised July 2003

CD4026B, CD4033B Types

CMOS Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)
With Decoded 7-Segment Display Outputs and:
Display Enable — CD4026B
Ripple Blanking — CD4033B

■ CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

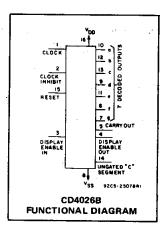
Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals péculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

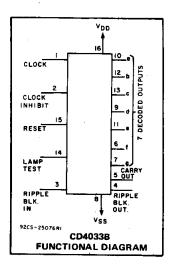
A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHI-BIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter. thus assuring proper counting sequence. The CARRY-OUT (Cout) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven

MAXIMUM RATINGS, Absolute-Maximum Values:

Features:

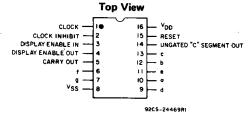
- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 6 MHz (typ.)
 at V_{DD}=10 V
- Ideal for low-power displays
- Display enable output (CD4026B)
- "Ripple blanking" and lamp test (CD4033B)
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Schmitt-triggered clock inputs
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices" Applications
- Decade counting 7-segment decimal display
- Frequency division 7-segment decimal displays
- Clocks, watches, timers
 (e.g. ÷60, ÷ 60, ÷ 12 counter/display)
- Counter/display driver for meter applications



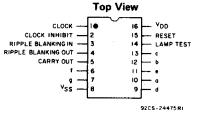


segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

TERMINAL DIAGRAMS



CD4026B



CD4033B

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) Voltages referenced to V_{SS} Terminal) -0.5V to +20V INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V DC INPUT CURRENT, ANY ONE INPUT ±10mA POWER DISSIPATION PER PACKAGE (P_D): For $T_A = -55^{\circ}C$ to +100°C 500mW For $T_A = +100^{\circ}C$ to +125°C Derate Linearity at 12mW/°C to 200mW DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A = FULL$ PACKAGE-TEMPERATURE RANGE (All Package Types) 000mW OPERATING-TEMPERATURE RANGE (T_{SC}) 55°C to +125°C STORAGE TEMPERATURE RANGE (T_{SC}) -65°C to +150°C LEAD TEMPERATURE (DURING SOLDERING): At distance 1/18 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD		UNITS		
A CONTRACTOR OF THE CONTRACTOR	(V)	MIN.	MAX.	00	
Supply-Voltage Range (For T _A Temperature Range)	\ = Full Package		3	18	V
Clock Input Frequency, 1	CL	5 10 15	- -	2.5 5.5 8	MHz
Clock Pulse Width,	WCL.	5 10 15	220 100 80	- - -	
Clock Rise and Fall Time, 1	rCL ^{, t} fCL	5 10 15	- 	Unlimited	:
Clock Inhibit Set Up Time, t	SU	5 10 15	200 50 30	- -	ns
Reset Pulse Width, t	W	5 10 15	200 100 50	- - -	e.
Reset Removal Time		5 10 15	30 15 10	- -	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-	CONE	ıs	LIMITS AT INDICATED TEM				MPERA'	UNITS			
ISTIC	Vo	VIN	v_{DD}						+25		014113
	(V)	(V)	(V)	-55	-4 0	+85	+125	Min.	Тур.	Max.	
Quiescent Device	-	0,5	5	5	5	150	150		0.04	5	
Current,		0,10	10	10	10	300	300	_	0.04	10	μА
IDD Max.	-	0,15	15	20	20	600	600	-	0.04	20]
	_	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low	0.4	0,5	- 5	0.64	0.61	0.42	0.36	0.51	1	-	
(Sink) Current	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	. 1]
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-]
Output High	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1		mA
(Source)	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	1	
Current, IOH Min.	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	:	
TOH WITH	13.5	0,15	15	-4.2	-4	2.8	-2.4	-3.4	-6.8	-	
Output Voltage:	_	0,5	5	0.05				-	0	0.05	
Low-Level,	_	0,10	10	0.05				+	- 0	0.05	
VOL Max.	_	0,15	15	0.05					0	0.05	v
Output Voltage:	_	0,5	5	4.95				4.95	5	-]
High Level,	-	0,10	10		9.95				10	-	
VOH Min.	_	0,15	15		14	.95		14.95	15	-	
Input Low	0.5, 4.5	_	5		1	.5		-		1.5	
Voltage,	1, 9	_	10			3			_	3	
VIL Max.	1.5,13.5	_	15			4		-	<u> </u>	4	l v
Input High Voltage, VIH Min.	0.5, 4.5	-	5		,	3.5		3.5	_		\ \ \
	1, 9		10		7				_	-	
	1.5,13.5	-	15			1		11	<u> </u>	_]
Input Current IN Max.	-	0,18	18	±0.1	±0.1	±1	±1		±10 ⁻⁵	±0.1	μΑ

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

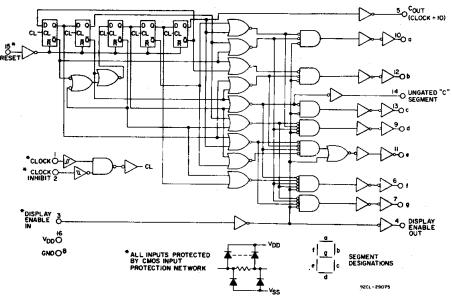


Fig. 1 - CD4026B logic diagram.

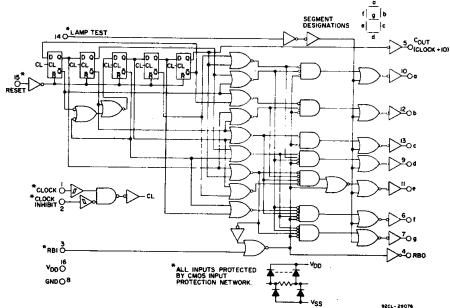


Fig. 2 - CD4033B logic diagram.

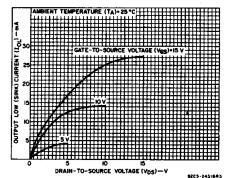


Fig. 6 — Typical n-channel output low (sink) current characteristics.

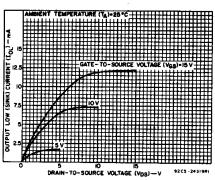


Fig. 7 — Minimum n-channel output low (sink) current characteristics.

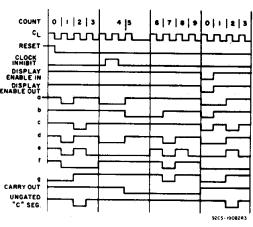


Fig. 3 — CD4026B timing diagram.

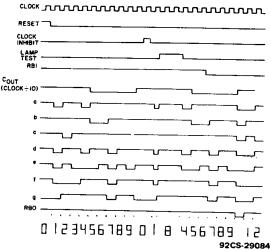


Fig. 4 -- CD4033B timing diagram.

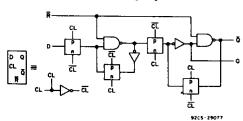


Fig. 5 - Detail of typical flip-flop stage for both types.

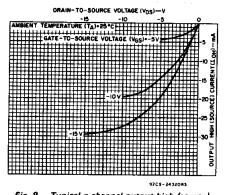


Fig. 8 — Typical p-channel output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r , t_f = 20 ns, C_L = 50 pF, R_L = 200 k Ω

		TEST CONDITIONS			LIMIT	s	
CHARACTERISTIC			V _{DD}	t -		Max.	UNITS
CLOCKED OPERATION					• •		·
Propagation Delay Time;	^t PLH ^{, t} PHL		5	_	250	500	
Carry-Out Line		•	10 15		100	200	
<u> </u>		 	 		75	150	
Decode Outlines			5		350	700	
			10		125	250	ns
Transition Time:			15		90	180	
Carry-Out Line	^t THL ^{, t} TLH		5	<u> </u>	100	200	
Carry-Out Line	÷ .		10	-	50	100	
Mariana Charles a F		 	15	-	25	50	
Maximum Clock Input Fred	dneuch, tCT▼		5	2.5	5	<u> </u>	
Secretary of the second of the			10	5.5	11	-	MHz
			15	8	16	<u> </u>	
Min. Clock Pulse Width,	t _W .	÷	5		110	220	
			10		50	100	
Clock and Clock Inhibit Di			15		40	80	
Clock and Clock Inhibit Ris			5				
	^t rCL ^{, t} fCL	4,	10 15	Un	limite	d	ns
Average Input Capacitance,	CIN	Any Input		_	5	7	рF
RESET OPERATION							
Propagation Delay Time;			5	_	275	550	
To Carry-Out Line,	^t PLH		10	_	120	240	
		1	15	_	80	160	
To Decode Out Lines,	^t PHL ^{, t} PLH		5	_	300	600	
			10	_	125	250	
			15	-	90	180	ns
Min. Reset Pulse Width,	ťw		5	_	100	120	
j.			10	-	50	100	
		1	15	_	25	50	
Ain. Reset Removal Time			5	_	0	30	
			10	-	0	15	
<u> </u>			15	_]	0	10	

[▲] Measured with respect to carry-out line.

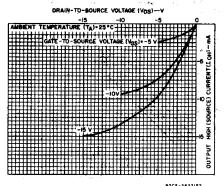


Fig. 9 – Minimum p-channel output high (source) current characteristics.

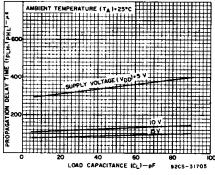


Fig. 10 — Typical propagation delay time as a function of load capacitance for decoded outputs.

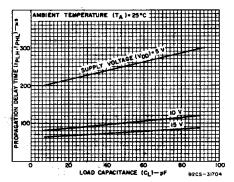


Fig. 11 — Typical propagation delay time as a function of load capacitance for carry-out outputs.

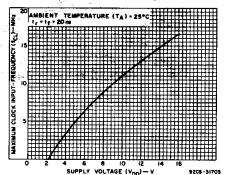
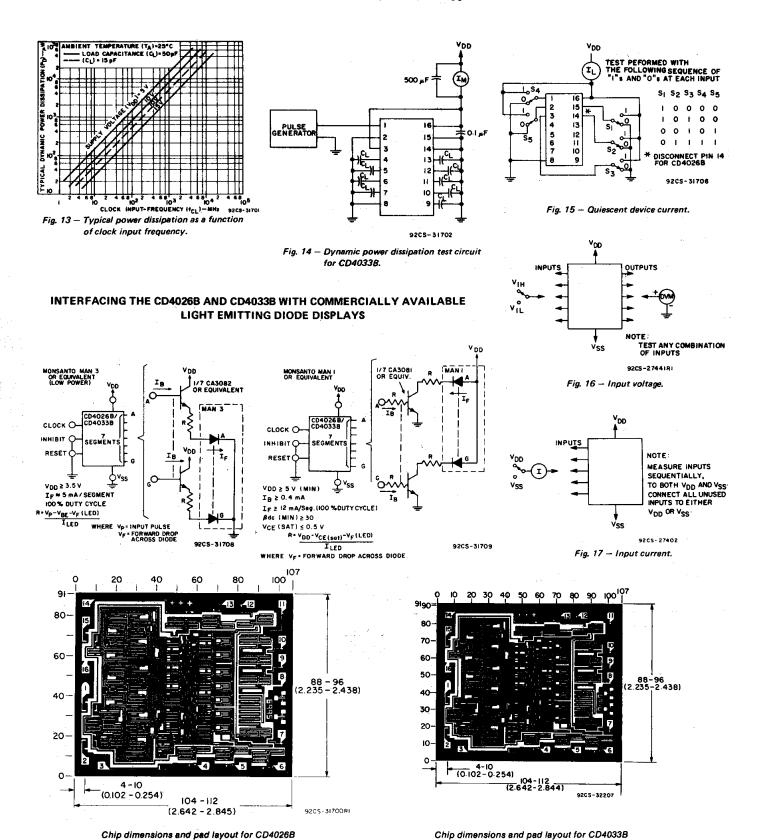


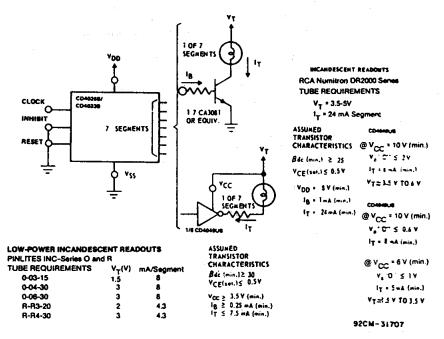
Fig. 12 - Typical maximum clock input-frequency as a function of supply voltage.



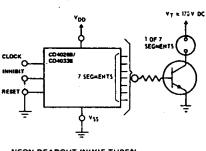
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

3-74

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES*



* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10 V.



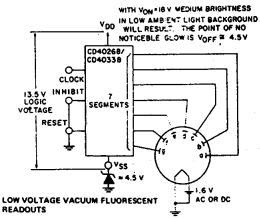
NEON READOUT (NIXIE TUBE*)

- 1. Alco Electronics -- MG19
- 2. Burroughs 85971, B7971, B8971

TUBE REQUIREMENTS	mA Segme		
Alco MG19	180	. 0.5	
Burroughs B5971	170	. 3	
Burroughs B7971, B8971.	170	. 6	

▲ (Trademark) Burroughs Corp.
TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff — 0.05 mA

 $V(BR)CER \cdot \cdot \cdot \cdot > V_{\Upsilon}$ β_{dc} (min.) ≥ 30 92CS-31710



- 1. Tung-Sol DIGIVAC S/G ‡ Type DT1704A or DT1705C
- 2. Nippon Electric (NEC); Type DG12E or LD915 TUBE REQUIREMENTS: 100 to 300 µA/segment at tube voltages of 12 V to 25 V depending on required brightness Filament requirement 45 m ≠ at 1.6 V, ac or dc.
- 3 (Trademark) Wagner Electric Co.

92 (5-317)

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4026BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4026BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4026BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4026BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4033BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4033BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4033BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4033BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4033BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

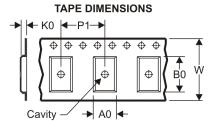
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4026BNSR	so	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4026BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4026BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4026BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

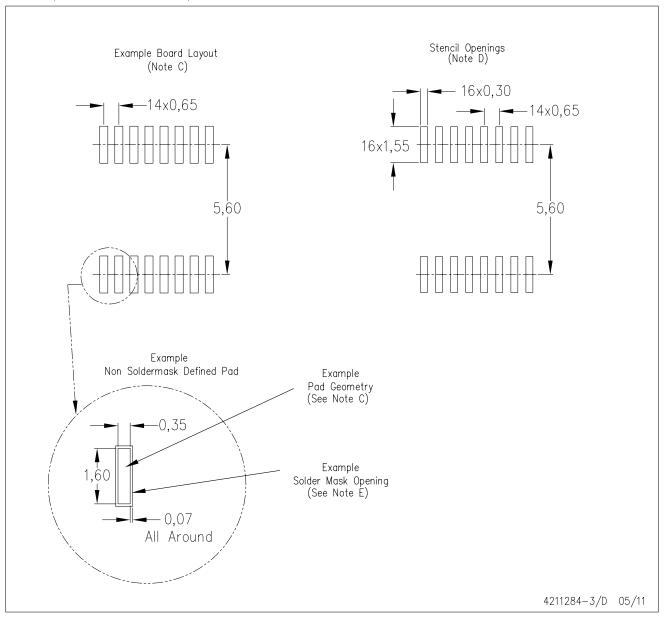


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

TI E2E Community Home Page

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

e2e.ti.com