TEXAS INSTRUMENTS

LOGIC MARKING GUIDELINES

Older Logic package types were large enough to permit the complete device name to be symbolized on the package. Newer package types are smaller and Logic product names are longer requiring the reduction of symbolized character count. Information in the following tables is intended to help interpret TI's Logic symbolization.

Table 1 defines a "name rule" (A, B, or C) based on the package for a specific device type. Each name rule differs in the number of symbolized characters for that package. Name rule A uses the complete, or fully qualified, device name. Name rules B and C include fewer characters, respectively. Table 2 is a listing of the various logic products by name rule.

Example:

Assume a 48–pin TVSOP with the symbolization VH***. Locate the 48–pin TVSOP (DGV) package in Table 1, and find the name rule used (C). Proceed to Table 2, and find VH*** in the Name Rule C column. The complete device number, SN74ALVCH16***, is located in the Name Rule A column.

See the following information and Tables 3 and 4 for Little–Logic (PicoGate Logic, Microgate Logic, and NanoStar™) packages.

Table 1: Name Rule Decision Tree

Package	No. Pins	Name Rule	Package Designator
LFBGA	96	C	GKE
	114	C	GKF
PDIP	8	A	P
	14, 16, 20	A	N
	24, 28	A	NP, NT
PLCC	28	A	FN
	44	B	FN
	68	A	FN
QSOP	16, 20, 24	B	DBQ
SOIC	8	C	D
	14, 16	B	D
	16, 20, 24, 28	B	DW
QFP	52	B	RC
	80	A	PH
	100, 132	A	PQ
SOP	8	C	PS
	14, 16, 20, 24	B	NS
SSOP	14, 16, 20, 24, 28, 30, 38	C	DB
	28, 48, 56	B	DL
TSSOP	8, 14, 16, 20, 24, 28	C	PW
	48, 56, 64	B	DGG
TVSOP	14, 16, 20, 24, 48, 56	C	DGV
	80	B	DBB
TQFP	52	B	PAH
	64	B	PAG, PM
	80	B	PN
	100	B	PZ, PCA
	120	B	PCB
VFBGA	20	C	GQN
	56	C	GQL

Table 2: Typical Logic Package Symbolization Guidelines

Name Rule A	Name Rule B	Name Rule C
74AC***	AC***	AC***
74AC11***	AC11***	AE***
74ACT***	ACT***	AD***
74ACT1***	ACT1***	AU***
74ACT11***	ACT11***	AT***
CD4***	CD4***	CM***
CD4***	CD4***M†	CM***
CD74AC***	AC***M	HL***
CD74AC40	AC40***M	HY***
CD74ACT***	ACT***M	HM***
CD74ACT40***	ACT40***M	HZ***
CD74FCT***	74FCT***M	FC***
CD74FCT***	74FCT***M	FCT***SM‡
CD74HC***	HC***M	HJ***
CD74HC40***	HC40***M	HP***
CD74HCT***	HCT***M	HK***
CD74HCT40***	HCT40***M	HR***
CY29FCT***	29FCT***	FY***–*§
CY74FCT***	FCT***	FT***–*§
CY74FCT16***	FCT16***	FD***§
CY74FCT2***	FCT2***	FR***–*§
PCF8***	PCF8***	PF***
SN64BCT***	DCT***	DT***
SN64BCT2***	DCT2***	DA***
SN64BCT25***	DCT25***	DC***
SN64BCT29***	DCT29***	DD***
SN74ABT***	ABT***	AB***
SN74ABT***–S	ABT***–S	AB***–S
SN74ABT16***	ABT16***	AH***
SN74ABT162***	ABT162***	AH2***
SN74ABT18***	ABT18***	AJ***
SN74ABT2***	ABT2***	AA***
SN74ABT5***	ABT5***	AF***
SN74ABT8***	ABT8***	AG***
SN74ABTE16***	ABTE16***	AN***
SN74ABTH***	ABTH***	AK***
SN74ABTH16***	ABTH16***	AM***
SN74ABTH162***	ABTH162***	AM2***
SN74ABTH18***	ABTH18***	AL***
SN74ABTR2***	ABTR2***	AR***
SN74AHC***	AHC***	HA***

Name Rule A	Name Rule B	Name Rule C
SN74AHC16***	AHC16***	HE***
SN74AHCH16***	AHCH16***	HH***
SN74AHCT***	AHCT***	HB***
SN74AHCT16***	AHCT16***	HF***
SN74AHCTH16***	AHCTH16***	HG***
SN74AHCU***	AHCU***	HD***
SN74ALB16***	ALB16***	AV***
SN74ALS***	ALS***	G***
SN74ALVC***	ALVC***	VA***
SN74ALVC16***	ALVC16***	VC***
SN74ALVC162***	ALVC162***	VC2***
SN74ALVCH***	ALVCH***	VB***
SN74ALVCH16***	ALVCH16***	VH***
SN74ALVCH162***	ALVCH162***	VH2***
SN74ALVCH32***	ALVCH32***	ACH***
SN74ALVCHG16***	ALVCHG16***	VG***
SN74ALVCHG162***	ALVCHG162***	VG2***
SN74ALVCHR16***	ALVCHR16***	VR***
SN74ALVCHR162***	ALVCHR162***	VR2***
SN74ALVCHS162***	ALVCHS162***	VS2***
SN74ALVTH16***	ALVTH16***	VT***
SN74ALVTH162***	ALVTH162***	VT2***
SN74ALVTH32***	ALVTH32***	VL***
SN74AS***	AS***	AS***
SN74AS***	74AS***¶	AS***
SN74AVC***	AVC***	AVC***
SN74AVC16***	AVC16***	CVA***
SN74AVC32***	AVC32***	ACV***
SN74AVCC16***	AVCC16***	AW***
SN74AVCH16***	AVCH16***	CVH***
SN74BCT***	BCT***	BT***
SN74BCT11***	BCT11***	BB***
SN74BCT2***	BCT2***	BA***
SN74BCT25***	BCT25***	BC***
SN74BCT29***	BCT29***	BD***
SN74BCT8***	BCT8***	BG***
SN74CBT***	CBT***	CT***
SN74CBT16***	CBT16***	CY***
SN74CBT3***	CBT3***	CU***
SN74CBT6***	CBT6***	CT6***
SN74CBTD***	CBTD***	CD***

† For SOIC (D and DW) only
‡ For DB package only
§ Speed grade
¶ For NS package only

Table 2: Typical Logic Package Symbolization Guidelines (continued)

Name Rule A	Name Rule B	Name Rule C
SN74CBTD16***	CBTD16***	CYD***
SN74CBTD3***	CBTD3***	CC***
SN74CBTH16***	CBTH16***	CYH***
SN74CBTK***	CBTK***	BK***
SN74CBTK16***	CBTK16***	CP***
SN74CBTK32***	CBTK32***	KT***
SN74CBTLV16***	CBTLV16***	CN***
SN74CBTLV3***	CBTLV3***	CL***
SN74CBTR16***	CBTR16***	CZ***
SN74CBTS***	CBTS***	CS***
SN74CBTS16***	CBTS16***	CYS***
SN74CBTS3***	CBTS3***	CR***
SN74F***	F***	F***
SN74F***	74F***¶	F***
SN74GTLP***	GTLP***	GT***
SN74GTLP1***	GTLP1***	GP***
SN74GTLPH***	GTLPH***	GH***
SN74GTLPH16***	GTLPH16***	GL***
SN74GTLPH32***	GTLPH32***	GM***
SN74HC***	HC***	HC***
SN74HCT***	HCT***	HT***
SN74HCU***	HCU***	HU***
SN74LS***	LS***	LS***
SN74LS***	74LS***¶	LS***
SN74LV***	LV***	LV***
SN74LV***	74LV***¶	LV***
SN74LVC***	LVC***	LC***
SN74LVC16***	LVC16***	LD***
SN74LVC2***	LVC2***	LE***
SN74LVC32***	LVC32***	NC***
SN74LVC4***	LVC4***	LJ***
SN74LVC8***	LVC8***	LC8***

Name Rule A	Name Rule B	Name Rule C
SN74LVCC3***	LVCC3***	LH***
SN74LVCC4***	LVCC4***	LG***
SN74LVCH***	LVCH***	LCH***
SN74LVCH16***	LVCH16***	LDH***
SN74LVCH162***	LVCH162***	LN2***
SN74LVCH32***	LVCH32***	CH***
SN74LVCHR162***	LVCHR162***	LR2***
SN74LVCR2***	LVCR2***	LER***
SN74LVCU***	LVCU***	LCU***
SN74LVCZ***	LVCZ***	CV***
SN74LVCZ16***	LVCZ16***	CW***
SN74LVT***	LVT***	LX***
SN74LVT***–S	LVT***–S	LX***–S
SN74LVT162***	LVT162***	LZ***
SN74LVT18***	LVT18***	T18***
SN74LVT2***	LVT2***	LY***
SN74LVT32***	LVT32***	VJ***
SN74LVTH***	LVTH***	LXH***
SN74LVTH16***	LVTH16***	LL***
SN74LVTH162***	LVTH162***	LL2***
SN74LVTH2***	LVTH2***	LK***
SN74LVTH32***	LVTH32***	HV***
SN74LVTR***	LVTR***	LXR***
SN74LVTT***	LVTT***	LXT***
SN74LVTZ***	LVTZ***	LXZ***
SN74LVU***	LVU***	LU***
SN74S***	S***	S***
SN74S***	74S***¶	S***
SN74SSTV16***	SSTV16***	SS***
SN74TVC16***	TVC16***	TW***
SN74TVC3***	TVC3***	TT***

† For SOIC (D and DW) only
‡ For DB package only
§ Speed grade
¶ For NS package only

DCK, DBV, AND YEA 5–PIN SOT PACKAGES FOR LITTLE LOGIC

The DCK (PicoGate Logic), DBV (Microgate Logic), and NanoStar 5–pin packages are very small and have space for only three or four characters for device–name marking. The format of the characters is 1, 2, 3, or 1, 2, 3, 4 where:

Package	DCK	DBV	YEA	TABLE
Device technology	1	1	1	See Table 3
Device function	2	2, 3	2	See Table 4
Wafer fabrication/assembly test site code	3	4	3	

Tables 3 and 4 list the possible device technology and function codes for the 5–pin packages. In some cases, the tables may list a device technology or function not yet available. The wafer fabrication and assembly–test site is coded into the final character for both packages. Additional tracking information is coded into “dots” or marks adjacent to the device pins. For further information about a specific device, please contact your local field sales office or the TI Product Information Center.

PicoGate Logic

PicoGate Logic uses a three–character name rule. The first character denotes the technology family, the second character denotes device function, and the third character denotes a wafer fabrication and assembly–test facility combination (for internal tracking, here denoted by x).

Example

A PicoGate Logic device with a package code of BAx is an SN74AHCT1G00DBV.

Microgate Logic

Microgate Logic uses a four–character name rule. The first character denotes the technology family, the second and third characters denote device function, and the fourth character denotes a wafer fabrication and assembly–test facility combination (for internal tracking, here denoted by x).

Example

A Microgate Logic device with a package code of A02x is an SN74AHC1G02DCK.

NanoStar Package

The NanoStar package uses a three–character name rule. The first character denotes the technology family, the second character denotes device function, and the third character denotes a wafer fabrication and assembly–test facility combination (for internal tracking, here denoted by x).

Note: For NanoStar packages, the three–character device name is preceded by three additional characters denoting year (Y), month (M), and sequence code (L).

Example

A NanoStar package logic device with a package code of YMLCAx is an SN74LVC1G00YEA.

Table 3: Little Logic Device Technology Codes

Technology	Code
AHC	A
AHCT	B
CBT	S
CBTD	P
LVC1G*	C
CBTLV1G	V

Table 4: Little Logic Device Function Codes

Function	DCK	DBV/DCT/DCU
00	A	00
02	B	02
04	C	04
05	5	05
06	T	06
07	V	07
08	E	08
14	F	14
17	7	17
32	G	32
34		34
53		53
66	6	66

Function	DCK	DBV/DCT/DCU
74		74
79	R	79
80	X	80
86	H	86
125	M	25
126	N	26
132	Y	3B
157		57
240	K	40
241		41
245		45
384	8	8D
U04	D	U4

LOGIC PACKAGE MOISTURE SENSITIVITY

The information in Table 5 was derived using the test procedures in JEDEC J-STD-020/JEDEC J-STD-033. The Floor Life column lists the time that products can be exposed to the open air while in inventory or on the manufacturing floor. The worst–case environmental conditions are given. The Soak Requirements column lists the preconditioning, or soak, conditions used when testing to determine the floor–life exposure time.

Table 5: Moisture–Sensitivity Levels (JEDEC J–STD–020/JEDEC J–STD–033)

Level	Floor Life		Standard Soak Requirements		Accelerated Soak Requirements	
	Conditions	Time (hours)	Conditions	Time (hours)	Conditions	Time (hours)
1	≤ 30°C/ 85% RH	Unlimited	85°C/ 85% RH	168		
2	≤ 30°C/ 85% RH	1 year	85°C/ 60% RH	168		
2a	≤ 30°C/ 85% RH	4 weeks	30°C/ 60% RH	696	60°C/ 60% RH	120
3	≤ 30°C/ 85% RH	168	30°C/ 60% RH	192	60°C/ 60% RH	40
4	≤ 30°C/ 85% RH	72	30°C/ 60% RH	96	60°C/ 60% RH	20
5	≤ 30°C/ 85% RH	48	30°C/ 60% RH	72	60°C/ 60% RH	15
5a	≤ 30°C/ 85% RH	24	30°C/ 60% RH	48	60°C/ 60% RH	10
6	≤ 30°C/ 85% RH	Time on label	30°C/ 60% RH	Time on label		

RH = Relative humidity

For more information, see:

Packaging Material Standards for Moisture–Sensitive Items, EIA Std EIA–583
Symbol and Labels for Moisture–Sensitive Devices, EIA/JEDEC Engineering Publication EIA/JEP113–B, May 1999
Guidelines for the Packing, Handling, and Repacking of Moisture–Sensitive Components, EIA/JEDEC Publication EIA/JEP124, December 1995

Table 6 lists the moisture sensitivity of TI packages by level. Some packages differ in level by pin count. moisture–sensitivity level.

Table 6: Package Moisture Sensitivity Levels

Package	Level 1	Level 2	Level 2A	Level 3	Level 4
PLCC	FN (20/28)			FN (44/68)	
SOT	DBV (5) DCK (5)				
SOP	NS (14/16/20) PS (8)				
SOIC	D (8/14/16) DW (16/20/24/28)				
SSOP	DB (14/16/20/24/28/30/38) DBQ (16/20/24) DL (28/48/56)				
TSSOP	DCT (8) DCU (8) DGG (48/56/64) PW (8/14/16/20/24)				
TVSOP	DBB (80) DGV (14/16/20/24/48/56)				
QFP		RC (52)			
TQFP		PAG (64) PCA (100) PN (80) PZ (100)			PM (64)
MicroStar BGA				GKE (96) GKF (114)	
MicroStar Jr. BGA			GQN (20) GQL (56)		
NanoStar	YEA (5/8)				

NOTES:
1. No current device packages are moisture–sensitivity levels 5 or 6.
2. Some device types in these packages may have different moisture–sensitivity levels than shown.

TI's through–hole packages (N, NT) have not been tested per the JEDEC J-STD-020/JEDEC J-STD-033 standards. Due to the nature of the through–hole PCB soldering process, the component package is shielded from the solder wave by the PC board and is not subjected to the higher reflow temperatures experienced by surface–mount components.

TI's through–hole component packages are classified as not moisture sensitive.

TEXAS INSTRUMENTS

LOGIC DEVICE PACK QUANTITIES

Tables 7 through 10 list the standard pack quantities, by package type, for tubes, reels, boxes, and trays, respectively.

Table 7: Tube Quantities

	PIN COUNT									
	8	14	16	20	24	28	44	48	56	68
DIP	50	25	25	20	15	13	N/A	N/A	N/A	N/A
PLCC	N/A	N/A	N/A	46	N/A	37	26	N/A	N/A	18
SOIC	75	50	40	25	25	20	N/A	N/A	N/A	N/A
SSOP	N/A	N/A	NS	N/A	N/A	40	N/A	25	20	N/A

NOTE 1: QSOP (DBQ) and EIAJ devices (DB, NS, PS, and PW packages) are not available in tubes.

Table 8: Reel Quantities

		Package Designator	Units per Reel
DSBGA†	96/114 pin	YEAR	3000
EIAJ surface mount		DBR/DBLE, NSR/NSLE, PWR/PWLE	2000
LFBGA	96/114 pin	GKE, GKF	1000
PLCC	28 pin	FNR	750
	44 pin	FNR	500
QSOP	16/20/24 pin	DBQR	2500
SSOP	48/56 pin	DLR	1000
SOIC/SOP	14/16 pin	DR	2500
	Wide body 16 pin	DWR	2000
	20/24 pin	DWR	2000
	28 pin	DWR	1000
TQFP	64 pin	PMR	1000
TSSOP		DGGR	2000

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

Table 9: Box Quantities

		Package Designator	Units per Box
DIP		N	1000
		NT	750
		NP	700
SOIC		D, DW	1000
SSOP	48/56 pin	DL	1000

Table 10: Tray Quantities

		Package Designator	Units per Tray
TQFP	64 pin	PM	160