Migrating From AT87C51xxx to AT89C51xxx.

Introduction

This document details the differences between AT87C51X OTP Product and AT89C51X Product. The migration from OTP to Flash versions can be done after checking changes versus features.

C51 Microcontrollers

Application Note

Rev. 4214B–8051–12/02

Pin compatibility

AT89C51xxx is pin to pin and instruction compatible with AT87C51xxx

Package availibility

	PLCC44	VQFP44	VQFP64	PLCC68
AT87C51xxx	Yes	Yes	Yes	Yes
AT89C51xxx	Yes	Yes	Yes	Yes

Features

Features	AT87C51xxx	AT89C51xxx
Timer 0	Yes	Yes
Timer 1	Yes	Yes
Timer 2	Yes	Yes
Dual Data Pointer	Yes	Yes
On-chip code memory	16/32/64K Eeprom	16/32/64K Flash
In System Programming	No	Yes (over UART)
PCA High Speed Output Compare / Capture Pulse Width Modulator Watchdog Timer	 Yes Yes Yes Yes	 Yes Yes Yes Yes
Scratch pad Ram	256 bytes	256 bytes
Interrupt sources	7	9
Interrupt priority level	4	4
X2 mode	Yes	Yes
Asynchronous Port Reset	Yes	Yes
On-chip eXpanded RAM	Max. 768 bytes	Max.1792 bytes
XRAM configuration after reset	256 or 768 bytes	768 bytes
Hardware Watchdog Timer	Yes	Yes
Full duplex Enhanced UART	Yes	Yes
Low EMI(inhibit ale)	Yes	Yes
Power Control modes Idle Mode Power-down mode Power-off Flag	 Yes Yes Yes	 Yes Yes Yes

SFRs Registers

All the AT87C51xxx SFR are present in the AT89C51xxx.

The following table show in red the difference beetwen both partsj

	Bit addressable	**Non Bit addressable**							
	SFR0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 1111 1111							P5 byte Addressable 1111 1111	C7h
B8h	IPL0 X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 0XXX X0X0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX00 1000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

Table 1. CKCON0 Register in AT89C51xxx

CKCON0 - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	Reserved	
6	WDX2	**Watchdog Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	**Programmable Counter Array Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SIX2	**Enhanced UART Clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer2 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	**Timer1 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	**Timer0 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	**CPU Clock** Cleared to select 12 clock periods per machine cycle (STD mode) for CPU and all the peripherals. Set to select 6clock periods per machine cycle (X2 mode) and to enable the individual peripherals'X2' bits. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), Default setting, X2 is cleared.

Reset Value = 0000 000'HSB. X2'b (See "Hardware Security Byte")
Not bit addressable

On AT87C51xxx only bit 0 is avalaible in CKCON register, user must take care to not modify other bits using mask instruction.

Table 2. AUXR Register in AT89C51xxx

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
DPU	**-**	**M0**	**XRS2**	**XRS1**	**XRS0**	**EXTRAM**	**AO**

Bit Number	Bit Mnemonic	Description
7	DPU	**Disable Weak Pull-up** Cleared by software to activate the permanent weak pull-up (default) Set by software to disable the weak pull-up (reduce power consumption)
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	M0	**Pulse length** Cleared to stretch MOVX control: the RD/ and the WR/ pulse length is 6 clock periods (default). Set to stretch MOVX control: the RD/ and the WR/ pulse length is 30 clock periods.
4	XRS2	**XRAM Size : example for AT89C51RD2** XRS2 XRS1XRS0XRAM size 0 0 0 256 bytes 0 0 1 512 bytes 0 1 0 768 bytes(default) 0 1 1 1024 bytes 1 0 0 1792 bytes
3	XRS1	
2	XRS0	
1	EXTRAM	**EXTRAM bit** Cleared to access internal XRAM using movx @ Ri/ @ DPTR. Set to access external memory. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), default setting, XRAM selected.
0	AO	**ALE Output bit** Cleared, ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used). (default) Set, ALE is active only during a MOVX or MOVC instruction is used.

Reset Value = 0X00 10'HSB. XRAM'0b
Not bit addressable

On AT87C51xxx only bit 0 and 1 are avalaible in AUXR register, user must take care to not modify other bits using mask instruction.

Table 3. AUXR1 register in AT89C51xxx

AUXR1- Auxiliary Register 1(0A2h)

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ENBOOT	**Enable Boot Flash** Cleared to disable boot ROM. Set to map the boot ROM between F800h - 0FFFFh.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	**This bit is a general purpose user flag. ***
2	0	**Always cleared.**
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Reset Value: XXXX XX0X0b

Not bit addressable

*Bit 2 stuck at 0; this allows to use INC AUXR1 to toggle DPS without changing GF3.

On AT87C51xxx only bit 0 and 3 are avalaible in AUXR1 register, user must take care to not modify other bits using mask instruction.

On AT89C51xxx, one more bit (ENBOOT) is added

Hardware Register

The Hardware Byte of AT89C51xxx include three additionnal bits :

- X2 : This Fuse bit forces the X2 clock mode of CPU at Reset
- BLJB : This bit forces the execution of Bootloader
- XRAM : This Fuse bit inhibits the internal XRAM

Table 4. Hardware Security Byte (HSB) of AT89C51xxx

7	6	5	4	3	2	1	0
X2	**BLJB**	**-**	**-**	**XRAM**	**LB2**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2	**X2 Mode** Programmed (‘0’ value) to force X2 mode (6 clocks per instruction) after reset. Unprogrammed (‘1’ Value) to force X1 mode, Standard Mode, after reset (Default).
6	BLJB	**Boot Loader Jump Bit** Unprogrammed (‘1’ value) to start the user’s application on next reset at address 0000h. Programmed (‘0’ value) to start the boot loader at address F800h on next reset (Default).
5	-	**Reserved**
4	-	**Reserved**
3	XRAM	**XRAM Config Bit (only programmable by programmer tools)** Programmed to inhibit XRAM after reset. Unprogrammed, this bit to valid XRAM after reset (Default).
2-0	LB2-0	**User Memory Lock Bits (only programmable by programmer tools)** See Table 5.

Boot Loader Jump Bit (BLJB)

One bit of the HSB, the BLJB bit, is used to force the boot address:

- When this bit is programmed (‘1’ value) the boot address is 0000h.
- When this bit is unprogrammed (‘1’ value) the boot address is F800h. By default, this bit is unprogrammed and the ISP is enabled.

Flash Memory Lock Bits

The three lock bits provide different levels of protection for the on-chip code and data, when programmed as shown in following table

Table 5. Program Lock Bits

Program Lock Bits				
Security Level	**LB0**	**LB1**	**LB2**	**Protection Description**
1	U	U	U	No program lock features enabled.
2	P	U	U	MOVC instruction executed from external program memory is disabled from fetching code Bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further parallel programming of the Flash is disabled. ISP and software programming with API are still allowed.
3	X	P	U	Same as 2, also verify through parallel programming interface is disabled.
4	X	X	P	Same as 3, also external execution is disabled. (Default)

Note: U: unprogrammed or "one" level.
P: programmed or "zero" level.
X: don't care
WARNING: Security level '2' and '3' should only be programmed after Flash and code verification.

These security bits protect the code access through the parallel programming interface. They are set by default to level 4. The code access through the ISP is still possible and is controlled by the "software security bits" which are stored in the extra Flash memory accessed by the ISP firmware.

To load a new application with the parallel programmer, a chip erase must first be done. This will set the HSB in its inactive state and will erase the Flash memory. The part reference can always be read using Flash parallel programming modes.

Default Values

The default value of the HSB provides parts ready to be programmed with ISP:

- BLJB: Programmed force ISP operation.
- X2: Unprogrammed to force X1 mode (Standard Mode).
- XRAM: Unprogrammed to valid XRAM
- LB2-0: Security level four to protect the code from a parallel access with maximum security.

Frequency range

AT87C51xxx:

X1 mode : 30MHz @3V and 40MHz @5V

X2 mode : 20MHz @3V and 30MHz @5V

AT89C51xxx :

X1 mode :40MHz @2.7-5.5V and 60MHz @4.5-5.5V

X2 mode : 20MHz @2.7-5.5V and 30MHz @4.5-5.5V