A Fully Parallel CMOS Analog Median Filter

Alejandro Díaz-Sánchez, Jaime Ramírez-Angulo, Antonio Lopez-Martin, and Edgar Sánchez-Sinencio

***Abstract*—A fully integrated CMOS implementation of a continuous-time analog median filter is presented. The median filter uses two compact analog circuits as building blocks to implement the variable delay and median detection. Median detectors are based on current saturating transconductance comparators, while the time delay is implemented using first-order all-pass filters. Both circuits allow modular expansion for the implementation of large median filter array processors. Based on these blocks, a new fast technique for parallel image processing is presented. It is shown that an image of 91 $\times$ 80 pixels can be processed in less than 8 μs using an array of median filter cells. Experimental results of a test chip prototype in 2-μm CMOS MOSIS technology are presented.**

***Index Terms*—Analog delay cells, analog median filter, CMOS analog circuits, parallel image processing, transconductance comparators.**

I. Introduction

MEDIAN filtering is a widely employed nonlinear operation in image and speech processing [1]. In the first case, it is mainly used to remove impulsive and high-frequency noise while preserving sharp edges. The median of a sequence of data is defined as the datum, which has the same number of data with larger values as the number of data with lower values in the ordered sequence. In the case of sequences with an odd number of elements, the median is always one element of the sequence. In the case of sequences with an even number of elements, the median is given by the arithmetic mean of the two data in the middle of the ordered sequence.

Median filters use a window that moves over the data, replacing the original datum with the computed median [2]. Despite their popularity, digital implementations of real-time median filters are computationally expensive because they need to perform a sorting operation for each pixel in order to compute the median [3]. Since each datum must be compared to the others, the digital circuitry needed to perform the median of a set of data is relatively complex, requires a large silicon area, and has high power dissipation, particularly for high-speed applications. Therefore, it does not allow real-time parallel median filtering, despite that some efforts have been directed to reduce the number of data involved in the median computations [4].

Recent research in high-speed analog implementations of median filters has been based on the use of bipolar and MOS transistors (e.g., [5]), most of them with a restricted number of inputs allowed [5], [6]. In order to solve the limitations in the number of inputs, running-median implementations have been used [7]. In the case of CMOS implementations, the relatively low transconductance gain of the MOS transistor produces a smooth corner effect (i.e., the median does not follow corners accurately) in the nonlinear transfer function of the median circuit. Some reported implementations have used feedback configurations to overcome this problem [6], [8], [9], but their structures also become highly complex for arrays with more than three data. Therefore, real-time parallel image-processing applications remain unresolved. Recent studies proposed approximations to parallel processing using analog CMOS circuits [10]–[12].

This paper presents a new CMOS implementation of a highly parallel analog median filter whose main characteristic is the continuous-time parallel processing of the signal. The presented implementation processes an $m \times n$ image (where m is the number of rows and n the number of columns) by columns using, for this purpose, a bank of m median filter cells. The median of the image is obtained after n delays. Each median filter cell constitutes a mask that processes a neighborhood of 3×3 pixels. The median filters are based on two compact circuit building blocks, i.e.: 1) continuous-time analog delay elements based on first order all-pass circuits and 2) median detector circuits using high-gain CMOS transconductance comparators that saturate in current. The presented median filter uses the principle of balanced saturation described by Li and Holmes [13], but it is based on current instead of voltage saturation. Median filter cells can operate at high frequency and use only NMOS and PMOS transistors. Median filter detectors presented here are not limited to an odd number of data, computing the even and odd cases. Experimental results of the basic cells from a test chip prototype are presented. Simulation results of a 91 $\times$ 80 image, processed using a median filter array with 91 cells operating in parallel, are shown.

II. Building Blocks of the Analog Median Filter

Here, the basic building blocks of median filters are introduced. Fig. 1 shows a block diagram of the implemented median filter. The input signal is brought into a delay line, which allows the filter to access previous values of the input signal. The delay line is implemented using a cascade of first-order all-pass circuits described in Section II-A. Section II-B describes the

Manuscript received July 8, 2001; revised September 25, 2003. This paper was recommended by Associate Editor G. Cauwenberghs.

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Digital Object Identifier 10.1109/TCSII.2003.822442

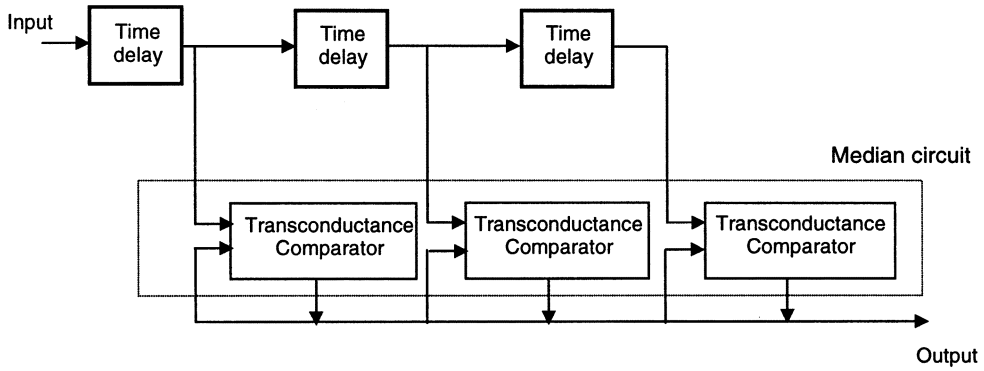


Fig. 1. Block diagram of the median filter.

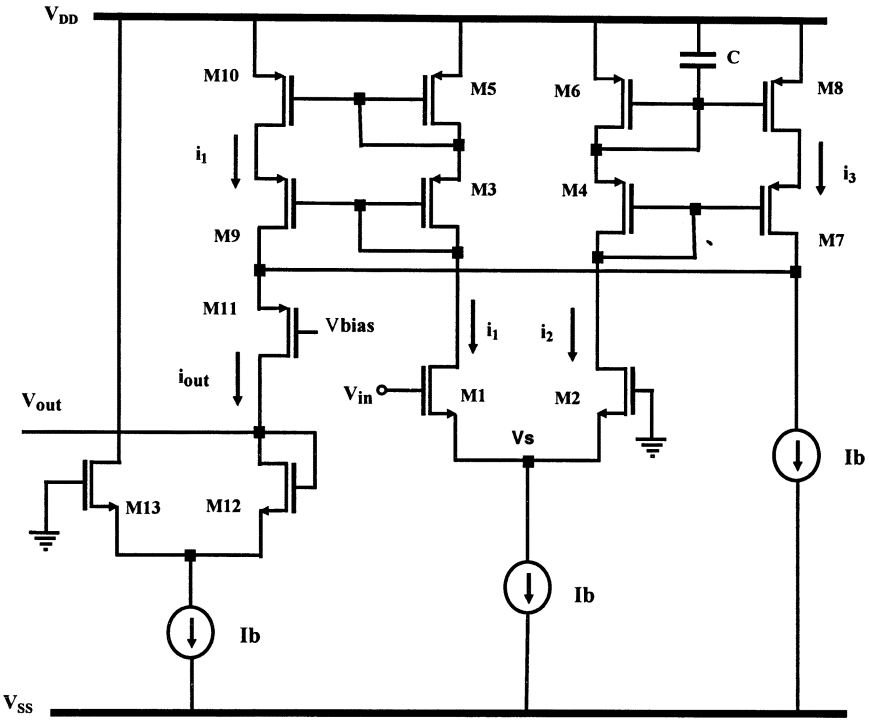


Fig. 2. Analog delay circuit.

transconductance comparators used to build the median circuit detector.

A. Analog Delay Cell

As mentioned above, an all-pass circuit is used for the implementation of the analog delay. Fig. 2 shows the CMOS implementation, indicating the ac small-signal branch currents. The circuit operates as follows: the input voltage applied to transistor M1 produces complementary currents I_1 and I_2 through the input branches M3-M5 and M4–M6 of the PMOS current mirrors, given by

$$I_1 = \frac{I_b}{2} + i_1$$
$$I_2 = \frac{I_b}{2} + i_2. \tag{1}$$

Neglecting channel length modulation effects, the ac currents i_1, i_2 are given by

$$i_1 = g_{\mathrm{m1,2}} v_{\mathrm{in}} = -i_2 \tag{2}$$

where $g_{\mathrm{m1,2}}$ is the small-signal transconductance gain of the differential pair transistors M1 and M2. Selecting $(\mathrm{W/L})_{\mathrm{M7-M8}} = 2(\mathrm{W/L})_{\mathrm{M4-M6}}$, we obtain

$$i_3 = 2\frac{\frac{g_{\mathrm{m5,6}}}{C}}{s + \frac{g_{\mathrm{m5,6}}}{C}} i_2 \tag{3}$$

where C is the capacitor value and $g_{\mathrm{m5,6}}$ is the small-signal transconductance gain of M5 and M6 transistors (Fig. 2). The ac small-signal current through M11 is given by

$$i_{\mathrm{out}} = i_1 + i_3 = i_1 + 2\frac{\frac{g_{\mathrm{m5,6}}}{C}}{s + \frac{g_{\mathrm{m5,6}}}{C}} i_2 = \frac{s - \frac{g_{\mathrm{m5,6}}}{C}}{s + \frac{g_{\mathrm{m5,6}}}{C}} g_{\mathrm{m1,2}} v_{\mathrm{in}}. \tag{4}$$

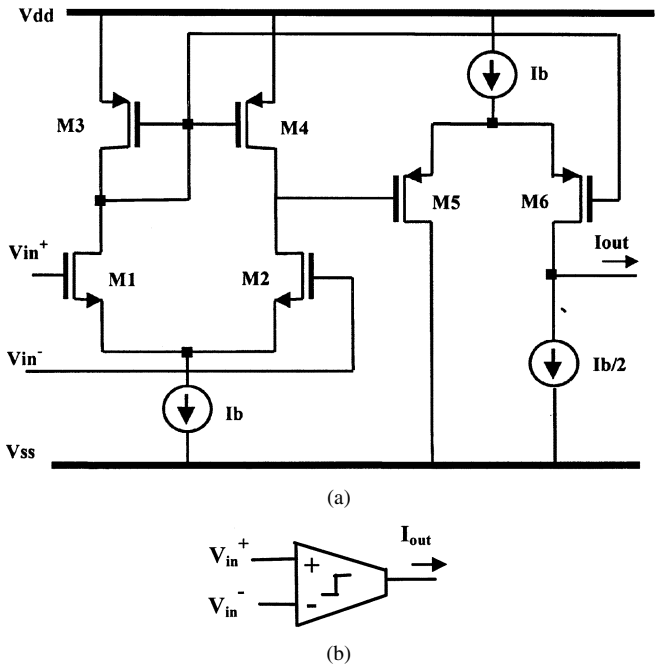


Fig. 3. High-gain stage circuit. (a) Internal structure. (b) Symbol.

If we choose $(\mathrm{W/L})_{\mathrm{M12,M13}} = (\mathrm{W/L})_{\mathrm{M1,M2}}$, the transfer function is then a first-order all-pass transfer function given by

$$H(s) = \frac{v_o}{v_{\mathrm{in}}} = \frac{s - \dfrac{g_{\mathrm{m5,6}}}{C}}{s + \dfrac{g_{\mathrm{m5,6}}}{C}} \tag{5a}$$

$$|H(s)| = 1$$

$$\angle H(s) = -2\tan^{-1}\left(\frac{\omega C}{g_{\mathrm{m5,6}}}\right) \tag{5b}$$

and the group delay is given by

$$\tau(\omega) = 2\frac{\dfrac{g_{\mathrm{m5,6}}}{C}}{\omega^2 + \left(\dfrac{g_{\mathrm{m5,6}}}{C}\right)^2}. \tag{6}$$

B. Transconductance Comparator

Fig. 3 shows a two-stage high-gain CMOS transconductance comparator circuit. In order to obtain high transconductance gain, it uses a cascade of two differential pairs. The gain of this circuit is comparable to that of a bipolar stage and is required in order to avoid the corner smoothing error observed in other CMOS implementations. The first differential stage (M1 and M2), is connected as a voltage amplifier and has a voltage gain given by

$$A_0 = \frac{g_{\mathrm{m1,2}}}{g_{o2} + g_{o4}} \tag{7}$$

while the second differential pair (M5 and M6) is connected as a transconductance amplifier with transconductance gain $g_{\mathrm{m5,6}}$. Since the second stage saturates in current with $I_{\mathrm{out}} = \pm I_b/2$, its response to input voltage changes occurs faster than for previously reported applications [6], [8], [9]. This circuit behaves as a high-gain operational transconductance amplifier (OTA), and its dc transconductance characteristic is shown in Fig. 4. The overall small signal transconductance gain is given by

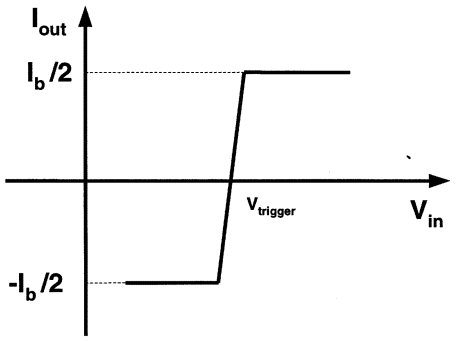


Fig. 4. DC transfer characteristic of two-stage CMOS transconductance comparator.

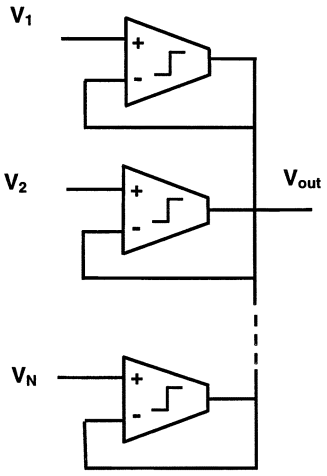


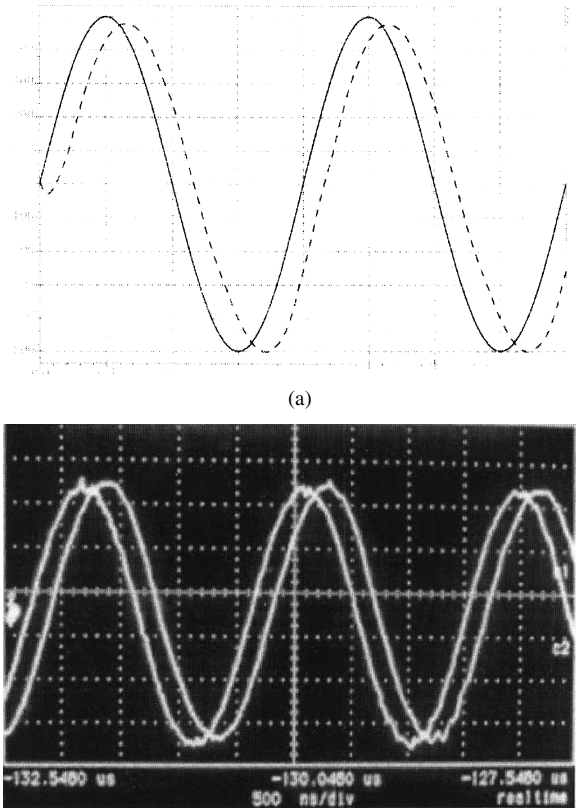
Fig. 5. Median circuit detector.

$$g_{mC} = \frac{g_{\mathrm{m1,2}} g_{\mathrm{m5,6}}}{g_{o2} + g_{o4}} = A_0 g_{\mathrm{m5,6}}. \tag{8}$$

This gain can be on the order of several tens of milliamperes per volt and, as mentioned above, is similar to the transconductance gain achievable by a bipolar transistor differential stage.

III. Median Circuit

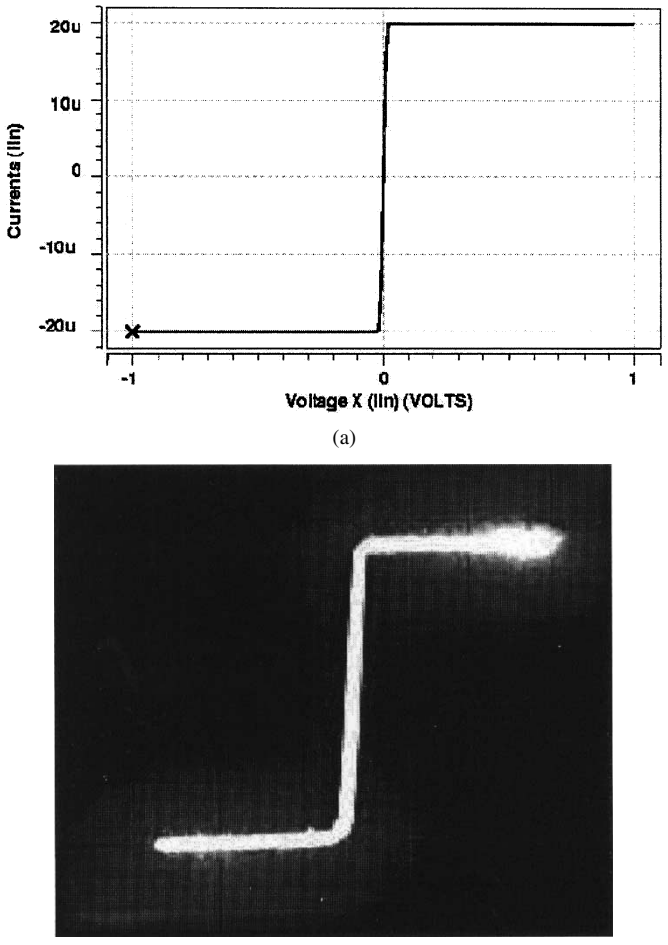
The median detector circuit is shown in Fig. 5. It uses one transconductance comparator per input, where the number of inputs corresponds to the number of points in the mask that is used to process a pixel neighborhood (see Section V). A similar circuit was described by Mead in 1989 [14]. However, the high gain, achieved by using a two-stage transconductor, improves the median detector response. During circuit operation, the output current of transconductors whose input data are above the median saturate in the positive direction, driving a saturation current $i_{\mathrm{out}}^{+} = I_b/2$ into the node labeled V_{out}. Meanwhile, for transconductors whose input data are below the median, the output current will be $i_{\mathrm{out}}^{-} = -I_b/2$. Since the number of data below the median is the same as those above the median, the sum of the output currents of all saturated comparators equals zero. The output current is also zero for the comparator for which $V_{\mathrm{out}} = V_{\mathrm{inmed}}$. This is due to the fact that



(a)

(b)

Fig. 6. CMOS analog delay input and output signals. (a) Simulated results. (b) Experimental results. Vertical axis is 120 mV/div. Horizontal axis is 500 ns/div.



(a)

(b)

Fig. 7. DC performance of the composite OTA. Vertical axis 10 μA/div. Horizontal axis 1 V/div. (a) Simulation results. (b) Experimental results.

this transconductor operates in its linear region with both inputs at (approximately) the same potential. V_{inmed} is the input voltage corresponding to the median of the data set. For any median filter with odd number of inputs, the output voltage will follow the input in order to obtain a transconductor whose input is the median of the data set. For median filters with even number of inputs, the pair of transconductors with the middle values will operate in their linear region maintaining the sum of the output currents to zero. If $io_{\text{med}+1/2}$ and $io_{\text{med}-1/2}$ are the currents at the output of the OTAs with the middle values, while $V\text{in}_{\text{med}+1/2}$ and $V\text{in}_{\text{med}-1/2}$ are the corresponding input values $io_{\text{med}+1/2} = -io_{\text{med}-1/2}$, and the output voltage will be given by

$$V_{\text{out}} = \frac{V\text{in}_{\text{med}-1/2} + V\text{in}_{\text{med}+1/2}}{2}. \tag{9}$$

Therefore, for even number of inputs, the average of the two input voltages of the OTAs with the middle values will be at the output of the median filter.

IV. Experimental and Simulation Results

Here, we present experimental results of a test-chip prototype fabricated in a 2-μm double-poly double-metal (DPDM) CMOS technology (through MOSIS). The chip included the two basic circuit building blocks: an all-pass filter to implement the delay line, a transconductance comparator, as well as a three input median filter, according to the scheme of Fig. 5. The NMOS transistors dimensions employed for the differential pairs in the fabricated circuit where $\text{W/L} = 6\ \mu\text{m}/3\ \mu\text{m}$, and the current mirror PMOS transistors have dimensions $\text{W/L} = 16\ \mu\text{m}/3\ \mu\text{m}$. The value of C was 2 pF. Biasing currents in all circuits had values $I_b = 60\ \mu$A, and were implemented with wide-swing low-voltage cascode current mirrors with dimensions $\text{W/L} = 24\ \mu\text{m}/2\ \mu\text{m}$. Simulation and experimental results of the delay line for a sinusoidal signal of 500 kHz are shown in Fig. 6 with a 200-ns delay. Since the time delay is a function of the capacitor and of the bias current I_b, it can be easily programmed. Simulations established that variations in the bias current from 40 to 80 μA lead to a delay that varies from 100 to 350 ns.

The simulated and experimental dc transconductance characteristic (I_{out} versus V_{in}) of the transconductance comparator for $I_b = 40\ \mu$A is shown in Fig. 7(a) and (b), respectively. Simulations show a rise time of 2 ns and a settling time of 4 ns, significantly lower than for a conventional single-stage OTA, as shown in Fig. 7(a).

Fig. 8 shows the measured dc transfer characteristic of the median filter with inputs $V_1 = -0.5$ V and $V_2 = 0.5$ V. The dc sweep was applied to V_3. Note that corners are very sharp. Fig. 9 shows the measured dc error of the median output, i.e., the difference of the output from the ideal median. Constant

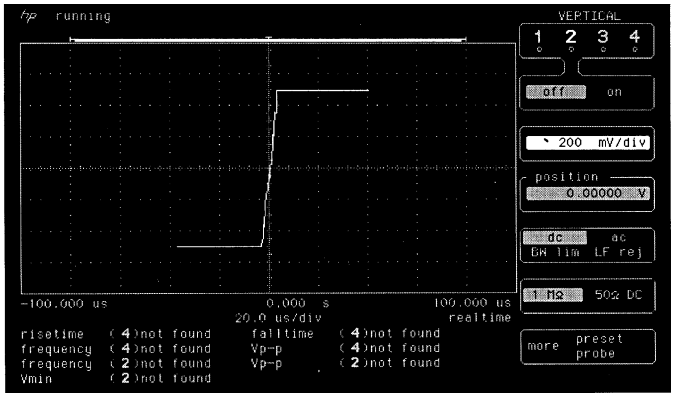


Fig. 8. Measured dc transfer characteristic of median filter for inputs V1 $=$ -0.5 V and V2 $=$ 0.5 V. Vertical scale is 200 mV/div.

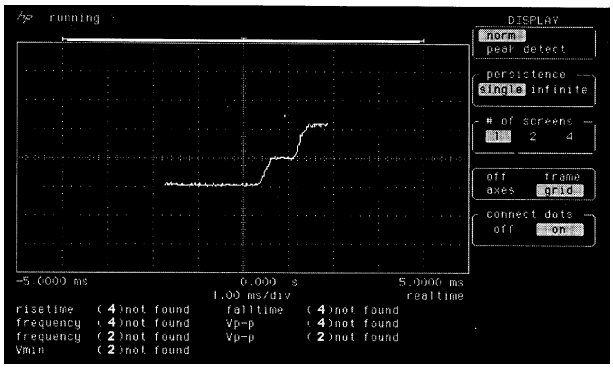


Fig. 9. Experimental dc error from median for inputs $v1 = 150$ mV and $v2 = 350$ mV. Vertical scale is 20 mV/div.

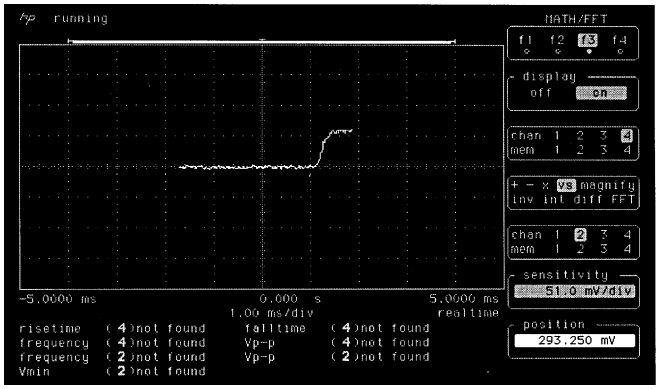
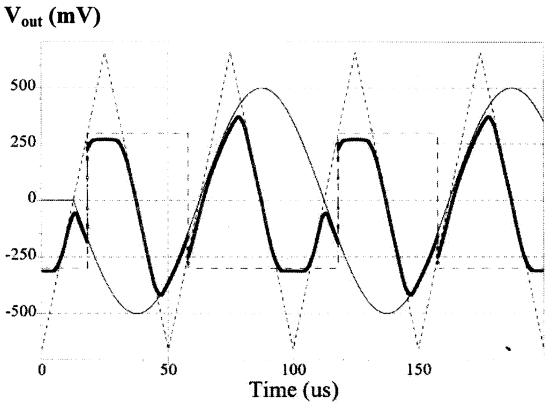


Fig. 10. Rejection to the nonmedian input. Measured output voltage variation for V1 $=$ V2 $=$ 350 mV.

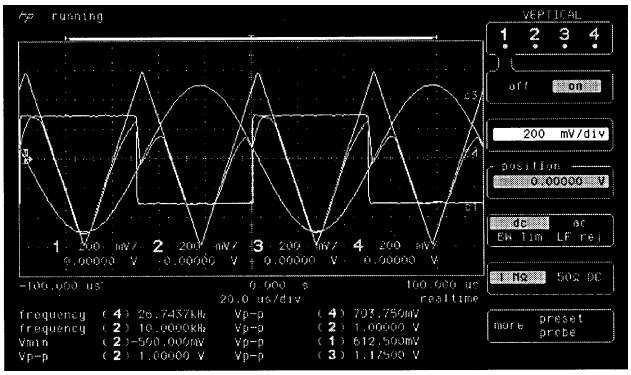
voltages of 0.15 and 0.35 V were applied to inputs V_1 and V_2, respectively. The input offset of the comparators constitutes a significant contribution to this error.

Another important dc measurement is the rejection of the nonmedian output [6]. Fig. 10 shows the measured output voltage variation when two of the inputs were held to a common constant voltage of 0.35 V.

Fig. 11(a) shows the simulated performance of a three-input median circuit, while Fig. 11(b) shows experimental performance of the fabricated three-input median circuit. Observe that the output (thick trace) follows the median of the inputs, which are sinusoidal, square, and triangular waveforms. Bias



(a)



(b)

Fig. 11. Median circuit detector. (a) Simulated response. (b) Experimental results. Vertical axis is 200 mV/div. Horizontal axis is 20 $\mu s/$div.

currents were set to 60 μA, while supply voltages were ± 2.5 V. A power consumption of 14 mW for a 3×3 median detector cell was measured.

V. Column Processor Array

A median filter array was conceived for its utilization as a column array processor for image processing. It is implemented in a modular fashion using the blocks described in Section II. Consider an image with $m \times n$ pixels (m rows and n columns). The image information is processed by shifting columns of pixel data into a column processor formed by an array of m median filter masks $(\phi_1, \phi_2, \ldots, \phi_m)$. Each mask takes the input data of nine pixels: three rows and three columns. The data taken by adjacent masks overlap by two rows (see Fig. 12). A block diagram of the nine pixels median filter cell (mask) is shown in Fig. 13. It consists of nine transconductance comparators and delay elements in a 3×3 array. Fig. 12 illustrates the way data are processed one column at a time: filter mask Φ_I process data of three pixels in three consecutive rows of the image. The data corresponding to the pixels at times t_{k-2}, t_{k-1}, and t_k of the rows $n+2$, $n+1$, and n are processed into the median data $M(t_{k-1}, n+1)$, as is shown in Fig. 12(a). Meanwhile, mask filter Φ_2 processes data corresponding to rows $n+1$, n, and $n-1$, which are processed into the median data $M(t_{k-1}, n)$. A similar procedure is performed by filter mask Φ_3. Next, a new center value is available at time t_k, with column vector output $M(t_k)$, as shown in Fig. 12(b), and t_{k+1} with column vector

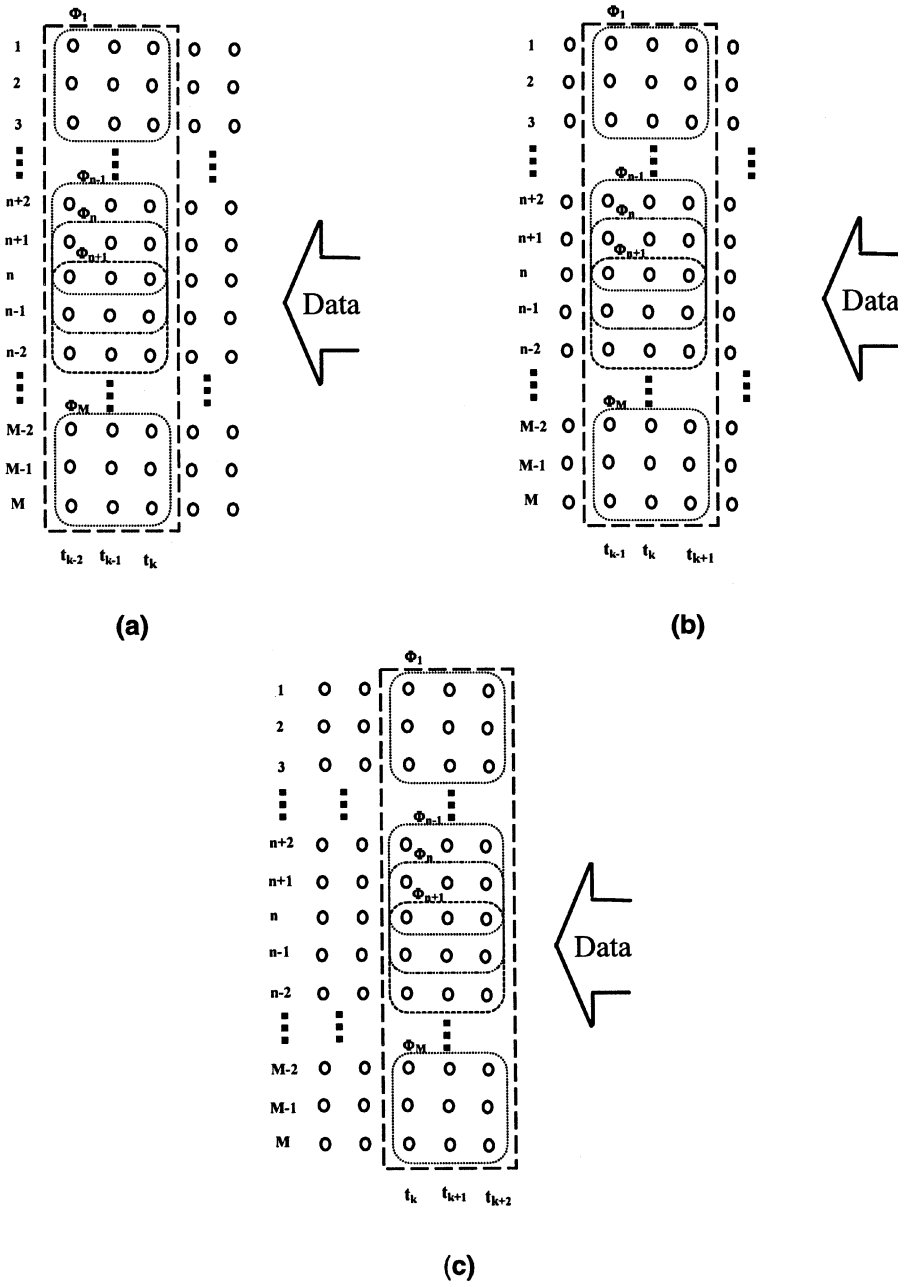


Fig. 12. Processing image by columns using an array of median filters.

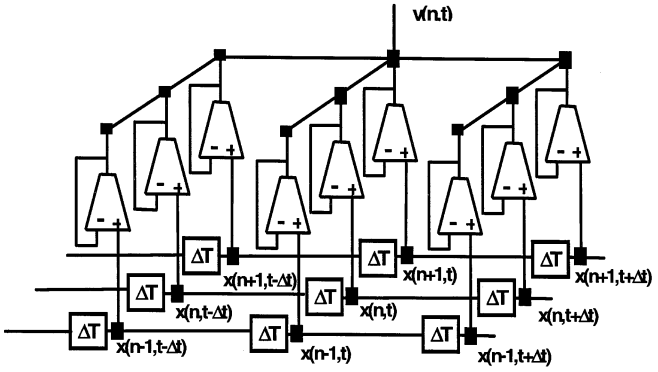


Fig. 13. Structure of 3 × 3 pixels median filter mask.

output $M(t_{k+1})$, as shown in Fig. 12(c). The array of m analog median filter masks works in parallel and generates as output, every delay interval, a column with the median values of the column in the original image. In order to process a complete image, the procedure will be completed in n delays. The time required to process an image is $n+2$ analog delays. The continuous-time operation discards any synchronization requirements. In order to test the median filter array, SPICE circuit-level simulations (using the median filter cells described in Section IV) of a 91-mask array, which was used to process an image of 91 × 80 pixels corrupted with 15% salt and pepper noise, were performed. The original image is shown in Fig. 14(a), while Fig. 14(b) shows the corrupted image. The image was processed taking 80 columns with 91 data each. All the rows were taken at the input as continuous-time signals, and processed in parallel. The time required to compute the median of the entire image was approximately 30 μs. Fig. 14(c) shows the reconstructed analog median filter output. A comparison of the mean square

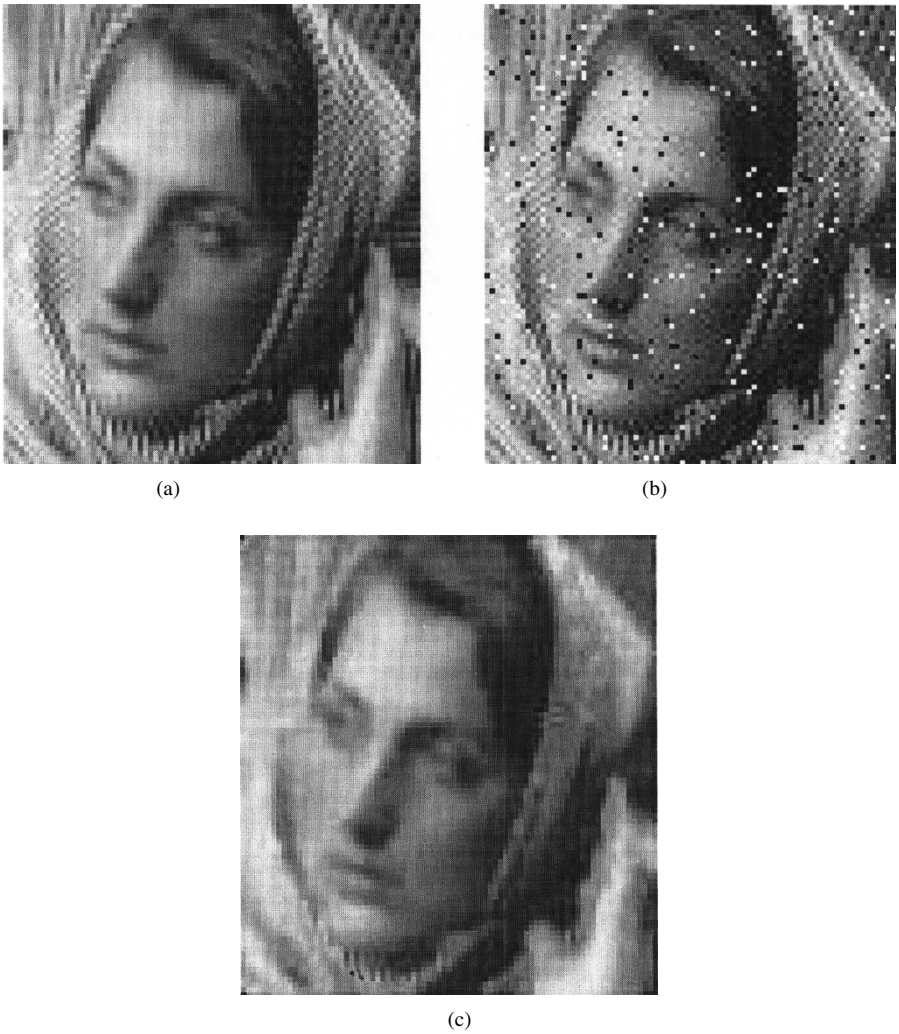


Fig. 14. (a) Original image. (b) Image corrupted with 15% salt and pepper noise. (c) Reconstructed image.

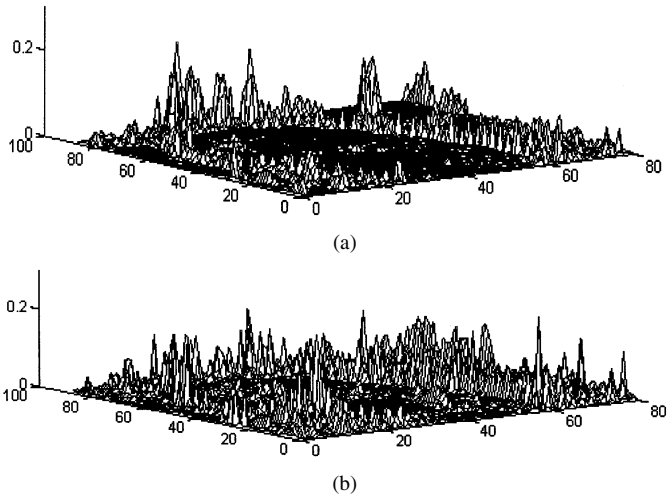


Fig. 15. Mean squared error. (a) Software reconstructed image. (b) Reconstructed image using the analog median array processor.

errors (with respect to the original image) of the software reconstructed image (using MATLAB) and of the median filter reconstructed image is shown in Fig. 15(a) and (b), respectively. In spite of the fact that the mean square error is greater than the filtered image obtained using MATLAB (5.2% and 4.1%, respectively), the edge error is reduced.

VI. CONCLUSIONS

An efficient and fast CMOS analog median filter has been introduced that consists of only two compact building blocks: analog delay cells using first-order all-pass circuits and transconductance comparators. Its application for the implementation of modular array processors for high-speed median filtering of images has been discussed. This processor has a modular structure. The basic building blocks, as well as a three-input median filter cell have been designed, fabricated, and experimentally characterized. The analog delay element has a delay range from 100 to 350 ns and uses bias currents that can be varied from 40 to 80 μA. The median circuit cell proposed occupies an area of 352×389 μm^2 in 2-μm CMOS technology and it is very compact compared with previously reported applications [6], [8], [9]. The compactness of the design allows the implementation of large highly parallel real-time analog image processors. The continuous-time characteristic of the design discards any synchronization requirements. Given that the median filter presented operates directly on analog

signals, A/D and D/A conversions are not required. The delays in the line can be easily and individually controlled using the bias currents of the delay elements, thus allowing additional design flexibility, and opens the door for the implementation of weighted median filters. Besides image processing, the median filter structure presented here can be used for a wide variety of high-speed applications in communications, as well as in other fields.

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