EXPERIMENT 170 - Combinational Logic Problems

The purpose of this practical is to reinforce your proficiency in dealing with combinational logic networks. Two networks are analysed and their internal operational deduced. The functions extracted are then examined and additional terms are designed so as to reduce race hazards from the overall system. Truth tables and Karnaugh maps are used for the design and a logic tutor is used to prove your design. Keep a log of all you do in the lab.

1) Combinational Logic and Hazards

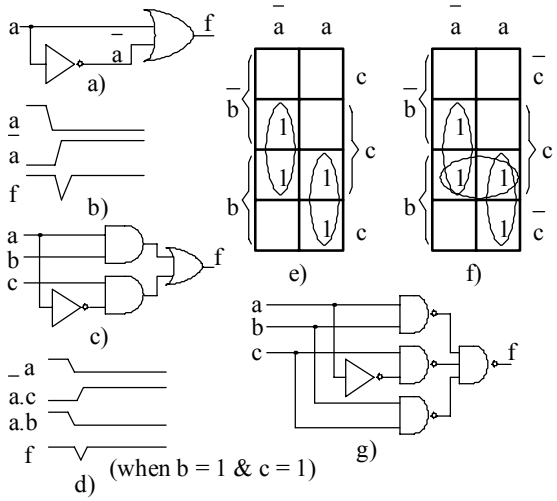

Figure 1

A combinational logic circuit is one whose output is a function of its inputs only, whereas a sequential logic circuit is one whose output is a function of its current and previous inputs. One problem with these networks is that race hazards exist when a short glitch occurs just after an input changes.

Consider figure 1a; this shows a circuit for $f = a + \bar{a}$; the output for this is 1 under static conditions. However, because of the propagation delay of the signal through an inverter, when a changes from 1 to 0, there is a brief time when both a and $\bar{a}$ are 0, hence f is 0 for a short time, as shown in figure 1b. This glitch occurs because of a *race hazard*.

Now consider the circuit in figure 1c, for function $f = a.b + \bar{a}.c$.

When b and c are both 1, this reduces to $f = a + \bar{a}$, when there is a hazard when a changes from 1 to 0, as shown in figure 1d. The karnaugh map for this function is shown in figure 1e, and the adjacent squares for a.b and $\bar{a}.c$ are circled. However, as shown in figure 1f, two of these squares can also be circled, for the term b.c.

Thus the function could be written as $f = a.b + \bar{a}.c + b.c$.

The advantage of including this term is that hazards do not occur; this is because the hazard occurs when b and c are both 1, so the b.c term will be 1. b.c is called the *hazard* term. Figure 1g has the complete circuit, including the hazard term, which has been implemented using NAND gates instead of AND and OR gates.

2) Procedure

For this practical, two combinational networks are provided.

a) Three input combinational logic network

The network in figure 2 is provided on a logic tutor socket. The circuit is designed to exaggerate the problem of race hazards. Devise a test scheme for the network so that you can observe the hazard on an oscilloscope. Draw you test circuit and the waveforms you observe. Derive the hazard elimination term required, implement and test. N.B. The hazard spike might be too short to observe directly on the oscilloscope so you might need to devise a detection circuit (think about the type of systems when hazards matter!).

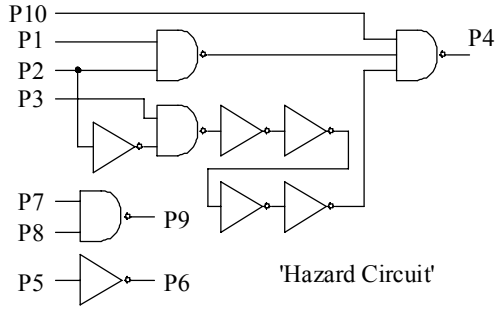

Figure 2

Note, Pn in the figure is the pin number on the logic tutor socket, on which the associated signal appears. You should also ensure the circuit is provided with +5V and GND.

b) Four input combinational logic network

This circuit is in a programmable logic array (PLA) in a logic tutor carrier marked E170. The PLA has a mode control for selecting one of two circuits (only one being used here), and various inputs which are processed by the circuit in the PAL to produce an output (shown in the left hand side of figure 3). The PLA contains an AND-OR network of the form shown in figure 3, for which the four AND terms are brought out to output pins as well as the function output. Pin 1 of the PLA is the Mode pin; in this part of the experiment connect this pin to logic 0, and the circuit in the PLA has four inputs.

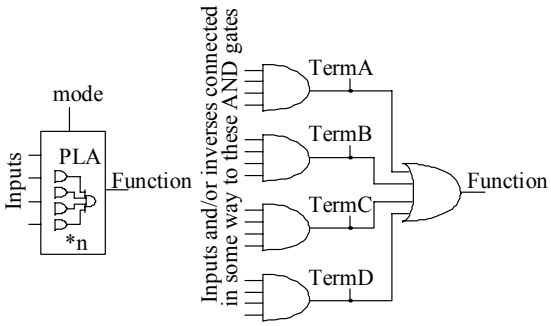

Figure 3

The function is of the form: Function = TermA + TermB + TermC + TermD and the four Term signals are the outputs of the AND gates whose inputs are some combination of InputA, InputB, InputC and InputD and their inverses. The inputs, terms and outputs are connected to the following pins:

2 - Input A; 3 - InputB; 4 - InputC; 5 - InputD;
17 - TermA; 16 - TermB; 15 - TermC; 14 - TermD;
13 - Function

Construct a truth table showing TermA, TermB, TermC, TermD and Function for all combinations of inputs. Plot a Karnaugh Map of Function, and show on it the groupings of TermA, TermB, TermC and TermD. Find any race hazards, mark these in a different colour on your Karnaugh Map and hence derive the hazard terms to guard against hazards. Devise a network of gates to eliminate the race hazards; build and confirm the operation of your network.

Conclusion

This should include comments on all your observations.

R.J.M and P.R.M. updated 13/3/04